imall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

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MCD56-08io8B

=

=

=2x 800 V

60 A

1.24 V

 V_{RRM}

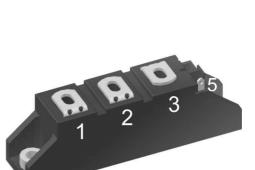
I TAV

VT

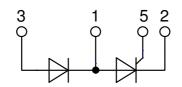
Thyristor \ Diode Module

Phase	leg
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Part number MCD56-08io8B



Backside: isolated **E**72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al2O3-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-240AA

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

Terms Conditions of usage:

The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact your local sales office. Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact your local sales office. Should you intend to use the product in aviation, in health or life endangering or life support applications, please notify. For any such application we urgently recommend

to perform joint risk and quality assessments;
the conclusion of quality agreements;

- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

IXYS reserves the right to change limits, conditions and dimensions.

Data according to IEC 60747and per semiconductor unless otherwise specified

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MCD56-08io8B

Rectifier					Ratings	5	1
Symbol	Definition	Conditions		min.	typ.	max.	Unit
V _{RSM/DSM}	max. non-repetitive reverse/forwa	ard blocking voltage	$T_{VJ} = 25^{\circ}C$			900	۷
V _{RRM/DRM}	max. repetitive reverse/forward b	locking voltage	$T_{VJ} = 25^{\circ}C$			800	٧
R/D	reverse current, drain current	$V_{R/D} = 800 V$	$T_{vJ} = 25^{\circ}C$			200	μA
		V _{R/D} = 800 V	$T_{vJ} = 125^{\circ}C$			5	mA
V _T	forward voltage drop	$I_{T} = 100 \text{ A}$	$T_{vJ} = 25^{\circ}C$			1.26	٧
		$I_{T} = 200 \text{ A}$				1.57	٧
		$I_{T} = 100 \text{ A}$	$T_{vJ} = 125^{\circ}C$			1.24	٧
		$I_{T} = 200 \text{ A}$				1.62	٧
I TAV	average forward current	$T_c = 85^{\circ}C$	$T_{vJ} = 125^{\circ}C$			60	A
T(RMS)	RMS forward current	180° sine				94	A
V _{T0}	threshold voltage		$T_{vJ} = 125^{\circ}C$			0.85	٧
r _T	slope resistance } for power lo	oss calculation only				3.7	mΩ
R _{thJC}	thermal resistance junction to cas	se				0.45	K/W
R _{thCH}	thermal resistance case to heatsi	nk			0.20		K/W
P _{tot}	total power dissipation		$T_c = 25^{\circ}C$			222	W
I _{TSM}	max. forward surge current	t = 10 ms; (50 Hz), sine	$T_{vJ} = 45^{\circ}C$			1.50	kA
		t = 8,3 ms; (60 Hz), sine	$V_{R} = 0 V$			1.62	kA
		t = 10 ms; (50 Hz), sine	T _{vJ} = 125°C			1.28	kA
		t = 8,3 ms; (60 Hz), sine	$V_{R} = 0 V$			1.38	kА
l²t	value for fusing	t = 10 ms; (50 Hz), sine	$T_{vJ} = 45^{\circ}C$			11.3	kA²s
		t = 8,3 ms; (60 Hz), sine	$V_{R} = 0 V$			10.9	kA ² s
		t = 10 ms; (50 Hz), sine	T _{v.i} = 125°C			8.13	kA ² s
		t = 8,3 ms; (60 Hz), sine	$V_{R} = 0 V$			7.87	kA²s
C	junction capacitance	$V_{B} = 400 V f = 1 MHz$	$T_{vJ} = 25^{\circ}C$		74		pF
P _{GM}	max. gate power dissipation	t _P = 30 μs	T _c = 125°C			10	W
		t _P = 300 μs				5	W
P _{GAV}	average gate power dissipation	• •				0.5	w
(di/dt) _{cr}	critical rate of rise of current	T _{v.i} = 125 °C; f = 50 Hz re	epetitive, $I_{T} = 150 \text{ A}$			150	A/μs
(/0		$t_{\rm P}$ = 200 µs; $di_{\rm G}/dt$ = 0.45 A/µs; -	•				
			on-repet., $I_{\tau} = 60 \text{ A}$			500	A/μs
(dv/dt) _{cr}	critical rate of rise of voltage	$V = \frac{2}{3} V_{\text{DRM}}$	$T_{v,i} = 125^{\circ}C$			1000	1
(, , cr		$R_{GK} = \infty$; method 1 (linear volta					
V _{GT}	gate trigger voltage	$\frac{V_{\rm D}}{V_{\rm D}} = 6 \text{V}$	$\frac{1}{T_{v,l}} = 25^{\circ}C$			1.5	v
- GI	J		$T_{y_{J}} = -40^{\circ}C$			1.6	v
I _{gt}	gate trigger current	$V_{D} = 6 V$	$T_{VJ} = 25^{\circ}C$			100	mA
GT	gale ingger eurrent	$\mathbf{v}_{\mathrm{D}} = 0 \ \mathbf{v}$	$T_{VJ} = -40^{\circ}C$			200	mA
V _{gd}	gate non-trigger voltage	$V_{D} = \frac{2}{3} V_{DBM}$	$T_{VJ} = 125^{\circ}C$			0.2	V
	gate non-trigger current	$\mathbf{v}_{\mathrm{D}} = 73 \mathbf{v}_{\mathrm{DRM}}$	T _{VJ} = 125 O			10	_
	latching current	t _ 10.00	$T_{y_J} = 25 ^{\circ}C$			450	mA mA
I.	latening current	$t_p = 10 \ \mu s$ $I_G = 0.45 \ A; \ di_G / dt = 0.45 \ A / \mu s$				450	mA
I _H	holding current	$V_{D} = 6 V R_{GK} = \infty$	$T_{vJ} = 25 \degree C$			200	mA
t _{gd}	gate controlled delay time	$V_{D} = \frac{1}{2} V_{DRM}$	$T_{vJ} = 25 ^{\circ}C$			2	με
-		$I_{\rm G} = 0.45 \text{A}; \text{di}_{\rm G}/\text{dt} = 0.45 \text{A}/\mu\text{s}$	3				
tq	turn-off time	$V_{\rm B} = 100 \text{ V}; \ \text{I}_{\rm T} = 150 \text{ A}; \ \text{V} = \frac{2}{3}$			150		μs
7		$di/dt = 10 \text{ A}/\mu \text{s} dv/dt = 20 \text{ V}$					

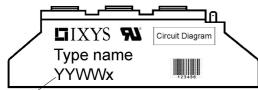
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MCD56-08io8B

Package TO-240AA				F	Ratings	S		
Symbol	Definition	Conditions			min.	typ.	max.	Unit
	RMS current	per terminal					200	Α
T _{vj}	virtual junction temperature				-40		125	°C
T _{op}	operation temperature				-40		100	°C
T _{stg}	storage temperature				-40		125	°C
Weight						81		g
M _D	mounting torque				2.5		4	Nm
M _T	terminal torque				2.5		4	Nm
d _{Spp/App}	oroopaga distance on surfa	ce striking distance through air	terminal to terminal	13.0	9.7			mm
d _{Spb/Apb}	creepage distance on suna	ce striking distance through an	terminal to backside	16.0	16.0			mm
V	isolation voltage	t = 1 second			3600			V
		t = 1 minute	50/60 Hz, RMS; liso∟ ≤ 1 mA		3000			V



Date Code

ſ	Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
	Standard	MCD56-08io8B	MCD56-08io8B	Box	36	457698

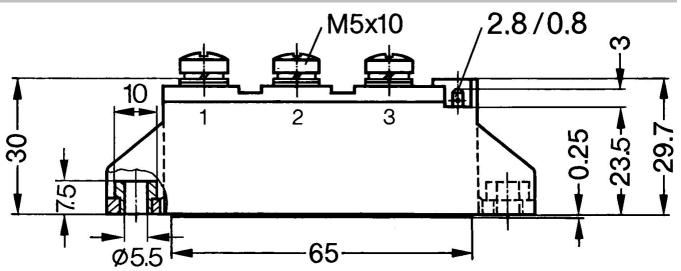
Similar Part	Package	Voltage class
MCMA65PD1200TB	TO-240AA-1B	1200
MCMA85PD1200TB	TO-240AA-1B	1200

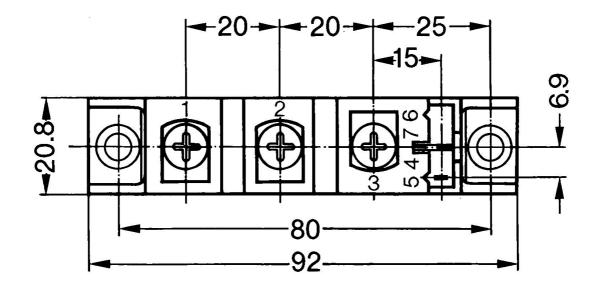
Equiva	lent Circuits for	Simulation	* on die level	T _{vJ} = 125 °C
	⊢R₀−	Thyristor		
V _{0 max}	threshold voltage	0.85		V
$\mathbf{R}_{0 \max}$	slope resistance *	2.5		mΩ

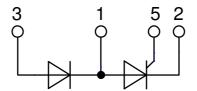
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Outlines TO-240AA







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DC

100

150

180° sin 120° J⊓L

60°.Л. 30° П

120

100

80

60

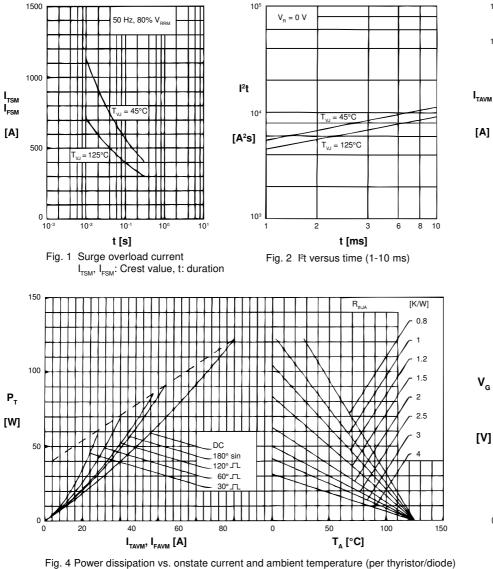
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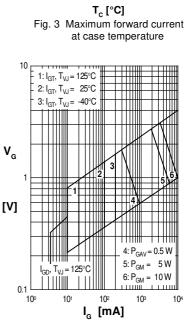
20

0

0

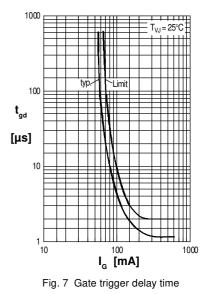
Thyristor





50

Fig. 5 Gate trigger charact.



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Fig. 6 Three phase rectifier bridge: Power dissipation versus direct output current and ambient temperature

0

50

T_^ [°C]

Circuit B6 3x MCC56 or

3x MCD56

150

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100

I_{dAVM} [A]

150

R_{thK}

[K/W]

0.1

0.15 0.2

0.25

0.3

0.4

0.5

0.6

100

50

600

500

400

300 [W]

200

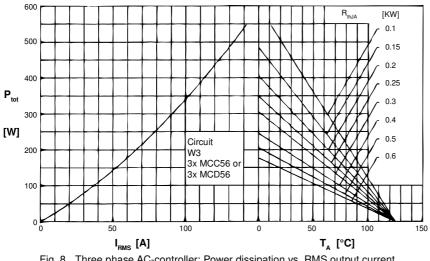
100

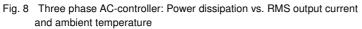
0

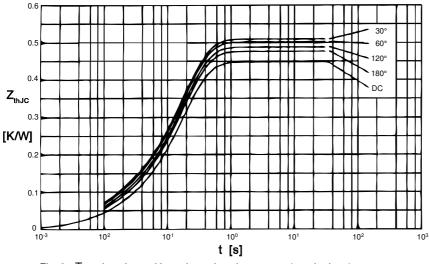
 \mathbf{P}_{tot}

MCD56-08io8B

Rectifier



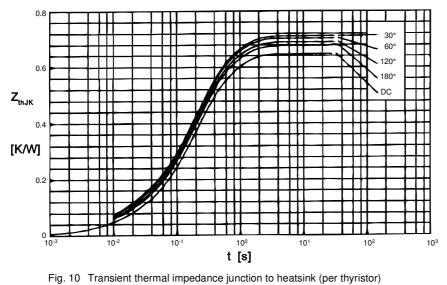




R _{thJC} for vari	ous conduction angles d:
d R	_{hJC} [K/W]
DC	0.450
180°	0.470
120°	0.490
60°	0.505
30°	0.520
Constants for i R_{thi} [K/V	or Z _{thJC} calculation: /] t, [s]
1 0.014	0.0150

1	0.014	0.0150
2	0.026	0.0095
3	0.410	0.1750

Fig. 9 Transient thermal impedance junction to case (per thyristor)



a	R _{thJK} [K/W]	
DC	0.650	
180°	0.670	
120°	0.690	

 R_{thJK} for various conduction angles d:

Constants f	for Z	calculation:
-------------	-------	--------------

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0.705

0.720

i	R _{thi} [K/W]	t _i [s]
1	0.014	0.0150
2	0.026	0.0095
3	0.410	0.1750
4	0.200	0.6700

60°

30°

Fig. 10	I ransient ther	mai impedance	e junction to	neatsink (per tnyr	ISTO

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