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MCF51AG128 ColdFire Microcontroller
Covers: MCF51AG128 and MCF51AG96

MCF51AG128

80 LQFP
14 mm × 14 mm

64 LQFP
10 mm × 10 mm

48 LQFP
7 mm x 7mm

64 QFP
14 mm × 14 mm

The MCF51AG128 is a member of the ColdFire® family of 32-bit variable-length reduced instruction set (RISC) microcontroller. This document provides an overview of the MCF51AG128 series MCUs, focusing on its highly integrated and diverse feature set.

The MCF51AG128 derivative are low-cost, low-power, and high-performance 32-bit ColdFire V1 microcontroller units (MCUs) designed for industrial and appliance applications. It is an ideal upgrade for designs based on the MC9S08AC128 series of 8-bit microcontrollers.

The MCF51AG128 features the following functional units:

- 32-bit Version 1 ColdFire® central processor unit (CPU)
  - Up to 50.33 MHz ColdFire CPU from 2.7 V to 5.5 V
  - Provide 0.94 Dhrystone 2.1 DMIPS per MHz performance when running from internal RAM (0.76 DMIPS per MHz when running from flash)
  - Implements Coldfire Instruction Set Revision C (ISA_C)
- On-chip memory
  - Up to 128 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 16 KB random access memory (RAM)
  - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
  - Three ultra-low power stop modes and reduced power wait mode
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
- System Protection
  - Advanced independent clocked watchdog (WDOG) with features like, robust refresh mechanism, windowed mode, high granulation timeout, fast test of timeout, and always forces a reset
  - Additional external watchdog monitor (EWM) to help reset external circuits

- Low-voltage detection with reset or interrupt
- Separate low voltage warning with selectable trip points
- Illegal opcode and illegal address detection with reset
- Flash block protection for each array to prevent accidental write/erasure
- Hardware CRC module to support fast cyclic redundancy checks
- Debug Support
  - Single-wire back ground debug interface
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger
  - On-chip trace buffer provides programmable start/stop recording conditions
  - Support for real-time program (and optional partial data) trace using the debug visibility bus
- DMA Controller
  - Four independently programmable DMA channels provide the means to directly transfer data between system memory and I/O peripherals
  - DMA enabled peripherals include IIC, SCI, SPI, FTM, HSCMP, ADC, RTC, and eGPIO, and the DMA request from these peripherals can be configured as DMA source or as an iEvent input
- CF1_INTC
  - Support of 44 peripheral I/O interrupt requests and seven software (one per level) interrupt requests
  - Fixed association between interrupt request source, level and priority, up to two requests can be remapped to the highest maskable level and priority
  - Unique vector number for each interrupt source
  - Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance
  - Ability to mask any individual or all interrupt sources
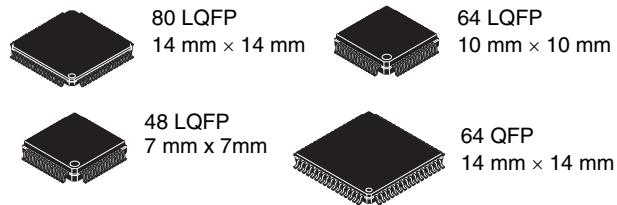
Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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- System Clock Sources
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Frequency-locked-loop (FLL) controlled by internal or external reference; trimmable internal reference allows 0.2% resolution and 2% deviation (1% across 0 to 70 °C)
- Peripherals
  - ADC — 24 analog inputs with 12 bits resolution; output formatted in 12-, 10- or 8-bit right-justified format; single or continuous conversion (automatic return to idle after single conversion); interrupt or DMA request when conversion complete; operation in low-power modes for lower noise operation; asynchronous clock source for lower noise operation; selectable asynchronous hardware conversion triggers from RTC, PDB, or iEvent; dual samples based on hardware triggers during ping-pong mode; on-chip temperature sensor
  - PDB — 16-bit of resolution with prescaler; seven possible trigger events input; positive transition of trigger event signal initiates the counter; support continuous trigger or single shot, bypass mode; supports two triggered delay outputs or ORed together; pulsed output could be used for HSCMP windowing signal
  - iEvent — User programmable combinational boolean output using the four selected iEvent input channels for use as interrupt requests, DMA transfer requests, or hardware triggers
  - FTM — Two 6-channel flexible timer/PWM modules with DMA request option; deadtime insertion is available for each complementary channel pair; channels operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs); 16-bit free-running counter; the load of the FTM registers which have write buffer can be synchronized; write protection for critical registers; backwards compatible with TPM
  - TPM — 16-bit free-running or modulo up/down count operation; two channels, each channel may be input capture, output compare, or edge-aligned PWM; one interrupt per channel plus terminal count interrupt
  - CRC — High speed hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial; error detection for all single, double, odd, and most multi-bit errors; programmable initial seed value
  - HSCMP — Two analog comparators with selectable interrupt on rising edge, falling edge, or either edges of comparator output; the positive and negative inputs of the comparator are both driven from 4-to-1 muxes; programmable voltage reference from two internal DACs; support DMA transfer
  - IIC — Compatible with IIC bus standard and SMBus version 2 features; up to 100 kbps with maximum bus loading; multi-master operation; software programmable for one of 64 different serial clock frequencies; programmable slave address and glitch input filter; interrupt driven byte-by-byte data transfer; arbitration lost interrupt with automatic mode switching from master to slave; calling address identification interrupt; bus busy detection; broadcast and 10-bit address extension; address matching causes wake-up when MCU is in Stop3 mode; DMA support
  - SCI — Two serial communications interface modules with optional 13-bit break; full-duplex, standard non-return-to-zero (NRZ) format; double-buffered transmitter and receiver with separate enables; 13-bit baud rate selection with /32 fractional divide; interrupt-driven or polled operation; hardware parity generation and checking; programmable 8-bit or 9-bit character length; receiver wakeup by idle-line or address-mark; address match feature in receiver to reduce address-mark wakeup ISR overhead; 1/16 bit-time noise detection; DMA transmission for both transmit and receive
  - SPI — Two serial peripheral interfaces with full-duplex or single-wire bidirectional option; double-buffered transmitter and receiver; master or slave mode operation; selectable MSB-first or LSB-first shifting; 8-bit or 16-bit data modes; programmable transmit bit rate; receive data buffer hardware match feature; DMA transmission for transmit and receive
- Input/Output
  - Up to 69 GPIOs and one Input-only pin
  - Interrupt or DMA request with selectable polarity on all input pins
  - Programmable glitch filter, hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
  - Independent pin value register to read logic level on digital pin
  - Up to 16 rapid general purpose I/O (RGPIO) pins connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

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1 MCF51AG128 Family Configurations

1.1 Device Comparison

The following table compares the various device derivatives available within the MCF51AG128 series MCUs.

Table 1. MCF51AG128 Series Device Comparison

Feature	MCF51AG128			MCF51AG96		
	80-pin	**64-pin**	**48-pin**	**80-pin**	**64-pin**	**48-pin**
Flash memory size (KB)	128			96		
RAM size (KB)	16					
ColdFire V1 core with BDM (background debug module)	Yes					
HSCMP (analog comparator)	2	2	1	2	2	1
ADC (analog-to-digital converter) channels (12-bit)	24	19	12	24	19	12
CRC (cyclic redundancy check)	Yes					
DAC	2	2	1	2	2	1
DMA controller	4-ch					
iEvent (intelligent Event module)	Yes					
EWM (External Watchdog Monitor)	Yes					
WDOG (Watchdog timer)	Yes					
RTC	Yes					
DBG (debug module)	Yes					
IIC (inter-integrated circuit)	1	1	No	1	1	No
IRQ (interrupt request input)	Yes					
INTC (interrupt controller)	Yes					
LVD (low-voltage detector)	Yes					
ICS (internal clock source)	Yes					
OSC (crystal oscillator)	Yes					
Port I/O[1]	69	53	39	69	53	39
RGPIO (rapid general-purpose I/O)	16	16	15	16	16	15
SCI (serial communications interface)	2					
SPI1 (serial peripheral interface)	Yes					
SPI2 (serial peripheral interface)	Yes	No	No	Yes	No	No
FTM1 (flexible timer module) channels	6[2]					
FTM2 channels	6[2]					

Feature	MCF51AG128			MCF51AG96		
	80-pin	**64-pin**	**48-pin**	**80-pin**	**64-pin**	**48-pin**
TPM3 (timer pulse-width modulator) channels	2					
Debug Visibility Bus	Yes	No	No	Yes	No	No

1 Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

2 Some pins of FTMx might not be bonded on small package, therefore these channels could be used as soft timer only.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AG128 series pins and modules.

Figure 1. MCF51AG128 Series MCUs Block Diagram

1.3   Features

Table 2 describes the functional units of the MCF51AG128 series.

Table 2. MCF51AG128 Series Functional Units

Functional Unit	Function
CF1Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants, and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provide a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
HSCMP1, HSCMP2 (analog comparators)	Compare two analog inputs
DAC1, DAC2 (digital-to-analog converter)	Provide programmable voltage reference for HSCMPx
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
ICS (internal clock source)	Provides clocking options for the device, including a frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the FLL
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1, SPI2 (8/16-bit serial peripheral interfaces)	Provide 8/16-bit 4-pin synchronous serial interface
DMA	Provides the means to directly transfer data between system memory and I/O peripherals
iEvent	Highly programmable module for creating combinational boolean outputs for use as interrupt requests, DMA transfer requests, or hardware triggers
EWM (External Watchdog Monitor)	Additional watchdog system to help reset external circuits

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Table 2. MCF51AG128 Series Functional Units (continued)

Functional Unit	Function
WDOG (Watchdog timer)	keeps a watch on the system functioning and resets it in case of its failure
RTC (Real Time Counter)	Provides a constant time-base with optional interrupt

1.4   Pin Assignments

This section describes the pin assignments for the available packages.

Figure 2 shows the pinout of the 80-pin LQFP.
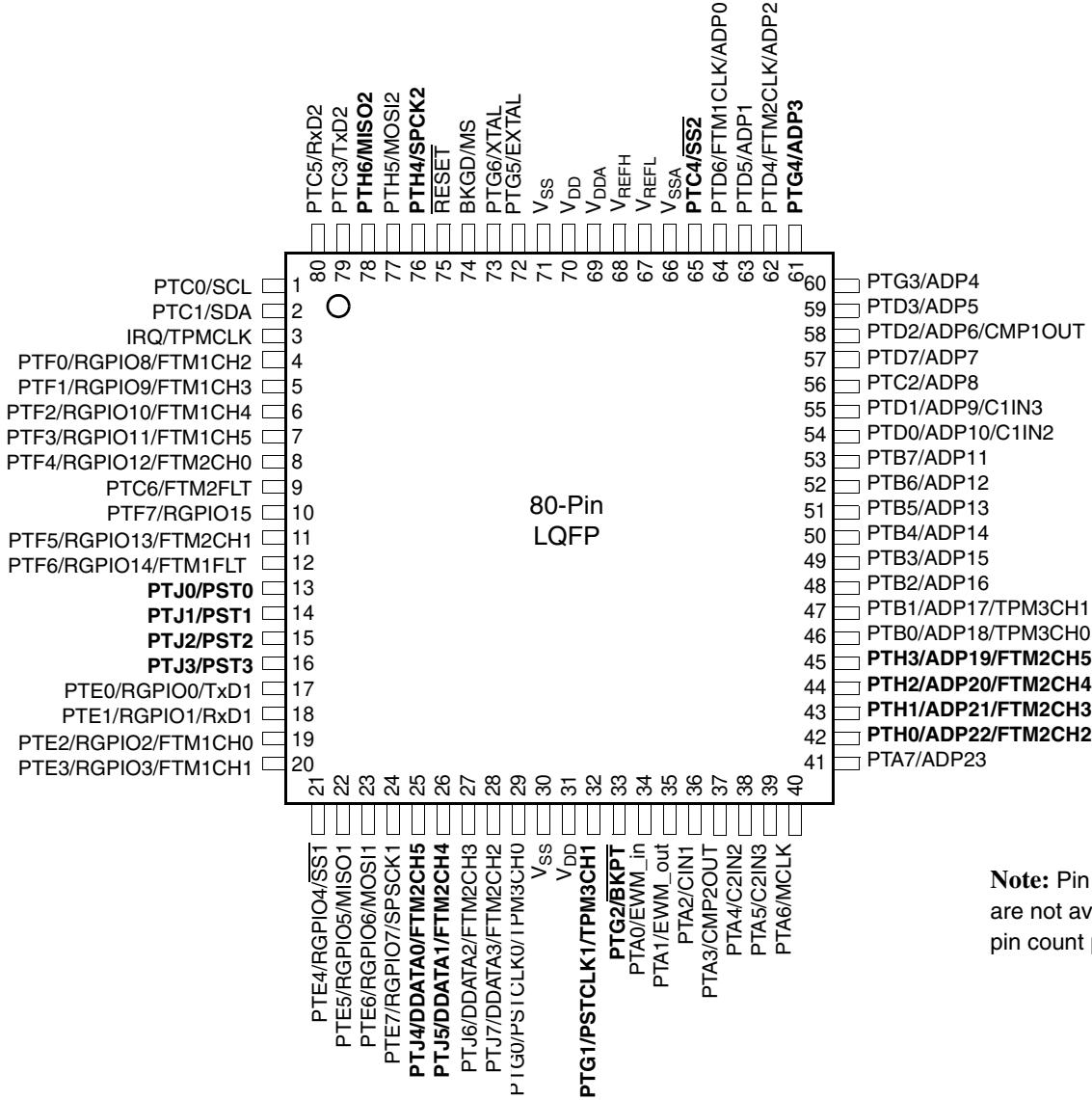
Figure 2. 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.
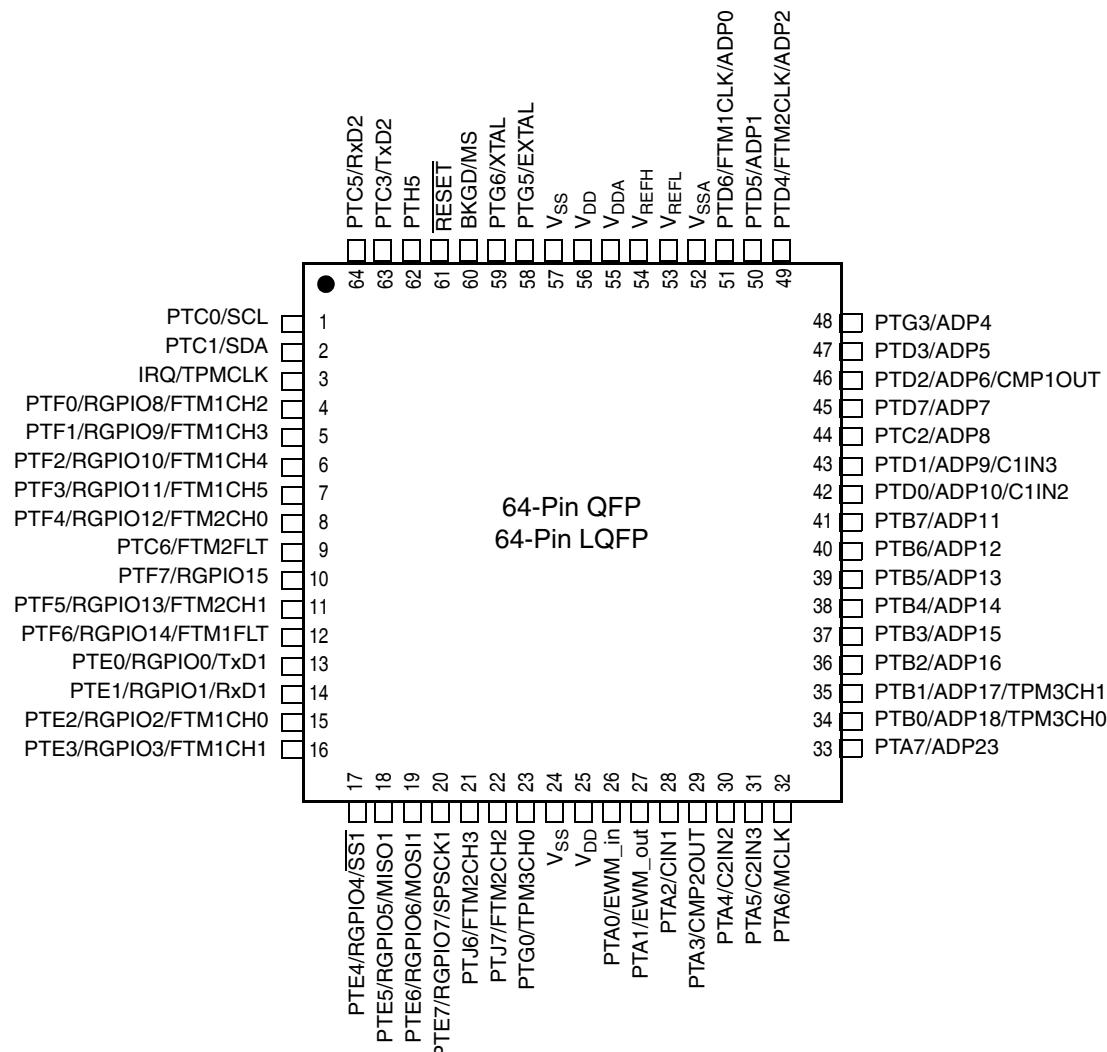
Figure 3. 64-Pin QFP and LQFP

Figure 4 shows the pinout of the 48-pin LQFP.
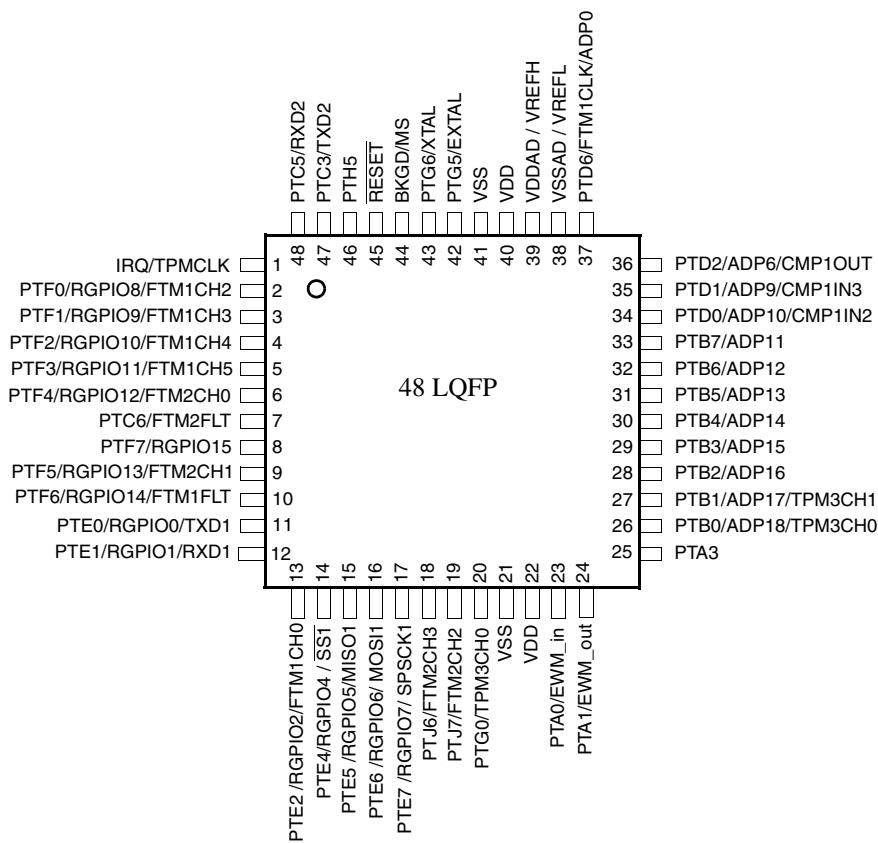
Figure 4. 48-Pin LQFP

Table 3 shows the package pin assignments.

Table 3. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest		
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**
1	1	—	PTC0	SCL	
2	2	—	PTC1	SDA	
3	3	1	IRQ	TPMCLK[1]	
4	4	2	PTF0	RGPIO8	FTM1CH2
5	5	3	PTF1	RGPIO9	FTM1CH3
6	6	4	PTF2	RGPIO10	FTM1CH4
7	7	5	PTF3	RGPIO11	FTM1CH5
8	8	6	PTF4	RGPIO12	FTM2CH0
9	9	7	PTC6	FTM2FLT	
10	10	8	PTF7	RGPIO15	
11	11	9	PTF5	RGPIO13	FTM2CH1
12	12	10	PTF6	RGPIO14	FTM1FLT
13	—	—	PTJ0	PST0	
14	—	—	PTJ1	PST1	
15	—	—	PTJ2	PST2	
16	—	—	PTJ3	PST3	
17	13	11	PTE0	RGPIO0	TxD1
18	14	12	PTE1	RGPIO1	RxD1
19	15	13	PTE2	RGPIO2	FTM1CH0
20	16	—	PTE3	RGPIO3	FTM1CH1
21	17	14	PTE4	RGPIO4	$\overline{SS1}$
22	18	15	PTE5	RGPIO5	MISO1
23	19	16	PTE6	RGPIO6	MOSI1
24	20	17	PTE7	RGPIO7	SPSCK1
25	—	—	PTJ4	DDATA0	FTM2CH5
26	—	—	PTJ5	DDATA1	FTM2CH4
27	21	18	PTJ6	DDATA2	FTM2CH3
28	22	19	PTJ7	DDATA3	FTM2CH2
29	23	20	PTG0	PSTCLK0	TPM3CH0
30	24	21	V_{SS}		
31	25	22	V_{DD}		
32	—	—	PTG1	PSTCLK1	TPM3CH1
33	—	—	PTG2	$\overline{BKPT}$	
34	26	23	PTA0	EWM_in	
35	27	24	PTA1	EWM_out	
36	28	—	PTA2	CIN1	
37	29	25	PTA3	CMP2OUT	
38	30	—	PTA4	C2IN2	
39	31	—	PTA5	C2IN3	
40	32	—	PTA6	MCLK	

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Table 3. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest		
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**
41	33	—	PTA7	ADP23	
42	—	—	PTH0	ADP22	FTM2CH2
43	—	—	PTH1	ADP21	FTM2CH3
44	—	—	PTH2	ADP20	FTM2CH4
45	—	—	PTH3	ADP19	FTM2CH5
46	34	26	PTB0	ADP18	TPM3CH0
47	35	27	PTB1	ADP17	TPM3CH1
48	36	28	PTB2	ADP16	
49	37	29	PTB3	ADP15	
50	38	30	PTB4	ADP14	
51	39	31	PTB5	ADP13	
52	40	32	PTB6	ADP12	
53	41	33	PTB7	ADP11	
54	42	34	PTD0	ADP10	C1IN2
55	43	35	PTD1	ADP9	C1IN3
56	44	—	PTC2	ADP8	
57	45	—	PTD7	ADP7	
58	46	36	PTD2	ADP6	CMP1OUT
59	47	—	PTD3	ADP5	
60	48	—	PTG3	ADP4	
61	—	—	PTG4	ADP3	
62	49	—	PTD4	FTM2CLK	ADP2
63	50	—	PTD5	ADP1	
64	51	37	PTD6	FTM1CLK	ADP0
65	—	—	PTC4	$\overline{SS2}$	
66	52	38	V_{SSA}		
67	53	38	V_{REFL}		
68	54	39	V_{REFH}		
69	55	39	V_{DDA}		
70	56	40	V_{DD}		
71	57	41	V_{SS}		
72	58	42	PTG5	EXTAL	
73	59	43	PTG6	XTAL	
74	60	44	BKGD	MS	
75	61	45	$\overline{RESET}$		
76	—	—	PTH4	SPSCK2	
77	62	46	PTH5	MOSI2	
78	—	—	PTH6	MISO2	
79	63	47	PTC3	TxD2	
80	64	48	PTC5	RxD2	

1 TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of
reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and
TPM3 respectively.

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AG128 series MCUs, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled "C" in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 5. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to 5.8	V
Input voltage	V_{In}	−0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	−55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 6. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	−40 to 105	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s		56	
	2s2p		45	
64-pin QFP				
	1s	θ_{JA}	54	°C/W
	2s2p		41	
64-pin LQFP				
	1s		67	
	2s2p		49	
48-pin LQFP				
	1s		69	
	2s2p		51	

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1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction to Ambient Natural Convection
3. 1s — Single layer board, one signal layer
4. 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$ *Eqn. 1*

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C)$$ *Eqn. 2*

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2$$ *Eqn. 3*

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—

Table 7. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit	—	−2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	±500	—	V
3	Latch-up Current at T_A = 85°C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = −5 mA 3 V, I_{Load} = −1.5 mA 5V, I_{Load} = −3 mA, PTC0 and PTC1 3V, I_{Load} = −1.5 mA, PTC0 and PTC1	V_{OH}	V_{DD} − 1.5 V_{DD} − 0.8 V_{DD} − 0.4 V_{DD} − 0.4	— — — —	— — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = −20 mA 3 V, I_{Load} = −8 mA 5V, I_{Load} = −12 mA, PTC0 and PTC1 3V, I_{Load} = −8 mA, PTC0 and PTC1		V_{DD} − 1.5 V_{DD} − 0.8 V_{DD} − 0.4 V_{DD} − 0.4	— — — —	— — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 1.5 mA 5V, I_{Load} = 3 mA, PTC0 and PTC1 3V, I_{Load} = 1.5 mA, PTC0 and PTC1	V_{OL}	— — — —	— — — —	1.5 0.8 0.4 0.4	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 20 mA 3 V, I_{Load} = 8 mA 5V, I_{Load} = 12 mA, PTC0 and PTC1 3V, I_{Load} = 8 mA, PTC0 and PTC1		— — — —	— — — —	1.5 0.8 0.4 0.4	V
4	C	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	— —	— —	100 60	mA
5	C	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	— —	— —	100 60	mA

Table 9. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
6	P	Input high voltage; all digital inputs	V_{IH}	$0.65 \times V_{DD}$	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	$0.35 \times V_{DD}$	V
8	D	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$	—	—	mV
9	P	Input leakage current; input only pins[2]	$|I_{In}|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[2]	$|I_{OZ}|$	—	0.1	1	μA
11	P	Internal pullup resistors[3] Internal pullup resistorsPTC0 and PTC1	R_{PU}	20 10	45 22	65 32	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t_{POR}	10	—	—	μs

16	P	Low-voltage detection threshold — high range
		  V_{DD} falling
		  V_{DD} rising
			V_{LVD1}	
				
				3.9
				4.0
					
					4.0
					4.1
						
						4.1
						4.2
							V

17	P	Low-voltage detection threshold — low range
		  V_{DD} falling
		  V_{DD} rising
			V_{LVD0}	
				
				2.48
				2.54
					
					2.56
					2.62
						
						2.64
						2.70
							V

18	P	Low-voltage warning threshold — high range 1
		  V_{DD} falling
		  V_{DD} rising
			V_{LVW3}	
				
				4.5
				4.6
					
					4.6
					4.7
						
						4.7
						4.8
							V

19	P	Low-voltage warning threshold — high range 0
		  V_{DD} falling
		  V_{DD} rising
			V_{LVW2}	
				
				4.2
				4.3
					
					4.3
					4.4
						
						4.4
						4.5
							V

20	P	Low-voltage warning threshold low range 1
		  V_{DD} falling
		  V_{DD} rising
			V_{LVW1}	
				
				2.84
				2.90
					
					2.92
					2.98
						
						3.00
						3.06
							V

21	P	Low-voltage warning threshold — low range 0
		  V_{DD} falling
		  V_{DD} rising
			V_{LVW0}	
				
				2.66
				2.72
					
					2.74
					2.80
						
						2.82
						2.88
							V

22	T	Low-voltage inhibit reset/recover hysteresis
		  5 V
		  3 V
			V_{hys}	
				—
				—
					
					100
					60
						
						—
						—
							mV

23	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V

24	D	DC injection current[5][6][7][8] (single pin limit)
		  $V_{IN} > V_{DD}$
		  $V_{IN} < V_{SS}$
			I_{IC}	
				0
				0
					
					—
					—
						
						2
						−0.2
							mA

		DC injection current (Total MCU limit, includes sum of all stressed pins)
		  $V_{IN} > V_{DD}$
		  $V_{IN} < V_{SS}$
				
				0
				0
					
					—
					—
						
						25
						−5
							mA

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[1] Typical values are based on characterization data at 25°C unless otherwise stated.

[2] Measured with $V_{In} = V_{DD}$ or V_{SS}.

[3] Measured with $V_{In} = V_{SS}$.

[4] Measured with $V_{In} = V_{DD}$.

[5] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[6] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[7] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[8] The $\overline{RESET}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.
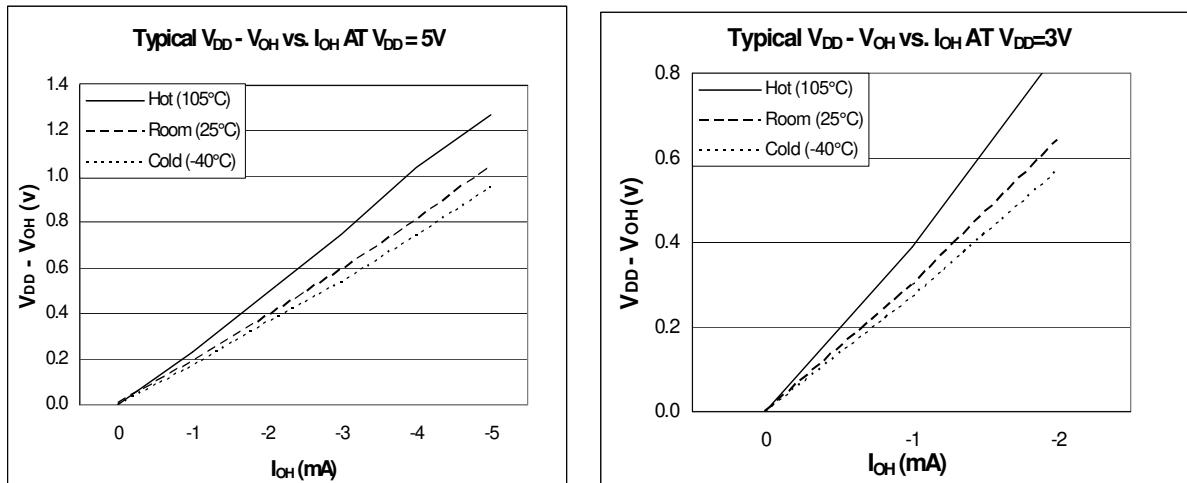

Figure 5. Typical I_{OH} vs. $V_{DD} - V_{OH}$ (Low Drive,PTxDSn = 0)
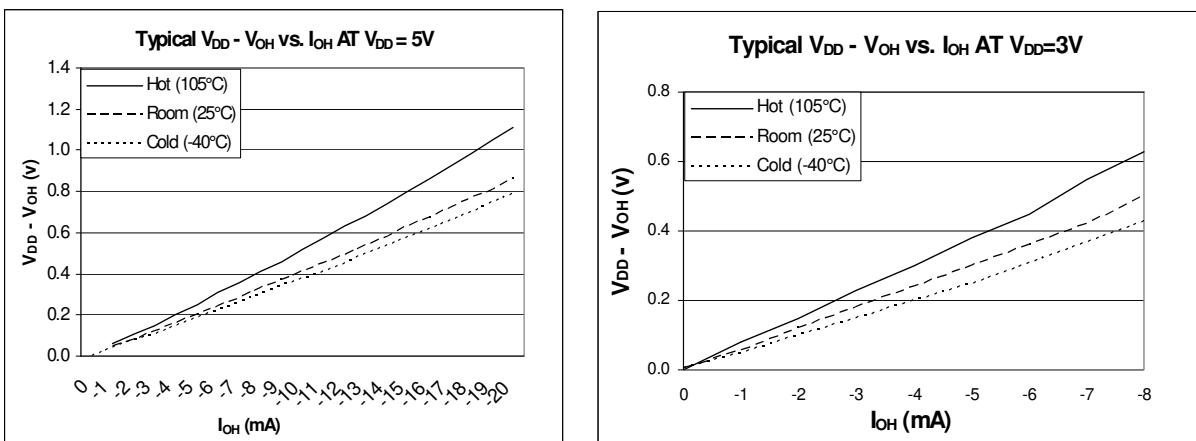
**Figure 6. Typical I_{OH} vs. $V_{DD} - V_{OH}$ (High Drive, PTxDSn = 1)**

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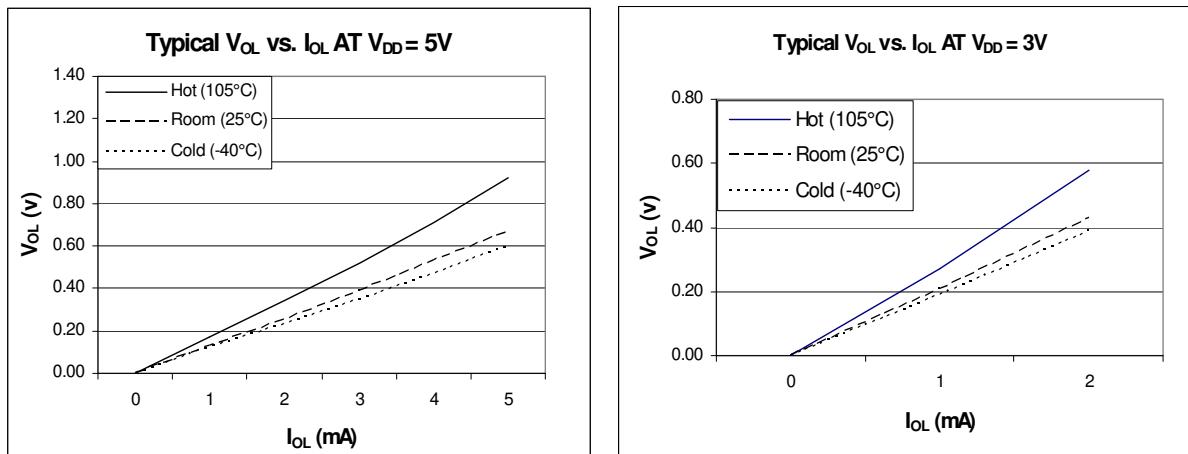
**Figure 7. Typical I$_{OL}$ vs. V$_{OL}$ (Low Drive, PTxDSn = 0)**
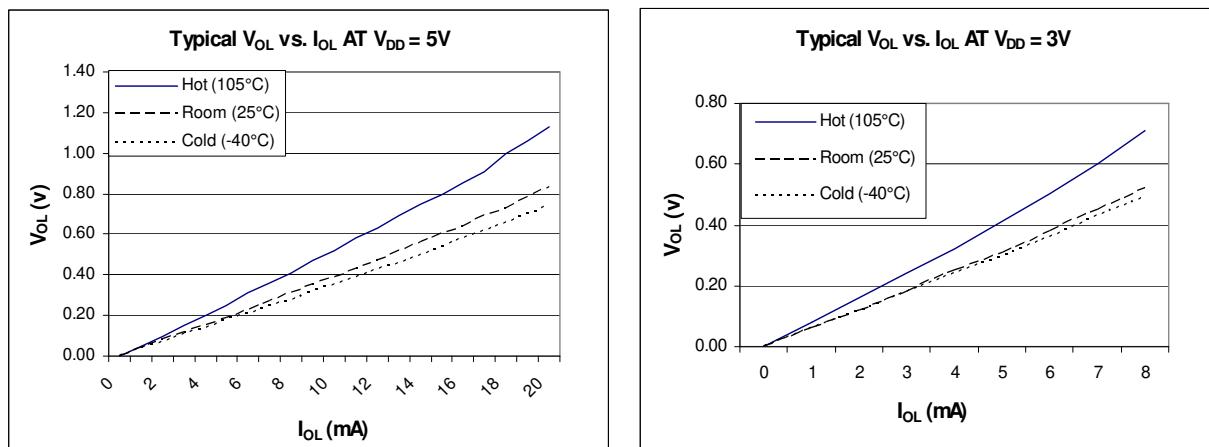
Figure 8. Typical I$_{OL}$ vs. V$_{OL}$ (High Drive, PTxDSn = 1)

2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at 4 MHz CPU clock (All Peripheral Clocks are ON)	RI_{DD}	5	5.8	7	mA
				3	5.7	7	
2	C	Run supply current[3] measured at 16 MHz CPU clock (All Peripheral Clocks are ON)		5	21	25	mA
				3	20.9	25	
3	C	Run supply current[3] measured at 32 MHz CPU clock (All Peripheral Clocks are ON)		5	39.2	50	mA
				3	39.1	50	
4	P	Run supply current[3] measured at 50MHz CPU clock (All Peripheral Clocks are ON)		5	57.9	70	mA
				3	57.8	70	
5	C	Run supply current[3] measured at 4 MHz CPU clock (All Peripheral Clocks are OFF[4])	RI_{DD}	5	4.7	6	mA
				3	4.6	6	
6	C	Run supply current[3] measured at 16 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	16.1	20	mA
				3	15.9	20	
7	C	Run supply current[3] measured at 32 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	29	35	mA
				3	28.9	35	
8	C	Run supply current[3] measured at 50 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	44.1	50	mA
				3	44.0	50	
9	C	Wait supply current[3] measured at 4 MHz CPU clock	WI_{DD}	5	3.2	5	mA
				3	3.2	5	
10	C	Wait supply current[3] measured at 16 MHz CPU clock		5	10.1	13	mA
				3	10	13	
11	C	Wait supply current[3] measured at 32 MHz CPU clock		5	19	25	mA
				3	18.8	25	
12	C	Wait supply current[3] measured at 50 MHz CPU clock		5	29.2	40	mA
				3	29	40	
13	C P C	Stop2 mode supply current −40 °C 25 °C 105 °C	$S2I_{DD}$	5	1.17 1.35 28.6	3 3 40	µA
	C P C	−40 °C 25 °C 105 °C		3	1.0 1.34 26.8	3 3 40	µA

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Table 10. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
14	C P C	Stop3 mode supply current −40 °C 25 °C 105 °C	S3I_{DD}	5	1.2 1.7 43.3	3 3 60	μA
	C P C	−40 °C 25 °C 105 °C		3	1.04 1.6 45.5	3 3 60	μA
15	C P C	Stop4 mode supply current −40 °C 25 °C 105 °C	S4I_{DD}	5	106 109 155	130 130 170	μA
	C P C	−40 °C 25 °C 105 °C		3	95 98 142	130 130 170	μA
16	C	RTC adder to stop2 or stop3[5], 25 °C	S23I_{DDRTC}	5	300	—	nA
				3	300	—	nA
17	C	Adder to stop3 for oscillator enabled[6] (ERCLKEN = 1 and EREFSTEN = 1)	S3I_{DDOSC}	5, 3	5	—	μA

[1] Typicals are measured at 25 °C.

[2] Values given here are preliminary estimates prior to completing characterization.

[3] Code run from flash, FEI mode, and does not include any dc loads on port pins. Bus CLK= (CPU CLK/2)

[4] GPIO filters are working on LPO clock.

[5] Most customers are expected to use auto-wakeup from stop2 or stop3 instead of the higher current wait mode.

[6] Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).
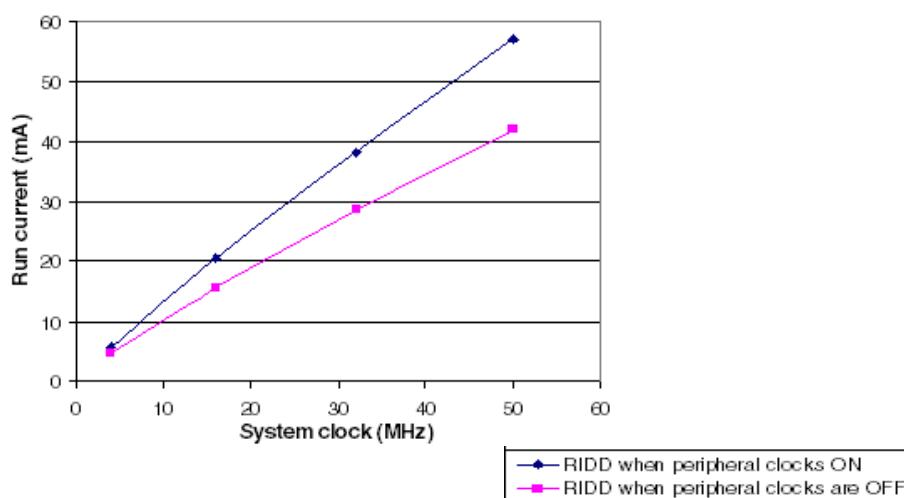

Figure 9. Run Current at Different Conditions

2.7 High Speed Comparator (HSCMP) Electricals

Table 11. HSCMP Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current, high speed mode (EN = 1, PMODE = 1)	I_{DDAHS}	—	200	—	μA
3	T	Supply current, low speed mode (EN = 1, PMODE = 0)	I_{DDALS}	—	20	—	μA
4	—	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
5	D	Analog input offset voltage	V_{AIO}	—	5	40	mV
6	D	Analog Comparator hysteresis	V_H	3.0	9.0	20.0	mV
7	D	Propagation delay, high speed mode (EN = 1, PMODE = 1)	t_{DHS}	—	70	120	ns
8	D	Propagation delay, low speed mode (EN = 1, PMODE = 0)	t_{DLS}	—	400	600	ns
9	D	Analog Comparator initialization delay	t_{AINIT}	—	400	—	ns

2.8 Digital to Analog (DAC) Characteristics

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DDA}	2.7	—	5.5	V
2	D	Supply current (enabled)	I_{DDAC}	—	—	20	μA
3	D	Supply current (stand-by)	I_{DDACS}	—	—	150	nA
4	D	DAC reference input voltage	V_{in1}, V_{in2}	V_{SSA}	—	V_{DDA}	V
5	D	DAC setup delay	t_{PRGST}	—	1000	—	nS
6	D	DAC step size	V_{step}	$3V_{in}/128$	$V_{in}/32$	$5V_{in}/128$	V
7	D	DAC output voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.9 ADC Characteristics

Table 12. 5V 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
			Delta to V_{DD} $(V_{DD} - V_{DDA})$[2]	ΔV_{DDA}	−100	0	100	mV	—
2	D	Ground voltage	Delta to V_{SS} $(V_{SS} - V_{SSA})$[2]	ΔV_{SSA}	−100	0	100	mV	—

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Table 12. 5V 12-bit ADC Operating Conditions (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
3	D	Ref Voltage High	—	V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	—
4	D	Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSA}	V_{SSA}	V	—
5	D	Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
6	C	Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
7	C	Input Resistance	—	R_{ADIN}	—	3	5	kΩ	—
8	C	Analog Source Resistance	12 bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	C		10 bit mode $f_{ADCK} > 4$ MHz $f_{ADCK} < 4$ MHz		— —	— —	5 10		
	C		8 bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	D		Low Power (ADLPC = 1)		0.4	—	4.0		—

[1] Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] DC potential difference.

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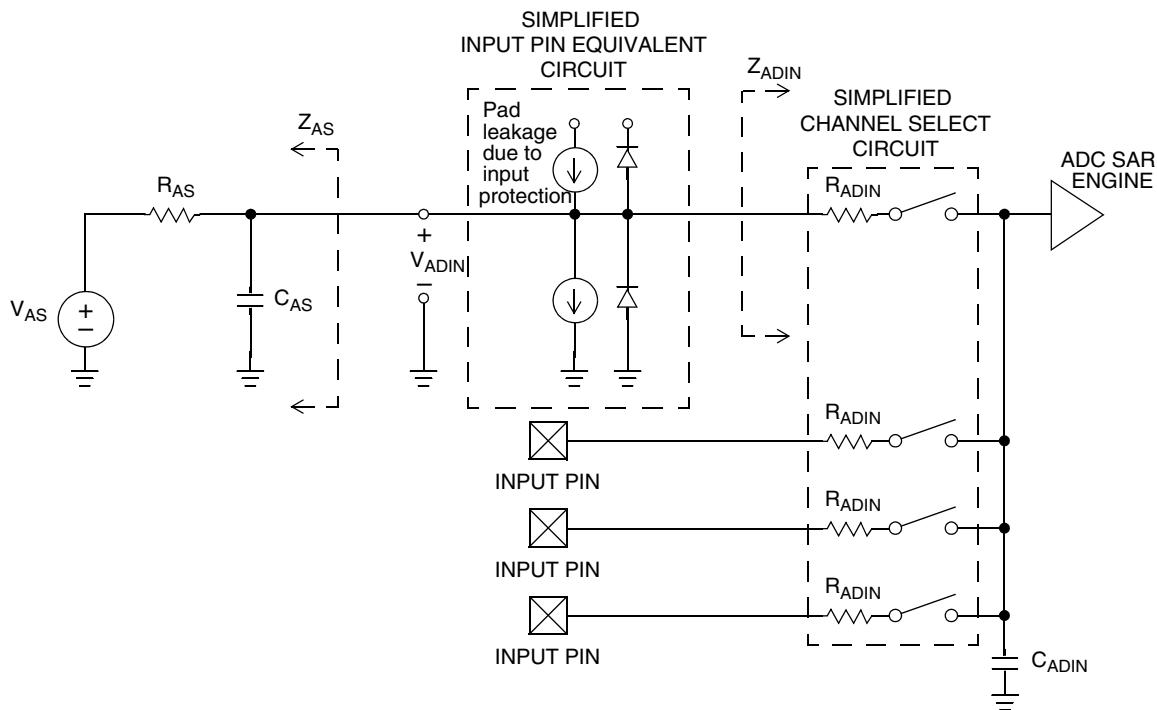
Figure 10. ADC Input Impedance Equivalency Diagram

Table 13. 5 V 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	181	—	μA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	334	—	μA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	385	—	μA	—
4	D	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.717	1	mA	—
5	T	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.065	1	μA	—