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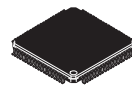
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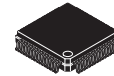
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MCF51JM128



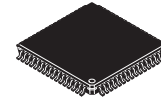
80 LQFP
14 mm × 14 mm



64 LQFP
10 mm × 10 mm



44 LQFP
10 mm × 10 mm



64 QFP
14 mm × 14 mm

MCF51JM128 ColdFire Microcontroller

The MCF51JM128 is a member of the ColdFire family of 32-bit reduced instruction set computing (RISC) microprocessors. This document provides an overview of the MCF51JM128 series, focusing on its highly integrated and diverse feature set.

The MCF51JM128 series is based on the V1 ColdFire core and operates at processor core speeds up to 50.33 MHz. As part of Freescale's Controller Continuum[®], it is an ideal upgrade for designs based on the MC9S08JM60 series of 8-bit microcontrollers.

The MCF51JM128 features the following functional units:

- V1 ColdFire core with background debug module
- Up to 128 KB of flash memory
- Up to 16 KB of static RAM (SRAM)
- Multipurpose clock generator (MCG)
- Dual-role Universal Serial Bus On-The-Go device (USBOTG)
- Controller-area network (MSCAN)
- Cryptographic acceleration unit (CAU)
- Random number generator accelerator (RNGA)
- Analog comparators (ACMP)
- Analog-to-digital converter (ADC) with up to 12 channels
- Two Inter-integrated circuit (IIC) modules
- Two serial peripheral interfaces (SPI)
- Two serial communications interfaces (SCI)
- Carrier modulation timer (CMT)
- Eight-channel timer/pulse-width modulators (TPM)
- Real-time counter (RTC)
- 66 general-purpose input/output (GPIO) modules plus Interrupt request input
- Eight keyboard interrupts (KBI)
- 16-bit Rapid GPIO

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Table of Contents

1	MCF51JM128 Family Configurations	3
1.1	Device Comparison	3
1.2	Block Diagram	4
1.3	Features	5
1.4	Part Numbers	8
1.5	Pinouts and Packaging	10
2	Preliminary Electrical Characteristics	15
2.1	Parameter Classification	15
2.2	Absolute Maximum Ratings	15
2.3	Thermal Characteristics	16
2.4	Electrostatic Discharge (ESD) Protection Characteristics	17
2.5	DC Characteristics	18
2.6	Supply Current Characteristics	21
2.7	Analog Comparator (ACMP) Electricals	23
2.8	ADC Characteristics	23
2.9	External Oscillator (XOSC) Characteristics	26
2.10	MCG Specifications	27
2.11	AC Characteristics	28
2.12	SPI Characteristics	31
2.13	Flash Specifications	34
2.14	USB Electricals	34
2.15	EMC Performance	35
3	Mechanical Outline Drawings	36
3.1	80-pin LQFP	36
3.2	64-pin LQFP	39
3.3	64-pin QFP	42
3.4	44-pin LQFP	45
4	Revision History	48

List of Figures

Figure 1.	MCF51JM128 Block Diagram	4
Figure 2.	80-pin LQFP	10
Figure 3.	64-pin QFP and LQFP	11
Figure 4.	44-pin LQFP	12
Figure 5.	Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)	20
Figure 6.	Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)	20
Figure 7.	Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)	21
Figure 8.	Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)	21
Figure 9.	ADC Input Impedance Equivalency Diagram	24
Figure 10.	Reset Timing	29
Figure 11.	IRQ/KBIPx Timing	29
Figure 12.	Timer External Clock	29

Figure 13.	Timer Input Capture Pulse	30
Figure 14.	SPI Master Timing (CPHA = 0)	32
Figure 15.	SPI Master Timing (CPHA = 1)	32
Figure 16.	SPI Slave Timing (CPHA = 0)	33
Figure 17.	SPI Slave Timing (CPHA = 1)	33
Figure 18.	80-pin LQFP Diagram - I	36
Figure 19.	80-pin LQFP Diagram - II	37
Figure 20.	80-pin LQFP Diagram - III	38
Figure 21.	64-pin LQFP Diagram - I	39
Figure 22.	64-pin LQFP Diagram - II	40
Figure 23.	64-pin LQFP Diagram - III	41
Figure 24.	64-pin QFP Diagram - I	42
Figure 25.	64-pin QFP Diagram - II	43
Figure 26.	64-pin QFP Diagram - III	44
Figure 27.	44-pin LQFP Diagram - I	45
Figure 28.	44-pin LQFP Diagram - II	46
Figure 29.	44-pin LQFP Diagram - III	47

List of Tables

Table 1.	MCF51JM128 Series Device Comparison	3
Table 2.	MCF51JM128 Series Functional Units	5
Table 3.	Orderable Part Number Summary	8
Table 4.	Pin Assignments by Package and Pin Sharing Priority	12
Table 5.	Parameter Classifications	15
Table 6.	Absolute Maximum Ratings	16
Table 7.	Thermal Characteristics	16
Table 8.	ESD and Latch-up Test Conditions	17
Table 9.	ESD and Latch-Up Protection Characteristics	18
Table 10.	DC Characteristics	18
Table 11.	Supply Current Characteristics	21
Table 12.	Analog Comparator Electrical Specifications	23
Table 13.	5 Volt 12-bit ADC Operating Conditions	23
Table 14.	5 Volt 12-bit ADC Characteristics (VREFH = VDDA, VREFL = VSSA)	24
Table 15.	Oscillator Electrical Specifications (Temperature Range = -40 to 105°C Ambient)	26
Table 16.	MCG Frequency Specifications (Temperature Range = -40 to 125°C Ambient)	27
Table 17.	Control Timing	28
Table 18.	TPM Input Timing	29
Table 19.	MSCAN Wake-up Pulse Characteristics	30
Table 20.	SPI Timing	31
Table 21.	Flash Characteristics	34
Table 22.	Internal USB 3.3V Voltage Regulator Characteristics	35
Table 23.	Internal Revision History	50
Table 24.	Changes Between Revisions	51

1 MCF51JM128 Family Configurations

1.1 Device Comparison

The MCF51JM128 series consists of the devices compared in [Table 1](#).

Table 1. MCF51JM128 Series Device Comparison

Feature	MCF51JM128			MCF51JM64			MCF51JM32		
	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin	80-pin	64-pin	44-pin
Flash memory size (KB)	128			64			32		
RAM size (KB)	16			16			16		
V1 ColdFire core with BDM (background debug module)	Yes								
ACMP (analog comparator)	Yes								
ADC channels (12-bit)	12		8	12		8	12		8
CAN (controller area network)	Yes	Yes	No	Yes	Yes	No	Yes	Yes	No
RNGA + CAU	Yes ¹								
CMT (carrier modulator timer)	Yes								
COP (computer operating properly)	Yes								
IIC1 (inter-integrated circuit)	Yes								
IIC2	Yes	No		Yes	No		Yes	No	
IRQ (interrupt request input)	Yes								
KBI (keyboard interrupts)	8	8	6	8	8	6	8	8	6
LVD (low-voltage detector)	Yes								
MCG (multipurpose clock generator)	Yes								
Port I/O ²	66	51	33	66	51	33	66	51	33
RGPIO (rapid general-purpose I/O)	16	6	0	16	6	0	16	6	0
RTC (real-time counter)	Yes								
SCI1 (serial communications interface)	Yes								
SCI2	Yes								
SPI1 (serial peripheral interface)	Yes								
SPI2	Yes								
TPM1 (timer/pulse-width modulator) channels	6	6	4	6	6	4	6	6	4
TPM2 channels	2								
USBOTG (USB On-The-Go dual-role controller)	Yes								
XOSC (crystal oscillator)	Yes								

¹ Only existed on special part number

² Up to 16 pins on Ports A, H, and J are shared with the ColdFire Rapid GPIO module.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51JM128 series pins and modules.

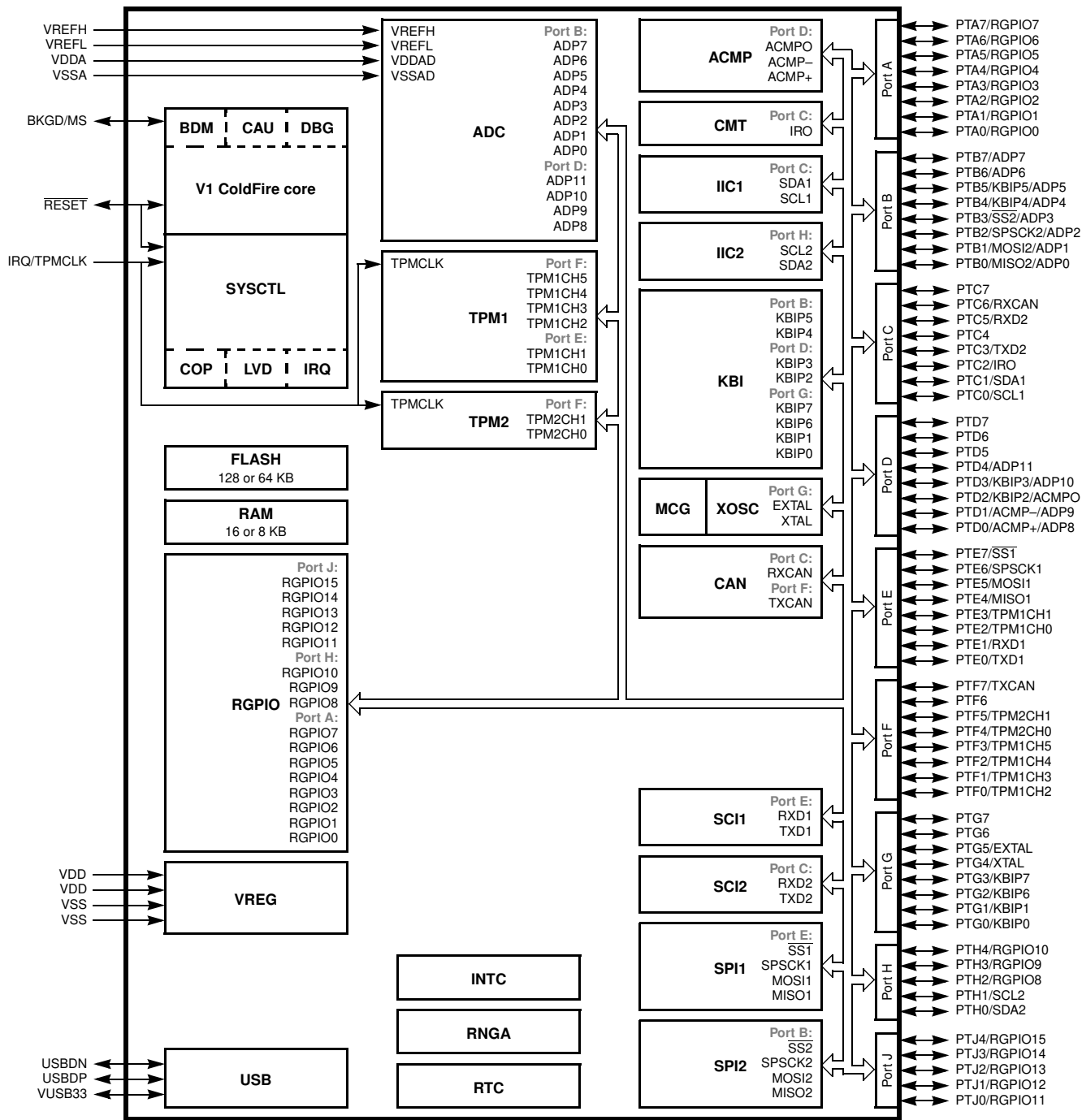


Figure 1. MCF51JM128 Block Diagram

1.3 Features

Table 2 describes the functional units of the MCF51JM128 series.

Table 2. MCF51JM128 Series Functional Units

Unit	Function
CF1CORE (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides a single-pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
SYSCCTL (system control)	Provides LVD, COP, external interrupt request, and so on
FLASH (flash memory)	Provides storage for program code and constants
RAM (random-access memory)	Provides storage for program code, constants, and variables
RGPIO (rapid general-purpose input/output)	Allows I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management throughout the device
USBOTG (USB On-The-Go)	Supports the USB On-The-Go dual-role controller
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
TPM1, TPM2 (timer/pulse-width modulators)	Provide a variety of timing-based features
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
CAU (cryptographic acceleration unit)	Co-processor support for DES, 3DES, AES, MD5, and SHA-1
RNGA (random number generator accelerator)	32-bit random number generator that complies with FIPS-140
RTC (real-time counter)	Provides a constant-time base with optional interrupt
ACMP (analog comparator)	Compares two analog inputs
CMT (carrier modulator timer)	Infrared output used for the Remote Controller
IIC1, IIC2 (inter-integrated circuits)	Supports the standard IIC communications protocol
KBI (keyboard interrupt)	Provides pin interrupt capabilities
MCG (multipurpose clock generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources
XOSC (crystal oscillator)	Supports low/high range crystals
CAN (controller area network)	Supports standard CAN communications protocol
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs that can support RS-232 and LIN protocols
SPI1, SPI2 (serial peripheral interfaces)	Provide a 4-pin synchronous serial interface

1.3.1 Feature List

- 32-bit Version 1 ColdFire Central Processor Unit (CPU)
 - Up to 50.33 MHz at 2.7 V – 5.5 V
 - Performance (Dhrystone 2.1):
 - 0.94 Dhrystone 2.1 MIPS per MHz when running from internal RAM
 - 0.76 Dhrystone 2.1 MIPS per MHz when running from flash
 - Implements Instruction Set Revision C (ISA_C)
 - Supports up to 30 peripheral interrupt requests and seven software interrupts
- On-chip memory
 - Up to 128 KB Flash memory with read/program/erase over full operating voltage and temperature range
 - Up to 16 KB static random access memory (RAM)
 - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-saving modes
 - Two low-power stop plus wait modes
 - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents; this behavior allows clocks to remain enabled to specific peripherals in Stop3 mode
 - Very lower power real-time counter for use in run, wait, and stop modes with internal and external clock sources
- Four Clock Source Options
 - Oscillator (XOSC) — Loop-control Pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - FLL/PLL controlled by internal or external reference
 - Trimmable internal reference allows 0.2% resolution and 2% deviation
- System protection features
 - Watchdog computer operating properly (COP) reset with option to run from dedicated 1 kHz internal clock source or bus clock
 - Low-voltage detection with reset or interrupt; selectable trip points
 - Illegal opcode and illegal address detection with programmable reset or exception response
 - Flash block protection
- Debug support
 - Single-wire Background debug interface
 - 4 Program Counters plus two address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
 - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Universal Serial Bus (USB) On-The-Go dual-role controller
 - Full-speed USB device controller
 - Fully compliant with USB specification 1.1 and 2.0
 - 16 bidirectional endpoints, with double buffering to provide the maximum throughput
 - Supports control, bulk, interrupt, and isochronous endpoints
 - Supports bus-powered capability with low-power consumption
 - Full-speed / low-speed host controller
 - Host mode allows control, bulk, interrupt, and isochronous transfers
 - OTG protocol logic
 - On-chip USB transceiver
 - On-chip 3.3 V USB regulator and pull-up resistors save system cost

- Controller area network (MSCAN)
 - Implementation of the CAN protocol — Version 2.0A/B
 - Five receive buffers with FIFO storage scheme
 - Three transmit buffers with internal prioritization using a “local priority” concept
 - Flexible maskable identifier filter programmable as 2x32-bit, 4x16-bit, or 8x8-bit
 - Programmable wakeup functionality with integrated low-pass filter
 - Programmable loopback mode supports self-test operation
 - Programmable bus-off recovery functionality
 - Internal timer for time-stamping of received and transmitted messages
- Cryptographic acceleration unit (CAU)
 - Co-processor support of DES, 3DES, AES, MD5, and SHA-1
- Random number generator accelerator (RNGA)
 - 32-bit random number generator that complies with FIPS-140
- Analog-to-digital converter (ADC)
 - 12-channel, 12-bit resolution
 - Output formatted in 12-, 10-, or 8-bit right-justified format
 - Single or continuous conversion, and selectable asynchronous hardware conversion trigger
 - Operation in Stop3 mode
 - Automatic compare function
 - Internal temperature sensor
- Analog comparators (ACMP)
 - Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
 - Option to compare to fixed internal bandgap reference voltage
 - Option to route output to TPM module
 - Operation in Stop3 mode
- Inter-integrated circuit (IIC)
 - Up to 100 kbps with maximum bus loading
 - Multi-master operation
 - Programmable slave address
 - Supports broadcast mode and 10-bit address extension
- Serial communications interfaces (SCI)
 - Two SCIs with full-duplex, non-return-to-zero (NRZ) format
 - LIN master extended break generation
 - LIN slave extended break detection
 - Programmable 8-bit or 9-bit character length
 - Wake up on active edge
- Serial peripheral interfaces (SPI)
 - Two serial peripheral interfaces with full-duplex or single-wire bidirectional
 - Double-buffered transmit and receive
 - Programmable transmit bit rate, phase, polarity, and Slave Select output
 - MSB-first or LSB-first shifting
- Timer/pulse width modulator (TPM)
 - 16-bit free-running or modulo up/down count operation
 - Up to eight channels, where each channel can be an input capture, output compare, or edge-aligned PWM
 - One interrupt per channel plus terminal count interrupt

MCF51JM128 Family Configurations

- RTC
 - 8-bit modulus counter with binary- or decimal-based prescaler
 - External clock source for precise time base, time-of-day, calendar or task scheduling functions
 - Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Carrier modulator timer (CMT)
 - carrier generator, modulator, and transmitter drive the infrared out (IRO) pin
 - operation in independent high/low time control, baseband, FSK, and direct IRO control modes
- Input/Output
 - 66 GPIOs
 - Eight keyboard interrupt pins with selectable polarity
 - Hysteresis and configurable pull-up device on all input pins; configurable slew rate and drive strength on all output pins
 - 16 bits of Rapid GPIO connected to the processor's local 32-bit platform bus with set, clear, and faster toggle functionality

1.4 Part Numbers

Table 3. Orderable Part Number Summary

Freescal Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51JM128EVLK	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	80 LQFP	-40 to +105 °C
MCF51JM128VLK	MCF51JM128 ColdFire Microcontroller	128 / 16	80 LQFP	-40 to +105 °C
MCF51JM128EVLH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 LQFP	-40 to +105 °C
MCF51JM128VLH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 LQFP	-40 to +105 °C
MCF51JM128EVQH	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	64 QFP	-40 to +105 °C
MCF51JM128VQH	MCF51JM128 ColdFire Microcontroller	128 / 16	64 QFP	-40 to +105 °C
MCF51JM128EVL D	MCF51JM128 ColdFire Microcontroller with CAU and RNGA Enabled	128 / 16	44 LQFP	-40 to +105 °C
MCF51JM128VLD	MCF51JM128 ColdFire Microcontroller	128 / 16	44 LQFP	-40 to +105 °C
MCF51JM64EVLK	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	80 LQFP	-40 to +105 °C
MCF51JM64VLK	MCF51JM64 ColdFire Microcontroller	64 / 16	80 LQFP	-40 to +105 °C
MCF51JM64EVLH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 LQFP	-40 to +105 °C
MCF51JM64VLH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 LQFP	-40 to +105 °C
MCF51JM64EVQH	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	64 QFP	-40 to +105 °C
MCF51JM64VQH	MCF51JM64 ColdFire Microcontroller	64 / 16	64 QFP	-40 to +105 °C

Table 3. Orderable Part Number Summary (continued)

MCF51JM64EVLD	MCF51JM64 ColdFire Microcontroller with CAU and RNGA Enabled	64 / 16	44 LQFP	-40 to +105 °C
MCF51JM64VLD	MCF51JM64 ColdFire Microcontroller	64 / 16	44 LQFP	-40 to +105 °C
MCF51JM32EVLK	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	80 LQFP	-40 to +105 °C
MCF51JM32VLK	MCF51JM32 ColdFire Microcontroller	32 / 16	80 LQFP	-40 to +105 °C
MCF51JM32EVLH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 LQFP	-40 to +105 °C
MCF51JM32VLH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 LQFP	-40 to +105 °C
MCF51JM32EVQH	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	64 QFP	-40 to +105 °C
MCF51JM32VQH	MCF51JM32 ColdFire Microcontroller	32 / 16	64 QFP	-40 to +105 °C
MCF51JM32EVLD	MCF51JM32 ColdFire Microcontroller with CAU and RNGA Enabled	32 / 16	44 LQFP	-40 to +105 °C
MCF51JM32VLD	MCF51JM32 ColdFire Microcontroller	32 / 16	44 LQFP	-40 to +105 °C

1.5 Pinouts and Packaging

Figure 2 shows the pinout of the 80-pin LQFP.

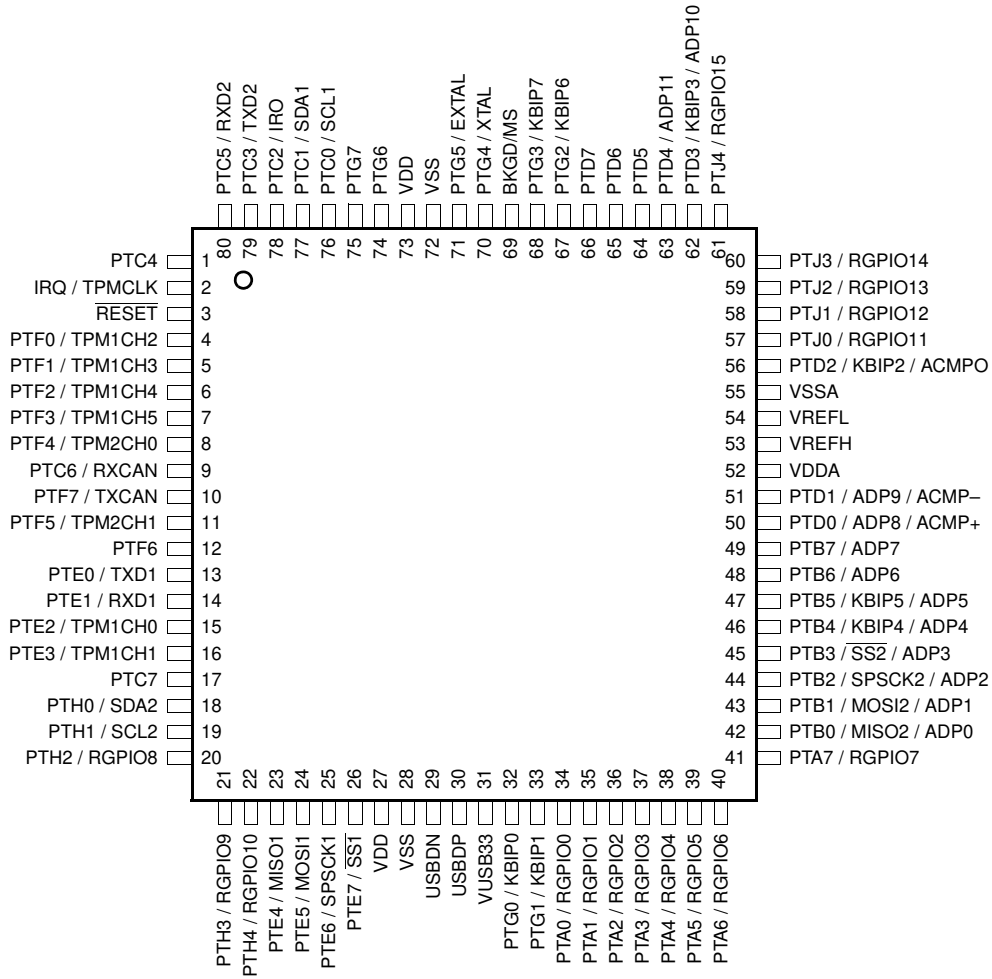


Figure 2. 80-pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

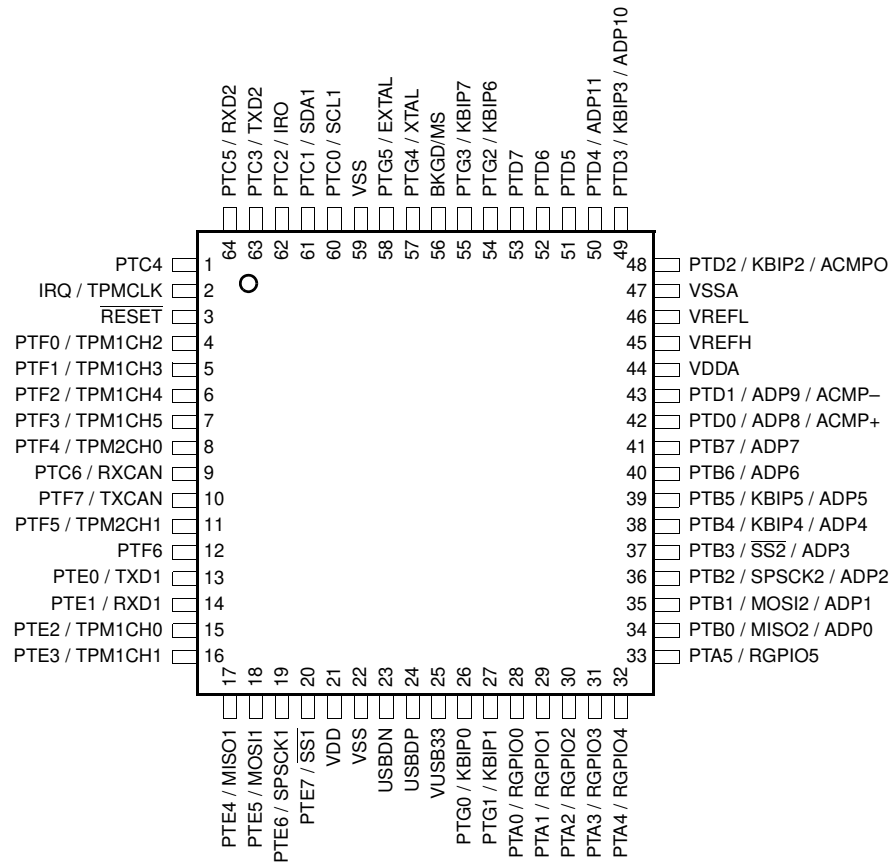


Figure 3. 64-pin QFP and LQFP

MCF51JM128 Family Configurations

Figure 4 shows the pinout of the 44-pin LQFP.

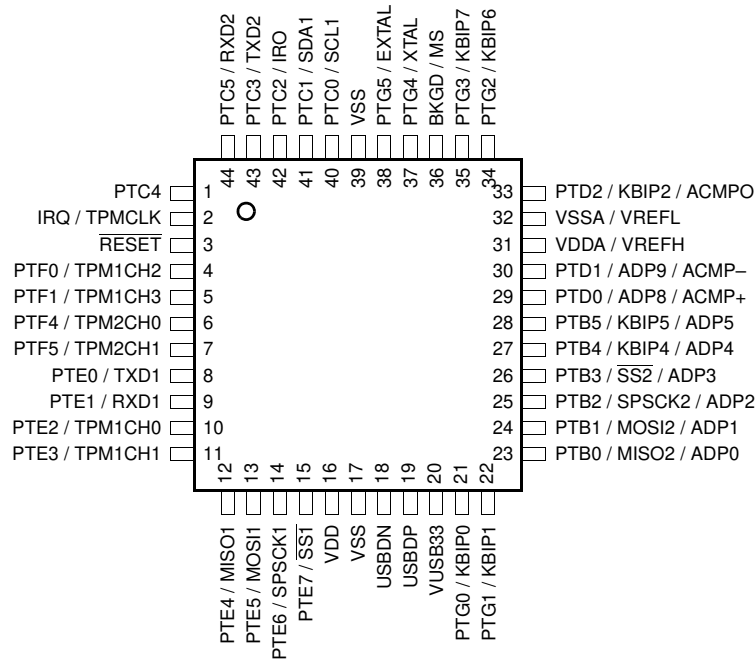


Figure 4. 44-pin LQFP

Table 4 shows the package pin assignments.

Table 4. Pin Assignments by Package and Pin Sharing Priority

Pin Number			<-- Lowest Priority --> Highest		
80	64	44	Port Pin	Alt 1	Alt 2
1	1	1	PTC4		—
2	2	2	—	IRQ	TPMCLK
3	3	3	—	RESET	—
4	4	4	PTF0	TPM1CH2	—
5	5	5	PTF1	TPM1CH3	—
6	6	—	PTF2	TPM1CH4	—
7	7	—	PTF3	TPM1CH5	—
8	8	6	PTF4	TPM2CH0	BUSCLK_OUT
9	9	—	PTC6	RXCAN	—
10	10	—	PTF7	TXCAN	—
11	11	7	PTF5	TPM2CH1	—
12	12	—	PTF6	—	—
13	13	8	PTE0	TXD1	—
14	14	9	PTE1	RXD1	—
15	15	10	PTE2	TPM1CH0	—

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest Priority --> Highest		
80	64	44	Port Pin	Alt 1	Alt 2
16	16	11	PTE3	TPM1CH1	—
17	—	—	PTC7	—	—
18	—	—	PTH0	SDA2	—
19	—	—	PTH1	SCL2	—
20	—	—	PTH2	RGPIO8	—
21	—	—	PTH3	RGPIO9	—
22	—	—	PTH4	RGPIO10	—
23	17	12	PTE4	MISO1	—
24	18	13	PTE5	MOSI1	—
25	19	14	PTE6	SPSCK1	—
26	20	15	PTE7	$\overline{SS1}$	—
27	21	16	—	—	VDD
28	22	17	—	—	VSS
29	23	18	—	—	USB _{BDN}
30	24	19	—	—	USB _{BDP}
31	25	20	—	—	VUSB33
32	26	21	PTG0	KBIP0	USB_ALT_CLK
33	27	22	PTG1	KBIP1	—
34	28	—	PTA0	RGPIO0	USB_SESSVLD
35	29	—	PTA1	RGPIO1	USB_SESEND
36	30	—	PTA2	RGPIO2	USB_VBUSVLD
37	31	—	PTA3	RGPIO3	USB_PULLUP(D+)
38	32	—	PTA4	RGPIO4	USB_DM_DOWN
39	33	—	PTA5	RGPIO5	USB_DP_DOWN
40	—	—	PTA6	RGPIO6	USB_ID
41	—	—	PTA7	RGPIO7	—
42	34	23	PTB0	MISO2	ADP0
43	35	24	PTB1	MOSI2	ADP1
44	36	25	PTB2	SPSCK2	ADP2
45	37	26	PTB3	$\overline{SS2}$	ADP3
46	38	27	PTB4	KBIP4	ADP4
47	39	28	PTB5	KBIP5	ADP5
48	40	—	PTB6	ADP6	—

Table 4. Pin Assignments by Package and Pin Sharing Priority (continued)

Pin Number			<-- Lowest Priority --> Highest		
80	64	44	Port Pin	Alt 1	Alt 2
49	41	—	PTB7	ADP7	—
50	42	29	PTD0	ADP8	ACMP+
51	43	30	PTD1	ADP9	ACMP-
52	44	31	—	—	VDDA
53	45		—	—	VREFH
54	46	32	—	—	VREFL
55	47		—	—	VSSA
56	48	33	PTD2	KBIP2	ACMPO
57	—	—	PTJ0	RGPIO11	—
58	—	—	PTJ1	RGPIO12	—
59	—	—	PTJ2	RGPIO13	—
60	—	—	PTJ3	RGPIO14	—
61	—	—	PTJ4	RGPIO15	—
62	49	—	PTD3	KBIP3	ADP10
63	50	—	PTD4	ADP11	—
64	51	—	PTD5	—	—
65	52	—	PTD6	—	—
66	53	—	PTD7	—	—
67	54	34	PTG2	KBIP6	—
68	55	35	PTG3	KBIP7	—
69	56	36	—	BKGD	MS
70	57	37	PTG4	XTAL	—
71	58	38	PTG5	EXTAL	—
72	59	39	—	—	VSS
73	—	—	—	—	VDD
74	—	—	PTG6	—	—
75	—	—	PTG7	—	—
76	60	40	PTC0	SCL1	—
77	61	41	PTC1	SDA1	—
78	62	42	PTC2	IRO	—
79	63	43	PTC3	TXD2	—
80	64	44	PTC5	RXD2	—

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JM128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 5. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled C in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 6](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, V_{SS} or V_{DD}).

Table 6. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to + 5.8	V
Input voltage	V_{In}	- 0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current (applies to all port pins) ^{1, 2, 3} Single pin limit	I_D	± 25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	-55 to +150	°C
Maximum junction temperature	T_J	150	°C

- ¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.
- ² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .
- ³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load shunt current is greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples: if no system clock is present or if the clock rate is low, which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is small.

Table 7. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	-40 to +105	°C
Thermal resistance ^{1,2,3,4}			
80-pin LQFP			
	1s	52	
	2s2p	40	
64-pin LQFP			
	1s	65	
	2s2p	47	
64-pin QFP	θ_{JA}		°C/W
	1s	54	
	2s2p	40	
44-pin LQFP			
	1s	69	
	2s2p	48	

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- ² Junction to Ambient Natural Convection

- ³ 1s - Single Layer Board, one signal layer
- ⁴ 2s2p - Four Layer Board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \tag{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
 θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
 $P_D = P_{int} + P_{I/O}$
 $P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
 $P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \tag{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \tag{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations 1 and 2 iteratively for any value of T_A .

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (<http://www.aecouncil.com/>) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 8. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	–	3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table 9. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	+/- 2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	+/- 500	—	V
3	Latch-up Current at $T_A = 105^\circ\text{C}$	I_{LAT}	+/- 100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 10. DC Characteristics

Num	C	Parameter	Symbol	Min	Typ ¹	Max	Unit
1		Operating voltage ²		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = -4$ mA 3 V, $I_{Load} = -2$ mA 5 V, $I_{Load} = -2$ mA 3 V, $I_{Load} = -1$ mA	V_{OH}	$V_{DD} - 1.5$	—	—	V
		$V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$		— — —	— — —		
3	P	Output high voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = -15$ mA 3 V, $I_{Load} = -8$ mA 5 V, $I_{Load} = -8$ mA 3 V, $I_{Load} = -4$ mA	V_{OH}	$V_{DD} - 1.5$	—	—	V
		$V_{DD} - 1.5$ $V_{DD} - 0.8$ $V_{DD} - 0.8$		— — —	— — —		
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, $I_{Load} = 4$ mA 3 V, $I_{Load} = 2$ mA 5 V, $I_{Load} = 2$ mA 3 V, $I_{Load} = 1$ mA	V_{OL}		—	1.5	V
				—	1.5		
4	P	Output low voltage — High Drive (PTxDSn = 1) 5 V, $I_{Load} = 15$ mA 3 V, $I_{Load} = 8$ mA 5 V, $I_{Load} = 8$ mA 3 V, $I_{Load} = 4$ mA	V_{OL}		—	0.8	V
				—	0.8		
4	P	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	— —	— —	100 60	mA
5	P	Output low current — Max total I_{OL} for all ports 5V 3V	I_{OLT}	— —	— —	100 60	mA
6	P	Input high voltage; all digital inputs	V_{IH}				V
		$V_{DD} = 5\text{V}$ $V_{DD} = 3\text{V}$		3.25 2.10	— —	— —	

Table 10. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typ ¹	Max	Unit
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	1.75 1.05	V
		$V_{DD} = 5V$ $V_{DD} = 3V$					
8	P	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$			mV
9	P	Input leakage current; input only pins ³	$ I_{In} $	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current ³	$ I_{OZ} $	—	0.1	1	μA
11	P	Internal pullup resistors ⁴	R_{PU}	20	45	65	k Ω
12	P	Internal pulldown resistors ⁵	R_{PD}	20	45	65	k Ω
13		Internal pullup resistor to USBDP (to V_{USB33})	R_{PUPD}	900 1425	1300 2400	1575 3090	k Ω
		Idle Transmit					
14	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
15	D	RAM retention voltage ⁶	V_{RAM}	—	0.6	1.0	V
16	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
17	D	POR rearm time	t_{POR}	10	—	—	μs
18	P	Low-voltage detection threshold — high range	V_{LVD1}	3.9 4.0	4.0 4.1	4.1 4.2	V
		V_{DD} falling V_{DD} rising					
19	P	Low-voltage detection threshold — low range	V_{LVD0}	2.48 2.54	2.56 2.62	2.64 2.70	V
		V_{DD} falling V_{DD} rising					
20	C	Low-voltage warning threshold — high range 1	V_{LVW3}	4.5 4.6	4.6 4.7	4.7 4.8	V
		V_{DD} falling V_{DD} rising					
21	P	Low-voltage warning threshold — high range 0	V_{LVW2}	4.2 4.3	4.3 4.4	4.4 4.5	V
		V_{DD} falling V_{DD} rising					
22	P	Low-voltage warning threshold low range 1	V_{LVW1}	2.84 2.90	2.92 2.98	3.00 3.06	V
		V_{DD} falling V_{DD} rising					
23	C	Low-voltage warning threshold — low range 0	V_{LVW0}	2.66 2.72	2.74 2.80	2.82 2.88	V
		V_{DD} falling V_{DD} rising					
24	T	Low-voltage inhibit reset/recover hysteresis	V_{hys}	— —	100 60	— —	mV
		5 V 3 V					

Preliminary Electrical Characteristics

- 1 Typical values are based on characterization data at 25°C unless otherwise stated.
- 2 Operating voltage with USB enabled can be found in [Section 2.14, "USB Electricals."](#)
- 3 Measured with $V_{In} = V_{DD}$ or V_{SS} .
- 4 Measured with $V_{In} = V_{SS}$.
- 5 Measured with $V_{In} = V_{DD}$.
- 6 This is the voltage below which the contents of RAM are not guaranteed to be maintained.

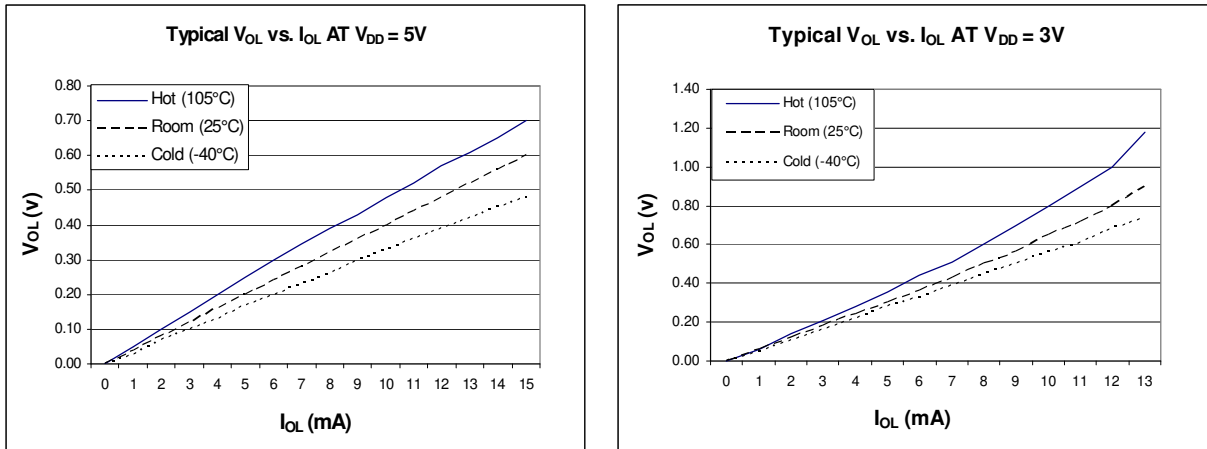


Figure 5. Typical Low-side Drive (sink) characteristics – High Drive (PTxDSn = 1)

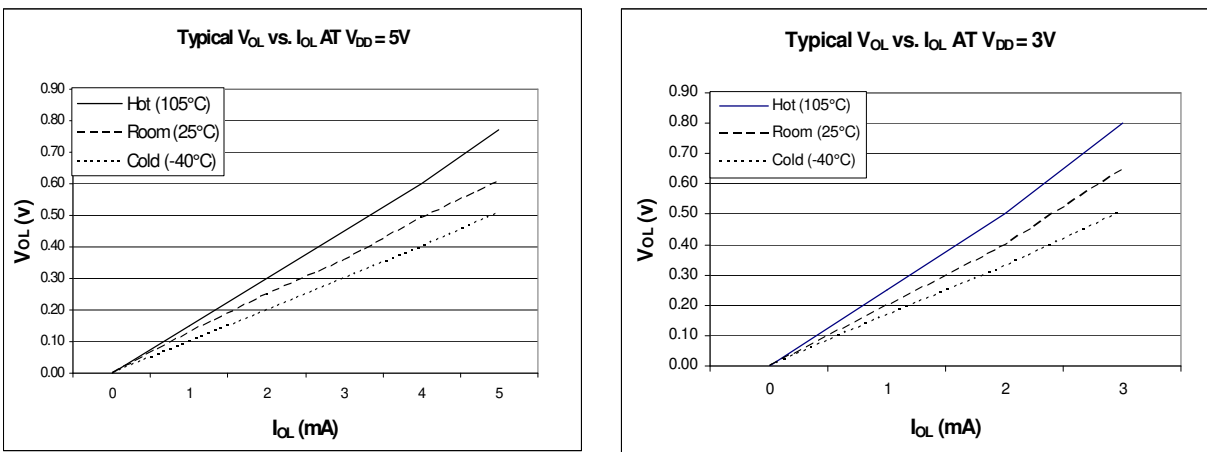


Figure 6. Typical Low-side Drive (sink) characteristics – Low Drive (PTxDSn = 0)

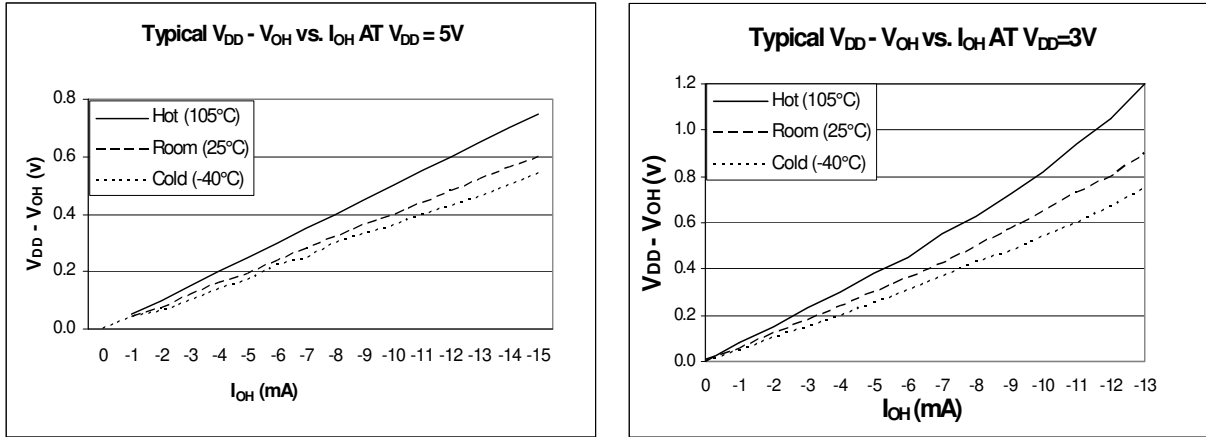


Figure 7. Typical High-side Drive (source) characteristics – High Drive (PTxDSn = 1)

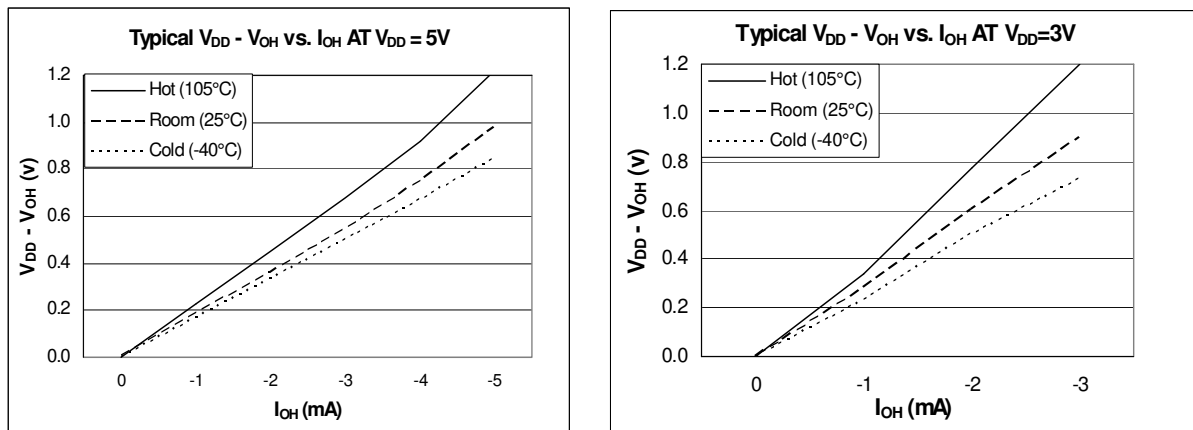


Figure 8. Typical High-side Drive (source) characteristics – Low Drive (PTxDSn = 0)

2.6 Supply Current Characteristics

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical ¹	Max ²	Unit
1	C	Run supply current ³ measured at (CPU clock = 2 MHz, $f_{BUS} = 1$ MHz)	$R_{I_{DD}}$	5	4.0	7	mA
				3	4.0	7	
2	P	Run supply current ³ measured at (CPU clock = 16 MHz, $f_{BUS} = 8$ MHz)		5	19	30	mA
				3	18.7	30	
3	C	Run supply current ³ measured at (CPU clock = 48 MHz, $f_{BUS} = 24$ MHz)		5	45	70	mA
				3	44	70	

Table 11. Supply Current Characteristics

Num	C	Parameter	Symbol	V _{DD} (V)	Typical ¹	Max ²	Unit	
4	C	Wait mode supply current ³ measured at (CPU clock = 2 MHz, f _{BUS} = 1 MHz)	W _I DD	5	2.03	3	mA	
				3	2	3		
5	C	Wait mode supply current ³ measured at (CPU clock = 16 MHz, f _{BUS} = 8 MHz)	W _I DD	5	7.73	12	mA	
				3	7.7	12		
6	C	Wait mode supply current ³ measured at (CPU clock = 48 MHz, f _{BUS} = 24 MHz)	W _I DD	5	22	30	mA	
				3	21.9	30		
7	C	Stop2 mode supply current	S2 _I DD	5	1.35	3	μA	
						3		3
				3	1.25	3		
						3		35
8	P	Stop3 mode supply current	S3 _I DD	5	1.41	3	μA	
						3		3
				3	1.35	3		
						3		35
9	C	Stop4 mode supply current	S4 _I DD	5	106	200	μA	
						3		96
				5	300	—		nA
						3		
11	P	Adder to stop3 for oscillator enabled ⁵ (ERCLKEN = 1 and EREFSTEN = 1)	S23 _I DDOSC	5	5	—	μA	
				3	5	—		

¹ Typicals are measured at 25°C.

² Values given here are preliminary estimates prior to completing characterization.

³ All modules' clocks are switched on, code runs from flash, in FEI mode, and there are no DC loads on port pins.

⁴ Most customers are expected to find that auto-wakeup from stop2 or stop3 can be used instead of the higher current wait mode.

⁵ Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0)

2.7 Analog Comparator (ACMP) Electricals

Table 12. Analog Comparator Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1		Supply voltage	V_{DD}	2.7	—	5.5	V
2		Supply current (active)	I_{DDAC}	—	20	35	μA
3		Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DD}	V
4		Analog input offset voltage	V_{AIO}		20	40	mV
5		Analog Comparator hysteresis	V_H	3.0	6.0	20.0	mV
6		Analog input leakage current	I_{ALKG}	--	--	1.0	μA
7		Analog Comparator initialization delay	t_{AINIT}	—	—	1.0	μs
8		Bandgap Voltage Reference Factory trimmed at $V_{DD} = 3.0\text{ V}$, Temp = 25°C	V_{BG}	1.19	1.20	1.21	V

2.8 ADC Characteristics

Table 13. 5 Volt 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	
	Delta to V_{DD} ($V_{DD} - V_{DDA}$) ²	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$) ²	ΔV_{SSA}	-100	0	+100	mV	
Ref Voltage High		V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	
Ref Voltage Low		V_{REFL}	V_{SSA}	V_{SSA}	V_{SSA}	V	
Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input Resistance		R_{ADIN}	—	3	5	k Ω	
Analog Source Resistance	12 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$	R_{AS}	—	—	2	k Ω	External to MCU
	10 bit mode $f_{ADCK} > 4\text{MHz}$ $f_{ADCK} < 4\text{MHz}$		—	—	5		
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

¹ Typical values assume $V_{DDA} = 5.0\text{V}$, Temp = 25°C, $f_{ADCK} = 1.0\text{MHz}$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

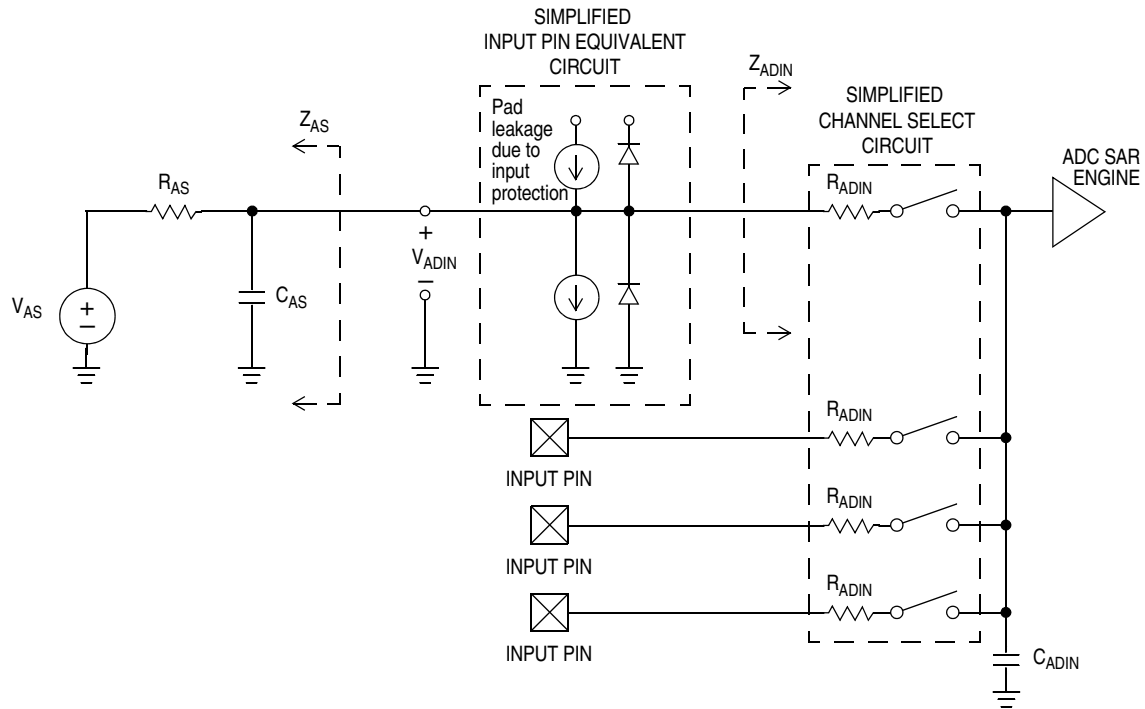


Figure 9. ADC Input Impedance Equivalency Diagram

Table 14. 5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	133	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	218	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	327	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		P	I_{DDAD}	—	0.582	1	mA	
Supply Current	Stop, Reset, Module Off		I_{DDAD}	—	0.011	1	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	T	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)			1.25	2	3.3		

Table 14.5 Volt 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	T	t_{ADC}	—	20	—	ADCK cycles	See Table 9 for conversion time variances
	Long Sample (ADLSMP=1)			—	40	—		
Sample Time	Short Sample (ADLSMP=0)	T	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)			—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	± 3.0	—	LSB ²	Includes quantization
	10 bit mode	P		—	± 1	± 2.5		
	8 bit mode	T		—	± 0.5	± 1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	± 1.75	—	LSB ²	
	10 bit mode ³	P		—	± 0.5	± 1.0		
	8 bit mode ³	T		—	± 0.3	± 0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	± 1.5	—	LSB ²	
	10 bit mode	T		—	± 0.5	± 1.0		
	8 bit mode	T		—	± 0.3	± 0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	± 1.5	—	LSB ²	$V_{ADIN} = V_{SSAD}$
	10 bit mode	P		—	± 0.5	± 1.5		
	8 bit mode	T		—	± 0.5	± 0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	± 1	—	LSB ²	$V_{ADIN} = V_{DDAD}$
	10 bit mode	T		—	± 0.5	± 1		
	8 bit mode	T		—	± 0.5	± 0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB ²	
	10 bit mode			—	—	± 0.5		
	8 bit mode			—	—	± 0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	± 1	—	LSB ²	Pad leakage ⁴ * R_{AS}
	10 bit mode			—	± 0.2	± 2.5		
	8 bit mode			—	± 0.1	± 1		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	1.396	—	V	
Temp Sensor Slope	-40°C - 25°C	D	m	—	3.266	—	mV/°C	
	25°C - 125°C			—	3.638	—		

¹ Typical values assume $V_{DDA} = 5.0V$, Temp = 25°C, $f_{ADCK} = 1.0MHz$ unless otherwise stated. Typical values are for reference only and are not tested in production.

² 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

³ Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

⁴ Based on input pad leakage current. Refer to pad electricals.