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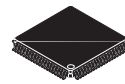
An Energy Efficient Solution by Freescale

MCF51QE128 Series

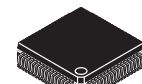
Covers: **MCF51QE128, MCF51QE96, MCF51QE64, MCF51QE32**

- 32-Bit Version 1 ColdFire® Central Processor Unit (CPU)
 - Up to 50.33-MHz ColdFire V1 CPU above 2.4V, 40-MHz CPU above 2.1V, and 20-MHz CPU above 1.8V, across temperature range
 - Provides 0.94 Dhrystone 2.1 MIPS per MHz performance when running from internal RAM (0.76 DMIPS/MHz from flash)
 - Implements Instruction Set Revision C (ISA_C)
 - Support for up to 30 peripheral interrupt requests and seven software interrupts
- On-Chip Memory
 - Flash read/program/erase over full operating voltage and temperature
 - Random-access memory (RAM)
 - Security circuitry to prevent unauthorized access to RAM and flash contents
- Power-Saving Modes
 - Two low power stop modes; reduced power wait mode
 - Peripheral clock enable register can disable clocks to unused modules, reducing currents; allows clocks to remain enabled to specific peripherals in stop3 mode
 - Very low power external oscillator can be used in stop3 mode to provide accurate clock to active peripherals
 - Very low power real time counter for use in run, wait, and stop modes with internal and external clock sources
 - 6 μ s typical wake up time from stop modes
- Clock Source Options
 - Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
 - Internal Clock Source (ICS) — FLL controlled by internal or external reference; precision trimming of internal reference allows 0.2% resolution and 2% deviation; supports CPU freq. from 2 to 50.33 MHz
- System Protection
 - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
 - Low-voltage detection with reset or interrupt; selectable trip points
 - Illegal opcode and illegal address detection with programmable reset or exception response
 - Flash block protection

MCF51QE128



80-LQFP
Case 917A
14 mm²



64-LQFP
Case 840F
10 mm²

- Development Support
 - Single-wire background debug interface
 - 4 PC plus 2 address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
 - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- ADC — 24-channel, 12-bit resolution; 2.5 μ s conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6V to 1.8V
- ACMPx — Two analog comparators with selectable interrupt on rising, falling, or either edge of comparator output; compare option to fixed internal bandgap reference voltage; outputs can be optionally routed to TPM module; operation in stop3
- SCIx — Two SCIs with full duplex non-return to zero (NRZ); LIN master extended break generation; LIN slave extended break detection; wake up on active edge
- SPIx — Two serial peripheral interfaces with Full-duplex or single-wire bidirectional; Double-buffered transmit and receive; MSB-first or LSB-first shifting
- IICx — Two IICs with; Up to 100 kbps with maximum bus loading; Multi-master operation; Programmable slave address; Interrupt driven byte-by-byte data transfer; supports broadcast mode and 10 bit addressing
- TPMx — One 6-channel and two 3-channel; Selectable input capture, output compare, or buffered edge- or center-aligned PWMs on each channel
- RTC — 8-bit modulus counter with binary or decimal based prescaler; External clock source for precise time base, time-of-day, calendar or task scheduling functions; Free running on-chip low power oscillator (1 kHz) for cyclic wake-up without external components
- Input/Output
 - 70 GPIOs and 1 input-only and 1 output-only pin
 - 16 KBI interrupts with selectable polarity
 - Hysteresis and configurable pull-up device on all input pins; Configurable slew rate and drive strength on all output pins.
 - SET/CLR registers on 16 pins (PTC and PTE)
 - 16 bits of Rapid GPIO connected to the CPU's high-speed local bus with set, clear, and toggle functionality

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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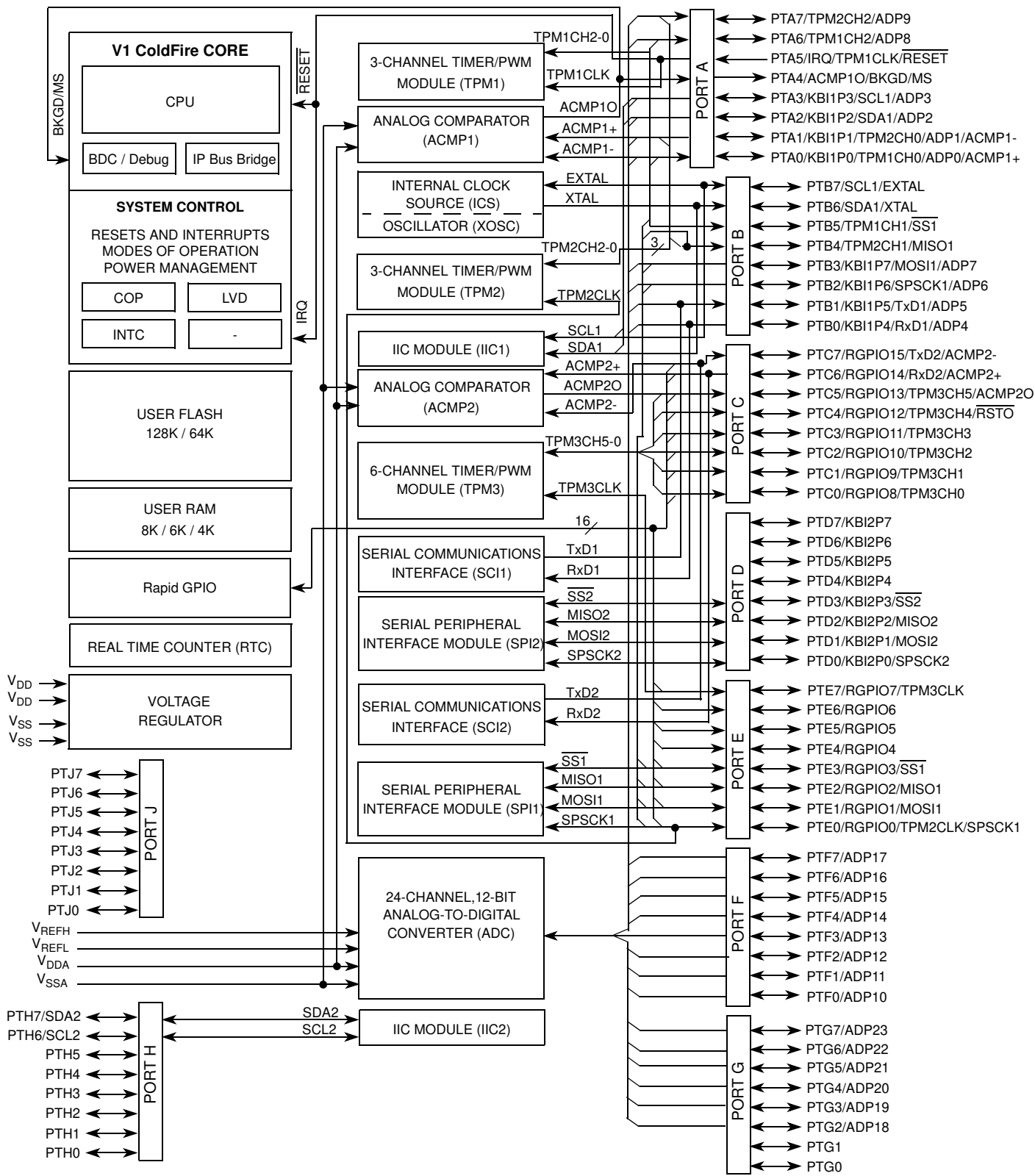


Figure 1. MCF51QE128 Series Block Diagram

1 MCF51QE128 Series Comparison

The following table compares the various device derivatives available within the MCF51QE128 series.

Table 1. MCF51QE128 Series Features by MCU and Package

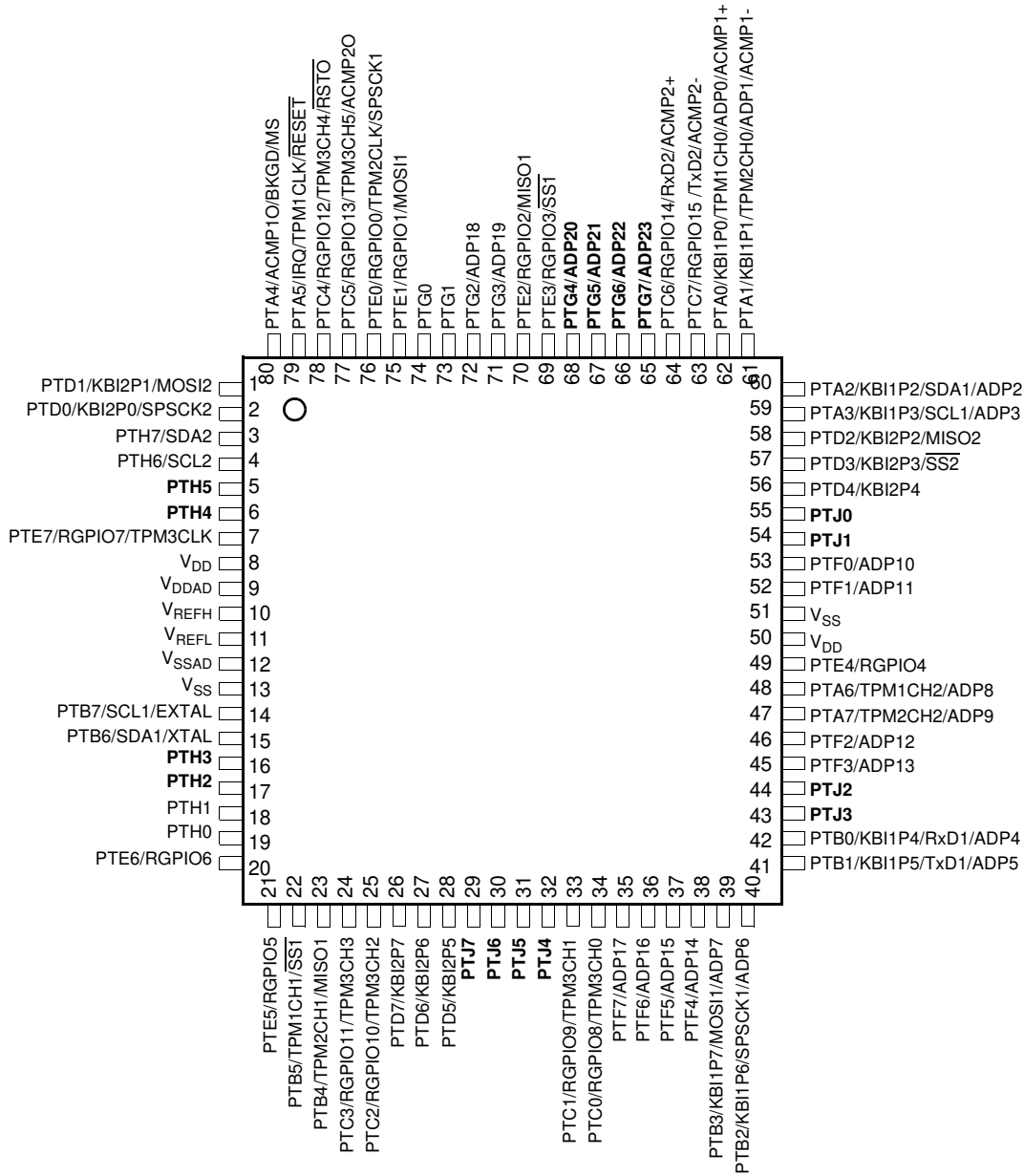
Feature	MCF51QE128		MCF51QE96		MCF51QE64	MCF51QE32
Flash size (bytes)	131072		98304		65536	32768
RAM size (bytes)	8192		8192		8192	8192
Pin quantity	80	64	80	64	64	64
Version 1 ColdFire core	yes					
ACMP1	yes					
ACMP2	yes					
ADC channels	24	20	24	20	20	20
DBG	yes					
ICS	yes					
IIC1	yes					
IIC2	yes					
KBI	16					
Port I/O ^{1, 2}	70	54	70	54	54	54
Rapid GPIO	yes					
RTC	yes					
SCI1	yes					
SCI2	yes					
SPI1	yes					
SPI2	yes					
External IRQ	yes					
TPM1 channels	3					
TPM2 channels	3					
TPM3 channels	6					
XOSC	yes					

¹ Port I/O count does not include the input-only PTA5/IRQ/TPM1CLK/RESET or the output-only PTA4/ACMP1O/BKGD/MS.

² 16 bits associated with Ports C and E are shadowed with ColdFire Rapid GPIO module.

2 Pin Assignments

This section describes the pin assignments for the available packages. See [Table 1](#) for pin availability by package pin-count.



Pins in **bold** are added from the next smaller package.

Figure 2. Pin Assignments in 80-Pin LQFP

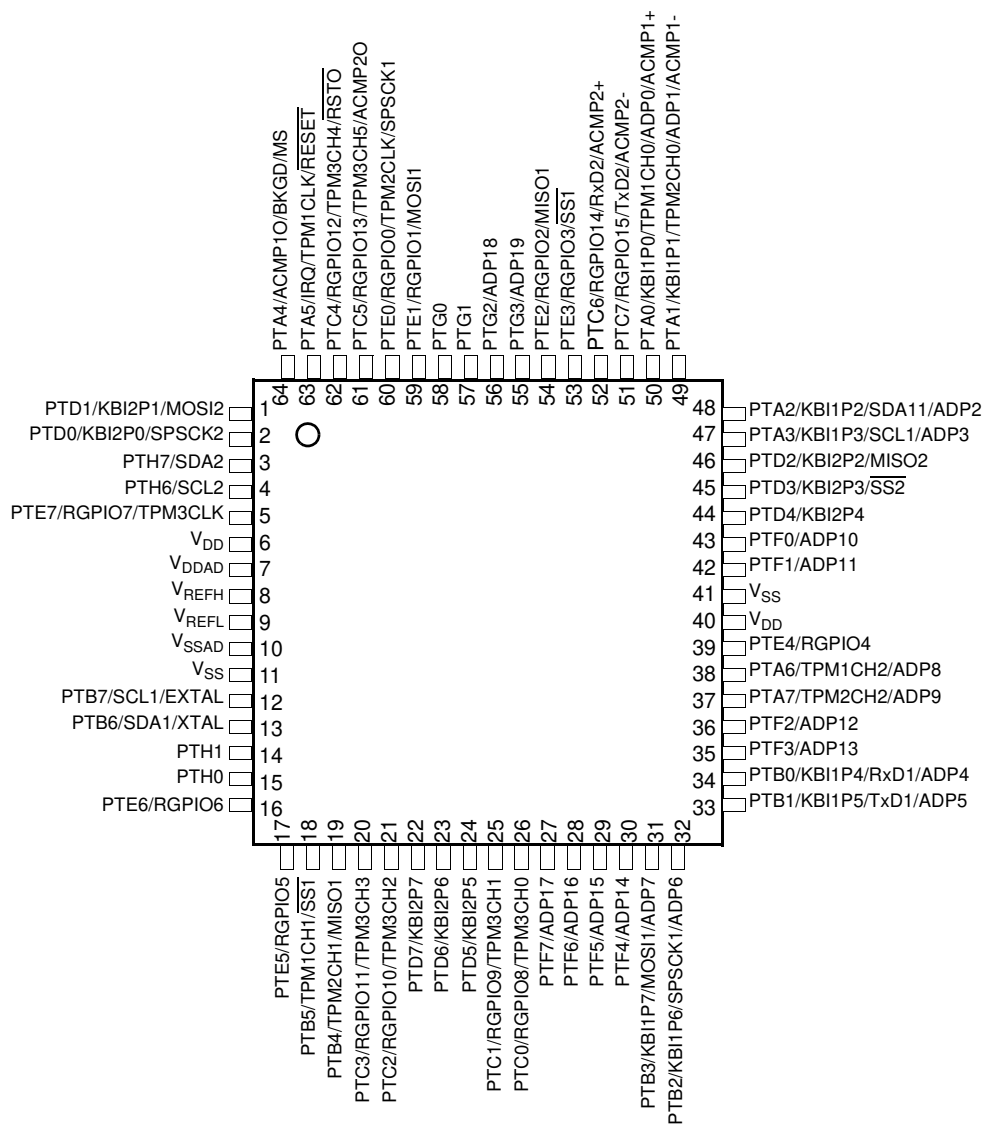


Figure 3. Pin Assignments in 64-Pin LQFP Package

Table 2. MCF51QE128 Series Pin Assignment by Package and Pin Sharing Priority

Pin Number		Lowest	←	Priority	→	Highest
80	64	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	PTD1	KBI2P1	MOSI2		
2	2	PTD0	KBI2P0	SPSCK2		
3	3	PTH7	SDA2			
4	4	PTH6	SCL2			
5	—	PTH5				
6	—	PTH4				
7	5	PTE7	RGPIO7	TPM3CLK		
8	6					V _{DD}
9	7					V _{DDAD}
10	8					V _{REFH}
11	9					V _{REFL}
12	10					V _{SSAD}
13	11					V _{SS}
14	12	PTB7	SCL1			EXTAL
15	13	PTB6	SDA1			XTAL
16	—	PTH3				
17	—	PTH2				
18	14	PTH1				
19	15	PTH0				
20	16	PTE6	RGPIO6			
21	17	PTE5	RGPIO5			
22	18	PTB5	TPM1CH1	SS1		
23	19	PTB4	TPM2CH1	MISO1		
24	20	PTC3	RGPIO11	TPM3CH3		
25	21	PTC2	RGPIO10	TPM3CH2		
26	22	PTD7	KBI2P7			
27	23	PTD6	KBI2P6			
28	24	PTD5	KBI2P5			
29	—	PTJ7				
30	—	PTJ6				
31	—	PTJ5				
32	—	PTJ4				
33	25	PTC1	RGPIO9	TPM3CH1		
34	26	PTC0	RGPIO8	TPM3CH0		
35	27	PTF7				ADP17
36	28	PTF6				ADP16
37	29	PTF5				ADP15
38	30	PTF4				ADP14
39	31	PTB3	KBI1P7	MOSI1 ¹		ADP7
40	32	PTB2	KBI1P6	SPSCK1		ADP6

Table 2. MCF51QE128 Series Pin Assignment by Package and Pin Sharing Priority (continued)

Pin Number		Lowest	←	Priority	→	Highest
80	64	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
41	33	PTB1	KBI1P5	TxD1		ADP5
42	34	PTB0	KBI1P4	RxD1		ADP4
43	—	PTJ3				
44	—	PTJ2				
45	35	PTF3				ADP13
46	36	PTF2				ADP12
47	37	PTA7	TPM2CH2			ADP9
48	38	PTA6	TPM1CH2			ADP8
49	39	PTE4	RGPIO4			
50	40					V _{DD}
51	41					V _{SS}
52	42	PTF1				ADP11
53	43	PTF0				ADP10
54	—	PTJ1				
55	—	PTJ0				
56	44	PTD4	KBI2P4			
57	45	PTD3	KBI2P3	SS2		
58	46	PTD2	KBI2P2	MISO2		
59	47	PTA3	KBI1P3	SCL1 ²		ADP3
60	48	PTA2	KBI1P2	SDA1		ADP2
61	49	PTA1	KBI1P1	TPM2CH0	ADP1	ACMP1-
62	50	PTA0	KBI1P0	TPM1CH0	ADP0	ACMP1+
63	51	PTC7	RGPIO15	TxD2		ACMP2-
64	52	PTC6	RGPIO14	RxD2		ACMP2+
65	—	PTG7				ADP23
66	—	PTG6				ADP22
67	—	PTG5				ADP21
68	—	PTG4				ADP20
69	53	PTE3	RGPIO3	SS1		
70	54	PTE2	RGPIO2	MISO1		
71	55	PTG3				ADP19
72	56	PTG2				ADP18
73	57	PTG1				
74	58	PTG0				
75	59	PTE1	RGPIO1	MOSI1		
76	60	PTE0	RGPIO0	TPM2CLK	SPSCK1	
77	61	PTC5	RGPIO13	TPM3CH5		ACMP20
78	62	PTC4	RGPIO12	TPM3CH4	RSTO	
79	63	PTA5	IRQ	TPM1CLK	RESET	
80	64	PTA4 ³	ACMP10	BKGD	MS	

- ¹ SPI1 pins ($\overline{SS1}$, MISO1, MOSI1, and SPSCCK2) can be repositioned using SPI1PS in SOPT2. Default locations are PTB5, PTB4, PTB3, and PTB2.
- ² IIC1 pins (SCL1 and SDA1) can be repositioned using IIC1PS in SOPT2. Default locations are PTA3 and PTA2, respectively.
- ³ The PTA4/ACMP1O/BKGD/MS is limited to output only for the port I/O function.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MCF51QE128 series of microcontrollers available at the time of publication.

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in [Table 4](#) may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	-0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	-0.3 to $V_{DD} + 0.3$	V
Instantaneous maximum current Single pin limit (applies to all port pins) ^{1, 2, 3}	I_D	± 25	mA
Storage temperature range	T_{stg}	-55 to 150	°C

- ¹ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.
- ² All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .
- ³ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged):			
MCF51QE64, MCF51QE96, and MCF51QE128:	T_A	-40 to 85	°C
MCF51QE32:		0 to 70	
Maximum junction temperature	T_{JM}	95	°C
Thermal resistance Single-layer board			
64-pin LQFP	θ_{JA}	69	°C/W
80-pin LQFP		60	
Thermal resistance Four-layer board			
64-pin LQFP	θ_{JA}	50	°C/W
80-pin LQFP		47	

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \text{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad \text{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \theta_{JA} \times (P_D)^2 \quad \text{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A .

3.5 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM) and the charge device model (CDM).

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 6. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series resistance	R1	1500	Ω
	Storage capacitance	C	100	pF
	Number of pulses per pin	—	3	
Machine	Series resistance	R1	0	Ω
	Storage capacitance	C	200	pF
	Number of pulses per pin	—	3	
Latch-up	Minimum input voltage limit		-2.5	V
	Maximum input voltage limit		7.5	V

Table 7. ESD and Latch-Up Protection Characteristics

No.	Rating ¹	Symbol	Min	Max	Unit
1	Human body model (HBM)	V_{HBM}	± 2000	—	V
2	Machine model (MM)	V_{MM}	± 200	—	V
3	Charge device model (CDM)	V_{CDM}	± 500	—	V
4	Latch-up current at $T_A = 85^\circ\text{C}$	I_{LAT}	± 100	—	mA

¹ Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ ¹	Max	Unit
1		Operating Voltage			1.8 ²		3.6	V
2	C	Output high voltage All I/O pins, low-drive strength All I/O pins, high-drive strength	V_{OH}	1.8 V, $I_{Load} = -2$ mA	$V_{DD} - 0.5$	—	—	V
	P			2.7 V, $I_{Load} = -10$ mA	$V_{DD} - 0.5$	—		
	T			2.3 V, $I_{Load} = -6$ mA	$V_{DD} - 0.5$	—		
	C			1.8V, $I_{Load} = -3$ mA	$V_{DD} - 0.5$	—		
3	D	Output high current Max total I_{OH} for all ports	I_{OHT}		—	—	100	mA
4	C	Output low voltage All I/O pins, low-drive strength All I/O pins, high-drive strength	V_{OL}	1.8 V, $I_{Load} = 2$ mA	—	—	0.5	V
	P			2.7 V, $I_{Load} = 10$ mA	—	—	0.5	
	T			2.3 V, $I_{Load} = 6$ mA	—	—	0.5	
	C			1.8 V, $I_{Load} = 3$ mA	—	—	0.5	
5	D	Output low current Max total I_{OL} for all ports	I_{OLT}		—	—	100	mA
6	P	Input high voltage all digital inputs	V_{IH}	$V_{DD} > 2.7$ V	$0.70 \times V_{DD}$	—	—	V
	C			$V_{DD} > 1.8$ V	$0.85 \times V_{DD}$	—	—	
7	P	Input low voltage all digital inputs	V_{IL}	$V_{DD} > 2.7$ V	—	—	$0.35 \times V_{DD}$	V
	C			$V_{DD} > 1.8$ V	—	—	$0.30 \times V_{DD}$	
8	C	Input hysteresis all digital inputs	V_{hys}		$0.06 \times V_{DD}$	—	—	mV
9	P	Input leakage current all input only pins (Per pin)	$ I_{In} $	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
10	P	Hi-Z (off-state) leakage current all input/output (per pin)	$ I_{OZ} $	$V_{In} = V_{DD}$ or V_{SS}	—	—	1	μA
11	P	Pull-up resistors all digital inputs, when enabled	R_{PU}		17.5	—	52.5	$\text{k}\Omega$

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ ¹	Max	Unit
12	D	DC injection current ^{3, 4, 5} Single pin limit	I_{IC}	$V_{IN} < V_{SS}, V_{IN} > V_{DD}$	-0.2	—	0.2	mA
		Total MCU limit, includes sum of all stressed pins			-5	—	5	mA
13	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
14	C	RAM retention voltage	V_{RAM}		—	0.6	1.0	V
15	C	POR re-arm voltage ⁶	V_{POR}		0.9	1.4	1.79	V
16	D	POR re-arm time	t_{POR}		10	—	—	μs
17	P	Low-voltage detection threshold — high range ⁷	V_{LVDH} ⁸	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
18	P	Low-voltage detection threshold — low range ⁷	V_{LVDL}	V_{DD} falling V_{DD} rising	1.80 1.86	1.82 1.90	1.91 1.99	V
19	P	Low-voltage warning threshold — high range ⁷	V_{LVWH}	V_{DD} falling V_{DD} rising	2.36 2.36	2.46 2.46	2.56 2.56	V
20	P	Low-voltage warning threshold — low range ⁷	V_{LVWL}	V_{DD} falling V_{DD} rising	2.11 2.16	2.16 2.21	2.22 2.27	V
21	C	Low-voltage inhibit reset/recover hysteresis ⁷	V_{hys}		—	50	—	mV
22	P	Bandgap Voltage Reference ⁹	V_{BG}		1.15	1.17	1.18	V

¹ Typical values are measured at 25°C. Characterized, not tested

² As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL} .

³ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁴ Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁵ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

⁶ Maximum is highest voltage that POR is guaranteed.

⁷ Low voltage detection and warning limits measured at 1 MHz bus frequency.

⁸ Run at 1 MHz bus frequency

⁹ Factory trimmed at $V_{DD} = 3.0$ V, Temp = 25°C

Electrical Characteristics

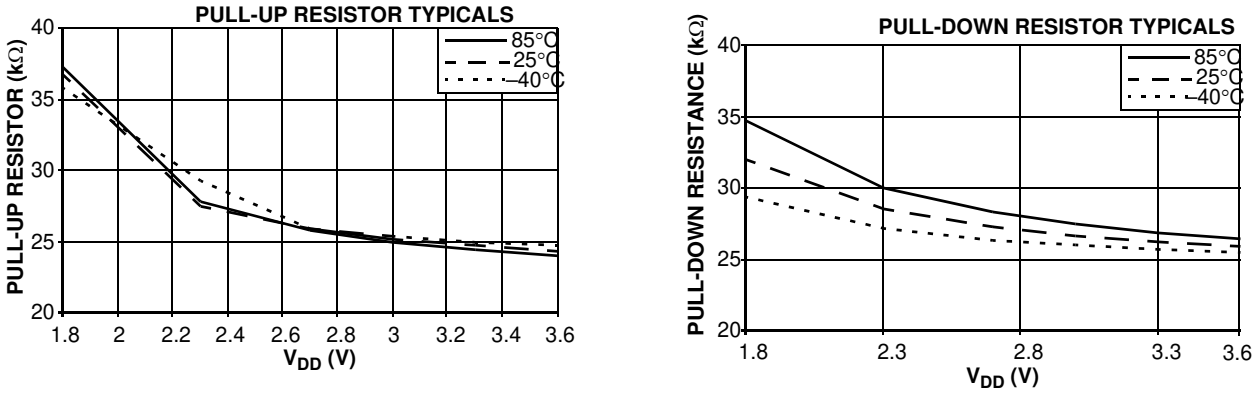


Figure 4. Pull-up and Pull-down Typical Resistor Values

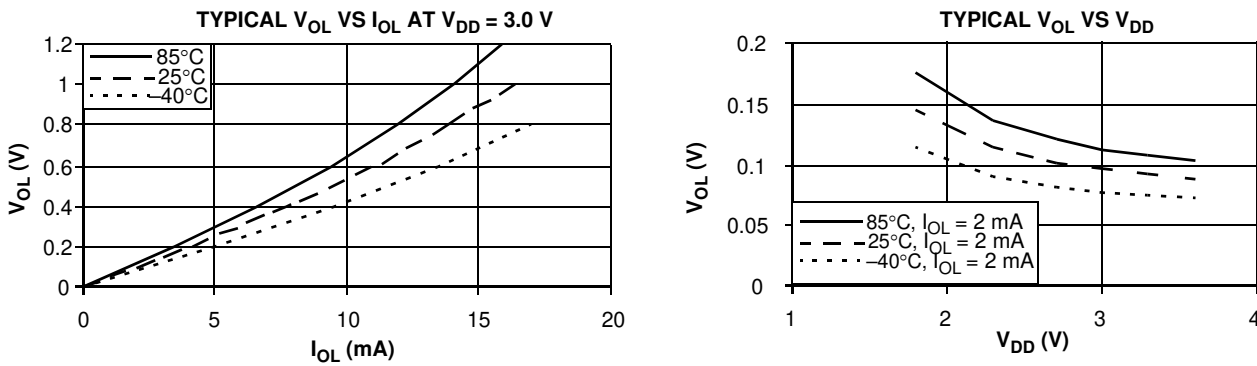


Figure 5. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

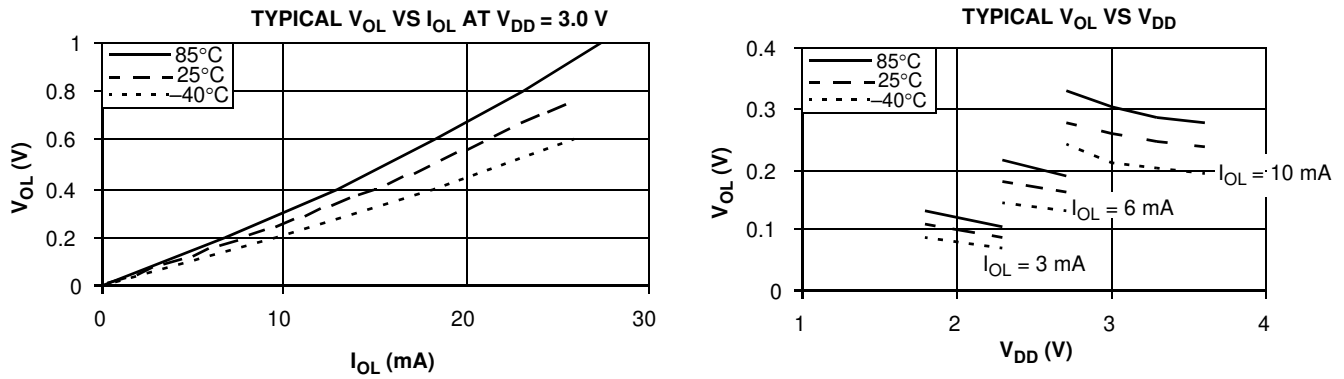


Figure 6. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

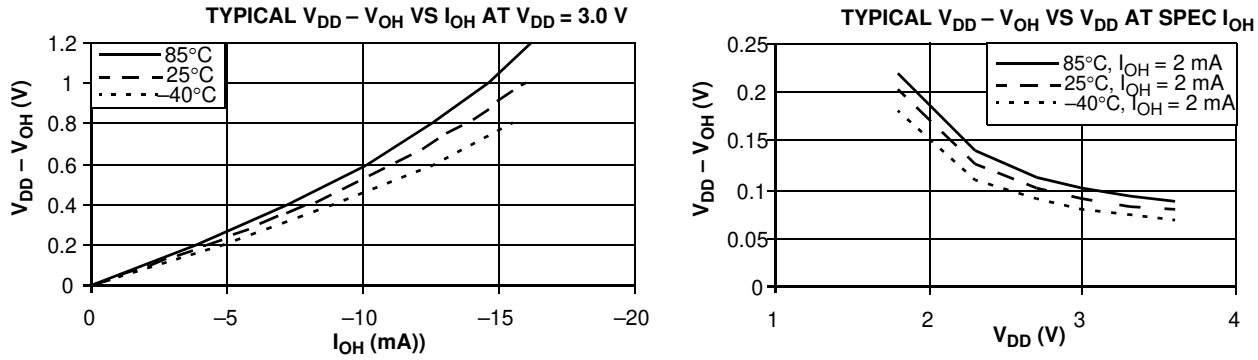


Figure 7. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

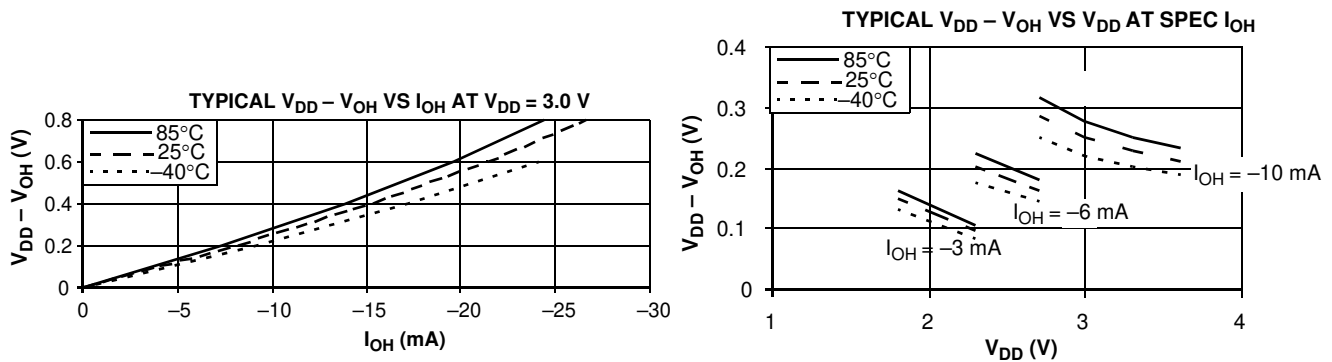


Figure 8. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ ¹	Max	Unit	Temp (°C)	
1	P	Run supply current FEI mode, all modules on	$R_{I_{DD}}$	25.165 MHz	3	32	35	mA	-40 to 25	
	P					32	35		85	
	T					20 MHz	28.0		—	-40 to 85
	T					8 MHz	13.2		—	
	T					1 MHz	2.4		—	
2	C	Run supply current FEI mode, all modules off	$R_{I_{DD}}$	25.165 MHz	3	28.1	29.6	mA	-40 to 85	
	T					20 MHz	22.9			—
	T					8 MHz	11.3			—
	T					1 MHz	2.0			—

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typ ¹	Max	Unit	Temp (°C)
3	T	Run supply current LPS=0, all modules off	R _I DD	16 kHz FBILP	3	203	—	μA	-40 to 85
	T			16 kHz FBELP		154	—		
4	T	Run supply current LPS=1, all modules off, running from Flash	R _I DD	16 kHz FBELP	3	50	—	μA	-40 to 85
5	C	Wait mode supply current FEI mode, all modules off	W _I DD	25.165 MHz	3	11	13.7	mA	-40 to 85
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	P	Stop2 mode supply current	S ₂ I _{DD}	n/a	3	0.6	0.8	μA	-40 to 25
	C					3.0	11		70
	P					8.0	20		85
	C					0.6	0.8		-40 to 25
	C					2.5	10		70
	C					6.0	12		85
7	P	Stop3 mode supply current No clocks active	S ₃ I _{DD}	n/a	3	0.8	1.3	μA	-40 to 25
	C					6.0	18		70
	P					18.0	28		85
	C					0.8	1.3		-40 to 25
	C					5.0	16		70
	C					12.0	20		85

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 10. Stop Mode Adders

Num	C	Parameter	Condition	Temperature (°C)				Units
				-40	25	70	85	
1	T	LPO		50	75	100	150	nA
2	T	ERREFSTEN	RANGE = HGO = 0	1000	1000	1100	1500	nA
3	T	IREFSTEN ¹		63	70	77	81	uA
4	T	RTC	does not include clock source current	50	75	100	150	nA
5	T	LVD ¹	LVDSE = 1	90	100	110	115	uA
6	T	ACMP ¹	not using the bandgap (BGBE = 0)	18	20	22	23	uA
7	T	ADC ¹	ADLPC = ADLSMP = 1 not using the bandgap (BGBE = 0)	95	106	114	120	uA

¹ Not available in stop2 mode.

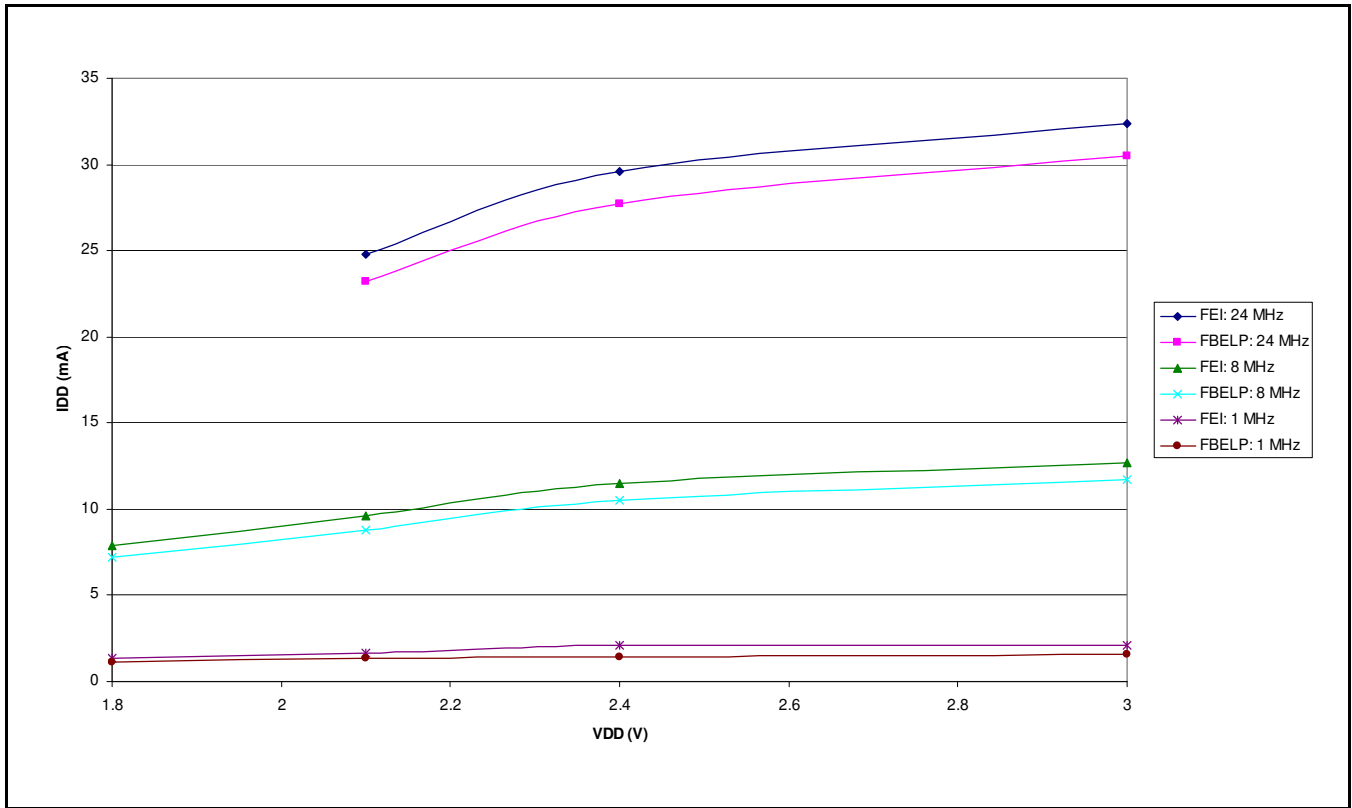


Figure 9. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD}
(ADC off, All Other Modules Enabled)

3.8 External Oscillator (XOSC) Characteristics

Reference [Figure 10](#) and [Figure 11](#) for crystal or resonator circuits.

Table 11. XOSC and ICS Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)					
		Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		High range (RANGE = 1), high gain (HGO = 1)	f_{hi}	1	—	16	MHz
		High range (RANGE = 1), low power (HGO = 0)	f_{hi}	1	—	8	MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1, C_2	See Note ² See Note ³			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0) ² Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	—	—	—	MΩ
				—	10	—	
				—	1	—	
4	D	Series resistor —		—	—	—	
		Low range, low power (RANGE = 0, HGO = 0) ²		—	0	—	
		Low range, high gain (RANGE = 0, HGO = 1)		—	100	—	
		High range, low power (RANGE = 1, HGO = 0)		—	0	0	
		High range, high gain (RANGE = 1, HGO = 1)		—	0	10	
		≥ 8 MHz		—	0	20	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
5	C	Crystal start-up time ⁴		—	200	—	
		Low range, low power	t_{CSTL}	—	400	—	
		Low range, high power		—	5	—	ms
		High range, low power	t_{CSTH}	—	15	—	
		High range, high power		—	15	—	
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1)		0.03125	—	40.0	MHz
		FEE or FBE mode	f_{extal}	0	—	50.33	MHz
		FBELP mode		0	—	50.33	MHz

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² Load capacitors (C_1, C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

³ See crystal or resonator manufacturer’s recommendation.

⁴ Proper PC board layout procedures must be followed to achieve specifications.

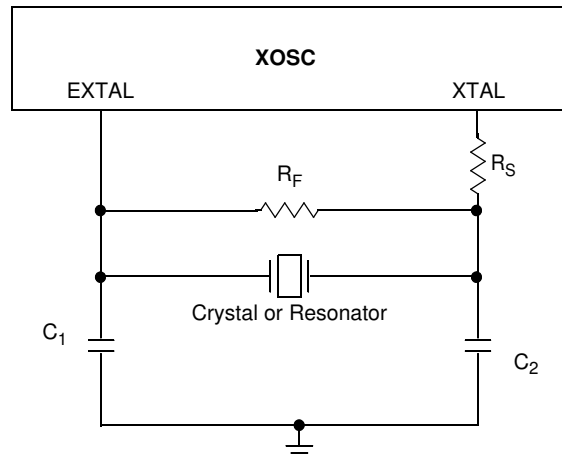


Figure 10. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

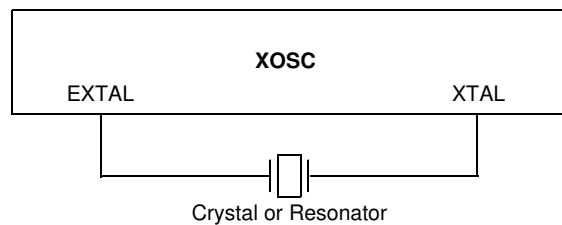


Figure 11. Typical Crystal or Resonator Circuit: Low Range/Low Gain

3.9 Internal Clock Source (ICS) Characteristics

 Table 12. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit	
1	P	Average internal reference frequency — factory trimmed at $V_{DD} = 3.6\text{ V}$ and temperature = 25°C	$f_{\text{int_ft}}$	—	32.768	—	kHz	
2	P	Internal reference frequency — user trimmed	$f_{\text{int_ut}}$	31.25	—	39.06	kHz	
3	T	Internal reference start-up time	t_{IRST}	—	60	100	μs	
4	P	DCO output frequency range — trimmed ²	$f_{\text{dco_u}}$	Low range (DRS=00)	16	—	20	MHz
	P			Mid range (DRS=01)	32	—	40	
	P			High range (DRS=10)	48	—	60	
5	P	DCO output frequency ² Reference = 32768 Hz and DMX32 = 1	$f_{\text{dco_DMX32}}$	Low range (DRS=00)	—	19.92	—	MHz
	P			Mid range (DRS=01)	—	39.85	—	
	P			High range (DRS=10)	—	59.77	—	
6	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{\text{dco_res_t}}$	—	± 0.1	± 0.2	$\%f_{\text{dco}}$	
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{\text{dco_res_t}}$	—	± 0.2	± 0.4	$\%f_{\text{dco}}$	

Table 12. ICS Frequency Specifications (Temperature Range = -40 to 85°C Ambient) (continued)

Num	C	Characteristic	Symbol	Min	Typ ¹	Max	Unit
8	C	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	% f_{dco}
9	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0°C to 70 °C	Δf_{dco_t}	—	± 0.5	± 1	% f_{dco}
10	C	FLL acquisition time ³	$t_{Acquire}$	—	—	1	ms
11	C	Long term jitter of DCO output clock (averaged over 2-ms interval) ⁴	C_{Jitter}	—	0.02	0.2	% f_{dco}

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

³ This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

⁴ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

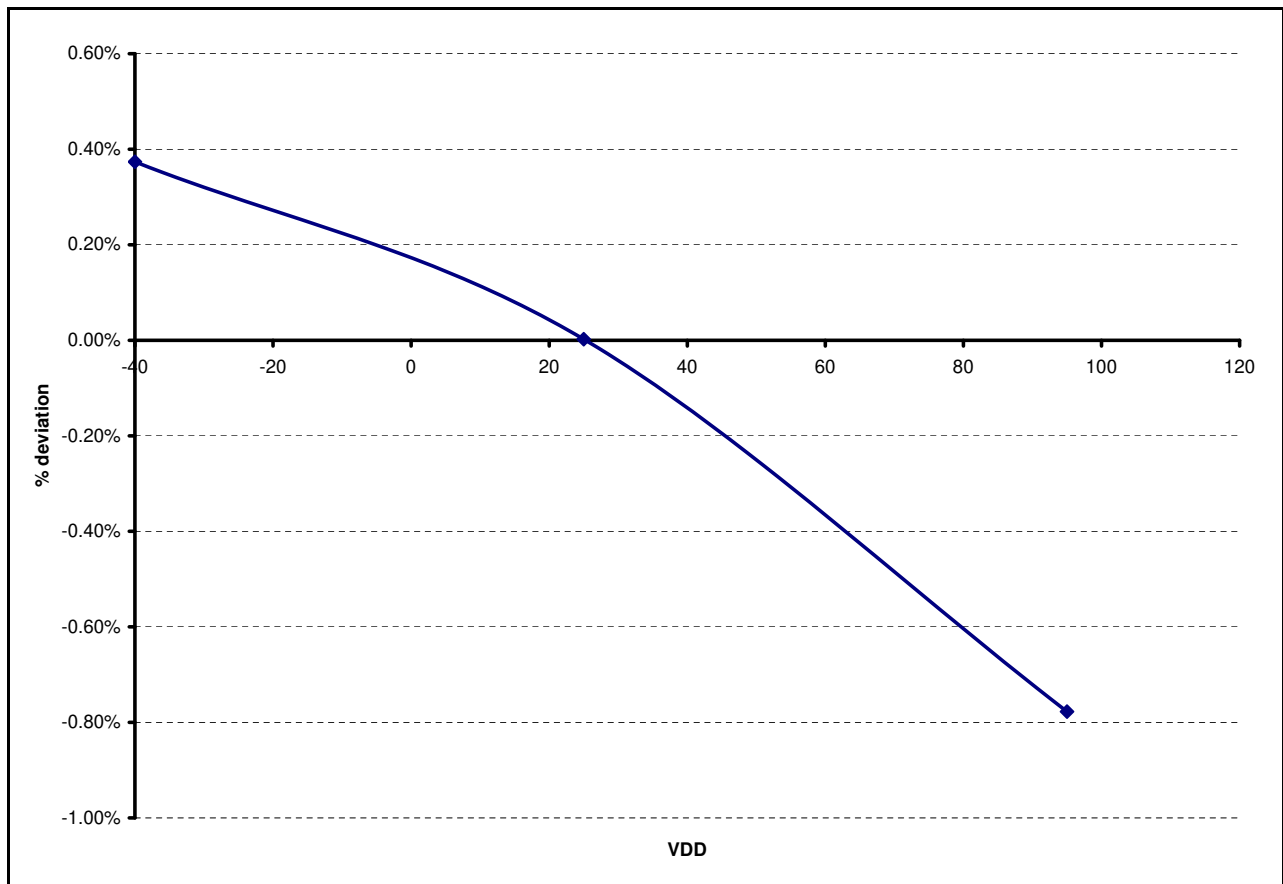
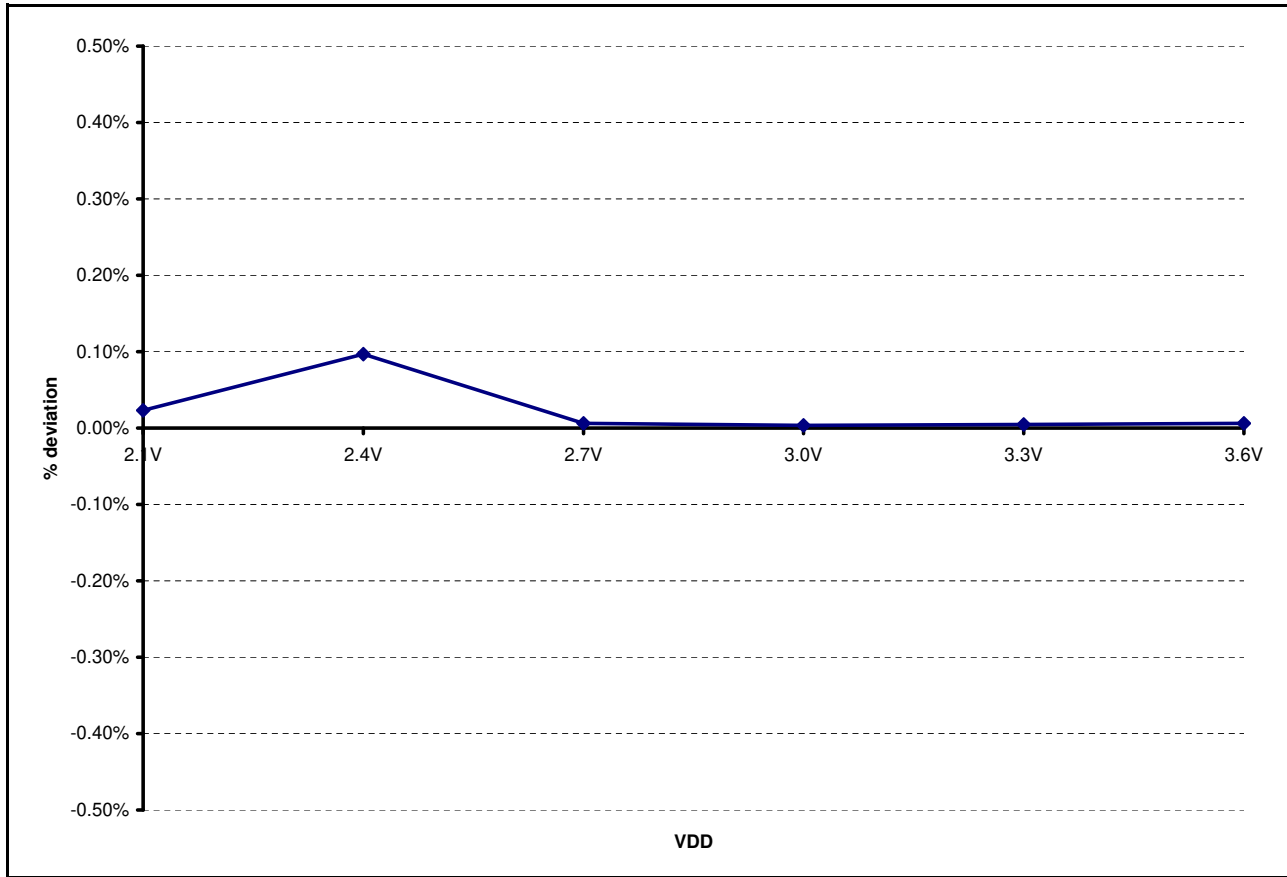


Figure 12. Deviation of DCO Output Across Temperature at $V_{DD} = 3.0$ V


 Figure 13. Deviation of DCO Output Across V_{DD} at 25°C

3.10 AC Characteristics

This section describes timing characteristics for each peripheral system.

3.10.1 Control Timing

Table 13. Control Timing

Num	C	Rating	Symbol	Min	Typ ¹	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$) V _{DD} ≥ 1.8V V _{DD} > 2.1V V _{DD} > 2.4V	f _{Bus}	dc	— — —	10 20 25.165	MHz
2	D	Internal low power oscillator period	t _{LPO}	700	—	1300	μs
3	D	External reset pulse width ²	t _{extrst}	100	—	—	ns
4	D	Reset low drive	t _{rstdrv}	34 × t _{cyc}	—	—	ns
5	D	BKGD/MS setup time after issuing background debug force reset to enter user or BDM modes	t _{MSSU}	500	—	—	ns
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes ³	t _{MSH}	100	—	—	μs

Table 13. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ ¹	Max	Unit
7	D	IRQ pulse width Asynchronous path ² Synchronous path ⁴	t_{LILH} , t_{IHIL}	100 $2 \times t_{cyc}$	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path ² Synchronous path ⁴	t_{LILH} , t_{IHIL}	100 $2 \times t_{cyc}$	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF) ⁵ Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise} , t_{Fall}	— —	8 31	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise} , t_{Fall}	— —	7 24	— —	ns
10		Voltage regulator recovery time	t_{VRR}	—	4	—	μ s

¹ Typical values are based on characterization data at $V_{DD} = 3.0V$, $25^{\circ}C$ unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset or interrupt pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD} .

⁴ This is the minimum assertion time in which the interrupt **may** be recognized. The correct protocol is to assert the interrupt request until it is explicitly negated by the interrupt service routine.

⁵ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40^{\circ}C$ to $85^{\circ}C$.

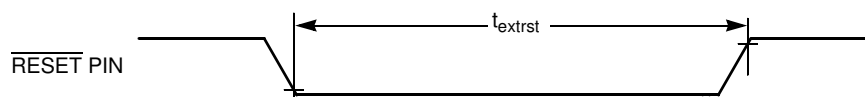


Figure 14. Reset Timing

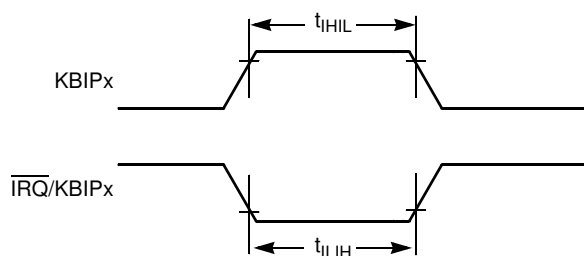


Figure 15. $\overline{IRQ/KBIPx}$ Timing

3.10.2 TPM Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 14. TPM Input Timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

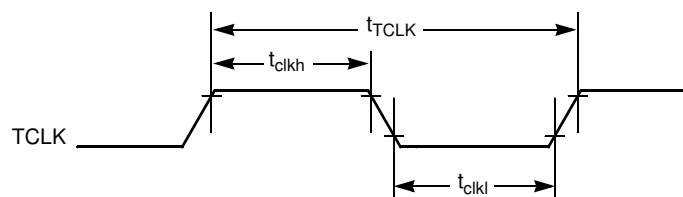


Figure 16. Timer External Clock

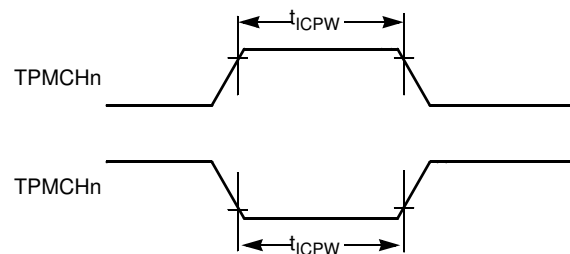


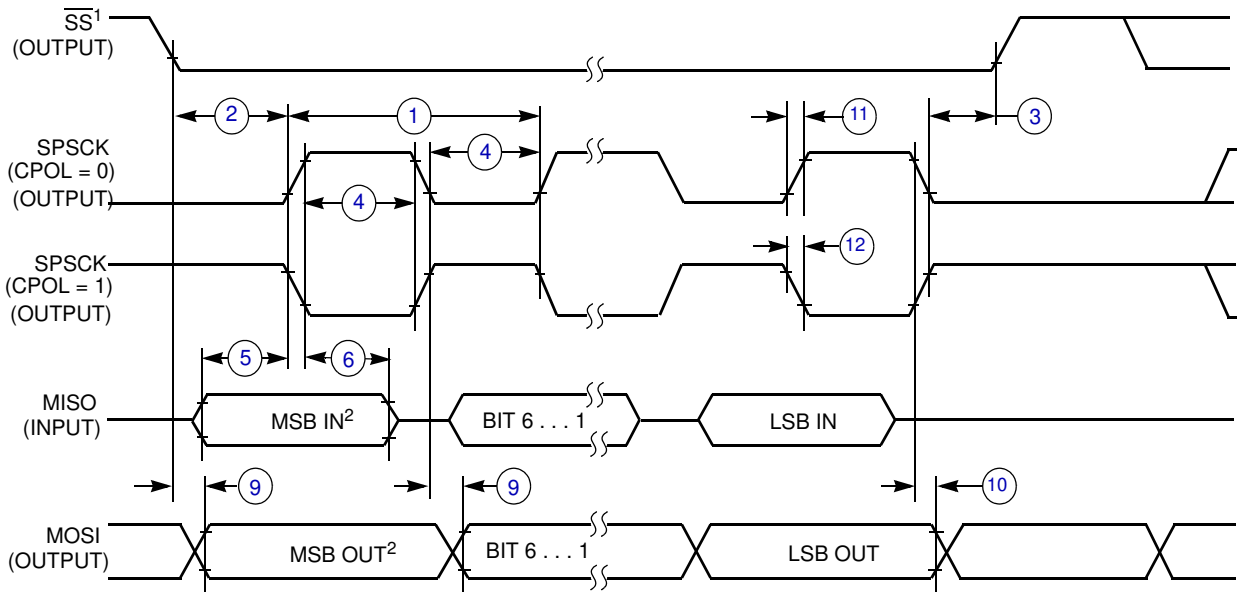
Figure 17. Timer Input Capture Pulse

3.10.3 SPI Timing

Table 15 and Figure 18 through Figure 21 describe the timing requirements for the SPI system.

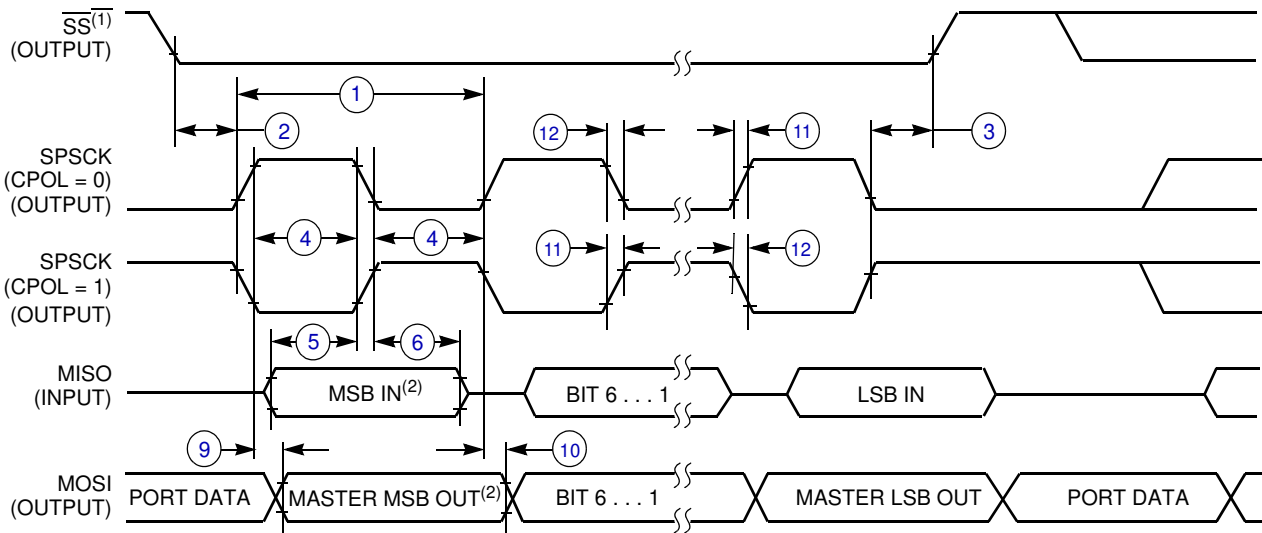
Table 15. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency	f_{op}	$f_{BUS}/2048$ 0	$f_{BUS}/2$ $f_{BUS}/4$	Hz
		Master				Hz
1	D	SPSCK period	t_{SPSCK}	2 4	2048 —	t_{cyc}
		Master				t_{cyc}
2	D	Enable lead time	t_{Lead}	1/2 1	— —	t_{SPSCK}
		Master				t_{cyc}
3	D	Enable lag time	t_{Lag}	1/2 1	— —	t_{SPSCK}
		Master				t_{cyc}
4	D	Clock (SPSCK) high or low time	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns
		Master				ns
5	D	Data setup time (inputs)	t_{SU}	15 15	— —	ns
		Master				ns
6	D	Data hold time (inputs)	t_{HI}	0 25	— —	ns
		Master				ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge)	t_v	— —	25 25	ns
		Master				ns
10	D	Data hold time (outputs)	t_{HO}	0 0	— —	ns
		Master				ns
11	D	Rise time	t_{RI} t_{RO}	— —	$t_{cyc} - 25$ 25	ns
		Input				ns
12	D	Fall time	t_{FI} t_{FO}	— —	$t_{cyc} - 25$ 25	ns
		Input				ns
		Output				ns



NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI Master Timing (CPHA = 0)


NOTES:

1. \overline{SS} output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 19. SPI Master Timing (CPHA = 1)