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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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**Freescale Semiconductor**
Data Sheet: Technical Data

MCF5208EC
Rev. 3, 9/2009

# MCF5208 ColdFire® Microprocessor Data Sheet

## Supports MCF5207 & MCF5208

by: Microcontroller Solutions Group

The MCF5207 and MCF5208 devices are highly-integrated, 32-bit microprocessors based on the version 2 ColdFire microarchitecture. Both devices contain a 16-Kbyte internal SRAM, an 8-Kbyte configurable cache, a 2-bank SDR/DDR SDRAM controller, a 16-channel DMA controller, up to three UARTs, a queued SPI, a low-power management modeule, and other peripherals that enable the MCF5207 and MCF5208 for use in industrial control and connectivity applications. The MCF5208 device also features a 10/100 Mbps fast ethernet controller.

This document provides detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of the MCF5207 and MCF5208 microprocessors. It was written from the perspective of the MCF5208 device. See the following section for a summary of differences between the two devices.

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# 1 MCF5207/8 Device Configurations

The following table compares the two devices described in this document:

**Table 1. MCF5207 & MCF5208 Configurations**

| Module | MCF5207 | MCF5208 |
|---|---|---|
| Version 2 ColdFire Core with EMAC (Enhanced Multiply-Accumulate Unit) | • | • |
| Core (System) Clock | up to 166.67 MHz | |
| Peripheral and External Bus Clock (Core clock ÷ 2) | up to 83.33 MHz | |
| Performance (Dhrystone/2.1 MIPS) | up to 159 | |
| Instruction/Data Cache | 8 Kbytes | |
| Static RAM (SRAM) | 16 Kbytes | |
| SDR/DDR SDRAM Controller | • | • |
| Fast Ethernet Controller (FEC) | — | • |
| Low-Power Management Module | • | • |
| UARTs | 3 | 3 |
| $I^2C$ | • | • |
| QSPI | • | • |
| 32-bit DMA Timers | 4 | 4 |
| Watchdog Timer (WDT) | • | • |
| Periodic Interrupt Timers (PIT) | 4 | 4 |
| Edge Port Module (EPORT) | • | • |
| Interrupt Controllers (INTC) | 1 | 1 |
| 16-channel Direct Memory Access (DMA) | • | • |
| FlexBus External Interface | • | • |
| General Purpose I/O Module (GPIO) | • | • |
| JTAG - IEEE® 1149.1 Test Access Port | • | • |
| Package | 144 LQFP<br>144 MAPBGA | 160 QFP<br>196 MAPBGA |

# 2 Ordering Information

**Table 2. Orderable Part Numbers**

| Freescale Part Number | Description | Speed | Temperature |
|---|---|---|---|
| MCF5207CAG166 | MCF5207 RISC Microprocessor, 144 LQFP | 166.67 MHz | –40° to +85° C |
| MCF5207CVM166 | MCF5207 RISC Microprocessor, 144 MAPBGA | 166.67 MHz | –40° to +85° C |
| MCF5208CAB166 | MCF5208 RISC Microprocessor, 160 QFP | 166.67 MHz | –40° to +85° C |
| MCF5208CVM166 | MCF5208 RISC Microprocessor, 196 MAPBGA | 166.67 MHz | –40° to +85° C |

# 3 Signal Descriptions

The following table lists all the MCF5208 pins grouped by function. The Dir column is the direction for the primary function of the pin only. Refer to Section 4, "Mechanicals and Pinouts" for package diagrams. For a more detailed discussion of the MCF5208 signals, consult the *MCF5208 Reference Manual* (MCF5208RM).

**NOTE**

In this table and throughout this document, a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

**NOTE**

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO default to their GPIO functionality.

**Table 3. MCF5207/8 Signal Information and Muxing**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| **Reset** | | | | | | | | | |
| $\overline{\text{RESET}}$[2] | — | — | — | I | EVDD | 82 | J10 | 90 | J14 |
| $\overline{\text{RSTOUT}}$ | — | — | — | O | EVDD | 74 | M12 | 82 | N14 |
| **Clock** | | | | | | | | | |
| EXTAL | — | — | — | I | EVDD | 78 | K12 | 86 | L14 |
| XTAL | — | — | — | O | EVDD | 80 | J12 | 88 | K14 |
| FB_CLK | — | — | — | O | SDVDD | 34 | L1 | 40 | N1 |
| **Mode Selection** | | | | | | | | | |
| $\overline{\text{RCON}}$[2] | — | — | — | I | EVDD | 144 | C4 | 160 | C3 |
| DRAMSEL | — | — | — | I | EVDD | 79 | H10 | 87 | K11 |
| **FlexBus** | | | | | | | | | |
| A[23:22] | — | $\overline{\text{FB\_CS}}$[5:4] | — | O | SDVDD | 118, 117 | B9, A10 | 126, 125 | B11, A11 |
| A[21:16] | — | — | — | O | SDVDD | 116–114, 112, 108, 107 | C9, A11, B10, A12, C11, B11 | 124, 123, 122, 120, 116, 115 | B12, A12, A13, B13, B14, C13 |
| A[15:14] | — | SD_BA[1:0][3] | — | O | SDVDD | 106, 105 | B12, C12 | 114, 113 | C14, D12 |
| A[13:11] | — | SD_A[13:11][3] | — | O | SDVDD | 104–102 | D11, E10, D12 | 112, 111, 110 | D13, D14, E11 |
| A10 | — | — | — | O | SDVDD | 101 | C10 | 109 | E12 |

**Table 3. MCF5207/8 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| A[9:0] | — | SD_A[9:0][3] | — | O | SDVDD | 100–91 | E11, D9, E12, F10, F11, E9, F12, G10, G12, F9 | 108–99 | E13, E14, F11–F14, G11–G14 |
| D[31:16] | — | SD_D[31:16][4] | — | I/O | SDVDD | 21–28, 40–47 | F1, F2, G1, G2, G4, G3, H1, H2, K3, L2, L3, K2, M3, J4, M4, K4 | 27–34, 46–53 | J4–J1, K4–K1, M3, N3, M4, N4, P4, L5, M5, N5 |
| D[15:0] | — | FB_D[31:16][4] | — | I/O | SDVDD | 8–15, 51–58 | B2, B1, C2, C1, D2, D1, E2, E1, L5, K5, L6, J6, M6, J7, L7, K7 | 16–23, 57–64 | F3–F1, G4–G1, H1, N6, P6, L7, M7, N7, P7, N8, P8 |
| $\overline{BE}/\overline{BWE}$[3:0] | PBE[3:0] | $\overline{SD\_DQM}$[3:0][3] | — | O | SDVDD | 20, 48, 18, 50 | F4, L4, E3, J5 | 26, 54, 24, 56 | H2, P5, H4, M6 |
| $\overline{OE}$ | PBUSCTL3 | — | — | O | SDVDD | 60 | J8 | 66 | M8 |
| $\overline{TA}$[2] | PBUSCTL2 | — | — | I | SDVDD | 90 | G11 | 98 | H14 |
| R/$\overline{W}$ | PBUSCTL1 | — | — | O | SDVDD | 59 | K6 | 65 | L8 |
| $\overline{TS}$ | PBUSCTL0 | $\overline{DACK0}$ | — | O | SDVDD | 4 | B3 | 12 | E3 |
| **Chip Selects** | | | | | | | | | |
| $\overline{FB\_CS}$[3:2] | PCS[3:2] | — | — | O | SDVDD | 119, 120 | D7, A9 | — | C11, A10 |
| $\overline{FB\_CS1}$ | PCS1 | $\overline{SD\_CS1}$ | — | O | SDVDD | 121 | C8 | 127 | B10 |
| $\overline{FB\_CS0}$ | — | — | — | O | SDVDD | 122 | B8 | 128 | C10 |
| **SDRAM Controller** | | | | | | | | | |
| SD_A10 | — | — | — | O | SDVDD | 37 | M1 | 43 | N2 |
| SD_CKE | — | — | — | O | SDVDD | 6 | C3 | 14 | E1 |
| SD_CLK | — | — | — | O | SDVDD | 31 | J1 | 37 | L1 |
| $\overline{SD\_CLK}$ | — | — | — | O | SDVDD | 32 | K1 | 38 | M1 |
| $\overline{SD\_CS0}$ | — | — | — | O | SDVDD | 7 | A1 | 15 | F4 |
| SD_DQS[3:2] | — | — | — | O | SDVDD | 19, 49 | F3, M5 | 25, 55 | H3, L6 |
| $\overline{SD\_SCAS}$ | — | — | — | O | SDVDD | 38 | M2 | 44 | P2 |
| $\overline{SD\_SRAS}$ | — | — | — | O | SDVDD | 39 | J2 | 45 | P3 |
| SD_SDR_DQS | — | — | — | O | SDVDD | 29 | H3 | 35 | L3 |
| $\overline{SD\_WE}$ | — | — | — | O | SDVDD | 5 | D3 | 13 | E2 |

**Table 3. MCF5207/8 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| **External Interrupts Port[5]** | | | | | | | | | |
| $\overline{\text{IRQ7}}$[2] | PIRQ7[2] | — | — | I | EVDD | 134 | A5 | 142 | C7 |
| $\overline{\text{IRQ4}}$[2] | PIRQ4[2] | $\overline{\text{DREQ0}}$[2] | — | I | EVDD | 133 | C6 | 141 | D7 |
| $\overline{\text{IRQ1}}$[2] | PIRQ1[2] | — | — | I | EVDD | 132 | B6 | 140 | D8 |
| **FEC** | | | | | | | | | |
| FEC_MDC | PFECI2C3 | I2C_SCL[2] | U2TXD | O | EVDD | — | — | 148 | D6 |
| FEC_MDIO | PFECI2C2 | I2C_SDA[2] | U2RXD | I/O | EVDD | — | — | 147 | C6 |
| FEC_TXCLK | PFECH7 | — | — | I | EVDD | — | — | 157 | B3 |
| — | PFECH6 | — | $\overline{\text{U1RTS}}$ | O | EVDD | 142 | A2 | — | — |
| FEC_TXEN | PFECH6 | — | $\overline{\text{U1RTS}}$ | O | EVDD | — | — | 158 | A2 |
| FEC_TXD0 | PFECH5 | — | — | O | EVDD | — | — | 3 | B1 |
| FEC_COL | PFECH4 | — | — | I | EVDD | — | — | 7 | D3 |
| FEC_RXCLK | PFECH3 | — | — | I | EVDD | — | — | 154 | B4 |
| FEC_RXDV | PFECH2 | — | — | I | EVDD | — | — | 153 | A4 |
| FEC_RXD0 | PFECH1 | — | — | I | EVDD | — | — | 152 | D5 |
| FEC_CRS | PFECH0 | — | — | I | EVDD | — | — | 8 | D2 |
| FEC_TXD[3:1] | PFECL[7:5] | — | — | O | EVDD | — | — | 6–4 | C1, C2, B2 |
| — | PFECL4 | — | $\overline{\text{U0RTS}}$ | O | EVDD | 141 | D5 | — | — |
| FEC_TXER | PFECL4 | — | $\overline{\text{U0RTS}}$ | O | EVDD | — | — | 156 | A3 |
| FEC_RXD[3:2] | PFECL[3:2] | — | — | I | EVDD | — | — | 149–150 | A5, B5 |
| — | PFECL1 | — | $\overline{\text{U1CTS}}$ | I | EVDD | 139 | B4 | — | — |
| FEC_RXD1 | PFECL1 | — | $\overline{\text{U1CTS}}$ | I | EVDD | — | — | 151 | C5 |
| — | PFECL0 | — | $\overline{\text{U0CTS}}$ | I | EVDD | 140 | E4 | — | — |
| FEC_RXER | PFECL0 | — | $\overline{\text{U0CTS}}$ | I | EVDD | — | — | 155 | C4 |
| **Note:** The MCF5207 does not contain an FEC module. However, the UART0 and UART1 control signals (as well as their GPIO signals) are available by setting the appropriate FEC GPIO port registers. | | | | | | | | | |
| **I²C** | | | | | | | | | |
| I2C_SDA[2] | PFECI2C0[2] | U2RXD[2] | — | I/O | EVDD | — | — | — | D1 |
| I2C_SCL[2] | PFECI2C1[2] | U2TXD[2] | — | I/O | EVDD | — | — | — | E4 |
| **DMA** | | | | | | | | | |
| $\overline{\text{DACK0}}$ and $\overline{\text{DREQ0}}$ do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and QSPI_CS2 for $\overline{\text{DACK0}}$, $\overline{\text{IRQ4}}$ and QSPI_DIN for $\overline{\text{DREQ0}}$. | | | | | | | | | |

**Table 3. MCF5207/8 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| **QSPI** | | | | | | | | | |
| QSPI_CS2 | PQSPI3 | $\overline{\text{DACK0}}$ | $\overline{\text{U2RTS}}$ | O | EVDD | 126 | A8 | 132 | D10 |
| QSPI_CLK | PQSPI0 | I2C_SCL[2] | — | O | EVDD | 127 | C7 | 133 | A9 |
| QSPI_DOUT | PQSPI1 | I2C_SDA[2] | — | O | EVDD | 128 | A7 | 134 | B9 |
| QSPI_DIN | PQSPI2 | $\overline{\text{DREQ0}}$[2] | $\overline{\text{U2CTS}}$ | I | EVDD | 129 | B7 | 135 | C9 |
| **Note:** The QSPI_CS1 and QSPI_CS0 signals are available on the $\overline{\text{U1CTS}}$, $\overline{\text{U1RTS}}$, $\overline{\text{U0CTS}}$, or $\overline{\text{U0RTS}}$ pins for the 196 and 160-pin packages. | | | | | | | | | |
| **UARTs** | | | | | | | | | |
| $\overline{\text{U1CTS}}$ | PUARTL7 | DT1IN | QSPI_CS1 | I | EVDD | — | — | 136 | D9 |
| $\overline{\text{U1RTS}}$ | PUARTL6 | DT1OUT | QSPI_CS1 | O | EVDD | — | — | 137 | C8 |
| U1TXD | PUARTL5 | — | — | O | EVDD | 131 | A6 | 139 | A8 |
| U1RXD | PUARTL4 | — | — | I | EVDD | 130 | D6 | 138 | B8 |
| $\overline{\text{U0CTS}}$ | PUARTL3 | DT0IN | QSPI_CS0 | I | EVDD | — | — | 76 | N12 |
| $\overline{\text{U0RTS}}$ | PUARTL2 | DT0OUT | QSPI_CS0 | O | EVDD | — | — | 77 | P12 |
| U0TXD | PUARTL1 | — | — | O | EVDD | 71 | L10 | 79 | P13 |
| U0RXD | PUARTL0 | — | — | I | EVDD | 70 | M10 | 78 | N13 |
| **Note:** The UART2 signals are multiplexed on the DMA Timers, QSPI, FEC, and I2C pins. For the MCF5207 devices, the UART0 and UART1 control signals are multiplexed internally on the FEC signals. | | | | | | | | | |
| **DMA Timers** | | | | | | | | | |
| DT3IN | PTIMER3 | DT3OUT | $\overline{\text{U2CTS}}$ | I | EVDD | 135 | B5 | 143 | B7 |
| DT2IN | PTIMER2 | DT2OUT | $\overline{\text{U2RTS}}$ | I | EVDD | 136 | C5 | 144 | A7 |
| DT1IN | PTIMER1 | DT1OUT | U2RXD | I | EVDD | 137 | A4 | 145 | A6 |
| DT0IN | PTIMER0 | DT0OUT | U2TXD | I | EVDD | 138 | A3 | 146 | B6 |
| **BDM/JTAG[6]** | | | | | | | | | |
| JTAG_EN[7] | — | — | — | I | EVDD | 83 | J11 | 91 | J13 |
| DSCLK | — | $\overline{\text{TRST}}$[2] | — | I | EVDD | 76 | K11 | 84 | L12 |
| PSTCLK | — | TCLK[2] | — | O | EVDD | 64 | M7 | 70 | P9 |
| $\overline{\text{BKPT}}$ | — | TMS[2] | — | I | EVDD | 75 | L12 | 83 | M14 |
| DSI | — | TDI[2] | — | I | EVDD | 77 | H9 | 85 | K12 |
| DSO | — | TDO | — | O | EVDD | 69 | M9 | 75 | M12 |
| DDATA[3:0] | — | — | — | O | EVDD | — | K9, L9, M11, M8 | — | P11, N11, M11, P10 |
| PST[3:0] | — | — | — | O | EVDD | — | L11, L8, K10, K8 | — | N10, M10, L10, L9 |

**Table 3. MCF5207/8 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate 1 | Alternate 2 | Dir.[1] | Voltage Domain | MCF5207 144 LQFP | MCF5207 144 MAPBGA | MCF5208 160 QFP | MCF5208 196 MAPBGA |
|---|---|---|---|---|---|---|---|---|---|
| ALLPST | — | — | — | O | EVDD | 67 | — | 73 | — |
| **Test** | | | | | | | | | |
| TEST[7] | — | — | — | I | EVDD | 109 | — | — | C12 |
| PLL_TEST | — | — | — | I | EVDD | — | — | — | M13 |
| **Power Supplies** | | | | | | | | | |
| EVDD | — | — | — | — | — | 1, 33, 63, 66, 72, 81, 87, 125 | E5–E6, F5, G8–G9, H7–H8 | 2, 9, 69, 72, 80, 89, 95, 131 | E5–E7, F5, F6, G5, H10, J9, J10, K8–K10, K13, M9 |
| IVDD | — | — | — | — | — | 30, 68, 84, 113, 143 | D4, D8, H4, H11, J9 | 36, 74, 92, 121, 159 | J12, D4, D11, H11, L4, L11, |
| PLL_VDD | — | — | — | — | — | 86 | H12 | 94 | H13 |
| SD_VDD | — | — | — | — | — | 3, 17, 35, 61, 89, 110, 123 | E7–E8, F8, G5, H5–H6, J3 | 11, 39, 41, 67, 97, 118, 129 | E8–E10, F9, F10, G10, H5, J5, J6, K5–K7, L2 |
| VSS | — | — | — | — | — | 2, 16, 36, 62, 65, 73, 88, 111, 124 | D10, F6–F7, G6–G7 | 1, 10, 42, 68, 71, 81, 96, 117, 119, 130 | A1, A14, F7–F8, G6–G9, H6–H9, J7–J8, L13, M2, N9, P1, P14 |
| PLL_VSS | — | — | — | — | — | 85 | — | 93 | H12 |

NOTES:
1 Refers to pin's primary function.
2 Pull-up enabled internally on this signal for this mode.
3 The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.
4 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.
5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.
6 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.
7 Pull-down enabled internally on this signal for this mode.

# 4 Mechanicals and Pinouts

Drawings in this section show the pinout and the packaging and mechanical characteristics of the MCF5207 and MCF5208 devices.

**NOTE**

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

## 4.1 Pinout—144 LQFP

Figure 1 shows a pinout of the MCF5207CAG166 device.

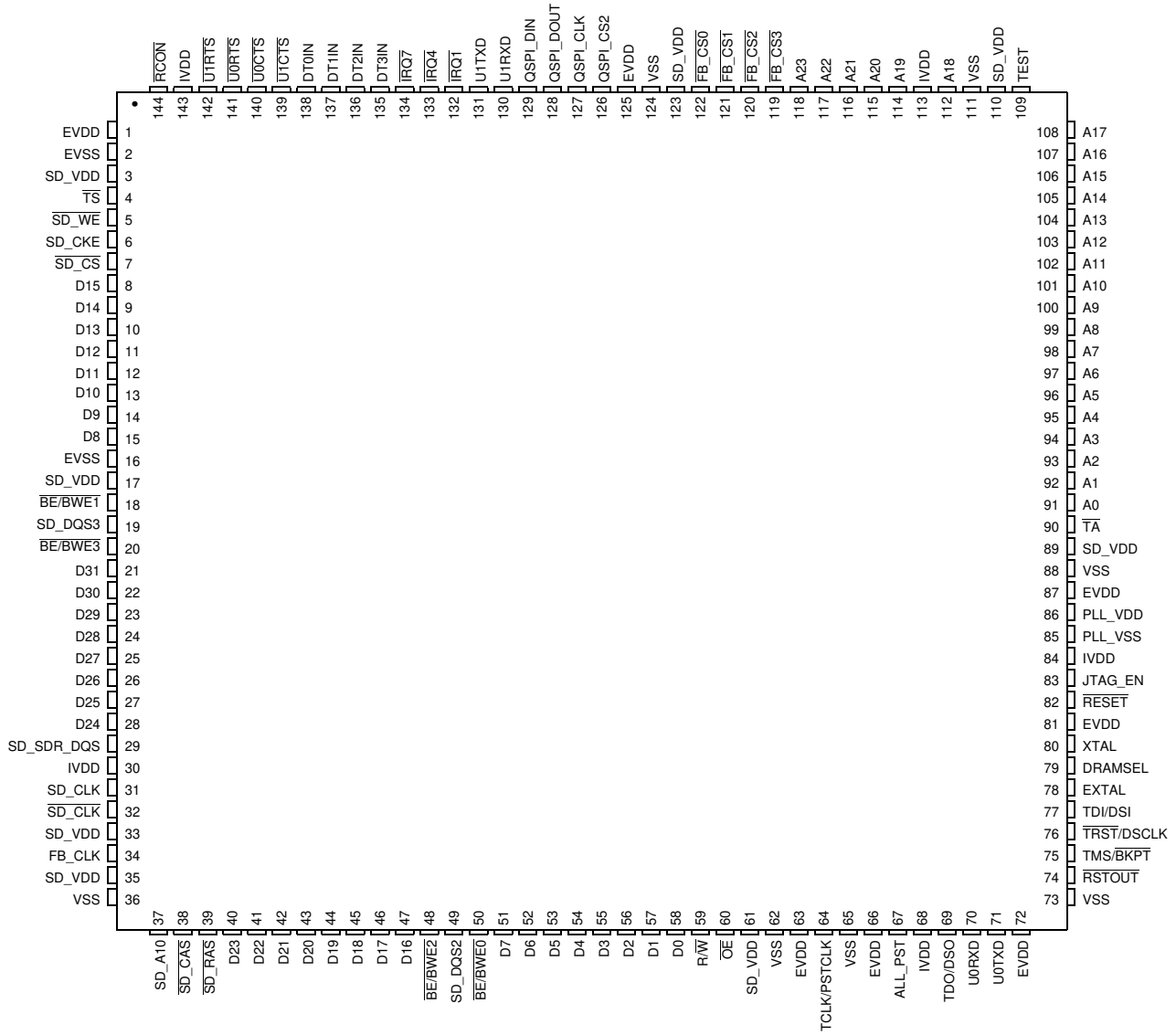



**Figure 1. MCF5207CAG166 Pinout Top View (144 LQFP)**

## 4.2 Package Dimensions—144 LQFP

Figure 2 and Figure 3 show MCF5207CAB166 package dimensions.

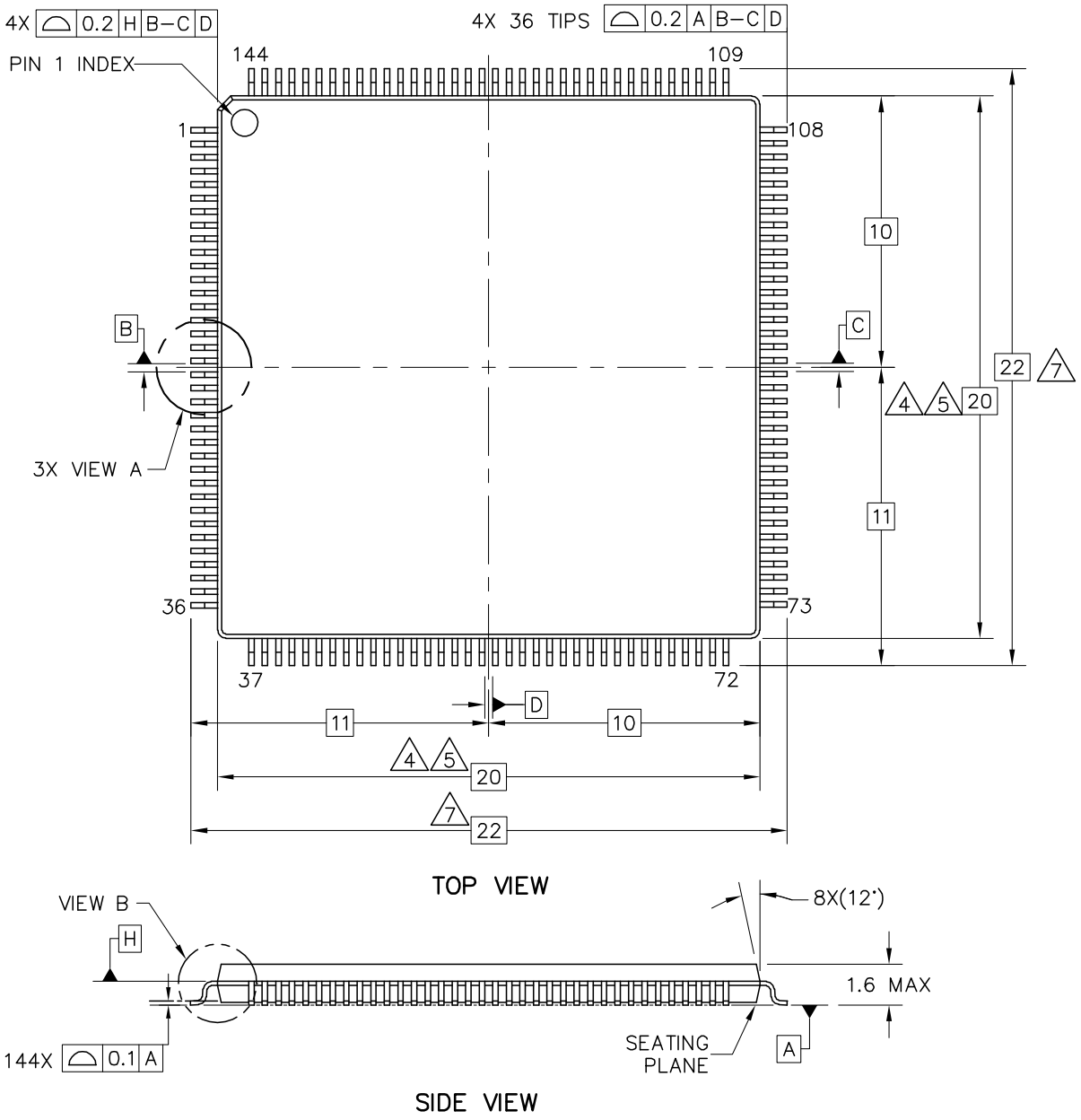
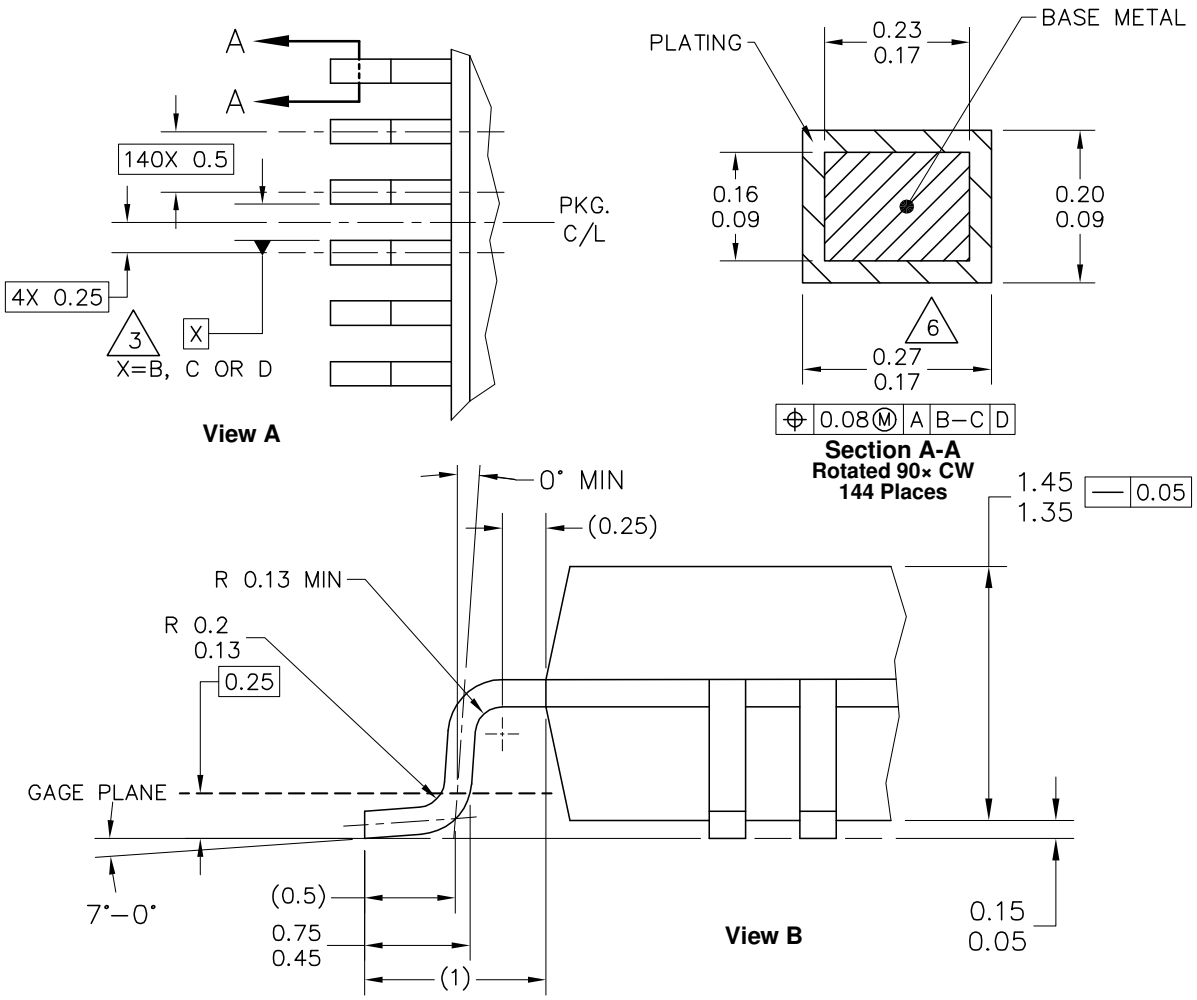



**Figure 2. MCF5207CAB166 Package Dimensions (Sheet 1 of 2)**




NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

**Figure 3. MCF5207CAB166 Package Dimensions (Sheet 2 of 2)**

# 4.3 Pinout—144 MAPBGA

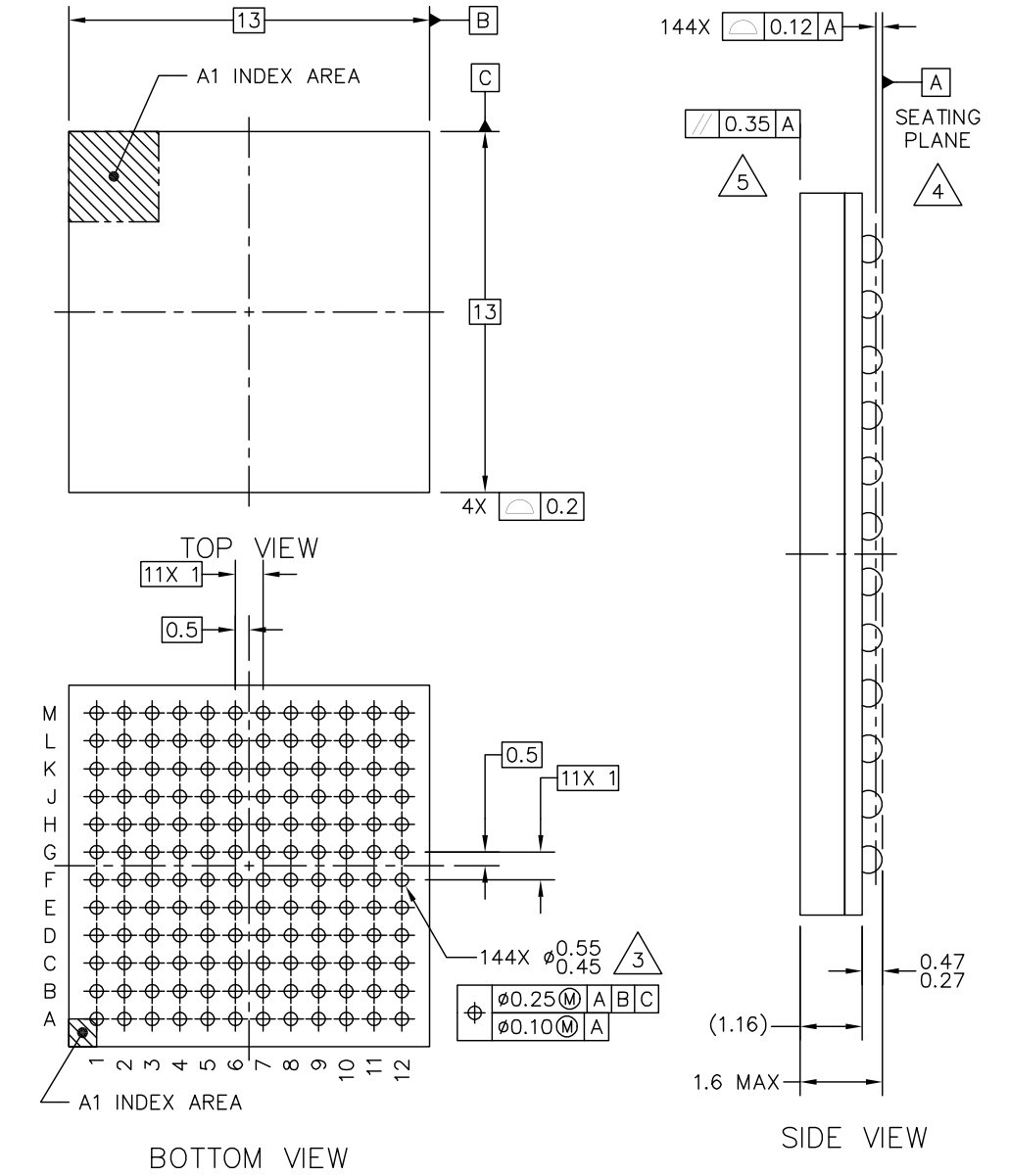
The pinout of the MCF5207CVM166 device is shown below.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | SD_CS | U1RTS | DT0IN | DT1IN | IRQ7 | U1TXD | QSPI_DOUT | QSPI_CS2 | FB_CS2 | A22 | A20 | A18 | A |
| B | D14 | D15 | TS | U1CTS | DT3IN | IRQ1 | QSPI_DIN | FB_CS0 | A23 | A19 | A16 | A15 | B |
| C | D12 | D13 | SD_CKE | RCON | DT2IN | IRQ4 | QSPI_CLK | FB_CS1 | A21 | A10 | A17 | A14 | C |
| D | D10 | D11 | SD_WE | IVDD | U0RTS | U1RXD | FB_CS3 | IVDD | A8 | VSS | A13 | A11 | D |
| E | D8 | D9 | BE/BWE1 | U0CTS | EVDD | EVDD | SD_VDD | SD_VDD | A4 | A12 | A9 | A7 | E |
| F | D31 | D30 | SD_DQS3 | BE/BWE3 | EVDD | VSS | VSS | SD_VDD | A0 | A6 | A5 | A3 | F |
| G | D29 | D28 | D26 | D27 | SD_VDD | VSS | VSS | EVDD | EVDD | A2 | TA | A1 | G |
| H | D25 | D24 | SD_SDR_DQS | IVDD | SD_VDD | SD_VDD | EVDD | EVDD | TDI/DSI | DRAM SEL | IVDD | PLL_VDD | H |
| J | SD_CLK | SD_RAS | SD_VDD | D18 | BE/BWE0 | D4 | D2 | OE | IVDD | RESET | JTAG_EN | XTAL | J |
| K | SD_CLK | D20 | D23 | D16 | D6 | R/W | D0 | PST0 | DDATA3 | PST1 | TRST/DSCLK | EXTAL | K |
| L | FB_CLK | D22 | D21 | BE/BWE2 | D7 | D5 | D1 | PST2 | DDATA2 | U0TXD | PST3 | TMS/BKPT | L |
| M | SD_A10 | SD_CAS | D19 | D17 | SD_DQS2 | D3 | TCLK/PSTCLK | DDATA0 | TDO/DSO | U0RXD | DDATA1 | RSTOUT | M |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |

**Figure 4. MCF5207CVM166 Pinout Top View (144 MAPBGA)**

# 4.4 Package Dimensions—144 MAPBGA

Figure 5 shows the MCF5207CAB166 package dimensions.




NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

**Figure 5. MCF5207CAB166 Package Dimensions (144 MAPBGA)**

# 4.5 Pinout—160 QFP

Figure 6 shows a pinout of the MCF5208CAB166 device.

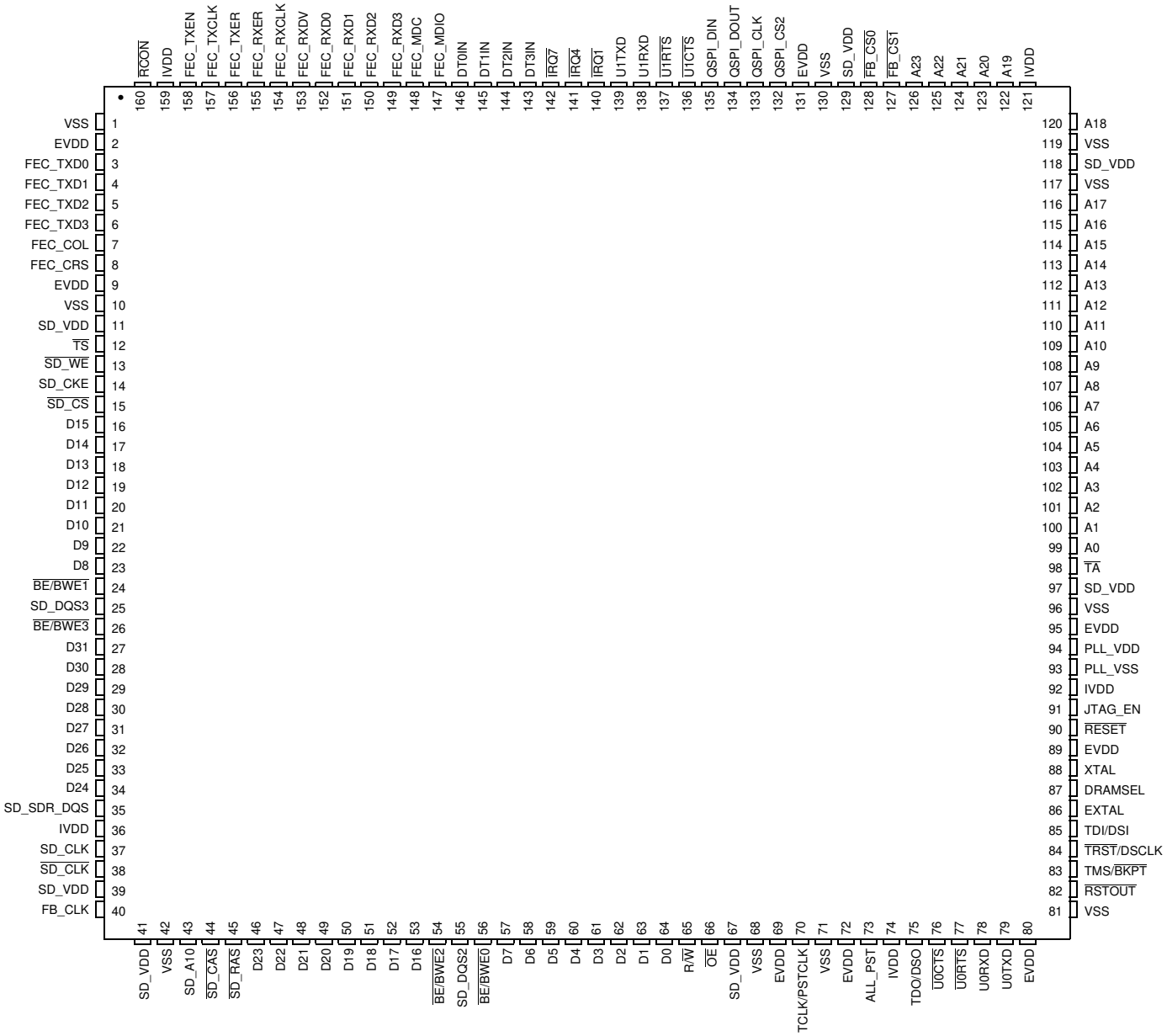



**Figure 6. MCF5208CAB166 Pinout Top View (160 QFP)**

## 4.6 Package Dimensions—160 QFP

The package dimensions of the MCF5208CAB166 device are shown in the figures below.

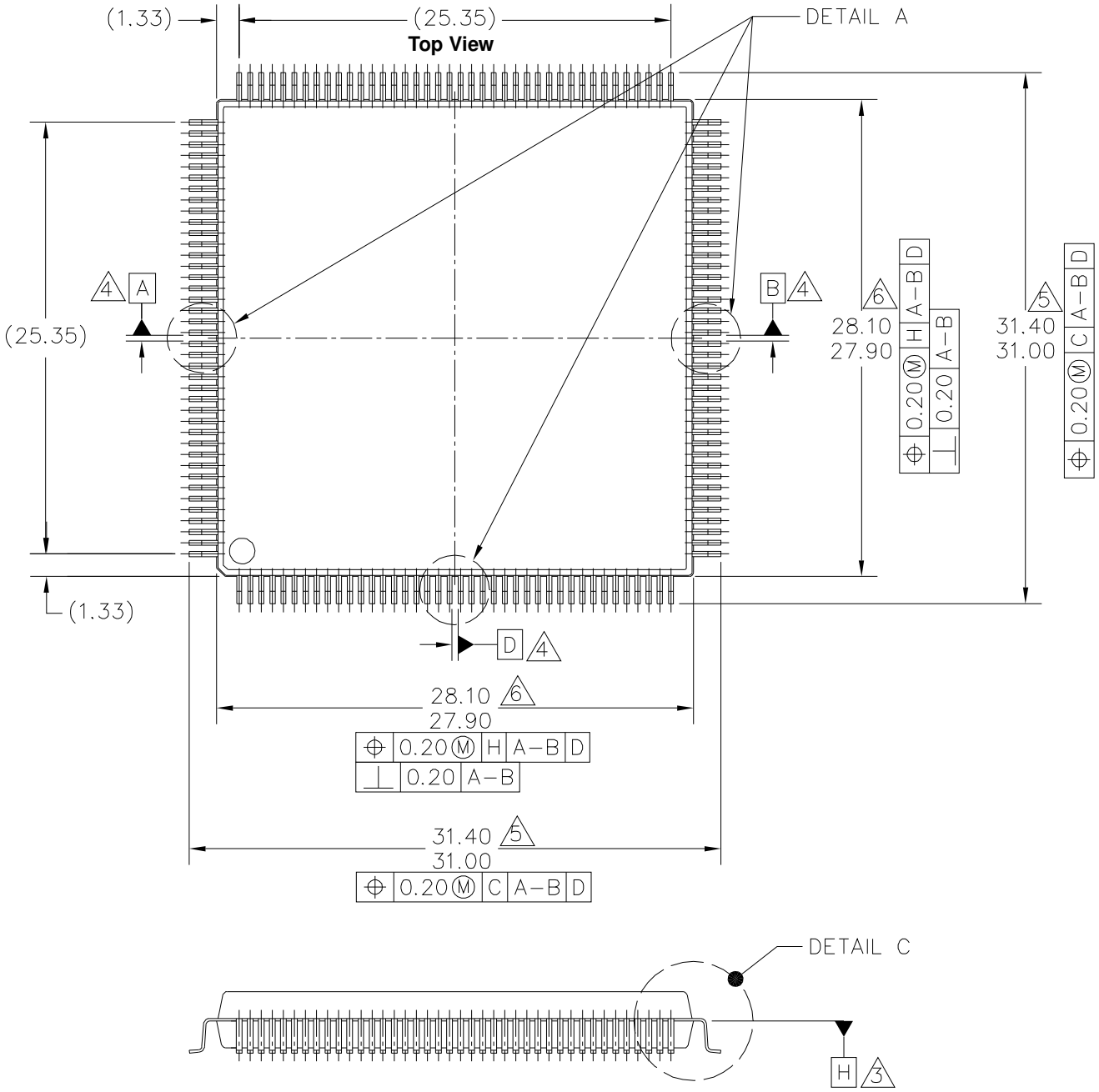
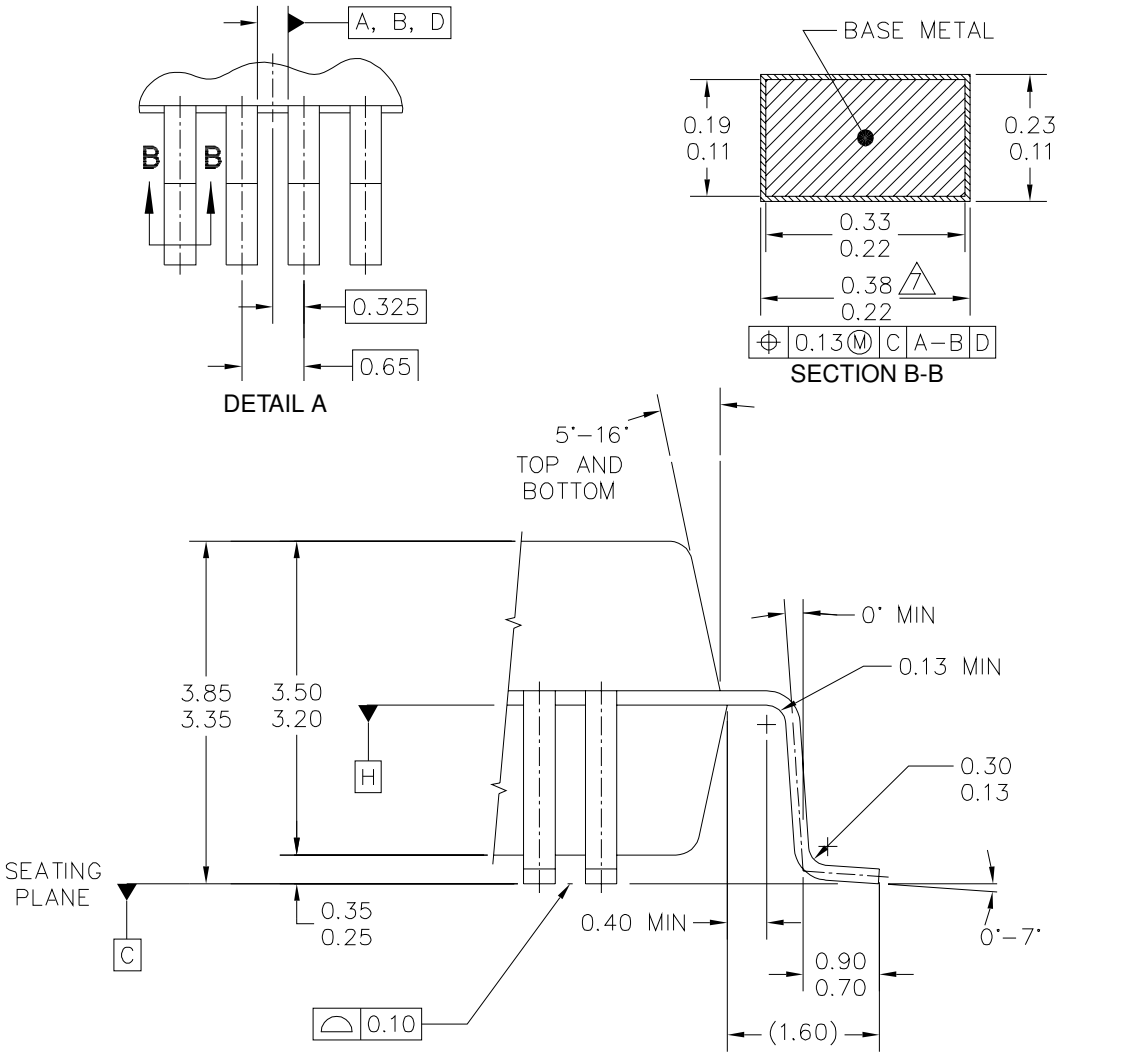



**Figure 7. MCF5208CAB166 Package Dimensions (Sheet 1 of 2)**




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

2. CONTROLLING DIMENSION: MILLIMETER.

3. DATUM PLANE IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. DATUMS TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

**Figure 8. MCF5208CAB166 Package Dimensions (Sheet 2 of 2)**

# 4.7 Pinout—196 MAPBGA

Figure 9 shows a pinout of the MCF5208CVM166 device.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | FEC_ TXEN | FEC_ TXER | FEC_ RXDV | FEC_ RXD3 | DT1IN | DT2IN | U1TXD | QSPI_ CLK | FB_CS2 | A22 | A20 | A19 | VSS | A |
| B | FEC_ TXD0 | FEC_ TXD1 | FEC_ TXCLK | FEC_ RXCLK | FEC_ RXD2 | DT0IN | DT3IN | U1RXD | QSPI_ DOUT | FB_CS1 | A23 | A21 | A18 | A17 | B |
| C | FEC_ TXD3 | FEC_ TXD2 | RCON | FEC_ RXER | FEC_ RXD1 | FEC_ MDIO | IRQ7 | U1RTS | QSPI_ DIN | FB_CS0 | FB_CS3 | TEST | A16 | A15 | C |
| D | I2C_SDA | FEC_ CRS | FEC_ COL | IVDD | FEC_ RXD0 | FEC_ MDC | IRQ4 | IRQ1 | U1CTS | QSPI_ CS2 | IVDD | A14 | A13 | A12 | D |
| E | SD_CKE | SD_WE | TS | I2C_SCL | EVDD | EVDD | EVDD | SD_VDD | SD_VDD | SD_VDD | A11 | A10 | A9 | A8 | E |
| F | D13 | D14 | D15 | SD_CS | EVDD | EVDD | VSS | VSS | SD_VDD | SD_VDD | A7 | A6 | A5 | A4 | F |
| G | D9 | D10 | D11 | D12 | EVDD | VSS | VSS | VSS | VSS | SD_VDD | A3 | A2 | A1 | A0 | G |
| H | D8 | BE/ BWE3 | SD_ DQS3 | BE/ BWE1 | SD_VDD | VSS | VSS | VSS | VSS | EVDD | IVDD | PLL_ VSS | PLL_ VDD | TA | H |
| J | D28 | D29 | D30 | D31 | SD_VDD | SD_VDD | VSS | VSS | EVDD | EVDD | NC | IVDD | JTAG_ EN | RESET | J |
| K | D24 | D25 | D26 | D27 | SD_VDD | SD_VDD | SD_VDD | EVDD | EVDD | EVDD | DRAM SEL | TDI/ DSI | EVDD | XTAL | K |
| L | SD_CLK | SD_VDD | SD_SDR _DQS | IVDD | D18 | SD_ DQS2 | D5 | R/W | PST0 | PST1 | IVDD | TRST/ DSCLK | VSS | EXTAL | L |
| M | SD_CLK | VSS | D23 | D21 | D17 | BE/ BWE0 | D4 | OE | EVDD | PST2 | DDATA1 | TDO/ DSO | PLL_ TEST | TMS/ BKPT | M |
| N | FB_CLK | SD_A10 | D22 | D20 | D16 | D7 | D3 | D1 | VSS | PST3 | DDATA2 | U0CTS | U0RXD | RSTOUT | N |
| P | VSS | SD_CAS | SD_RAS | D19 | BE/ BWE2 | D6 | D2 | D0 | TCLK/ PSTCLK | DDATA0 | DDATA3 | U0RTS | U0TXD | VSS | P |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

**Figure 9. MCF5208CVM166 Pinout Top View (196 MAPBGA)**

## 4.8 Package Dimensions—196 MAPBGA

The package dimensions for the MCF5208CVM166 device is shown below.

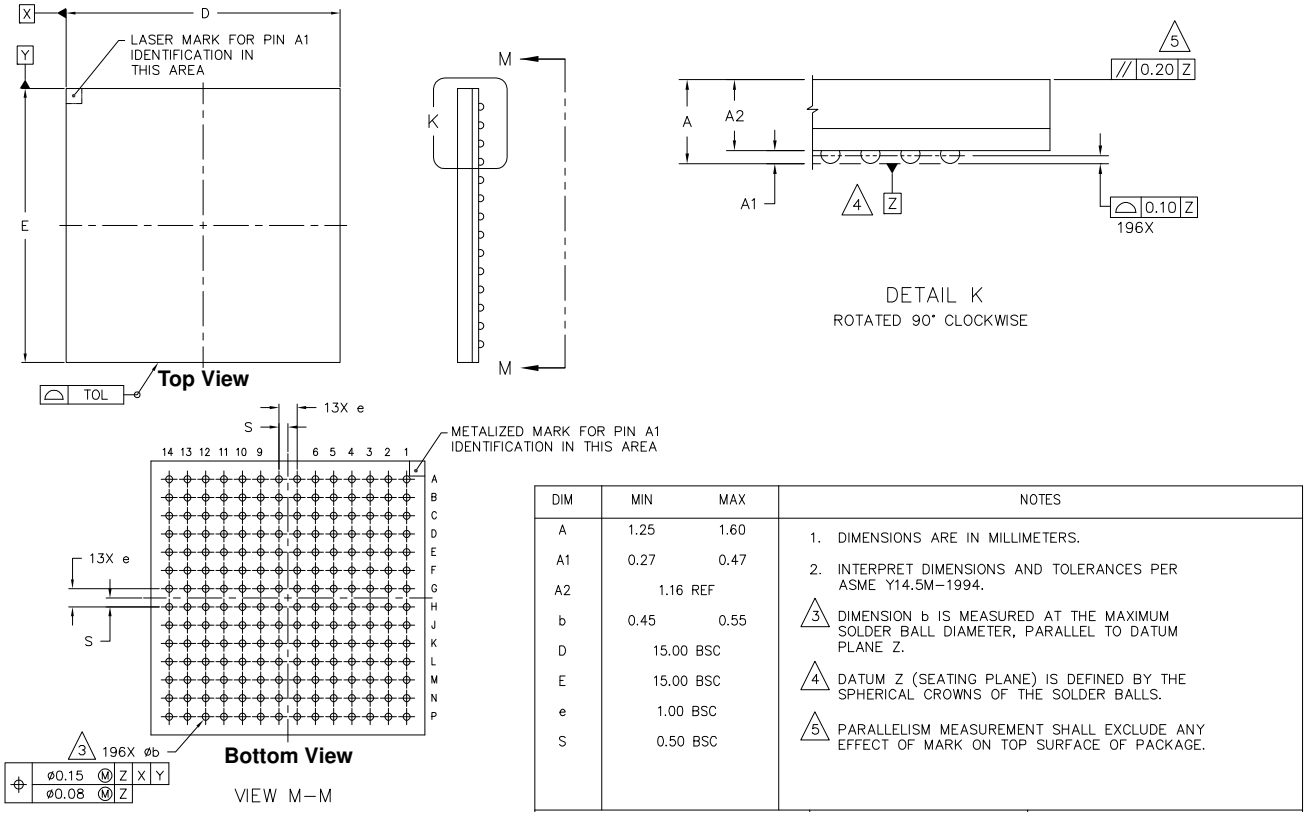



**Figure 10. MCF5208CVM166 Package Dimensions (196 MAPBGA)**

# 5 Electrical Characteristics

## 5.1 Maximum Ratings

**Table 4. Absolute Maximum Ratings[1, 2]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core Supply Voltage | $IV_{DD}$ | – 0.5 to +2.0 | V |
| CMOS Pad Supply Voltage | $EV_{DD}$ | – 0.3 to +4.0 | V |
| DDR/Memory Pad Supply Voltage | $SDV_{DD}$ | – 0.3 to +4.0 | V |
| PLL Supply Voltage | $PLLV_{DD}$ | – 0.3 to +2.0 | V |
| Digital Input Voltage [3] | $V_{IN}$ | – 0.3 to +3.6 | V |
| Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5] | $I_D$ | 25 | mA |

**Table 4. Absolute Maximum Ratings[1, 2] (continued)**

| | | | |
|---|---|---|---|
| Operating Temperature Range (Packaged) | $T_A$ ($T_L$ - $T_H$) | – 40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | – 55 to 150 | °C |

NOTES:
1. Functional operating conditions are given in Section 5.4, "DC Electrical Specifications". Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level ($V_{SS}$ or $EV_{DD}$).
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to $V_{SS}$ and $EV_{DD}$.
5. Power supply must maintain regulation within operating $EV_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $EV_{DD}$ and could result in external power supply going out of regulation. Ensure external $EV_{DD}$ load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating $EV_{DD}$ range during instantaneous and operating maximum current conditions.

# 5.2 Thermal Characteristics

Table 5 lists thermal resistance values

**Table 5. Thermal Characteristics**

| Characteristic | | Symbol | 196MBGA | 144MBGA | 160QFP | 144LQFP | Unit |
|---|---|---|---|---|---|---|---|
| Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JMA}$ | 47[1,2] | 47[1,2] | 49[1,2] | 65[1,2] | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 43[1,2] | 43[1,2] | 44[1,2] | 58[1,2] | °C/W |
| Junction to board | | $\theta_{JB}$ | 36[3] | 36[3] | 40[3] | 50[3] | °C/W |
| Junction to case | | $\theta_{JC}$ | 22[4] | 22[4] | 39[4] | 19[4] | °C/W |
| Junction to top of package | | $\Psi_{jt}$ | 6[1,5] | 6[1,5] | 12[1,6] | 5[1,7] | °C/W |
| Maximum operating junction temperature | | $T_j$ | 105 | 105 | 105 | 105 | °C |

NOTES:
1. $\theta_{JMA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JmA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

$T_A$ = Ambient Temperature, °C

$Q_{JMA}$ = Package Thermal Resistance, Junction-to-Ambient, ×C/W

$P_D$ = $P_{INT}$ + $P_{I/O}$

$P_{INT}$ = $I_{DD}$ × $IV_{DD}$, Watts – Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving Equation 1 and Equation 2 iteratively for any value of $T_A$.

# 5.3 ESD Protection

**Table 6. ESD Protection Characteristics[1, 2]**

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| ESD Target for Human Body Model | HBM | 2000 | V |

NOTES:
1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] A device is defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 5.4 DC Electrical Specifications

**Table 7. DC Electrical Specifications**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Core Supply Voltage | $IV_{DD}$ | 1.4 | 1.6 | V |
| PLL Supply Voltage | $PLLV_{DD}$ | 1.4 | 1.6 | V |
| CMOS Pad Supply Voltage | $EV_{DD}$ | 3.0 | 3.6 | V |
| SDRAM and FlexBus Supply Voltage<br>Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V)<br>DDR/Bus Pad Supply Voltage (nominal 2.5V)<br>SDR/Bus Pad Supply Voltage (nominal 3.3V) | $SDV_{DD}$ | <br>1.70<br>2.25<br>3.0 | <br>1.95<br>2.75<br>3.6 | V |
| CMOS Input High Voltage | $EV_{IH}$ | 2 | $EV_{DD}$ + 0.3 | V |
| CMOS Input Low Voltage | $EV_{IL}$ | $V_{SS}$ - 0.3 | 0.8 | V |
| CMOS Output High Voltage<br>$I_{OH}$ = –5.0 mA | $EV_{OH}$ | $EV_{DD}$ - 0.4 | — | V |
| CMOS Output Low Voltage<br>$I_{OL}$ = 5.0 mA | $EV_{OL}$ | — | 0.4 | V |
| SDRAM and FlexBus Input High Voltage<br>Mobile DDR/Bus Input High Voltage (nominal 1.8V)<br>DDR/Bus Pad Supply Voltage (nominal 2.5V)<br>SDR/Bus Pad Supply Voltage (nominal 3.3V) | $SDV_{IH}$ | <br>1.35<br>1.7<br>2 | <br>$SDV_{DD}$ + 0.3<br>$SDV_{DD}$ + 0.3<br>$SDV_{DD}$ + 0.3 | V |
| SDRAM and FlexBus Input Low Voltage<br>Mobile DDR/Bus Input High Voltage (nominal 1.8V)<br>DDR/Bus Pad Supply Voltage (nominal 2.5V)<br>SDR/Bus Pad Supply Voltage (nominal 3.3V) | $SDV_{IL}$ | <br>$V_{SS}$ - 0.3<br>$V_{SS}$ - 0.3<br>$V_{SS}$ - 0.3 | <br>0.45<br>0.8<br>0.8 | V |
| SDRAM and FlexBus Output High Voltage<br>Mobile DDR/Bus Input High Voltage (nominal 1.8V)<br>DDR/Bus Pad Supply Voltage (nominal 2.5V)<br>SDR/Bus Pad Supply Voltage (nominal 3.3V)<br>$I_{OH}$ = –5.0 mA for all modes | $SDV_{OH}$ | <br>$SDV_{DD}$ - 0.35<br>2.1<br>2.4 | <br>—<br>—<br>— | V |
| SDRAM and FlexBus Output Low Voltage<br>Mobile DDR/Bus Input High Voltage (nominal 1.8V)<br>DDR/Bus Pad Supply Voltage (nominal 2.5V)<br>SDR/Bus Pad Supply Voltage (nominal 3.3V)<br>$I_{OL}$ = 5.0 mA for all modes | $SDV_{OL}$ | <br>—<br>—<br>— | <br>0.3<br>0.3<br>0.5 | V |
| Input Leakage Current<br>$V_{in}$ = $IV_{DD}$ or $V_{SS}$, Input-only pins | $I_{in}$ | –1.0 | 1.0 | µA |

**Table 7. DC Electrical Specifications (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Weak Internal Pull Up Device Current, tested at $V_{IL}$ Max.[1] | $I_{APU}$ | -10 | - 130 | µA |
| Input Capacitance [2]<br>All input-only pins<br>All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |

NOTES:
1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

## 5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog $V_{DD}$ pins. The filter shown in Figure 11 should be connected between the board $V_{DD}$ and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

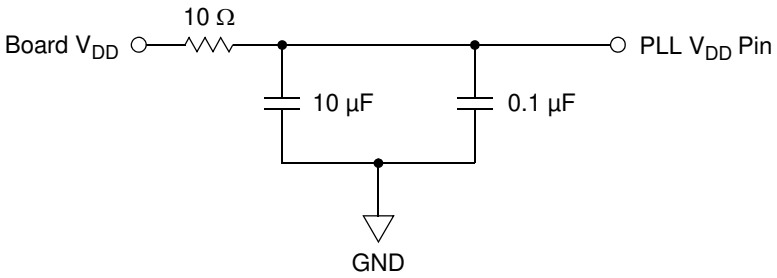



**Figure 11. System PLL $V_{DD}$ Power Filter**

## 5.4.2 Supply Voltage Sequencing and Separation Cautions

The relationship between $SDV_{DD}$ and $EV_{DD}$ is non-critical during power-up and power-down sequences. $SDV_{DD}$ (2.5V or 3.3V) and $EV_{DD}$ are specified relative to $IV_{DD}$.

### 5.4.2.1 Power Up Sequence

If $EV_{DD}/SDV_{DD}$ are powered up with $IV_{DD}$ at 0 V, the sense circuits in the I/O pads cause all pad output drivers connected to the $EV_{DD}/SDV_{DD}$ to be in a high impedance state. There is no limit on how long after $EV_{DD}/SDV_{DD}$ powers up before $IV_{DD}$ must power up. $IV_{DD}$ should not lead the $EV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ by more than 0.4 V during power ramp-up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

### 5.4.2.2 Power Down Sequence

If $IV_{DD}/PLLV_{DD}$ are powered down first, sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after $IV_{DD}$ and $PLLV_{DD}$ power down before $EV_{DD}$ or $SDV_{DD}$ must power down. $IV_{DD}$ should not lag $EV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ going low by more than

0.4 V during power down or there is an undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is:

1. Drop $IV_{DD}$/$PLLV_{DD}$ to 0 V.
2. Drop $EV_{DD}$/$SDV_{DD}$ supplies.

## 5.5 Current Consumption

All of the below current consumption data is lab data measured on a single device using an evaluation board. Table 8 shows the typical current consumption in low-power modes at various $f_{sys/2}$ frequencies. Current measurements are taken after executing a STOP instruction.

**Table 8. Current Consumption in Low-Power Mode[1,2]**

| Mode | Voltage (V) | Typical[3] (mA) | | | | | Peak[4] (mA) |
|---|---|---|---|---|---|---|---|
| | | 44 MHz | 56 MHz | 64 MHz | 72 MHz | 83.33 MHz | 83.33 MHz |
| Stop Mode 3 (Stop 11)[5] | 3.3 | 1.33 | | | | | |
| | 2.5 | 15.19 | | | | | |
| | 1.5 | 0.519 | | | | | |
| Stop Mode 2 (Stop 10)[5] | 3.3 | 1.93 | | | | | |
| | 2.5 | 15.19 | | | | | |
| | 1.5 | 1.25 | | | | | |
| Stop Mode 1 (Stop 01)[5] | 3.3 | 1.83 | | | | | |
| | 2.5 | 15.23 | | | | | |
| | 1.5 | 8.24 | 10.22 | 9.55 | 10.61 | 12.1 | 12.1 |
| Stop Mode 0 (Stop 00)[5] | 3.3 | 2.23 | 2.33 | 2.41 | 2.5 | 2.61 | 2.61 |
| | 2.5 | 16.2 | 16.47 | 16.62 | 16.91 | 17.24 | 17.24 |
| | 1.5 | 8.32 | 10.32 | 9.66 | 10.73 | 12.25 | 12.25 |
| Wait/Doze | 3.3 | 2.23 | 2.33 | 2.41 | 2..5 | 2.6 | 4.07 |
| | 2.5 | 16.2 | 16.48 | 16.62 | 16.91 | 17.24 | 18.77 |
| | 1.5 | 11.53 | 14.36 | 14.29 | 15.92 | 18.21 | 35.45 |
| Run | 3.3 | 6.79 | 9.02 | 14.56 | 19.54 | 29.12 | 30.43 |
| | 2.5 | 16.17 | 16.48 | 16.64 | 16.89 | 17.23 | 18.76 |
| | 1.5 | 16.29 | 20.36 | 21.13 | 23.57 | 27.0 | 44.1 |

NOTES:
1. All values are measured with a 3.30V $EV_{DD}$, 2.50V $SDV_{DD}$, and 1.5V $IV_{DD}$ power supplies. Tests performed at room temperature with pins configured for high drive strength.
2. Refer to the Power Management chapter in the *MCF5208 Reference Manual* for more information on low-power modes.
3. All peripheral clocks except UART0, FlexBus, INTC, reset controller, PLL, and Edge Port off before entering low-power mode. All code executed from flash.
4. Peak current measured while running a while(1) loop with all modules active.

5 See the description of the low-power control register (LCPR) in the *MCF5208 Reference Manual* for more information on stop modes 0–3.

The figure below illustrates the power consumption in a graphical format.

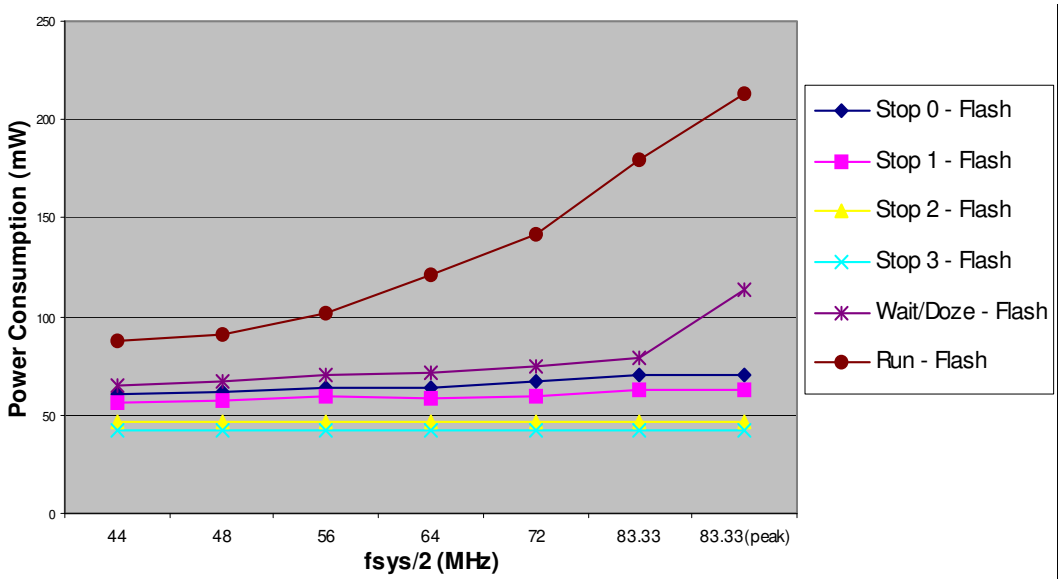



**Figure 12. Current Consumption in Low-Power Modes**

**Table 9. Typical Active Current Consumption Specifications[1]**

| $f_{sys/2}$ Frequency | Voltage (V) | Typical[2] Active (mA) | | Peak[3] Active (mA) |
|---|---|---|---|---|
| | | SRAM | Flash | |
| 1 MHz | 3.3 | 2.04 | 2.12 | 2.28 |
| | 2.5 | 15.24 | 15.32 | 15.24 |
| | 1.5 | 1.30 | 1.41 | 1.49 |
| 2 MHz | 3.3 | 2.23 | 2.40 | 3.57 |
| | 2.5 | 15.26 | 15.42 | 15.26 |
| | 1.5 | 1.71 | 1.92 | 2.09 |
| 4 MHz | 3.3 | 2.60 | 2.95 | 3.58 |
| | 2.5 | 15.30 | 15.61 | 15.30 |
| | 1.5 | 2.49 | 2.95 | 3.29 |
| 44 MHz | 3.3 | 7.61 | 17.67 | 25.34 |
| | 2.5 | 16.13 | 19.49 | 16.95 |
| | 1.5 | 24.04 | 28.72 | 39.02 |
| 48 MHz | 3.3 | 8.16 | 26.21 | 34.45 |
| | 2.5 | 16.28 | 20.06 | 17.17 |
| | 1.5 | 26.05 | 31.13 | 42.30 |

**Table 9. Typical Active Current Consumption Specifications[1] (continued)**

| $f_{sys/2}$ Frequency | Voltage (V) | Typical[2] Active (mA) | | Peak[3] Active (mA) |
|---|---|---|---|---|
| | | SRAM | Flash | |
| 56 MHz | 3.3 | 10.09 | 30.71 | 38.97 |
| | 2.5 | 16.43 | 20.71 | 17.65 |
| | 1.5 | 30.07 | 35.90 | 47.90 |
| 64 MHz | 3.3 | 15.72 | 31.37 | 42.10 |
| | 2.5 | 16.56 | 21.08 | 17.95 |
| | 1.5 | 32.19 | 38.72 | 53.50 |
| 72 MHz | 3.3 | 20.97 | 31.40 | 48.80 |
| | 2.5 | 16.87 | 21.70 | 18.20 |
| | 1.5 | 35.90 | 43.20 | 59.50 |
| 83.33 MHz | 3.3 | 31.37 | 25.83 | 48.60 |
| | 2.5 | 17.21 | 22.80 | 18.83 |
| | 1.5 | 41.10 | 49.40 | 67.50 |

NOTES:
1. All values are measured with a 3.30V $EV_{DD}$, 2.50V $SDV_{DD}$, and 1.5V $IV_{DD}$ power supplies. Tests performed at room temperature with pins configured for high drive strength.
2. CPU polling a status register. All peripheral clocks except UART0, FlexBus, INTC, reset controller, PLL, and edge port disabled.
3. Peak current measured while running a while(1) loop with all modules active.

# 5.6 Oscillator and PLL Electrical Characteristics

**Table 10. PLL Electrical Characteristics**

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|---|---|---|---|---|---|
| 1 | PLL Reference Frequency Range<br>Crystal reference<br>External reference | <br>$f_{ref\_crystal}$<br>$f_{ref\_ext}$ | <br>12<br>12 | <br>25[1]<br>40[1] | <br>MHz<br>MHz |
| 2 | Core frequency<br>CLKOUT Frequency[2] | $f_{sys}$<br>$f_{sys/2}$ | 488 x $10^{-6}$<br>244 x $10^{-6}$ | 166.66<br>83.33 | MHz<br>MHz |
| 3 | Crystal Start-up Time[3, 4] | $t_{cst}$ | — | 10 | ms |
| 4 | EXTAL Input High Voltage<br>Crystal Mode[5]<br>All other modes (External, Limp) | <br>$V_{IHEXT}$<br>$V_{IHEXT}$ | <br>$V_{XTAL}$ + 0.4<br>$E_{VDD}$/2 + 0.4 | <br>—<br>— | <br>V<br>V |
| 5 | EXTAL Input Low Voltage<br>Crystal Mode[5]<br>All other modes (External, Limp) | <br>$V_{ILEXT}$<br>$V_{ILEXT}$ | <br>—<br>— | <br>$V_{XTAL}$ - 0.4<br>$E_{VDD}$/2 - 0.4 | <br>V<br>V |
| 7 | PLL Lock Time [3, 6] | $t_{lpll}$ | — | 50000 | CLKIN |
| 8 | Duty Cycle of reference [3] | $t_{dc}$ | 40 | 60 | % |

**Table 10. PLL Electrical Characteristics (continued)**

| Num | Characteristic | Symbol | Min. Value | Max. Value | Unit |
|---|---|---|---|---|---|
| 9 | XTAL Current | $I_{XTAL}$ | 1 | 3 | mA |
| 10 | Total on-chip stray capacitance on XTAL | $C_{S\_XTAL}$ | | 1.5 | pF |
| 11 | Total on-chip stray capacitance on EXTAL | $C_{S\_EXTAL}$ | | 1.5 | pF |
| 12 | Crystal capacitive load | $C_L$ | | See crystal spec | |
| 13 | Discrete load capacitance for XTAL | $C_{L\_XTAL}$ | | $2*C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$ [7] | pF |
| 14 | Discrete load capacitance for EXTAL | $C_{L\_EXTAL}$ | | $2*C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$ [7] | pF |
| 17 | CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at $f_{SYS}$ Max<br>Peak-to-peak Jitter (Clock edge to clock edge)<br>Long Term Jitter | $C_{jitter}$ | <br>—<br>— | <br>10<br>TBD | <br>% $f_{sys/2}$<br>% $f_{sys/2}$ |
| 18 | Frequency Modulation Range Limit [3, 10, 11]<br>($f_{sys}$Max must not be exceeded) | $C_{mod}$ | 0.8 | 2.2 | %$f_{sys/2}$ |
| 19 | VCO Frequency. $f_{vco} = (f_{ref} * PFD)/4$ | $f_{vco}$ | 350 | 540 | MHz |

NOTES:
1 The maximum allowable input clock frequency when booting with the PLL enabled is 24 MHz. For higher input clock frequencies, the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.
2 All internal registers retain data at 0 Hz.
3 This parameter is guaranteed by characterization before qualification rather than 100% tested.
4 Proper PC board layout procedures must be followed to achieve specifications.
5 This parameter is guaranteed by design rather than 100% tested.
6 This specification is the PLL lock time only and does not include oscillator start-up time.
7 $C_{PCB\_EXTAL}$ and $C_{PCB\_XTAL}$ are the measured PCB stray capacitances on EXTAL and XTAL, respectively.
8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL $V_{DD}$, $EV_{DD}$, and $V_{SS}$ and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.
9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.
10 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100KHz.
11 Modulation range determined by hardware design.

## 5.7 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

**NOTE**

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.