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Freescale Semiconductor
Data Sheet: Advance Information

Document Number: MCF53017
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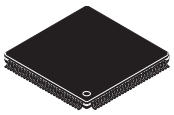
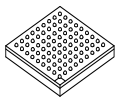
MCF53017



LQFP–208
28 x 28



MAPBGA–256
17 x 17

MCF5301*x* Data Sheet

Features

- Version 3 ColdFire® core with EMAC
- Up to 211 Dhrystone 2.1 MIPS @ 240 MHz
- 16 KBytes unified instruction/data cache
- 128 KBytes internal SRAM with standby power supply support
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- Enhanced Secure Digital Host Controller (eSDHC)
  - Supports CE-ATA, SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, MMC 4x, and MMC RS cards
- Two ISO7816 smart card interfaces
- IC identification module
- Voice-band audio codec with integrated speaker, microphone, headphone, and handset amplifiers
- 16- or 32-bit SDR, 16-bit DDR/mobile-DDR SDRAM controller
- USB 2.0 On-the-Go controller
- USB host controller
- 2 10/100 Ethernet MACs
- Coprocessor for acceleration of the DES, 3DES, AES, MD5, and SHA-1 algorithms
- Random number generator
- 16-channel DMA controller
- Synchronous serial interface
- 4 periodic interrupt timers
- 4 32-bit timers with DMA support
- Real-time clock (RTC) module with standby support
- DMA-supported serial peripheral interface (DSPI)
- 3 UARTs
- I^2C bus interface

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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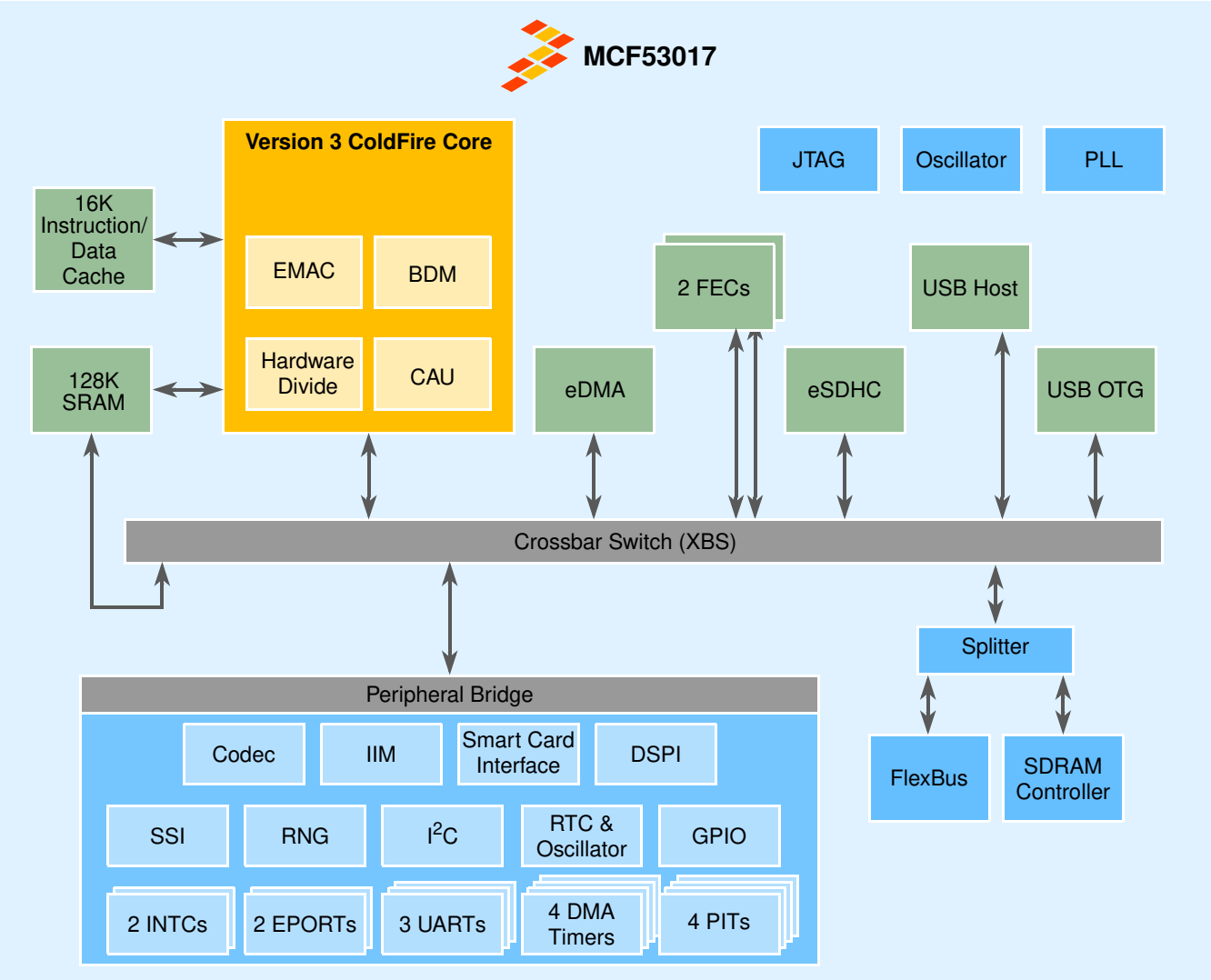


LEGEND

BDM	– Background debug module	**IIM**	– IC identification module
CAU	– Cryptography acceleration unit	**INTC**	– Interrupt controller
DSPI	– DMA serial peripheral interface	**JTAG**	– Joint Test Action Group interface
eDMA	– Enhanced direct memory access module	**PCI**	– Peripheral Component Interconnect
eSDHC	– Enhanced Secure Digital host controller	**PIT**	– Programmable interrupt timers
EMAC	– Enchanced multiply-accumulate unit	**PLL**	– Phase locked loop module
EPORT	– Edge port module	**RNG**	– Random number generator
FEC	– Fast Ethernet Controller	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-Integrated Circuit	**USB OTG**	– Universal Serial Bus On-the-Go controller

1 MCF5301*x* Family Comparison

The following table compares the various device derivatives available within the MCF5301*x* family.

Table 1. MCF5301*x* Family Configurations

Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
Version 3 ColdFire Core with EMAC (enhanced multiply-accumulate unit)	•	•	•	•	•	•	•	•
Core (system) clock	up to 240 MHz							
Peripheral and external bus clock (Core clock ÷ 3)	up to 80 MHz							
Performance (Dhrystone/2.1 MIPS)	up to 211							
Unified data/instruction cache	16 Kbytes							
Static RAM (SRAM)	128 Kbytes							
Voice-over-IP software	—	—	•	•	—	—	•	•
Cryptography acceleration unit (CAU)	—	•	—	•	—	•	—	•
Random number generator	—	•	—	•	—	•	—	•
Smart card interface (SIM)	1 port				2 ports			
Voice-band audio codec	•	•	•	•	•	•	•	•
Integrated audio amplifiers	—	—	—	—	•	•	•	•
IC identification module (IIM)	2 Kbits							
Enhanced Secure Digital host controller (eSDHC)	•	•	•	•	•	•	•	•
SDR/DDR SDRAM controller	•	•	•	•	•	•	•	•
FlexBus external interface	•	•	•	•	•	•	•	•
USB 2.0 On-the-Go	•	•	•	•	•	•	•	•
USB 2.0 Host	—	—	—	—	•	•	•	•
Synchronous serial interface (SSI)	•	•	•	•	•	•	•	•
Fast Ethernet controller (FEC)	2	2	2	2	2	2	2	2
UARTs	3	3	3	3	3	3	3	3
I^2C	•	•	•	•	•	•	•	•
DSPI	•	•	•	•	•	•	•	•
Real-time clock	•	•	•	•	•	•	•	•
32-bit DMA timers	4	4	4	4	4	4	4	4
Watchdog timer (WDT)	•	•	•	•	•	•	•	•
Periodic interrupt timers (PIT)	4	4	4	4	4	4	4	4
Edge port module (EPORT)	•	•	•	•	•	•	•	•
Interrupt controllers (INTC)	2	2	2	2	2	2	2	2

Table 1. MCF5301*x* Family Configurations (continued)

Module	MCF53010	MCF53011	MCF53012	MCF53013	MCF53014	MCF53015	MCF53016	MCF53017
16-channel direct memory access (DMA)	•	•	•	•	•	•	•	•
General purpose I/O Module (GPIO)	•	•	•	•	•	•	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•	•	•	•
Package	208 LQFP				256 MAPBGA			

2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Temperature
MCF53010CQT240	MCF53010 Microprocessor	208 LQFP	240 MHz	–40° to +85° C
MCF53011CQT240	MCF53011 Microprocessor			
MCF53012CQT240	MCF53012 Microprocessor			
MCF53013CQT240	MCF53013 Microprocessor			
MCF53014CMJ240J	MCF53014 Microprocessor	256 MAPBGA		
MCF53015CMJ240J	MCF53015 Microprocessor			
MCF53016CMJ240J	MCF53016 Microprocessor			
MCF53017CMJ240J	MCF53017 Microprocessor			
The following are not available from Freescale for import or sale in the United States prior to September 2010				
MCF53014CMJ240	MCF53014 Microprocessor	256 MAPBGA	240 MHz	–40° to +85° C
MCF53015CMJ240	MCF53015 Microprocessor			
MCF53016CMJ240	MCF53016 Microprocessor			
MCF53017CMJ240	MCF53017 Microprocessor			

3 Hardware Design Considerations

3.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 1 should be connected between the board IV_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated PV_{DD} pin as possible. The 10-ohm resistor in the given filter is required, do not implement the filter circuit using only capacitors. The PV_{DD} pins draw very little current, so concerns regarding voltage loss across the 10-ohm resistor are not valid.

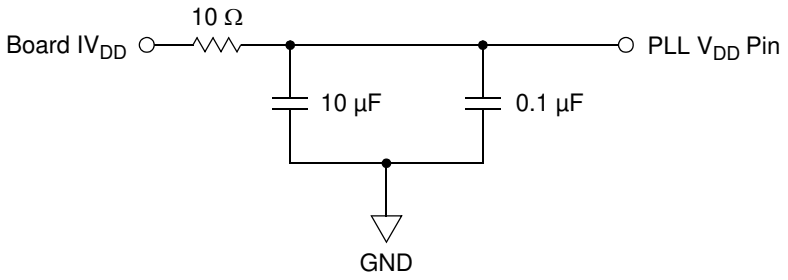


Figure 1. System PLL V_{DD} Power Filter

3.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

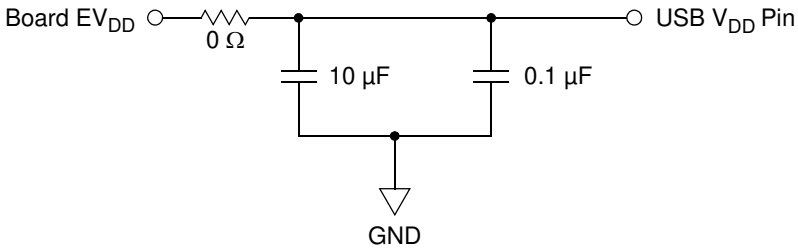


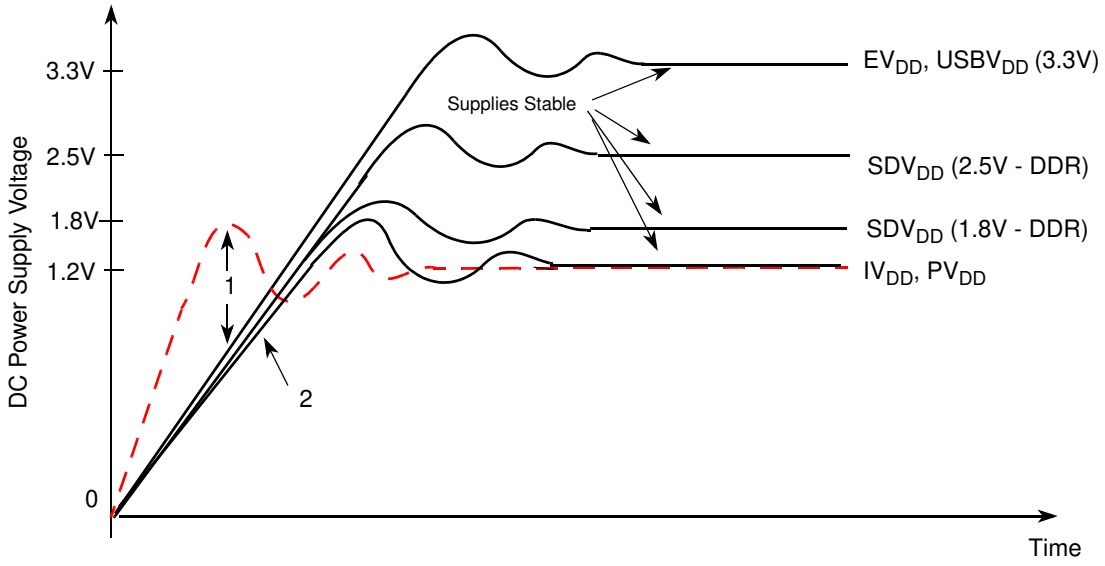
Figure 2. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

3.3 Supply Voltage Sequencing

Figure 3 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} (PV_{DD}), and internal logic / core V_{DD} (IV_{DD}). The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 1.8V) and EV_{DD} are specified relative to IV_{DD}.



Notes:
1. IV_{DD} should not exceed EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V at any time, including power-up.
2. Recommended that IV_{DD}/PV_{DD} should track EV_{DD}/SDV_{DD} up to 0.9V then separate for completion of ramps
3. Input voltage must not be greater than the supply voltage (EV_{DD}, SDV_{DD}, IV_{DD}, or PV_{DD}) by more than 0.5V at any time, including during power-up.
4. Use 1 microsecond or slower rise time for all supplies.

Figure 3. Supply Voltage Sequencing and Separation Cautions

3.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with the IV_{DD} at 0V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must power up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or PV_{DD} by more than 0.4V during power ramp up or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 microsecond to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 microsecond or slower rise time for all supplies.
2. IV_{DD}/PV_{DD} and EV_{DD}/SDV_{DD} should track up to 0.9V and then separate for the completion of ramps with EV_{DD}/SDV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

3.3.2 Power Down Sequence

If IV_{DD}/PV_{DD} are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and PV_{DD} power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or PV_{DD} going low by more than 0.4V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/PV_{DD} to 0V.
2. Drop EVDD/SDVDD supplies.

3.4 Power Consumption Specifications

Estimated maximum RUN mode power consumption measurements are shown in the below figure.

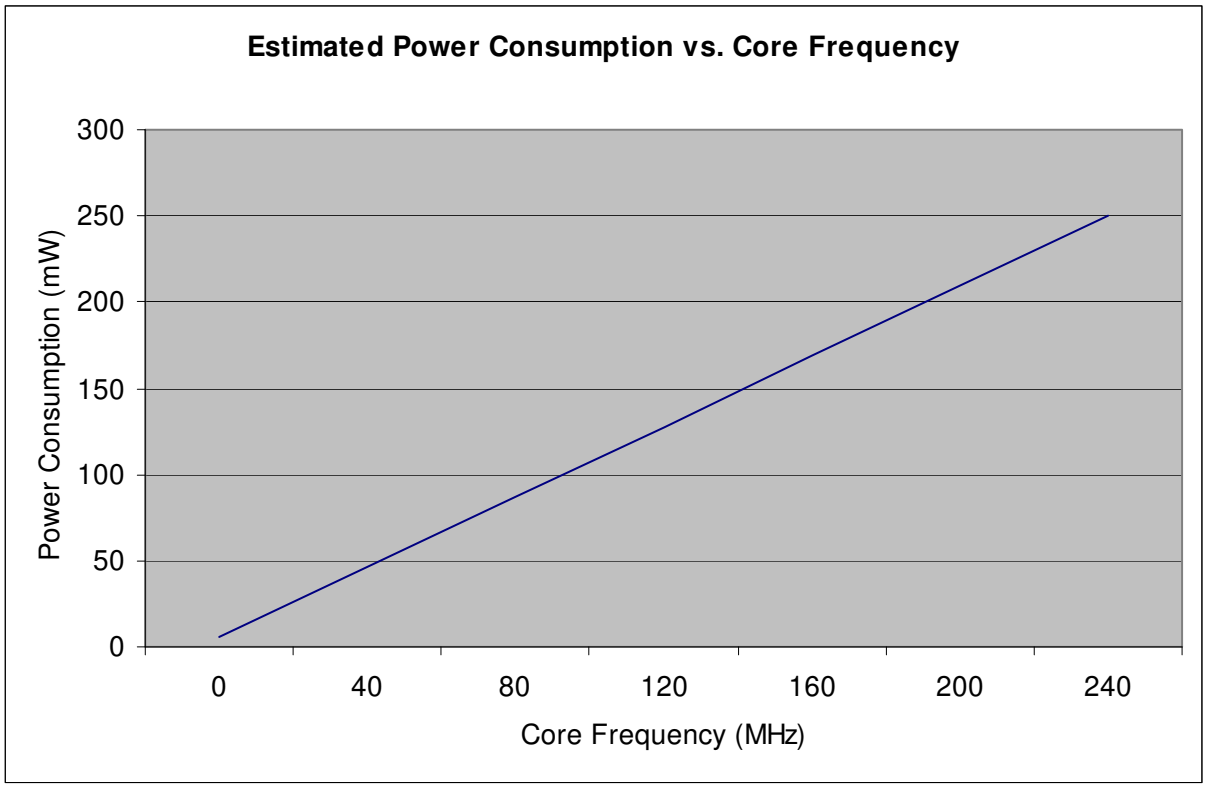


Figure 4. Estimated Maximum RUN Mode Power Consumption

Table 3 lists estimated maximum power and current consumption for the device in various operating modes.

Table 3. Estimated Maximum Power Consumption Specifications

Characteristic	Symbol	Typical	Max	Unit
Run Mode — Total Power Dissipation Static Dynamic		— — —	TBD TBD TBD	mW mW mW
Core Operating Supply Current [1] Run Mode	I_{DD}	—	82.9	mA
Pad Operating Supply Current Run Mode (application dependent) Wait Mode Stop Mode	EI_{DD}	 — — —	 TBD TBD TBD	 mA mA mA

[1] Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

Table 4. Current Measurementas at Different VCO vs. Core Frequencies

Stop Mode	480VCO, 240MHz core	240VCO, 120MHz core	480VCO, 120MHz core	480VCO, 48MHz core	Limp Mode, 20HMHz crystal
Executing	55.3mA	28.36mA	30.00mA	13.6mA	5.90mA
Run	39.5mA	20.3mA	22.02mA	10.29mA	4.42mA
Wait	16.28mA	8.53mA	10.23mA	5.53mA	2.43mA
Doze	16.19mA	8.53mA	10.18mA	5.55mA	2.41mA
Stop(0)	8.41mA	4.60mA	6.29mA	3.90mA	1.78mA
Stop(1)	8.13mA	4.48mA	6.15mA	3.88mA	1.77mA
Stop(2)	1.83mA	1.86mA	1.87mA	1.82mA	1.76mA
Stop(3)	0.65mA	0.66mA	0.67mA	0.67mA	0.65mA

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5301*x* pins grouped by function. The "Dir" column is the direction for the primary function of the pin only. Refer to Section 4.2, "Pinout—208 LQFP," and Section 4.3, "Pinout–256 MAPBGA," for package diagrams. For a more detailed discussion of the MCF3xx*x* signals, consult the *MCF5301x Reference Manual* (MCF53017RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_A23), while designations for multiple signals within a group use brackets (i.e., FB_A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO will default to their GPIO functionality. See Table 5 for a list of the exceptions.

Table 5. Special-Case Default Signal Functionality

Pin	Default Signal
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]
$\overline{\text{FB\_CS}}$[3:0]	$\overline{\text{FB\_CS}}$[3:0]
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$

Table 6. MCF5301*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Reset								
$\overline{\text{RESET}}$	—	—	—	U	I	EVDD	41	M3
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	42	N1
Clock								
EXTAL	—	—	—	—	I	EVDD	49	T2
XTAL	—	—	—	U[3]	O	EVDD	50	T3
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	55, 17	J5, G5
FlexBus								
FB_A[23:22]	—	$\overline{\text{FB\_CS}}$[3:2]	—	—	O	SDVDD	115, 114	P16, N16
FB_A[21:16]	—	—	—	—	O	SDVDD	113–108	R16, N14, N15, P15-13
FB_A[15:14]	—	SD_BA[1:0]	—	—	O	SDVDD	107, 106	R15, R14
FB_A[13:11]	—	SD_A[13:11]	—	—	O	SDVDD	105–103	N13, R12, R13
FB_A10	—	—	—	—	O	SDVDD	100	N12
FB_A[9:0]	—	SD_A[9:0]	—	—	O	SDVDD	99–97 95–89	P12, T14, T15, R11, P11, N11, T13, R10, T11, T12
FB_D[31:16]	—	SD_D[31:16]	—	—	I/O	SDVDD	208–198, 57–62, 64, 65	B3, A2, D6, C5, B4, A3, B5, C6, D12, C14, B14, C13, D11, B13, A14, A13
FB_D[15:0]	—	FB_D[31:16]	—	—	I/O	SDVDD	182–189, 177–170	B9, A9, A8, D7, B8, C8, D8, B7, C10, A10, B10, D10, C11, A11, B11, A12
FB_CLK	—	—	—	—	O	SDVDD	153	D13
$\overline{\text{FB\_BE/BWE}}$[3:0]	PBE[3:0]	SD_DQM[3:0]	—	—	O	SDVDD	197, 166, 179, 178	A4, B12, C9, D9
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	—	O	SDVDD	—	B6, C7
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	—	O	SDVDD	5	D2
$\overline{\text{FB\_CS0}}$	PCS0	$\overline{\text{FB\_CS4}}$	—	—	O	SDVDD	6	C2
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	SDVDD	1	D4
$\overline{\text{FB\_TA}}$	PFBCTL2	—	—	U	I	SDVDD	3	B2
FB_R/$\overline{\text{W}}$	PFBCTL1	—	—	—	O	SDVDD	2	C3
$\overline{\text{FB\_TS}}$	PFBCTL0	$\overline{\text{DACK0}}$	—	—	O	SDVDD	4	D3
SDRAM Controller								
SD_A10	—	—	—	—	O	SDVDD	206	C4

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
SD_CAS	—	—	—	—	O	SDVDD	154	D15
SD_CKE	—	—	—	—	O	SDVDD	151	B15
SD_CLK	—	—	—	—	O	SDVDD	190	A7
SD_CLK	—	—	—	—	O	SDVDD	191	A6
SD_CS0	—	—	—	—	O	SDVDD	155	A15
SD_DQS[1:0]	—	—	—	—	O	SDVDD	196, 167	C12, A5
SD_RAS	—	—	—	—	O	SDVDD	152	C15
SD_SDR_DQS	—	—	—	—	I	SDVDD	207	D5
SD_WE	—	—	—	—	O	SDVDD	150	D14
External Interrupts Port 1[4,5]								
IRQ1DEBUG[7:4]	PIRQ1DEBUG [7:4]	DDATA[3:0]	—	—	I	EVDD	—	H1, H4-2
IRQ1DEBUG[3:0]	PIRQ1DEBUG [3:0]	PST[3:0]	—	—	I	EVDD	—	K14, H14, K15, J13
IRQ1FEC7	PIRQ1FEC7	RMII1_CRS_DV	MII0_CRS	—	I	EVDD	29	J1
IRQ1FEC6	PIRQ1FEC6	RMII1_RXER	MII0_RXCLK	—	I	EVDD	30	J2
IRQ1FEC5	PIRQ1FEC5	RMII1_TXEN	MII0_TXCLK	—	I	EVDD	31	K4
IRQ1FEC4	PIRQ1FEC4	RMII1_REF_CLK	—	D	I	EVDD	32	J3
IRQ1FEC[3:2]	PIRQ1FEC[3:2]	RMII1_RXD[1:0]	MII0_RXD[3:2]	—	I	EVDD	33, 34	J4, K1
IRQ1FEC[1:0]	PIRQ1FEC[1:0]	RMII1_TXD[1:0]	MII0_TXD[3:2]	—	I	EVDD	35, 36	K2, L1
External Interrupts Port 0[5]								
IRQ07	PIRQ07	—	—	U	I	EVDD	10	E4
IRQ06	PIRQ06	—	USB_CLKIN	U	I	EVDD	—	L13
IRQ04	PIRQ04	DREQ0	—	U	I	EVDD	19	D1
IRQ01	PIRQ01	DREQ1	—	U	I	EVDD	11	F4
Enhanced Secure Digital Host Controller								
SDHC_DAT3	PSDHC5	—	—	UD	I/O	EVDD	60	N4
SDHC_DAT[2:0]	PSDHC[4:2]	—	—	U	I/O	EVDD	61–63	R5, N6, N5
SDHC_CMD	PSDHC1	—	—	U	I/O	EVDD	59	R4
SDHC_CLK	PSDHC0	—	—	—	O	EVDD	58	R3

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Codec								
CODEC_ADCN	—	AMP_MICN	—	—	I		85	P10
CODEC_ADCP	—	AMP_MICP	—	—	I		84	P9
CODEC_BGRVREF	—	—	—	—	I		86	N9
CODEC_DACN	—	AMP_HSN	—	—	O		75	R7
CODEC_DACP	—	AMP_HSP	—	—	O		67	R6
CODEC_REGBYP	—	—	—	—	I		81	P6
CODEC_REFN	—	—	—	—	I		79	P8
CODEC_REFP	—	—	—	—	I		78	P7
CODEC_VAG	—	—	—	—	I		82	N7
Amplifiers								
AMP_HPDUMMY	—	—	—	—	O		—	R9
AMP_HPOUT	—	—	—	—	O		—	R8
AMP_SPKRN	—	—	—	—	O		—	T9
AMP_SPKRP	—	—	—	—	O		—	T7
Smart Card interface 1								
SIM1_DATA	PSIM14	SSI_TXD	U1TXD	UD	I/O	EVDD	141	E14
SIM1_VEN	PSIM13	SSI_RXD	U1RXD	UD	O	EVDD	142	D16
SIM1_RST	PSIM12	SSI_FS	$\overline{\text{U1RTS}}$	—	O	EVDD	144	E13
SIM1_PD	PSIM11	SSI_BCLK	$\overline{\text{U1CTS}}$	—	O	EVDD	145	E15
SIM1_CLK	PSIM10	SSI_MCLK	—	—	O	EVDD	143	F13
Smart Card interface 0								
SIM0_DATA	PSIM04	—	—	—	I/O	EVDD	—	L3
SIM0_VEN	PSIM03	—	—	—	O	EVDD	—	M2
SIM0_RST	PSIM02	—	—	—	O	EVDD	—	F16
SIM0_PD	PSIM01	—	—	—	O	EVDD	—	L14
SIM0_CLK	PSIM00	—	—	—	O	EVDD	—	M16
USB On-the-Go								
USBO_DM	—	—	—	—	O	USB VDD	148	C16
USBO_DP	—	—	—	—	O	USB VDD	149	B16

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
USB Host								
USBH_DM	—	—	—	—	O	USB VDD	—	B1
USBH_DP	—	—	—	—	O	USB VDD	—	C1
FEC 1								
RMII1_MDC	PFECI2C5	—	MII0_TXER	—		EVDD	22	E1
RMII1_MDIO	PFECI2C4	—	MII0_COL	—		EVDD	23	F1
FEC 0								
RMII0_CRS_DV	PFEC06	—	MII0_RXDV	—		EVDD	131	G16
RMII0_RXD[1:0]	PFEC0[5:4]	—	MII0_RXD[1:0]	—		EVDD	130, 129	H15, H16
RMII0_RXER	PFEC03	—	MII0_RXER	—		EVDD	127	J16
RMII0_TXD[1:0]	PFEC0[2:1]	—	MII0_TXD[1:0]	—		EVDD	125, 124	J15, J14
RMII0_TXEN	PFEC00	—	MII0_TXEN	D		EVDD	123	K16
RMII0_MDC	PFECI2C3	—	MII0_MDC	—		EVDD	133	G14
RMII0_MDIO	PFECI2C2	—	MII0_MDIO	—		EVDD	132	G15
Real Time Clock								
RTC_EXTAL	—	—	—	—	I	EVDD	—	P1
RTC_XTAL	—	—	—	—	O	EVDD	—	R1
Synchronous Serial Interface								
SSI_RXD	PSSI4	—	U1RXD	UD	I	EVDD	—	N3
SSI_TXD	PSSI3	—	U1TXD	UD	O	EVDD	—	P3
SSI_FS	PSSI2	—	$\overline{\text{U1RTS}}$	—	I/O	EVDD	—	R2
SSI_MCLK	PSSI1	—	SSI_CLKIN	—	O	EVDD	—	P4
SSI_BCLK	PSSI0	—	$\overline{\text{U1CTS}}$	—	I/O	EVDD	—	P5
I^2C								
I2C_SCL	PFECI2C1	U2RXD	RMII1_MDC	U	I/O	EVDD	37	M1
I2C_SDA	PFECI2C0	U2TXD	RMII1_MDIO	U	I/O	EVDD	38	K3
DSPI								
DSPI_PCS3	PDSPI6	USBH_VBUS_EN	—	—	I/O	EVDD	—	P2
DSPI_PCS2	PDSPI5	USBH_VBUS_OC	—	—	I/O	EVDD	—	N2

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
DSPI_PCS1	PDSPI4	—	—	—	I/O	EVDD	140	F14
DSPI_PCS0/$\overline{SS}$	PDSPI3	$\overline{U2RTS}$	—	U	I/O	EVDD	137	G13
DSPI_SCK	PDSPI2	$\overline{U2CTS}$	—	—	I/O	EVDD	134	H13
DSPI_SIN	PDSPI1	U2RXD	—	—	I	EVDD	136	E16
DSPI_SOUT	PDSPI0	U2TXD	—	—	O	EVDD	135	F15
UARTs								
U2RXD	PUART5	—	—	—	I	EVDD	14	E2
U2TXD	PUART4	—	—	—	O	EVDD	18	F2
$\overline{U0CTS}$	PUART3	USBO_VBUS_EN	USB_PULLUP	—	I	EVDD	20	G4
$\overline{U0RTS}$	PUART2	USBO_VBUS_OC	—	—	O	EVDD	21	G3
U0RXD	PUART1	—	—	—	I	EVDD	27	G2
U0TXD	PUART0	—	—	—	O	EVDD	28	G1
DMA Timers								
T3IN	PTIMER3	T3OUT	IRQ03	—	I	EVDD	13	F3
T2IN	PTIMER2	T2OUT	IRQ02	—	I	EVDD	12	E3
T1IN	PTIMER1	T1OUT	$\overline{DACK1}$	—	I	EVDD	122	K13
T0IN	PTIMER0	T0OUT	CODEC_ALTCLK	—	I	EVDD	121	L16
BDM/JTAG[6]								
ALLPST	PDEBUG	—	—	—	O	EVDD	43	—
JTAG_EN	—	—	—	D	I	EVDD	64	M8
PSTCLK	—	TCLK	—	—	I	EVDD	65	T5
DSI	—	TDI	—	U	I	EVDD	66	T4
DSO	—	TDO	—	—	O	EVDD	120	M15
$\overline{BKPT}$	—	TMS	—	U	I	EVDD	119	M14
DSCLK	—	$\overline{TRST}$	—	U	I	EVDD	118	L15

Table 6. MCF5301*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF53010 MCF53011 MCF53012 MCF53013 208 LQFP	MCF53014 MCF53015 MCF53016 MCF53017 256 MAPBGA
Test								
TEST	—	—	—	D	I	EVDD	146	F12
Power Supplies								
IVDD	—	—	—	—	—	—	16, 44, 69, 77, 128, 169, 193	E9, F8, F9, H5, H6, H11, H12, J6, J11, L8, L9
EVDD	—	—	—	—	—	—	9, 24, 26, 40, 47, 51, 54, 57, 74, 126, 139, 195	F5, G6, G11, G12, J12, K6, K11, K12, L5-7, L10-12, M5-7, M12
SD_VDD	—	—	—	—	—	—	7, 102, 116, 156, 163, 181, 208	E5, E6, E10-12, F6, F7, F10, F11
VDD_OSC_A_PLL	—	—	—	—	—	—	46	M4
VDD_USBO	—	—	—	—	—	—	147	E7
VDD_USBH	—	—	—	—	—	—	—	E8
VDD_RTC	—	—	—	—	—	—	—	
AVDD_CODEC	—	—	—	—	—	—	80	N8
AVDD_SPKR	—	—	—	—	—	—	—	T8
VDD_EPM	—	—	—	—	—	—	96	M9
VSTBY_SRAM	—	—	—	—	—	—	—	L2
VSTBY_RTC	—	—	—	—	—	—	—	L4
VSS	—	—	—	—	—	—	8, 15, 25, 39, 45, 48, 52, 53, 56, 68, 73, 76, 101, 117, 138, 168, 180, 192, 194	A1, A16, G7-10, H7-10, J7-10, K7-10, T1, T16
VSS_CODEC	—	—	—	—	—	—	83	N10
AVSS_SPKR_HDST	—	—	—	—	—	—	—	T6
AVSS_SPKR_HP	—	—	—	—	—	—	—	T10

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 The edge port 1 signals are the primary functions on two sets of pins (IRQ1FEC*n* and IRQ1DEBUG*n*). If an IRQ1 function is configured on both pins, the IRQ1FEC*n* pin takes priority. The corresponding IRQ1DEBUG*n* pin is disconnected internally from the edge port 1 module.

5 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

6 If JTAG_EN is asserted, these pins default to alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

4.2 Pinout—208 LQFP

The pinout for the 208 LQFP devices is shown in Figure 5 and Figure 6.

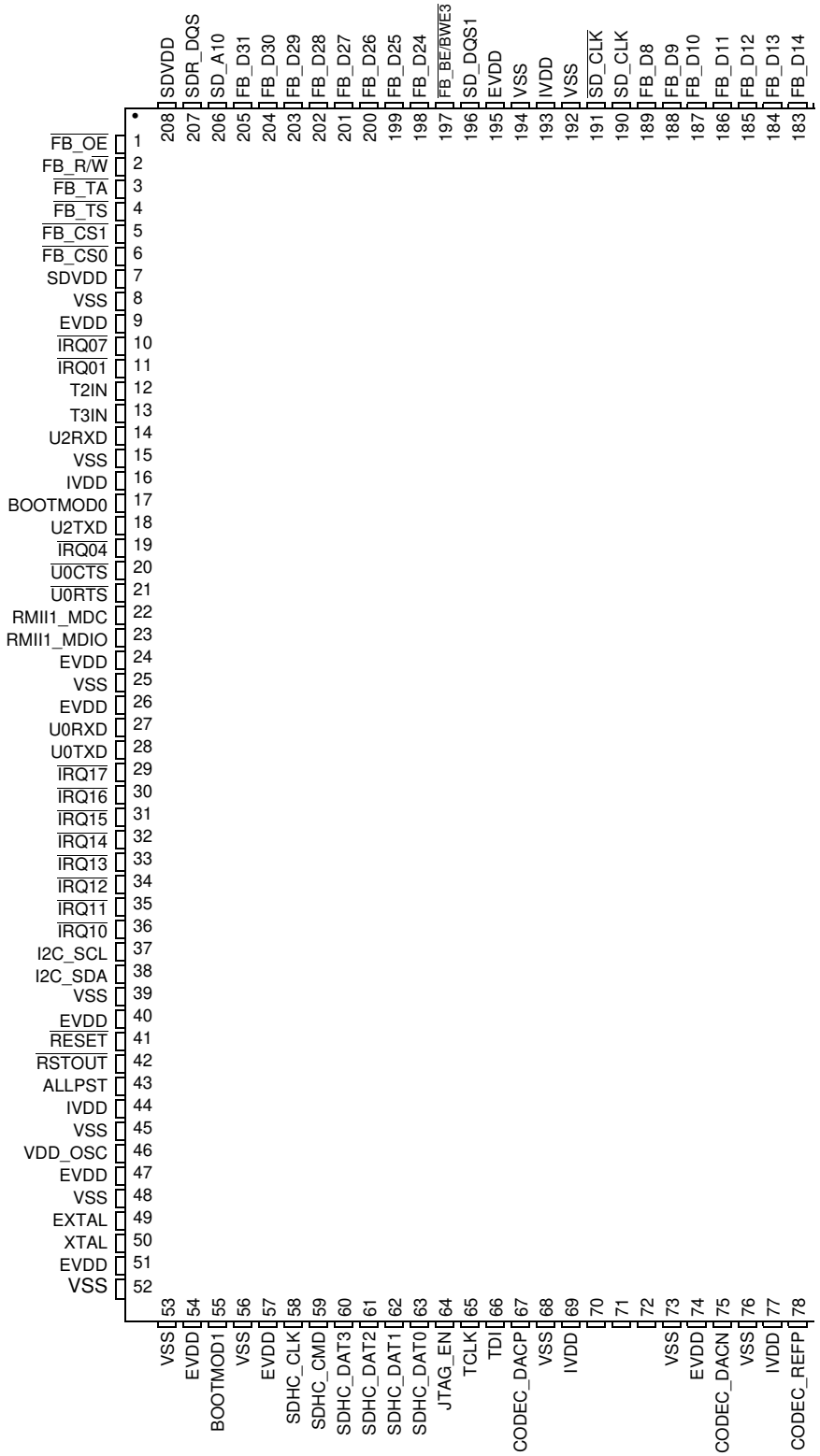


Figure 5. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Left (208 QFP)

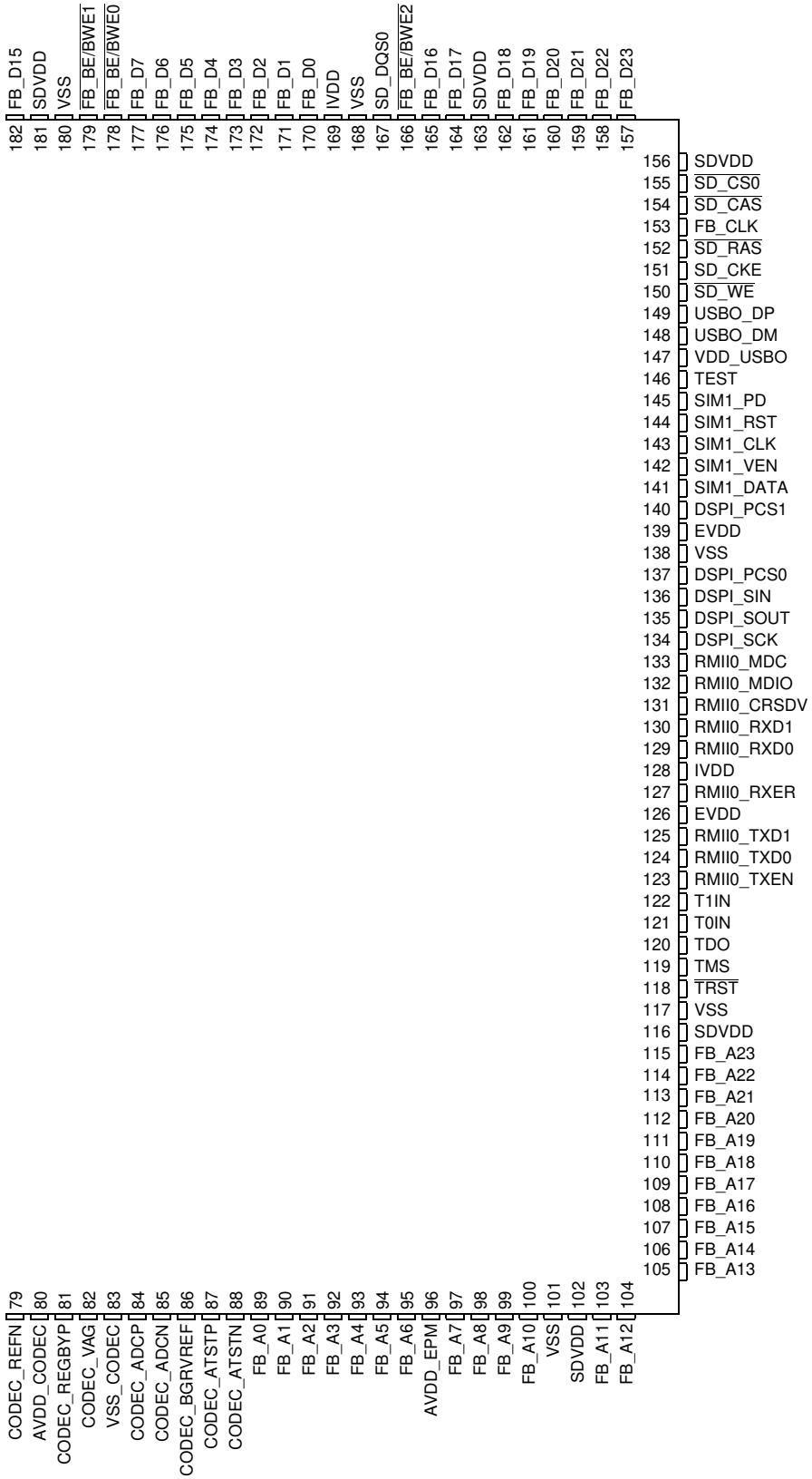


Figure 6. MCF53010, MCF53011, MCF53012, and MCF53013 Pinout Top View, Right (208 QFP)

4.3 Pinout–256 MAPBGA

The pinout for the MCF53014, MCF53015, MCF53016, and MCF53017 packages are shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FB_D 30	FB_D 26	FB_BE/ BWE3	SD_ DQS1	SD_ CLK	SD_ CLK	FB_D 13	FB_D 14	FB_D 6	FB_D 2	FB_D 0	FB_D 16	FB_D 17	SD_CS	VSS	A
B	USBH_ DM	FB_TA	FB_D 31	FB_D 27	FB_D 25	FB_CS5	FB_D 8	FB_D 11	FB_D 15	FB_D 5	FB_D 1	FB_BE/ BWE2	FB_D 18	FB_D 21	SD_ CKE	USBO_ DP	B
C	USBH_ DP	FB_CS0	FB_R/W	SD_A10	FB_D 28	FB_D 24	FB_CS4	FB_D 10	FB_BE/ BWE1	FB_D 7	FB_D 3	SD_ DQS2	FB_D 20	FB_D 22	SD_ RAS	USBO_ DM	C
D	IRQ04	FB_CS1	FB_TS	FB_OE	SD_SDR _DQS	FB_D 29	FB_D 12	FB_D 9	FB_BE/ BWE0	FB_D 4	FB_D 19	FB_D 23	FB_CLK	SD_ WE	SD_ CAS	SIM1_ VEN	D
E	RMII1_ MDC	U2RXD	T2IN	IRQ07	SDVDD	SDVDD	VDD_ USBO	VDD_ USBH	IVDD	SDVDD	SDVDD	SDVDD	SIM1_ RST	SIM1_ DATA	SIM1_ PD	DSPI_ SIN	E
F	RMII1_ MDIO	U2TXD	T3IN	IRQ01	EVDD	SDVDD	SDVDD	IVDD	IVDD	SDVDD	SDVDD	TEST	SIM1_ CLK	DSPI_ PCS1	DSPI_ SOUT	SIM0_ RST	F
G	U0TXD	U0RXD	U0RTS	U0CTS	BOOT MOD0	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	DSPI_ PCS0	RMII0_ MDC	RMII0_ MDIO	RMII0_ CRSDV	G
H	IRQ1 DEBUG7	IRQ1 DEBUG4	IRQ1 DEBUG5	IRQ1 DEBUG6	IVDD	IVDD	VSS	VSS	VSS	VSS	IVDD	IVDD	DSPI_ SCK	IRQ1 DEBUG2	RMII0_ RXD1	RMII0_ RXD0	H
J	IRQ1 FEC7	IRQ1 FEC6	IRQ1 FEC4	IRQ1 FEC3	BOOT MOD1	IVDD	VSS	VSS	VSS	VSS	IVDD	EVDD	IRQ1 DEBUG0	RMII0_ TXD0	RMII0_ TXD1	RMII0_ RXER	J
K	IRQ1 FEC2	IRQ1 FEC1	I2C_ SDA	IRQ1 FEC5	NC	EVDD	VSS	VSS	VSS	VSS	EVDD	EVDD	T1IN	IRQ1 DEBUG3	IRQ1 DEBUG1	RMII0_ TXEN	K
L	IRQ1 FEC0	VSTBY_ SRAM	SIM0_ DATA	VSTBY_ RTC	EVDD	EVDD	EVDD	IVDD	IVDD	EVDD	EVDD	EVDD	IRQ06	SIM0_ PD	TRST	T0IN	L
M	I2C_ SCL	SIM0_ VEN	RESET	VDD_ OSC_A_ PLL	EVDD	EVDD	EVDD	JTAG_ EN	VDD_ EPM	NC	NC	EVDD	NC	TMS	TDO	SIM0_ CLK	M
N	RST OUT	DSPI_ PCS2	SSI_ RXD	SDHC_ DAT3	SDHC_ DAT0	SDHC_ DAT1	CODEC _VAG	AVDD_ CODEC	CODEC _BGR VREF	VSS_ CODEC	FB_A4	FB_A10	FB_A13	FB_A20	FB_A19	FB_A22	N
P	RTC_ EXTAL	DSPI_ PCS3	SSI_ TXD	SSI_ MCLK	SSI_ BCLK	CODEC _REG BYP	CODEC _REFP	CODEC _REFN	CODEC _ADCP	CODEC _ADCN	FB_A5	FB_A9	FB_A16	FB_A17	FB_A18	FB_A23	P
R	RTC_ XTAL	SSI_FS	SDHC_ CLK	SDHC_ CMD	SDHC_ DAT2	CODEC _DACP	CODEC _DACN	AMP_ HP OUT	AMP_ HP DUMMY	FB_A2	FB_A6	FB_A12	FB_A11	FB_A14	FB_A15	FB_A21	R
T	VSS	EXTAL	XTAL	TDI	TCLK	AVSS_ SPKR_ HDST	AMP_ SPKRP	AVDD_ SPKR	AMP_ SPKRN	AVSS_ SPKR_ HP	FB_A1	FB_A0	FB_A3	FB_A8	FB_A7	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 7. MCF53014, MCF53015, MCF53016, and MCF53017 Pinout (256 MAPBGA)

5 Preliminary Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5301*x* microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	–0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	–0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	–0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	–0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	–0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L – T_H)	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

1 Functional operating conditions are given in Section 5.4, "DC Electrical Specifications." Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Insure external EV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	256 MAPBGA	208 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	36[1,2]	38[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	32[1,2]	33[1,2]	°C/W
Junction to board		θ_{JB}	25[3]	29[3]	°C/W
Junction to case		θ_{JC}	14[4]	11[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	3[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts – Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 9. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with JEDEC JESD22-A114 specification.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.08	1.32	V
SRAM Standby Voltage	$SRAMV_{STBY}$	1.08	1.32	V
RTC Standby Voltage	$RTCV_{STBY}$	3.0	3.6	V
PLL Supply Voltage	$PLLV_{DD}$	3.0	3.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.70 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	$0.51 \times EV_{DD}$	$EV_{DD} + 0.3$	V
CMOS Input Low Voltage	EV_{IL}	$V_{SS} - 0.3$	$0.42 \times EV_{DD}$	V
CMOS Output High Voltage $I_{OH} = -2.0$ mA	EV_{OH}	$0.8 \times EV_{DD}$	—	V
CMOS Output Low Voltage $I_{OL} = 2.0$ mA	EV_{OL}	—	$0.2 \times EV_{DD}$	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 $SDV_{DD} \times 0.7$ Vref+0.15 2	 SDV_{DD}+0.3 SDV_{DD}+0.3 $SDV_{DD} + 0.3$	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 –0.3 –0.3 $V_{SS} - 0.3$	 $SDV_{DD} \times 0.3$ Vref+0.15 0.8	V

Table 10. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 SDVDD × 0.9 SDV_{DD} – 0.35 2.9	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 SDV_{DD} × 0.1 0.35 0.4	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–2.5	2.5	µA
Weak Internal Pull-Up/Pull-down Device Current[1]	I_{APU}	10	315	µA
Selectable Weak Internal Pull-Up/Pull-down Device Current[2]	I_{APU}	25	150	µA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.
2 Refer to the signals section for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.

5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 8 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

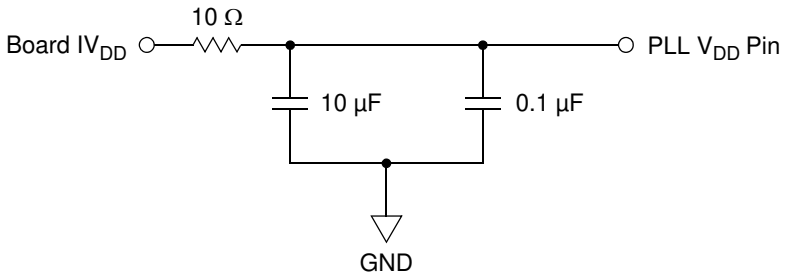


Figure 8. System PLL V_{DD} Power Filter

5.4.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 2 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

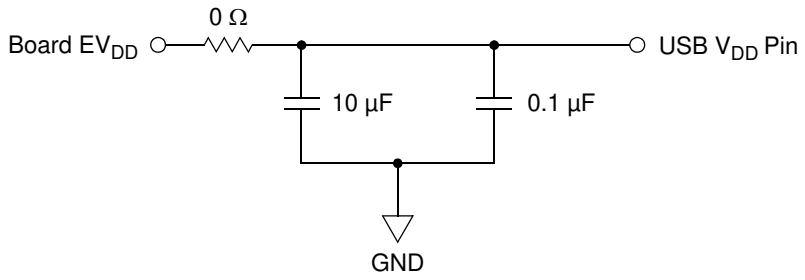


Figure 9. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

5.4.3 Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

5.4.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or $PLLV_{DD}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

5.4.3.2 Power Down Sequence

If IV_{DD}/$PLLV_{DD}$ are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop IV_{DD}/$PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

5.5 Oscillator and PLL Electrical Characteristics

Table 11. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 14 14	 25[1] 48[1]	 MHz MHz
2	Core frequency CLKOUT Frequency[2]	f_{sys} $f_{sys/3}$	488 x 10^{-6} 163 x 10^{-6}	240 80	MHz MHz
3	Crystal Start-up Time[3, 4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3, 6]	t_{lpll}	—	750	us
8	Duty Cycle of reference [3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
12	Crystal capacitive load	C_L	—	See crystal spec	
13	Discrete load capacitance for XTAL	C_{L_XTAL}	—	$2 \times C_L - C_{S\_XTAL} - C_{PCB\_XTAL}$[7]	pF
14	Discrete load capacitance for EXTAL	C_{L_EXTAL}	—	$2 \times C_L - C_{S\_EXTAL} - C_{PCB\_EXTAL}$[7]	pF
17	CLKOUT Period Jitter, [3, 4, 7, 8, 9] Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter	C_{jitter}	 — —	 TBD TBD	 % $f_{sys/3}$ % $f_{sys/3}$
18	Frequency Modulation Range Limit [3, 10, 11] (f_{sys}Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/3}$
19	VCO Frequency. $f_{vco} = (f_{ref} \times PFD)/4$	f_{vco}	200	667	MHz

1 The maximum allowable input clock frequency when booting with the PLL enabled is 24MHz. For higher input clock frequencies the processor must boot in LIMP mode to avoid violating the maximum allowable CPU frequency.
2 All internal registers retain data at 0 Hz.
3 This parameter is guaranteed by characterization before qualification rather than 100% tested.
4 Proper PC board layout procedures must be followed to achieve specifications.
5 This parameter is guaranteed by design rather than 100% tested.
6 This specification is the PLL lock time only and does not include oscillator start-up time..
7 C_{PCB_EXTAL} and C_{PCB_XTAL} are the measured PCB stray capacitances on EXTAL and XTAL, respectively.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

9 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.

10 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100kHz.

11 Modulation range determined by hardware design.

5.6 External Interface Timing Characteristics

Table 12 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 12 are shown in Figure 11 and Figure 12.

* The timings are also valid for inputs sampled on the negative clock edge.

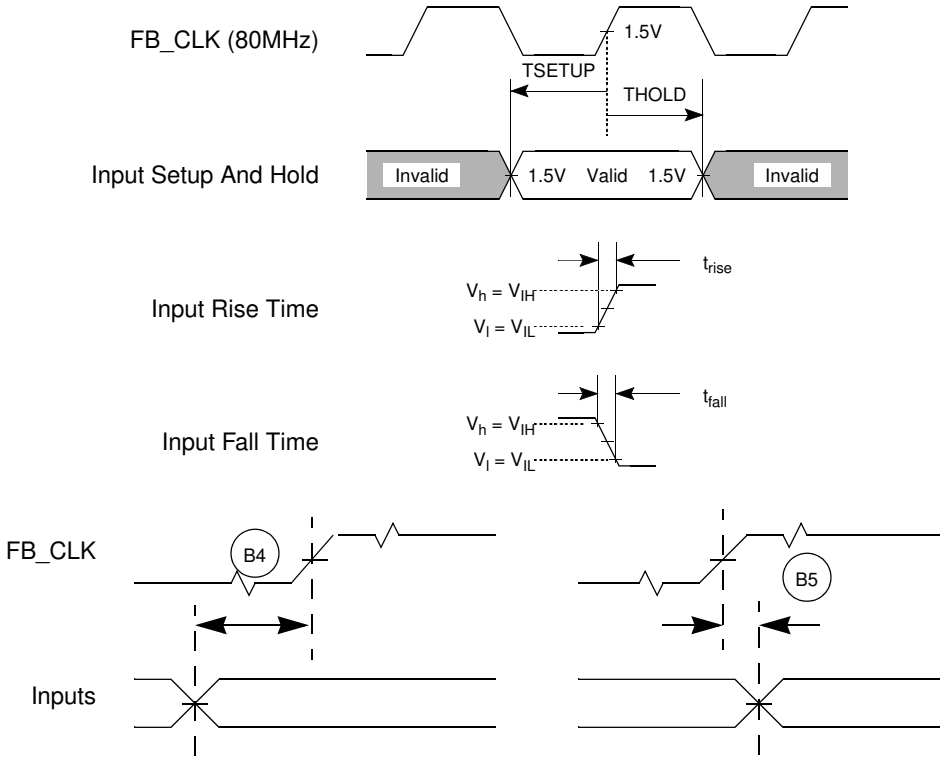


Figure 10. General Input Timing Requirements

5.6.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces.