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HC11

MC68HC11F1

Technical Data

Home Page:
www.freescale.com
email:
support@freescale.com
USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com
Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com
Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com
Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com
For Literature Requests Only:
Freescale Semiconductor
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303-675-2140
Fax: 303-675-2150
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SECTION 1INTRODUCTION

The MC68HC11F1 high-performance microcontroller unit (MCU) is an enhanced derivative of the M68HC11 family of microcontrollers and includes many advanced features. This MCU, with a nonmultiplexed expanded bus, is characterized by high speed and low power consumption. The fully static design allows operation at frequencies from 4 MHz to dc.

1.1 Features

- M68HC11 Central Processing Unit (CPU)
- Power Saving STOP and WAIT Modes
- 512 Bytes Electrically Erasable Programmable Read-Only Memory (EEPROM)
- 1024 Bytes RAM, Data Retained During Standby
- Nonmultiplexed Address and Data Buses
- Enhanced 16-Bit Timer
- Three Input Capture (IC) Channels
- Four Output Compare (OC) Channels
- One Additional Channel, Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog
- Enhanced Asynchronous Nonreturn to Zero (NRZ) Serial Communications Interface (SCI)
- Enhanced Synchronous Serial Peripheral Interface (SPI)
- Eight-Channel 8-Bit Analog-to-Digital (A/D) Converter
- Four Chip-Select Signal Outputs with Programmable Clock Stretching
  - — Two I/O Chip Selects
  - — One Program Chip Select
  - — One General-Purpose Chip Select
- Available in 68-Pin Plastic Leaded Chip Carrier (PLCC) and 80-Pin Plastic Quad Flat Pack (QFP)

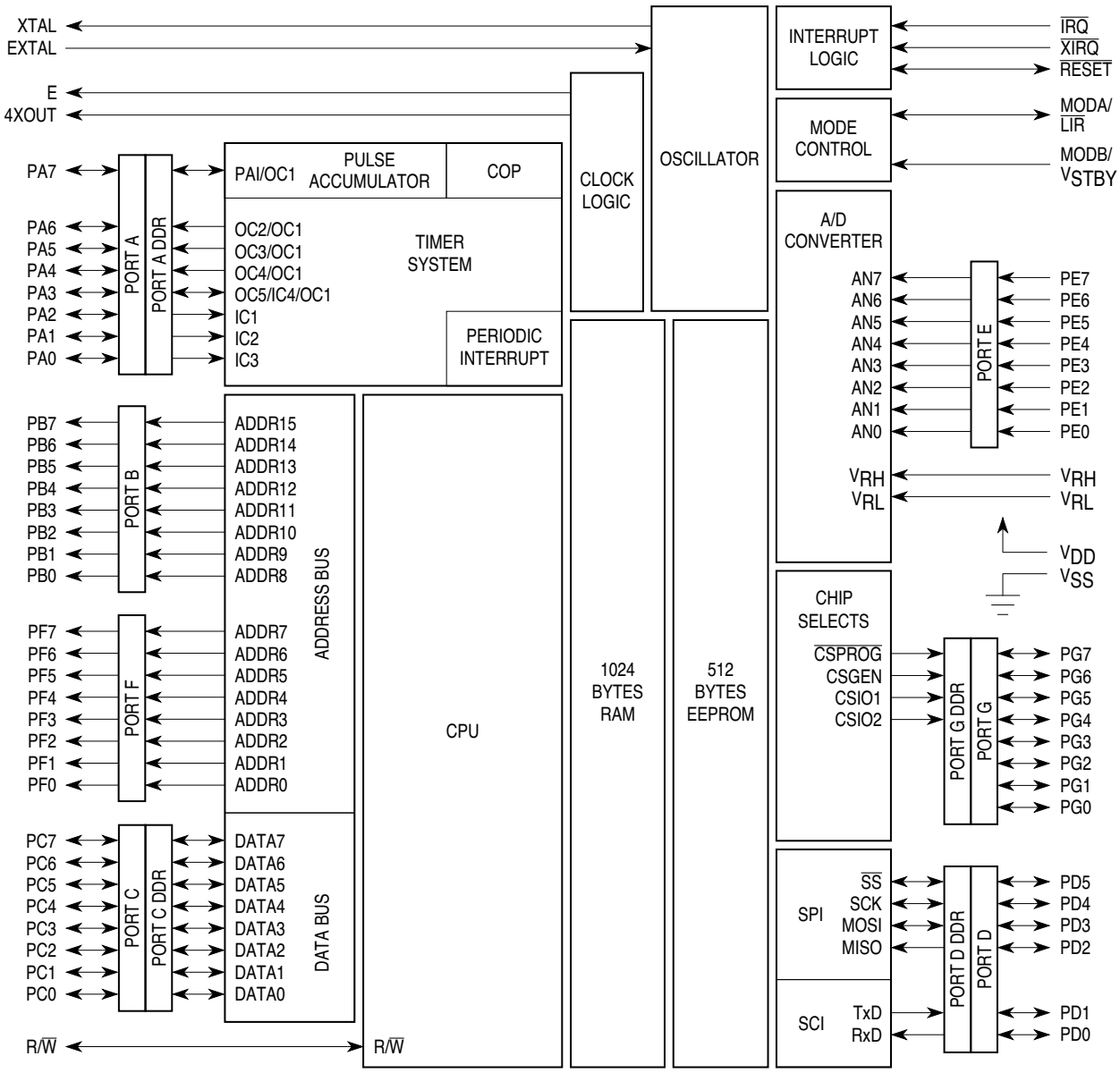

Figure 1-1 MC68HC11F1 Block Diagram

SECTION 2 PIN DESCRIPTIONS

The MC68HC11F1 MCU is available in a 68-pin plastic leaded chip carrier (PLCC) and an 80-pin plastic quad flat pack (QFP). Most pins on this MCU serve two or more functions, as described in the following paragraphs. **Figure 2-1** shows the pin assignments for the PLCC. **Figure 2-2** shows the pin assignments for the QFP.

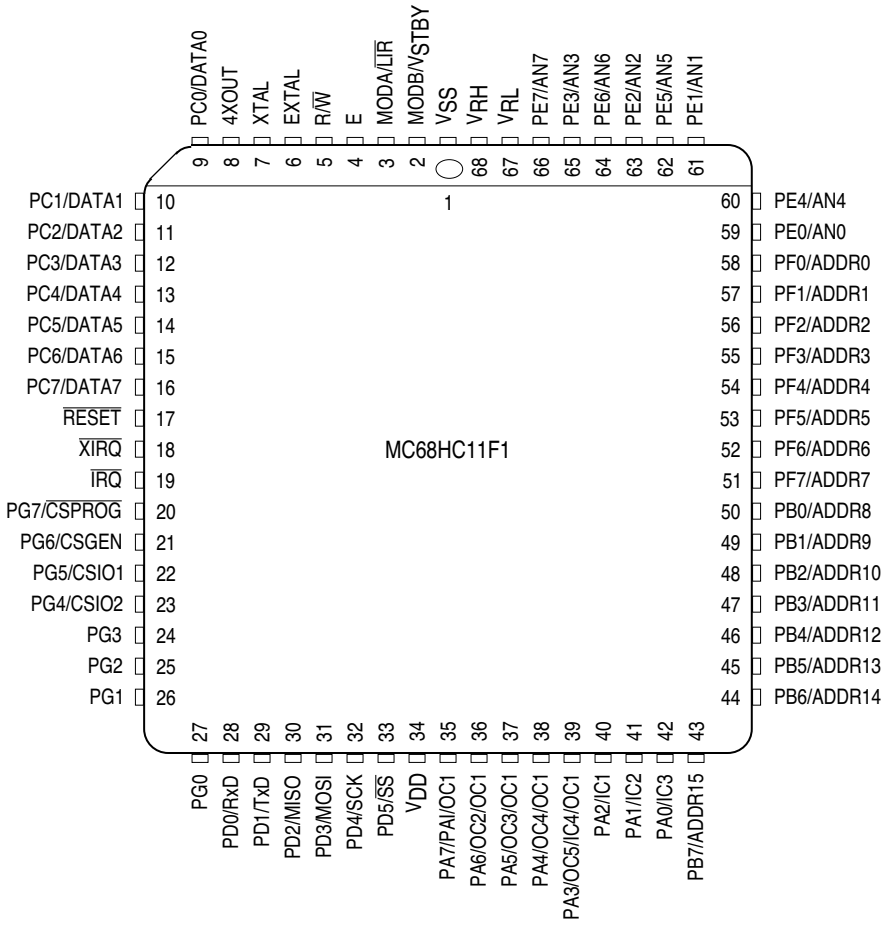

Figure 2-1 Pin Assignments for MC68HC11F1 68-Pin PLCC

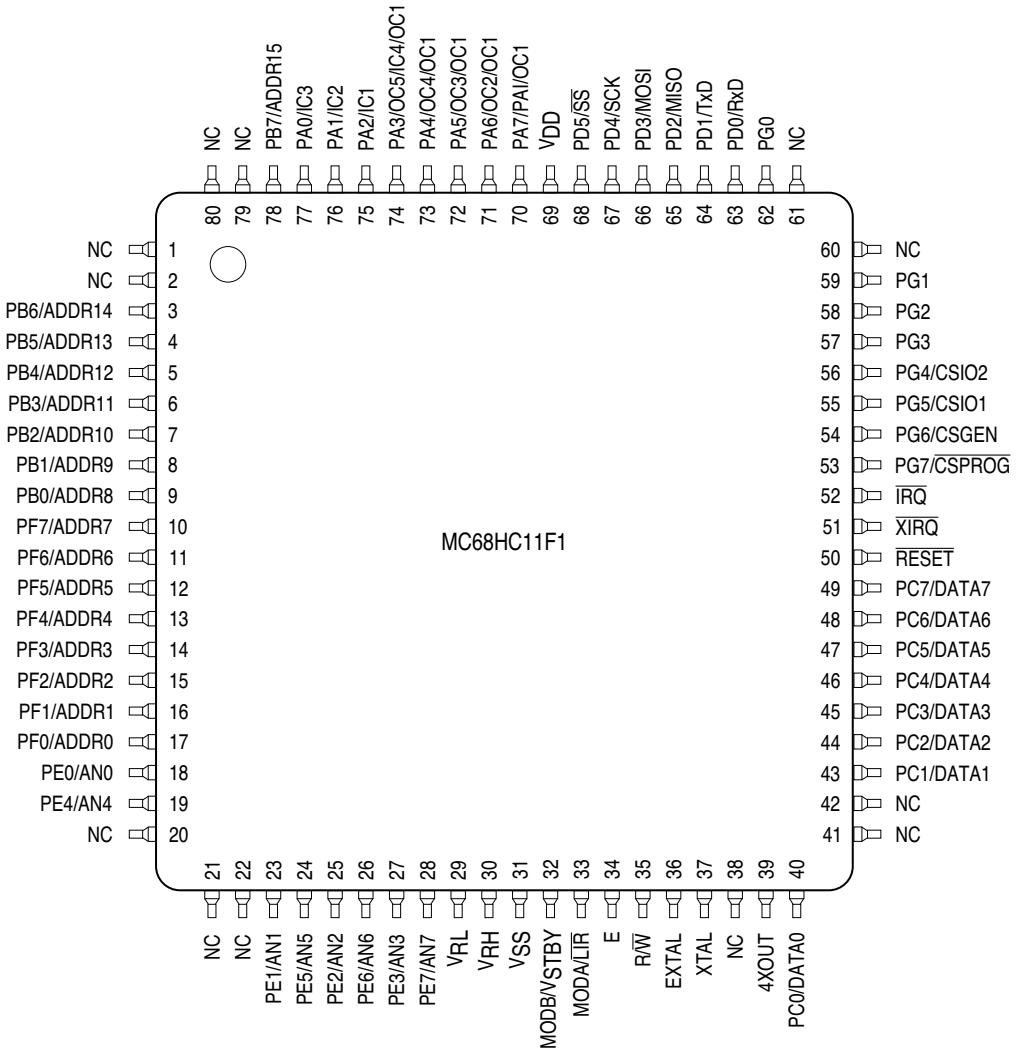

Figure 2-2 Pin Assignments for MC68HC11F1 80-Pin QFP

2.1 V_{DD} and V_{SS}

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the power supply, and V_{SS} is ground. The MCU operates from a single 5-volt (nominal) power supply. Very fast signal transitions occur on the MCU pins. The short rise and fall times place high, short duration current demands on the power supply. To prevent noise problems, provide good power-supply bypassing at the MCU. Also, use bypass capacitors that have good high-frequency characteristics and situate them as close to the MCU as possible. Bypass requirements vary, depending on how heavily the MCU pins are loaded.

2.2 Reset (RESET)

An active low bidirectional control signal, RESET, acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or COP watchdog circuit. The CPU distinguishes between internal and external reset conditions by sensing whether the reset pin rises to a logic one in less than two E-clock cycles after a reset has occurred. It is not advisable to connect an external resistor-capacitor (RC) power-up delay circuit to the reset pin of M68HC11 devices because the circuit charge time constant can cause the device to misinterpret the type of reset that occurred. Refer to **SECTION 5 RESETS AND INTERRUPTS** for further information.

Figure 2-3 illustrates a reset circuit that uses an external switch. Other circuits can be used, however, it is important to incorporate a low voltage interrupt (LVI) circuit to prevent operation at insufficient voltage levels which could result in erratic behavior or corruption of RAM.

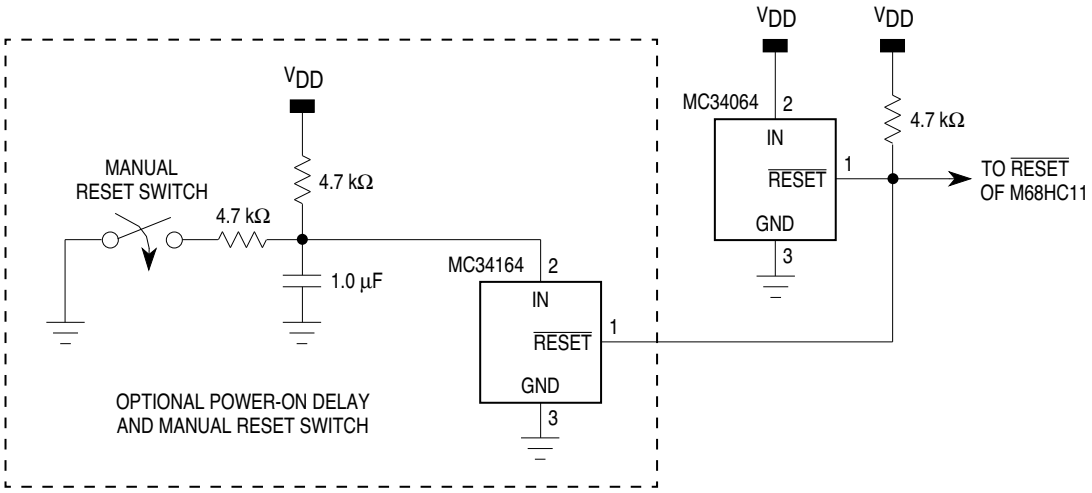

Figure 2-3 External Reset Circuit

2.3 E-Clock Output (E)

E is the output connection for the internally generated E clock. The signal from E is used as a timing reference. The frequency of the E-clock output is one fourth that of the input frequency at the EXTAL pin. When E-clock output is low, an internal process is taking place. When it is high, data is being accessed. All clocks, including the E clock, are halted when the MCU is in STOP mode. The E clock can be turned off in single-chip modes to reduce the effects of radio frequency interference (RFI). Refer to **SECTION 9 TIMING SYSTEM**.

2.4 Crystal Driver and External Clock Input (XTAL, EXTAL)

These two pins provide the interface for either a crystal or a CMOS-compatible clock to control the internal clock generator circuitry. Either a crystal oscillator or a CMOS compatible clock can be used. The resulting E-clock rate is the input frequency divided by four.

The XTAL pin is normally left unterminated when an external CMOS compatible clock is connected to the EXTAL pin. However, a 10 kΩ to 100 kΩ load resistor connected from the XTAL output to ground can be used to reduce RFI noise emission.

The XTAL output is normally used to drive a crystal. The XTAL output can be buffered with a high-impedance buffer, or it can be used to drive the EXTAL input of another M68HC11 device. Refer to **Figure 2-6**.

In all cases, use caution when designing circuitry associated with the oscillator pins. Load capacitances shown in the oscillator circuits include all stray layout capacitances. Refer to **Figure 2-4**, **Figure 2-5**, and **Figure 2-6**.

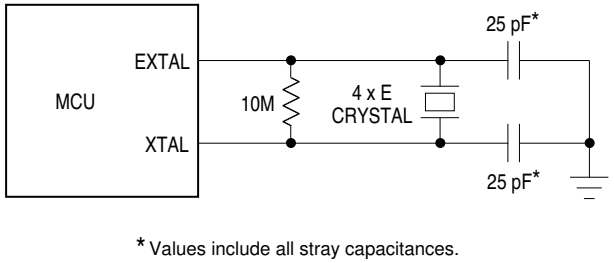

Figure 2-4 Common Crystal Connections

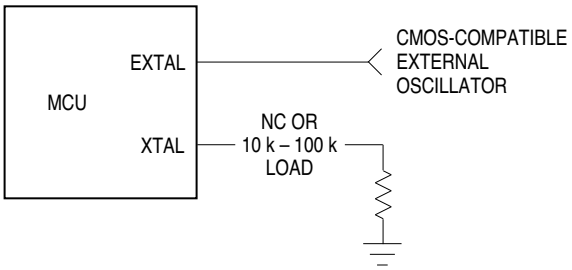

Figure 2-5 External Oscillator Connections

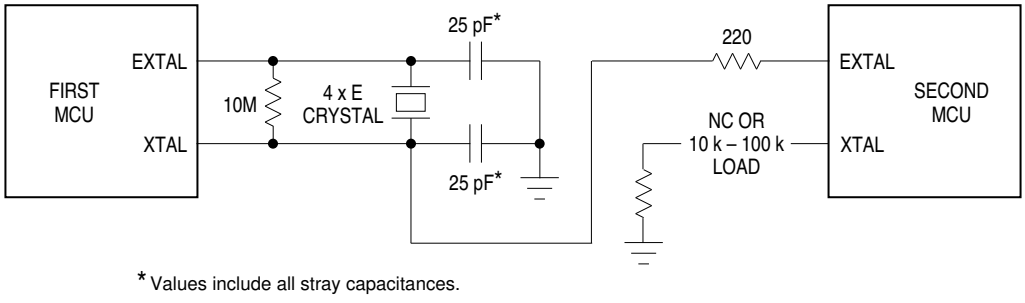

Figure 2-6 One Crystal Driving Two MCUs

2.5 Four Times E-Clock Frequency Output (4XOUT)

Although the circuit shown in **Figure 2-6** will work for any M68HC11 MCU, the MC68HC11F1 has an additional clock output that is four times the E-clock frequency. This output (4XOUT) can be used to directly drive the EXTAL input of another M68HC11 MCU. Refer to **Figure 2-7**. The 4XOUT output is enabled after reset and can be disabled by clearing the CLK4X bit in the OPT2 register.

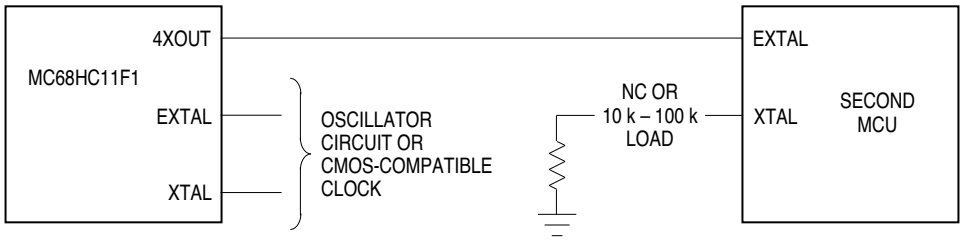

Figure 2-7 4XOUT Signal Driving a Second MCU

2.6 Interrupt Request ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ input provides a means of generating asynchronous interrupt requests for the CPU. Either falling-edge triggering or low-level triggering is selected by the IRQE bit in the OPTION register. $\overline{\text{IRQ}}$ is always configured for level-sensitive triggering at reset. Connect an external pull-up resistor, typically 4.7 kΩ, to V_{DD} when $\overline{\text{IRQ}}$ is used in a level-sensitive wired-OR configuration. Refer to **SECTION 5 RESETS AND INTERRUPTS**.

2.7 Non-Maskable Interrupt ($\overline{\text{XIRQ}}$)

The $\overline{\text{XIRQ}}$ input provides a means of requesting a non-maskable interrupt after reset initialization. During reset, the X bit in the condition code register (CCR) is set and any interrupt is masked until MCU software enables it. Because the $\overline{\text{XIRQ}}$ input is level sensitive, it can be connected to a multiple-source wired-OR network with an external pull-up resistor to V_{DD}. $\overline{\text{XIRQ}}$ is often used as a power loss detect interrupt.

Whenever $\overline{\text{XIRQ}}$ or $\overline{\text{IRQ}}$ are used with multiple interrupt sources ($\overline{\text{IRQ}}$ must be configured for level-sensitive operation if there is more than one source of $\overline{\text{IRQ}}$ interrupt), each source must drive the interrupt input with an open-drain type of driver to avoid contention between outputs. There should be a single pull-up resistor near the MCU interrupt input pin (typically 4.7 kΩ). There must also be an interlock mechanism at each interrupt source so that the source holds the interrupt line low until the MCU recognizes and acknowledges the interrupt request. If one or more interrupt sources are still pending after the MCU services a request, the interrupt line will still be held low and the MCU will be interrupted again as soon as the interrupt mask bit in the condition code register (CCR) is cleared (normally upon return from an interrupt). Refer to **SECTION 5 RESETS AND INTERRUPTS**.

2.8 MODA and MODB (MODA/$\overline{LIR}$ and MODB/V_{STBY})

During reset, MODA and MODB select one of the four operating modes. Refer to **SECTION 4 OPERATING MODES AND ON-CHIP MEMORY**.

After the operating mode has been selected, the $\overline{LIR}$ pin provides an open-drain output to indicate that execution of an instruction has begun. The LIR pin is configured for wired-OR operation (only pulls low). A series of E-clock cycles occurs during execution of each instruction. The $\overline{LIR}$ signal is asserted (drives low) during the first E-clock cycle of each instruction (opcode fetch). This output is provided for assistance in program debugging.

The V_{STBY} pin is used to input RAM standby power. The MCU is powered from the V_{DD} signal unless the difference between the level of V_{STBY} and V_{dd} is greater than one MOS threshold (about 0.7 volts). When these voltages differ by more than 0.7 volts, the internal 768-byte RAM and part of the reset logic are powered from V_{STBY} rather than V_{DD}. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

2.9 V_{RH} and V_{RL}

These pins provide the reference voltage for the analog-to-digital converter. Bypass capacitors should be used to minimize noise on these signals. Any noise on V_{RH} and V_{RL} will directly affect A/D accuracy.

2.10 R/$\overline{W}$

In expanded and test modes, R/$\overline{W}$ indicates the direction of transfers on the external data bus. A logic level one on this pin indicates that a read cycle is in progress. A logic zero on this pin indicates that a write cycle is in progress and that no external device should drive the data bus.

The E-clock can be used to enable external devices to drive data onto the data bus during the second half of a read bus cycle (E clock high). R/$\overline{W}$ can then be used to control the direction of data transfers. R/$\overline{W}$ drives low when data is being written to the external data bus. R/$\overline{W}$ will remain low during consecutive data bus write cycles, such as when a double-byte store occurs.

2.11 Port Signals

For the MC68HC11F1, 54 pins are arranged into six 8-bit ports: A, B, C, E, F, and G, and one 6-bit port (D). Each of these seven ports serves a purpose other than I/O, depending on the operating mode or peripheral functions selected. Note that ports B, C, and F are available for I/O functions only in single-chip and bootstrap modes. The pins of ports A, C, D, and G are fully bidirectional. Ports B and F are output-only ports. Port E is an input-only port. Refer to **Table 2-1** for details about the 54 port signals' functions within different operating modes.

Table 2-1 Port Signal Functions

Port/Bit	Single-Chip and Bootstrap Mode	Expanded and Special Test Mode
PA0	PA0/IC3	
PA1	PA1/IC2	
PA2	PA2/IC1	
PA3	PA3/OC5/IC4/OC1	
PA4	PA4/OC4/OC1	
PA5	PA5/OC3/OC1	
PA6	PA6/OC2/OC1	
PA7	PA7/PAI/OC1	
PB[7:0]	PB[7:0]	ADDR[15:8]
PC[7:0]	PC[7:0]	DATA[7:0]
PD0	PD0/RxD	
PD1	PD1/TxD	
PD2	PD2/MISO	
PD3	PD3/MOSI	
PD4	PD4/SCK	
PD5	PD5/$\overline{SS}$	
PE[7:0]	PE[7:0]/AN[7:0]	
PF[7:0]	PF[7:0]	ADDR[7:0]
PG0	PG0	
PG1	PG1	
PG2	PG2	
PG3	PG3	
PG4	PG4	PG4/CSIO2
PG5	PG5	PG5/CSIO1
PG6	PG6	PG6/CSGEN
PG7	PG7	PG7/$\overline{CSPROG}$

2.11.1 Port A

Port A is an 8-bit general-purpose I/O port with a data register (PORTA) and a data direction register (DDRA). Port A pins share functions with the 16-bit timer system. PORTA can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If written, PORTA stores the data in internal latches. It drives the pins only if they are configured as outputs. Writes to PORTA do not change the pin state when the pins are configured for timer output compares.

Out of reset, port A pins [7:0] are general-purpose high-impedance inputs. When the timer functions associated with these pins are disabled, the bits in DDRA govern the I/O state of the associated pin. For further information, refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

NOTE

When using the information about port functions, do not confuse pin function with the electrical state of the pin at reset. All general-purpose I/O pins configured as inputs at reset are in a high-impedance state. Port data registers reflect the logic state of the port at reset. The pin function is mode dependent.

2.11.2 Port B

Port B is an 8-bit output-only port. In single-chip modes, port B pins are general-purpose output pins (PB[7:0]). In expanded modes, port B pins act as the high-order address lines (ADDR[15:8]) of the address bus.

PORTB can be read at any time. Reads of PORTB return the pin driver input level. If PORTB is written, the data is stored in internal latches. It drives the pins only in single-chip or bootstrap mode. In expanded operating modes, port B pins are the high-order address outputs (ADDR[15:8]).

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.3 Port C

Port C is an 8-bit general-purpose I/O port with a data register (PORTC) and a data direction register (DDRC). In single-chip modes, port C pins are general-purpose I/O pins (PC[7:0]). In expanded modes, port C pins are configured as data bus pins (DATA[7:0]).

PORTC can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTC is written, the data is stored in internal latches. It drives the pins only if they are configured as outputs in single-chip or bootstrap mode. Port C pins are general-purpose inputs out of reset in single-chip and bootstrap modes. In expanded and test modes, these pins are data bus lines out of reset.

The CWOM control bit in the OPT2 register disables port C's P-channel output drivers. Because the N-channel driver is not affected by CWOM, setting CWOM causes port C to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTC bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port C bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port C can only be configured for wired-OR operation when the MCU is in single-chip or bootstrap modes.

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.4 Port D

Port D, a 6-bit general-purpose I/O port, has a data register (PORTD) and a data direction register (DDRD). The six port D lines (D[5:0]) can be used for general-purpose I/O, for the serial communications interface (SCI) and serial peripheral interface (SPI) subsystems.

PORTD can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTD is written, the data is stored in internal latches and can be driven only if port D is configured for general-purpose output.

The DWOM control bit in the SPCR register disables port D's P-channel output drivers. Because the N-channel driver is not affected by DWOM, setting DWOM causes port D to become an open-drain-type output port suitable for wired-OR operation. In wired-

OR mode, (PORTD bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port D bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port D can be configured for wired-OR operation in any operating mode.

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**, **SECTION 7 SERIAL COMMUNICATIONS INTERFACE**, and **SECTION 8 SERIAL PERIPHERAL INTERFACE**.

2.11.5 Port E

Port E is an 8-bit input-only port that is also used as the analog input port for the analog-to-digital converter. Port E pins that are not used for the A/D system can be used as general-purpose inputs. However, PORTE should not be read during the sample portion of an A/D conversion sequence.

Refer to **SECTION 10 ANALOG-TO-DIGITAL CONVERTER**.

2.11.6 Port F

Port F is an 8-bit output-only port. In single-chip mode, port F pins are general-purpose output pins (PF[7:0]). In expanded mode, port F pins act as the low-order address outputs (ADDR[7:0]).

PORTF can be read at any time. Reads of PORTF return the pin driver input level. If PORTF is written, the data is stored in internal latches. It drives the pins only in single-chip or bootstrap mode. In expanded operating modes, port F pins are the low-order address outputs (ADDR[7:0]).

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT**.

2.11.7 Port G

Port G is an 8-bit general-purpose I/O port. When enabled, four chip select signals are alternate functions of port G bits [7:4].

PORTG can be read at any time. Inputs return the pin level; outputs return the pin driver input level. If PORTG is written, the data is stored in internal latches. It drives the pins only if they are configured as outputs.

The GWOM control bit in the OPT2 register disables port G's P-channel output drivers. Because the N-channel driver is not affected by GWOM, setting GWOM causes port G to become an open-drain-type output port suitable for wired-OR operation. In wired-OR mode, (PORTG bits are at logic level zero), pins are actively driven low by the N-channel driver. When a port G bit is at logic level one, the associated pin is in a high-impedance state, as neither the N-channel nor the P-channel devices are active. It is customary to have an external pull-up resistor on lines that are driven by open-drain devices. Port G can be configured for wired-OR operation in any operating mode.

Refer to **SECTION 6 PARALLEL INPUT/OUTPUT** and **SECTION 4 OPERATING MODES AND ON-CHIP MEMORY**.

SECTION 3 CENTRAL PROCESSING UNIT

This section presents information on M68HC11 central processing unit (CPU) architecture. Data types, addressing modes, the instruction set, and the extended addressing range required to support this MCU's memory expansion feature are also included, as are special operations such as subroutine calls and interrupts.

The CPU is designed to treat all peripheral, I/O, and memory locations identically as addresses in the 64 Kbyte memory map. This is referred to as memory-mapped I/O. There are no special instructions for I/O that are separate from those used for memory. This architecture also allows accessing an operand from an external memory location with no execution-time penalty.

3.1 CPU Registers

M68HC11 CPU registers are an integral part of the CPU and are not addressed as if they were memory locations. The seven registers, discussed in the following paragraphs, are shown in **Figure 3-1**.