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# MC68HC705KJ1
# MC68HRC705KJ1
# MC68HLC705KJ1

Data Sheet

**M68HC05**
**Microcontrollers**

MC68HC705KJ1
Rev. 4.1
07/2005

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# MC68HC705JK1
# MC68HRC705KJ1
# MC68HLC705KJ1

**Data Sheet**

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

# Revision History

| Date | Revision Level | Description | Page Number(s) |
|---|---|---|---|
| April, 2002 | 3.0 | Figure 1-4. Crystal Connections with Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places | 17 |
| | | Figure 1-5. Crystal Connections without Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places | 17 |
| | | Figure 1-6. Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places | 18 |
| | | Figure 1-7. Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places | 18 |
| | | Figure 1-8. External Clock Connections — changed PA7 designator to OSC1 in two places | 19 |
| | | Figure B-1. Crystal Connections — added OSC2 designation | 105 |
| | | Table B-3. MC68HLC705KJ1 (Low Frequency) Order Numbers — Corrected table title | 106 |
| May, 2003 | 4.0 | Reformatted to new publications standards. | Throughout |
| | | Figure A-2. Typical Internal Operating Frequency for Various VDD at 25°C — RC Oscillator Option Only — replaced graph | 102 |
| July, 2005 | 4.1 | Updated to meet Freescale identity guidelines. | Throughout |

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# Chapter 1
# Introduction

## 1.1 Features

Features on the MC68HC705KJ1 include:

- Robust noise immunity
- 4.0-MHz internal operating frequency at 5.0 V
- 1240 Bytes of EPROM/OTPROM (electrically programmable read-only memory/one-time programmable read-only memory), including eight bytes for user vectors
- 64 bytes of user RAM
- Peripheral modules:
  - 15-stage multifunction timer
  - Computer operating properly (COP) watchdog
- 10 bidirectional input/output (I/O) lines, including:
  - 10-mA sink capability on all I/O pins
  - Software programmable pulldowns on all I/O pins
  - Keyboard scan with selectable interrupt on four I/O pins
  - 5.5-mA source capability on six I/O pins
- Selectable sensitivity on external interrupt (edge- and level-sensitive or edge-sensitive only)
- On-chip oscillator with connections for:
  - Crystal
  - Ceramic resonator
  - Resistor-capacitor (RC) oscillator (MC68HRC705KJ1) with or without external resistor
  - External clock
  - Low-speed (32-kHz) crystal (MC68HLC705KJ1)
- Memory-mapped I/O registers
- Fully static operation with no minimum clock speed
- Power-saving stop, halt, wait, and data-retention modes
- External interrupt mask bit and acknowledge bit
- Illegal address reset
- Internal steering diode and pullup resistor from $\overline{\text{RESET}}$ pin to $V_{DD}$
- Selectable EPROM security[1]
- Selectable oscillator bias resistor

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

## 1.2 Structure

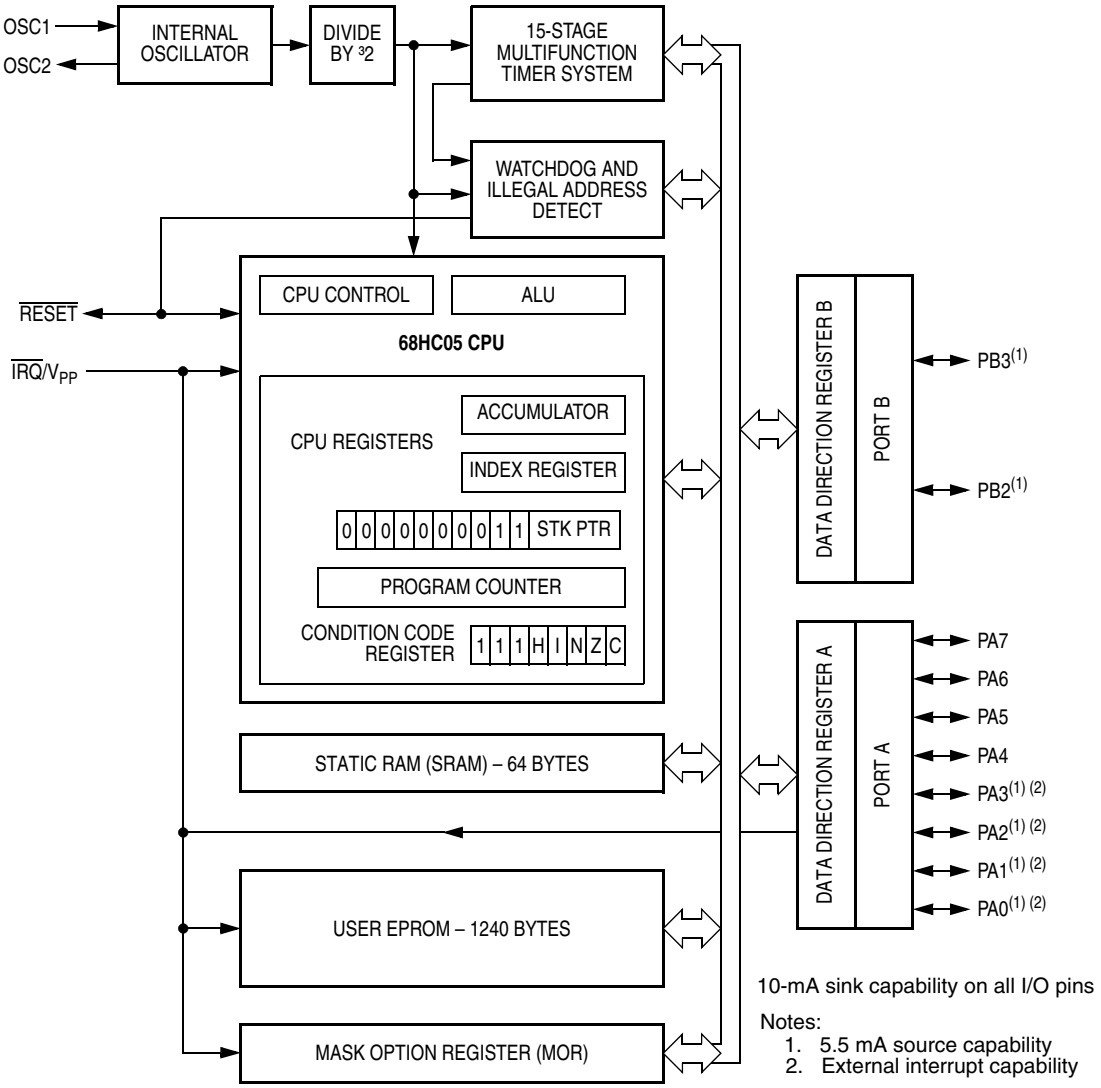



**Figure 1-1. Block Diagram**

## 1.3 Programmable Options

The options in Table 1-1 are programmable in the mask option register.

**Table 1-1. Programmable Options**

| Feature | Option |
|---|---|
| COP watchdog timer | Enabled or disabled |
| External interrupt triggering | Edge-sensitive only or edge- and level-sensitive |
| Port A $\overline{IRQ}$ pin interrupts | Enabled or disabled |
| Port pulldown resistors | Enabled or disabled |
| STOP instruction mode | Stop mode or halt mode |
| Crystal oscillator internal resistor | Enabled or disabled |
| EPROM security | Enabled or disabled |
| Short oscillator delay counter | Enabled or disabled |

## 1.4 Pin Functions

Pin assignments are shown in Figure 1-2 with the functions described in the following subsections.

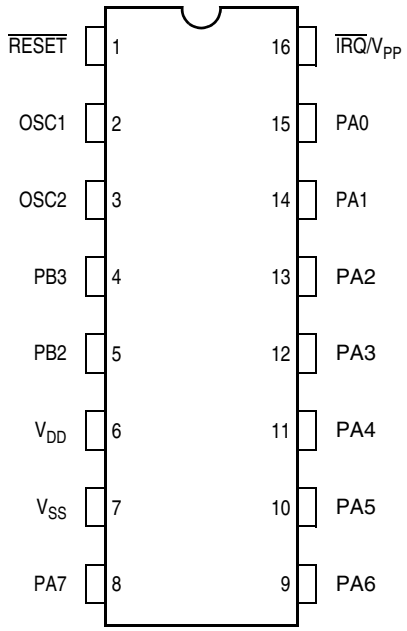



**Figure 1-2. Pin Assignments**

### 1.4.1 $V_{DD}$ and $V_{SS}$

$V_{DD}$ and $V_{SS}$ are the power supply and ground pins. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins, placing high, short-duration current demands on the power supply. To prevent noise problems, take special care, as Figure 1-3 shows, by placing the bypass capacitors as close as possible to the MCU. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.

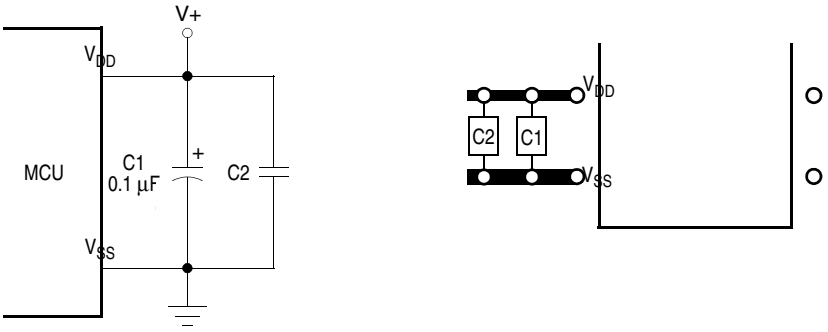



**Figure 1-3. Bypassing Layout Recommendation**

### 1.4.2 OSC1 and OSC2

The OSC1 and OSC2 pins are the connections for the on-chip oscillator. The oscillator can be driven by any of the following:

1. Standard crystal (See Figure 1-4 and Figure 1-5.)
2. Ceramic resonator (See Figure 1-6 and Figure 1-7.)
3. Resistor/capacitor (RC) oscillator (Refer to Appendix A MC68HRC705KJ1.)
4. External clock signal as shown in (See Figure 1-8.)
5. Low speed (32 kHz) crystal connections (Refer to Appendix B MC68HLC705KJ1.)

The frequency, $f_{OSC}$, of the oscillator or external clock source is divided by two to produce the internal operating frequency, $f_{OP}$.

#### *1.4.2.1 Crystal Oscillator*

Figure 1-4 and Figure 1-5 show a typical crystal oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal supplier's recommendations, as the crystal parameters determine the external component values required to provide reliable startup and maximum stability. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances.

To minimize output distortion, mount the crystal and capacitors as close as possible to the pins. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 for the crystal oscillator as a programmable mask option.

***NOTE***

*Use an AT-cut crystal and not an AT-strip crystal because the MCU can overdrive an AT-strip crystal.*

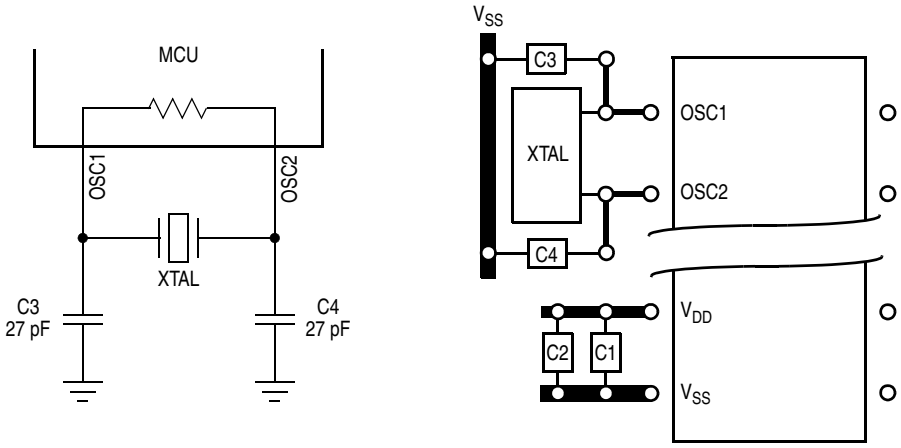



**Figure 1-4. Crystal Connections with Oscillator Internal Resistor Mask Option**

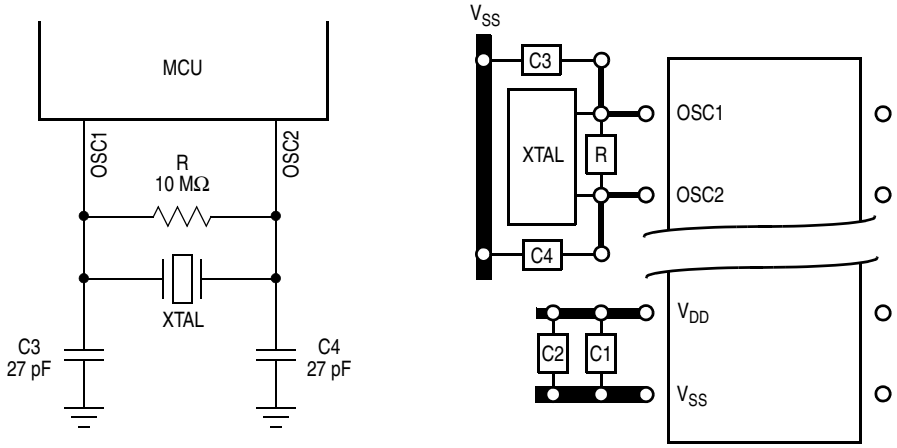



**Figure 1-5. Crystal Connections without Oscillator Internal Resistor Mask Option**

### *1.4.2.2 Ceramic Resonator Oscillator*

To reduce cost, use a ceramic resonator instead of the crystal. The circuits shown in Figure 1-6 and Figure 1-7 show ceramic resonator circuits. Follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

Mount the resonator and components as close as possible to the pins for startup stabilization and to minimize output distortion. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 as a programmable mask option.

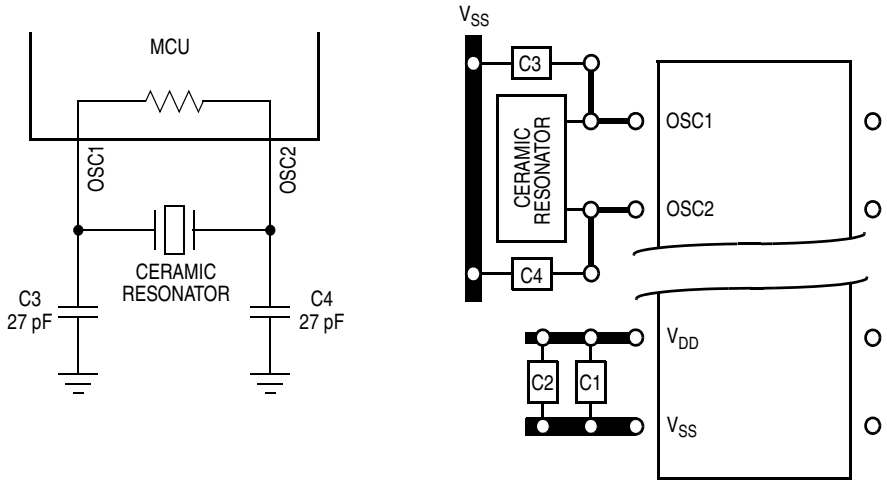



**Figure 1-6. Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option**

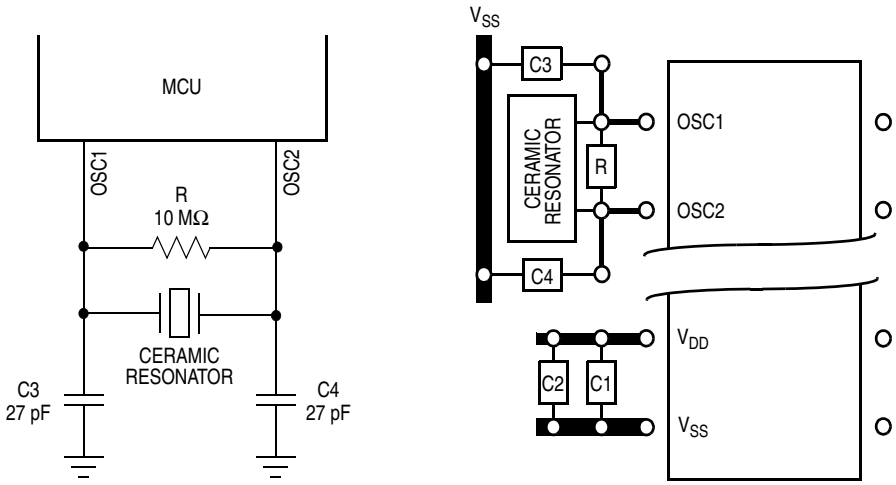



**Figure 1-7. Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option**

### *1.4.2.3 RC Oscillator*

Refer to Appendix A MC68HRC705KJ1.

#### *1.4.2.4 External Clock*

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in Figure 1-8. This configuration is possible regardless of whether the crystal/ceramic resonator or the RC oscillator is enabled.

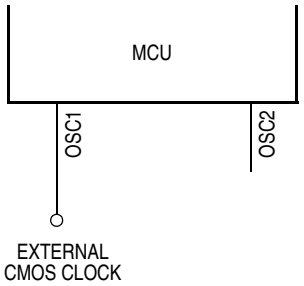



**Figure 1-8. External Clock Connections**

### 1.4.3 $\overline{\text{RESET}}$

Applying a logic 0 to the $\overline{\text{RESET}}$ pin forces the MCU to a known startup state. An internal reset also pulls the $\overline{\text{RESET}}$ pin low. An internal resistor to $V_{DD}$ pulls the $\overline{\text{RESET}}$ pin high. A steering diode between the $\overline{\text{RESET}}$ and $V_{DD}$ pins discharges any $\overline{\text{RESET}}$ pin voltage when power is removed from the MCU. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. Refer to Chapter 8 Resets and Interrupts for more information.

### 1.4.4 $\overline{\text{IRQ}}/V_{PP}$

The external interrupt/programming voltage pin ($\overline{\text{IRQ}}/V_{PP}$) drives the asynchronous IRQ interrupt function of the CPU. Additionally, it is used to program the user EPROM and mask option register. (See Chapter 2 Memory and Chapter 5 External Interrupt Module (IRQ).)

The LEVEL bit in the mask option register provides negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering for the interrupt function.

If level-sensitive triggering is selected, the $\overline{\text{IRQ}}/V_{PP}$ input requires an external resistor to $V_{DD}$ for wired-OR operation. If the $\overline{\text{IRQ}}/V_{PP}$ pin is not used, it must be tied to the $V_{DD}$ supply.

The $\overline{\text{IRQ}}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin should not exceed $V_{DD}$ except when the pin is being used for programming the EPROM.

***NOTE***

*The mask option register can enable the PA0–PA3 pins to function as external interrupt pins.*

### 1.4.5 PA0–PA7

These eight input/output (I/O) lines comprise port A, a general-purpose bidirectional I/O port. (See Chapter 5 External Interrupt Module (IRQ) for information on PA0–PA3 external interrupts.)

### 1.4.6 PB2 and PB3

These two I/O lines comprise port B, a general-purpose bidirectional I/O port.

# Chapter 2
# Memory

## 2.1 Introduction

This section provides:

- Memory map (Figure 2-1)
- Summary of the input/output registers (Figure 2-2)
- Description of:
  - Random-access memory (RAM)
  - EPROM/OTPROM (electrically programmable read-only memory/one-time programmable read-only memory)
  - Mask option register

Memory features include:

- 1232 Bytes of User EPROM, Plus Eight Bytes for User Vectors
- 64 Bytes of User RAM

## 2.2 Unimplemented Memory Locations

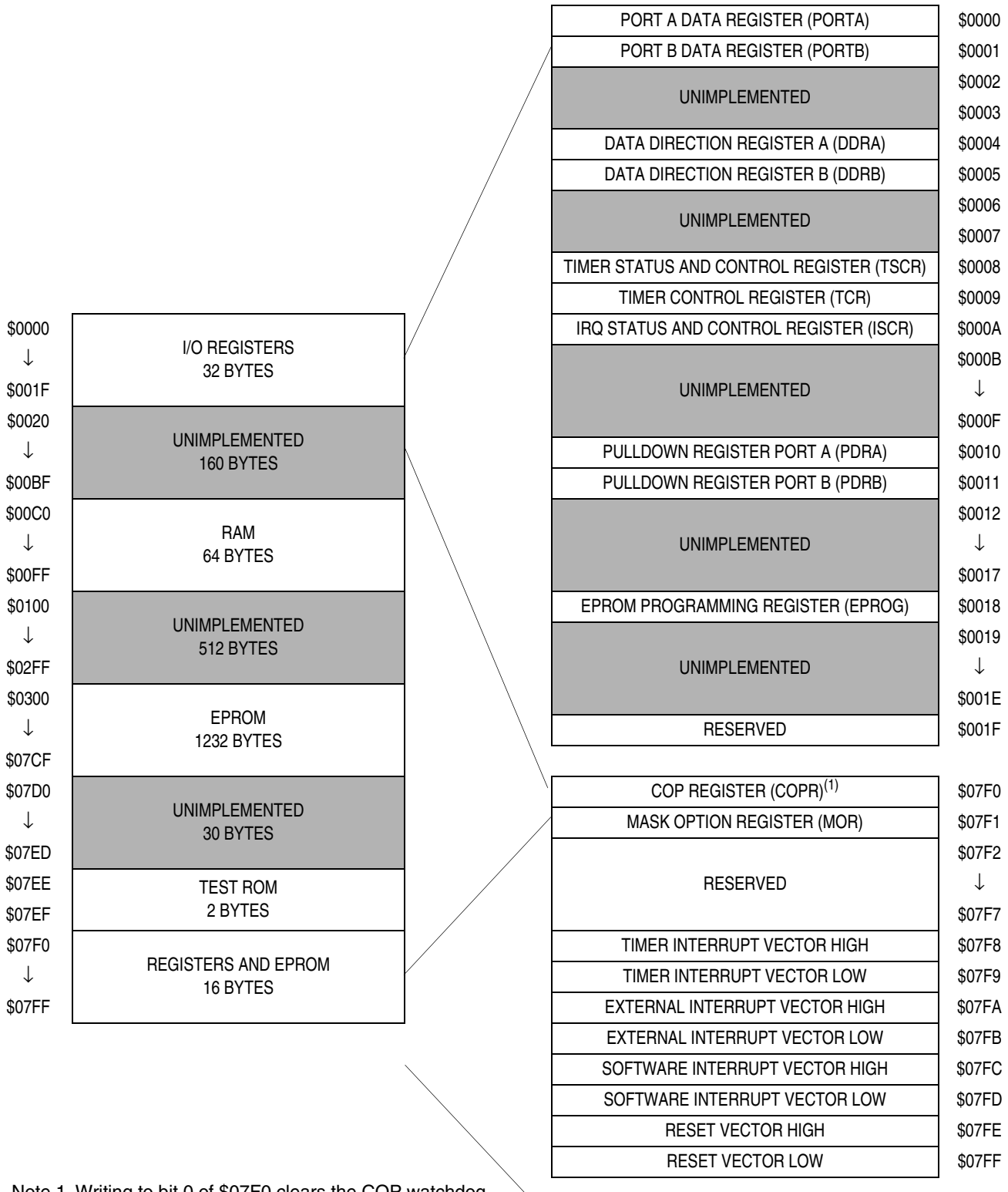
Accessing an unimplemented location can have unpredictable effects on MCU operation. In Figure 2-2 and in register figures in this document, unimplemented locations are shaded.

## 2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In Figure 2-2 and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.

## 2.4 Memory Map

See Figure 2-1.




Note 1. Writing to bit 0 of $07F0 clears the COP watchdog.

**Figure 2-1. Memory Map**

## 2.5 Input/Output Register Summary

| Addr. | Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $0000 | Port A Data Register (PORTA) See page 64. | Read: Write: | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| | | Reset: | Unaffected by reset | | | | | | | |
| $0001 | Port B Data Register (PORTB) See page 66. | Read: | 0 | 0 | Refer to Chapter 7 Parallel I/O Ports (PORTS) | | PB3 | PB2 | Refer to Chapter 7 Parallel I/O Ports (PORTS) | |
| | | Write: | | | | | | | | |
| | | Reset: | Unaffected by reset | | | | | | | |
| $0002 | Unimplemented | | | | | | | | | |
| $0003 | Unimplemented | | | | | | | | | |
| $0004 | Data Direction Register A (DDRA) See page 64. | Read: Write: | DDRA7 | DDRA6 | DDRA5 | DDRA4 | DDRA3 | DDRA2 | DDRA1 | DDRA0 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0005 | Data Direction Register B (DDRB) See page 67. | Read: | 0 | 0 | Refer to Chapter 7 Parallel I/O Ports (PORTS) | | DDRB3 | DDRB2 | Refer to Chapter 7 Parallel I/O Ports (PORTS) | |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0006 | Unimplemented | | | | | | | | | |
| $0007 | Unimplemented | | | | | | | | | |
| $0008 | Timer Status and Control Register (TSCR) See page 81. | Read: | TOF | RTIF | TOIE | RTIE | 0 | 0 | RT1 | RT0 |
| | | Write: | | | | | TOFR | RTIFR | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| $0009 | Timer Counter Register (TCR) See page 82. | Read: | TCR7 | TCR6 | TCR5 | TCR4 | TCR3 | TCR2 | TCR1 | TCR0 |
| | | Write: | | | | | | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $000A | IRQ Status and Control Register (ISCR) See page 54. | Read: | IRQE | 0 | 0 | 0 | IRQF | 0 | 0 | 0 |
| | | Write: | | | | R | | | IRQR | |
| | | Reset: | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented R = Reserved U = Unaffected

**Figure 2-2. I/O Register Summary (Sheet 1 of 2)**

| Addr. | Register Name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $000B | Unimplemented | | | | | | | | | |
| ↓ | | | | | | | | | | |
| $000F | Unimplemented | | | | | | | | | |
| $0010 | Pulldown Register Port A (PDRA) See page 65. | Read: | | | | | | | | |
| | | Write: | PDIA7 | PDIA6 | PDIA5 | PDIA4 | PDIA3 | PDIA2 | PDIA1 | PDIA0 |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0011 | Pulldown Register Port B (PDRB) See page 68. | Read: | | | | | | | | |
| | | Write: | | | Refer to Chapter 7 Parallel I/O Ports (PORTS) | | PDIB3 | PDIB2 | Refer to Chapter 7 Parallel I/O Ports (PORTS) | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0012 | Unimplemented | | | | | | | | | |
| ↓ | | | | | | | | | | |
| $0017 | Unimplemented | | | | | | | | | |
| $0018 | EPROM Programming Register (EPROG) See page 26. | Read: | 0 | 0 | 0 | 0 | 0 | ELAT | MPGM | EPGM |
| | | Write: | | R | R | R | R | | | |
| | | Reset: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0019 | Unimplemented | | | | | | | | | |
| ↓ | | | | | | | | | | |
| $001E | Unimplemented | | | | | | | | | |
| $001F | Reserved | | R | R | R | R | R | R | R | R |
| $07F0 | COP Register (COPR) See page 30. | Read: | | | | | | | | |
| | | Write: | | | | | | | | COPC |
| | | Reset: | U | U | U | U | U | U | U | 0 |
| $07F1 | Mask Option Register (MOR) See page 27. | Read: | SOSCD | EPMSEC | OSCRES | SWAIT | PDI | PIRQ | LEVEL | COPEN |
| | | Write: | | | | | | | | |
| | | Reset: | Unaffected by reset | | | | | | | |

= Unimplemented R = Reserved U = Unaffected

**Figure 2-2. I/O Register Summary (Sheet 2 of 2)**

## 2.6 RAM

The 64 addresses from $00C0 to $00FF serve as both the user RAM and the stack RAM. Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements when the CPU stores a byte on the stack and increments when the CPU retrieves a byte from the stack.

***NOTE***

*Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.*

## 2.7 EPROM/OTPROM

An MCU with a quartz window has 1240 bytes of erasable, programmable ROM (EPROM). The quartz window allows EPROM erasure with ultraviolet light.

***NOTE***

*Keep the quartz window covered with an opaque material except when erasing the MCU. Ambient light can affect MCU operation.*

In an MCU without the quartz window, the EPROM cannot be erased and serves as 1240 bytes of one-time programmable ROM (OTPROM).

The following addresses are user EPROM/OTPROM locations:

- $0300–$07CF
- $07F8–$07FF, used for user-defined interrupt and reset vectors

The COP register (COPR) is an EPROM/OTPROM location at address $07F0.

The mask option register (MOR) is an EPROM/OTPROM location at address $07F1.

### 2.7.1 EPROM/OTPROM Programming

The two ways to program the EPROM/OTPROM are:

- Manipulating the control bits in the EPROM programming register to program the EPROM/OTPROM on a byte-by-byte basis
- Programming the EPROM/OTPROM with the M68HC705J In-Circuit Simulator (M68HC705JICS) available from Freescale