Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MC68HC908JL8
MC68HC908JK8
MC68HC908KL8
MC68HC08JL8
MC68HC08JK8

Data Sheet

M68HC08
Microcontrollers

MC68HC908JL8
Rev. 3.1
3/2005

freescale.com

freescale™
semiconductor

MC68HC908JL8
MC68HC908JK8
MC68HC908KL8
MC68HC08JL8
MC68HC08JK8

Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://www.freescale.com

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
Mar 2005	3.1	Added IRQ timing to Table 17-5 . Control Timing (5V) and Table 17-8 . Control Timing (3V)	188, 190
Nov 2004	3	Chapter 9 Serial Communications Interface (SCI) — Corrected SCI module clock source from OSCCLK to Bus Clock throughout.	121–206
		Figure 13-2 . Keyboard Interrupt Block Diagram — Removed incorrect Schmitt trigger in block diagram.	168
		14.7.2 Stop Mode — STOP_ICLKDIS bit does not affect stop mode conditions for COP. Replaced section with new text.	176
		Added Appendix A MC68HC08JL8 — ROM parts.	201
		Added Appendix B MC68HC908KL8.	207
Nov 2002	2	First general release.	—

List of Chapters

Table of Contents

Chapter 5
System Integration Module (SIM)

Chapter 6
Oscillator (OSC)

Chapter 7
Monitor ROM (MON)

Chapter 8
Timer Interface Module (TIM)

Chapter 9
Serial Communications Interface (SCI)

Chapter 10
Analog-to-Digital Converter (ADC)

Chapter 11
Input/Output (I/O) Ports

Chapter 12
External Interrupt (IRQ)

Chapter 13
Keyboard Interrupt Module (KBI)

Chapter 14
Computer Operating Properly (COP)

Chapter 15
Low Voltage Inhibit (LVI)

Chapter 16
Break Module (BREAK)

Chapter 17
Electrical Specifications

Chapter 18
Mechanical Specifications

Chapter 19
Ordering Information

Appendix A
MC68HC08JL8

Appendix B
MC68HC908KL8

Chapter 1
General Description

1.1 Introduction

The MC68HC908JL8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Devices

Generic Part	Description	Pin Count
MC68HC908JL8	FLASH part	28 or 32
MC68HC908JK8	FLASH part	20
MC68HC08JL8	ROM part for MC68HC908JL8	28 or 32
MC68HC08JK8	ROM part for MC68HC908JK8	20
MC68HC908KL8	ADC-less MC68HC908JL8	28 or 32

1.2 Features

Features of the MC68HC908JL8 include the following:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- Low-power design; fully static with stop and wait modes
- Maximum internal bus frequency:
  - 8-MHz at 5V operating voltage
  - 4-MHz at 3V operating voltage
- Oscillator options:
  - Crystal or resonator
  - RC oscillator
- 8,192 bytes user program FLASH memory with security[1] feature
- 256 bytes of on-chip RAM
- Two 16-bit, 2-channel timer interface modules (TIM1 and TIM2) with selectable input capture, output compare, and PWM capability on each channel; external clock input option on TIM2
- 13-channel, 8-bit analog-to-digital converter (ADC)
- Serial communications interface module (SCI)
- 26 general-purpose input/output (I/O) ports:
  - 8 keyboard interrupt with internal pull-up

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

  - 11 LED drivers (sink)
  - 2 × 25mA open-drain I/O with pull-up
- Resident routines for in-circuit programming and EEPROM emulation
- System protection features:
  - Optional computer operating properly (COP) reset, driven by internal RC oscillator
  - Optional low-voltage detection with reset and selectable trip points for 3V and 5V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Master reset pin with internal pull-up and power-on reset
- $\overline{\text{IRQ}}$ with schmitt-trigger input and programmable pull-up
- 20-pin dual in-line package (PDIP), 20-pin small outline integrated package (SOIC), 28-pin PDIP, 28-pin SOIC, 32-pin shrink dual in-line package (SDIP), and 32-pin low-profile quad flat pack (LQFP)
- Specific features of the MC68HC908JL8 in 28-pin packages are:
  - 23 general-purpose I/Os only
  - 7 keyboard interrupt with internal pull-up
  - 10 LED drivers (sink)
  - 12-channel ADC
  - Timer I/O pins on TIM1 only
- Specific features of the MC68HC908JL8 in 20-pin packages are:
  - 15 general-purpose I/Os only
  - 1 keyboard interrupt with internal pull-up
  - 4 LED drivers (sink)
  - 10-channel ADC
  - Timer I/O pins on TIM1 only

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908JL8.

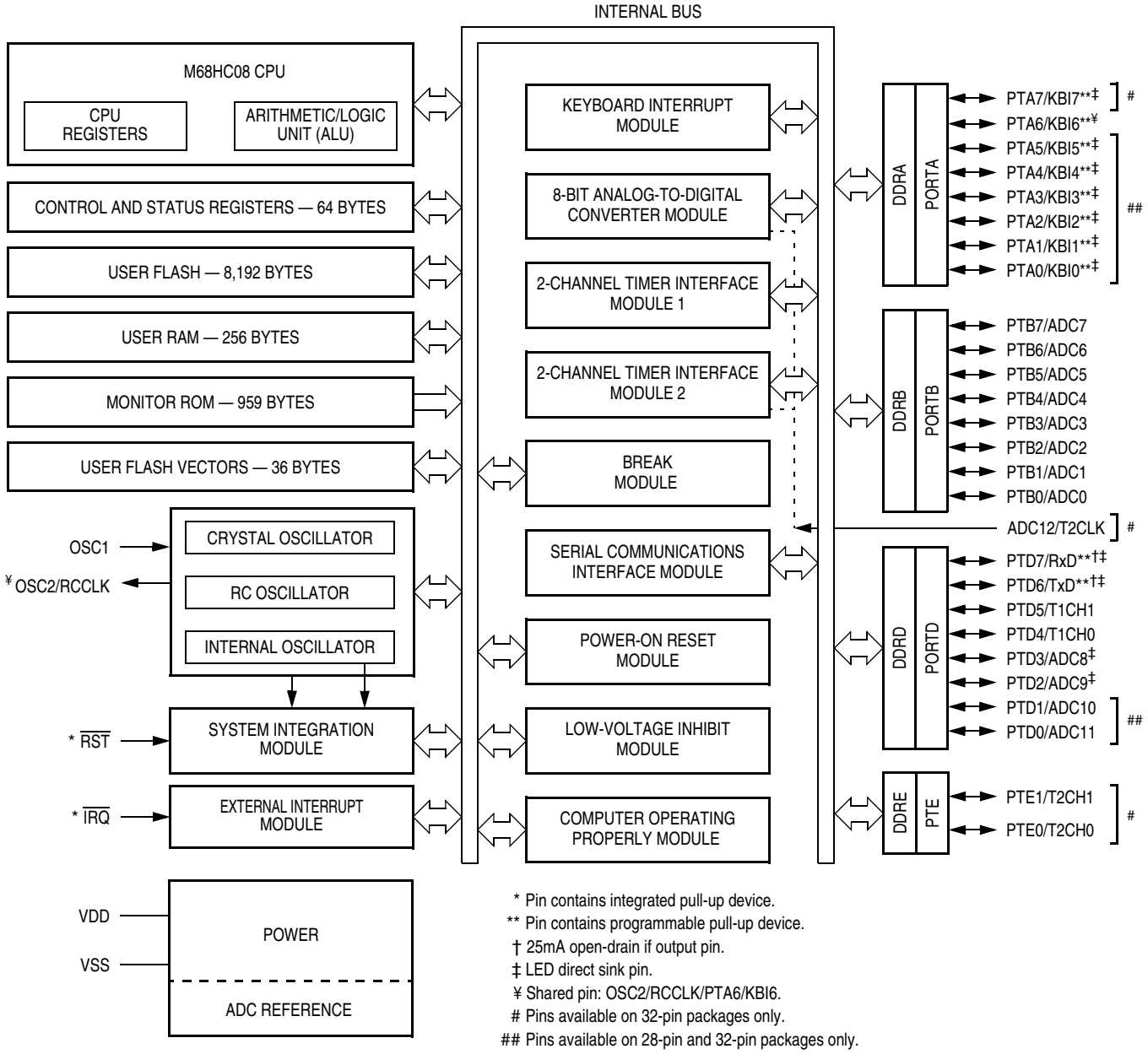


Figure 1-1. MC68HC908JL8 Block Diagram

1.4 Pin Assignments

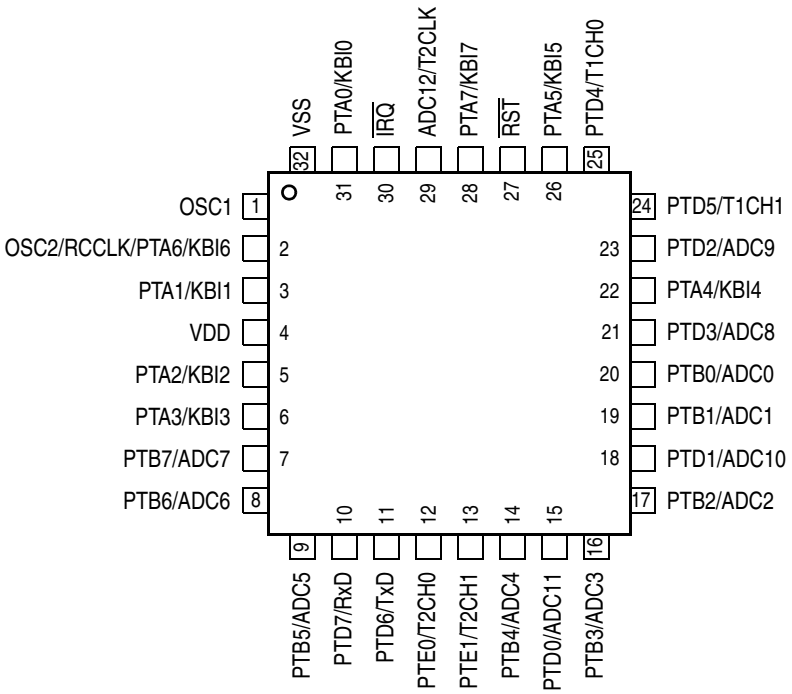


Figure 1-2. 32-Pin LQFP Pin Assignment

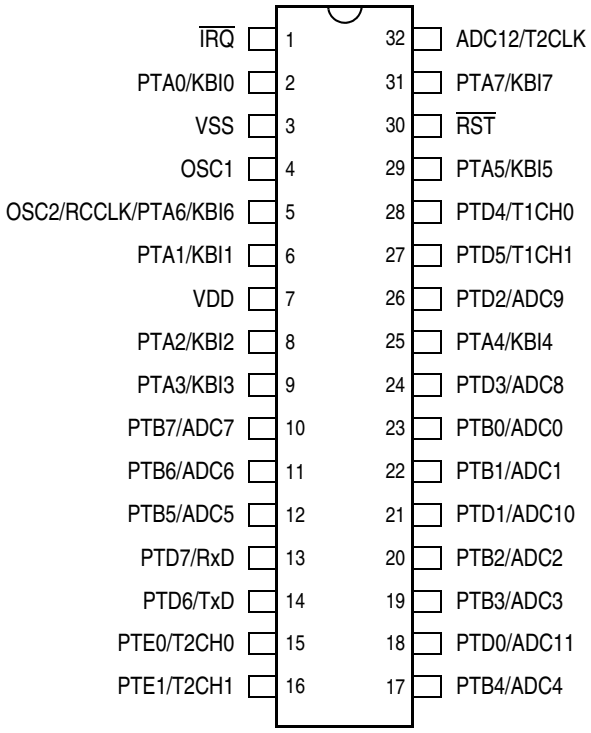
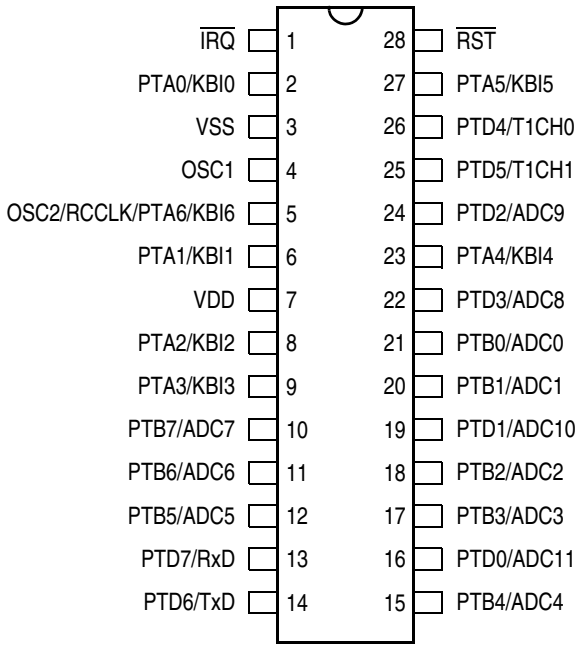


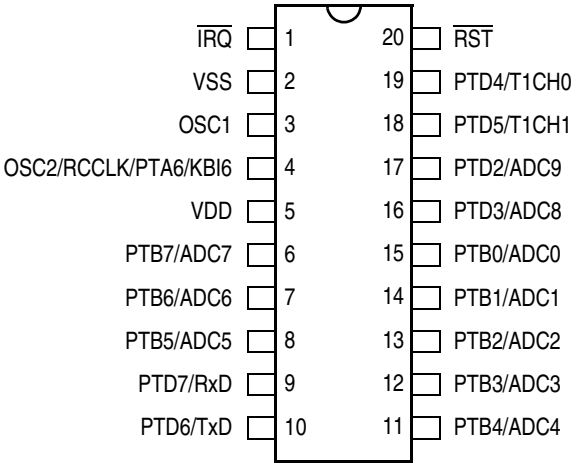
Figure 1-3. 32-Pin SDIP Pin Assignment



Pins not available on 28-pin packages	
	PTE0/T2CH0
	PTE1/T2CH1
	ADC12/T2CLK
PTA7/KBI7	

Internal pads are unconnected.
Set these unused port I/Os to output low.

Figure 1-4. 28-Pin PDIP/SOIC Pin Assignment



The 20-pin MC68HC908JL8 is designated MC68HC908JK8.

Pins not available on 20-pin packages	
PTA0/KBI0	PTD0/ADC11
PTA1/KBI1	PTD1/ADC10
PTA2/KBI2	
PTA3/KBI3	PTE0/T2CH0
PTA4/KBI4	PTE1/T2CH1
PTA5/KBI5	
	ADC12/T2CLK
PTA7/KBI7	

Internal pads are unconnected.
Set these unused port I/Os to output low.

Figure 1-5. 20-Pin PDIP/SOIC Pin Assignment

1.5 Pin Functions

Description of the pin functions are provided in Table 1-2.

Table 1-2. Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
VDD	Power supply.	In	5V or 3V
VSS	Power supply ground.	Out	0V
$\overline{RST}$	Reset input, active low; with internal pull-up and schmitt trigger input.	In/Out	VDD
$\overline{IRQ}$	External IRQ pin; with programmable internal pull-up and schmitt trigger input.	In	VDD
	Used for monitor mode entry.	In	VDD to V_{TST}
OSC1	Crystal or RC oscillator input.	In	VDD
OSC2/RCCLK	OSC2: crystal oscillator output; inverted OSC1 signal.	Out	VDD
	RCCLK: RC oscillator clock output.	Out	VDD
	Pin as PTA6/KBI6 (see PTA0–PTA7).	In/Out	VDD
ADC12/T2CLK	ADC12: channel-12 input of ADC.	In	VSS to VDD
	T2CLK: external input clock for TIM2.	In	VDD
PTA0–PTA7	8-bit general purpose I/O port.	In/Out	VDD
	Each pin has programmable internal pull-up when configured as input.	In	VDD
	Pins as keyboard interrupts, KBI0–KBI7.	In	VDD
	PTA0–PTA5 and PTA7 have LED direct sink capability.	Out	VSS
	PTA6 as OSC2/RCCLK.	Out	VDD
PTB0–PTB7	8-bit general purpose I/O port.	In/Out	VDD
	Pins as ADC input channels, ADC0–ADC7.	In	VSS to VDD
PTD0–PTD7	8-bit general purpose I/O port; with programmable internal pull-ups on PTD6–PTD7.	In/Out	VDD
	PTD0–PTD3 as ADC input channels, ADC11–ADC8.	Input	VSS to VDD
	PTD2–PTD3 and PTD6–PTD7 have LED direct sink capability	Out	VSS
	PTD4 as T1CH0 of TIM1.	In/Out	VDD
	PTD5 as T1CH1 of TIM1.	In/Out	VDD
	PTD6–PTD7 have configurable 25mA open-drain output.	Out	VSS
	PTD6 as TxD of SCI.	Out	VDD
	PTD7 as RxD of SCI.	In	VDD

Table 1-2. Pin Functions (Continued)

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
PTE0–PTE1	2-bit general purpose I/O port.	In/Out	VDD
	PTE0 as T2CH0 of TIM2.	In/Out	VDD
	PTE1 as T2CH1 of TIM2.	In/Out	VDD

NOTE

Devices in 28-pin packages, the following pins are not available: PTA7/KBI7, PTE0/T2CH0, PTE1/T2CH1, and ADC12/T2CLK.

Devices in 20-pin packages, the following pins are not available: PTA0/KBI0–PTA5/KBI5, PTD0/ADC11, PTD1/ADC10, PTA7/KBI7, PTE0/T2CH0, PTE1/T2CH1, and ADC12/T2CLK.

Chapter 2
Memory

2.1 Introduction

The CPU08 can address 64-kbytes of memory space. The memory map, shown in Figure 2-1, includes:

- 8,192 bytes of user FLASH memory
- 36 bytes of user-defined vectors
- 959 bytes of monitor ROM

2.2 I/O Section

Addresses $0000–$003F, shown in Figure 2-2, contain most of the control, status, and data registers. Additional I/O registers have the following addresses:

- $FE00; Break Status Register, BSR
- $FE01; Reset Status Register, RSR
- $FE02; Reserved
- $FE03; Break Flag Control Register, BFCR
- $FE04; Interrupt Status Register 1, INT1
- $FE05; Interrupt Status Register 2, INT2
- $FE06; Interrupt Status Register 3, INT3
- $FE07; Reserved
- $FE08; FLASH Control Register, FLCR
- $FE09; Reserved
- $FE0A; Reserved
- $FE0B; Reserved
- $FE0C; Break Address Register High, BRKH
- $FE0D; Break Address Register Low, BRKL
- $FE0E; Break Status and Control Register, BRKSCR
- $FE0F; Reserved
- $FFCF; FLASH Block Protect Register, FLBPR (FLASH register)
- $FFD0; Mask Option Register, MOR (FLASH register)
- $FFFF; COP Control Register, COPCTL

2.3 Monitor ROM

The 959 bytes at addresses $FC00–$FDFF and $FE10–$FFCE are reserved ROM addresses that contain the instructions for the monitor functions. (See Chapter 7 Monitor ROM (MON).)