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Freescale Semiconductor
Addendum

Document Number: QFN_Addendum
Rev. 0, 07/2014

Addendum for New QFN Package Migration

This addendum provides the changes to the 98A case outline numbers for products covered in this book. Case outlines were changed because of the migration from gold wire to copper wire in some packages. See the table below for the old (gold wire) package versus the new (copper wire) package.

To view the new drawing, go to Freescale.com and search on the new 98A package number for your device.

For more information about QFN package use, see EB806: *Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages*.

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

MC68HC908JW32

Data Sheet

M68HC08
Microcontrollers

MC68HC908JW32
Rev. 6
3/2009

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MC68HC908JW32

Data Sheet

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http://www.freescale.com

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description
January, 2005	2	First general release.
March, 2005	3	Second general release. Cleaned typos.
October, 2006	4	Table 4-1. Instruction Set Summary — Updated definition for the STOP instruction and added WAIT instruction.
		5.4 I/O Signals — Removed subsections referring to V_{DDA} and V_{SSA}.
		Figure 5-1. CGM Block Diagram — Corrected references to V_{DDA} and V_{SSA} to V_{DD} and V_{SS}.
		Figure 5-3. CGM External Connections — Removed V_{DD} connection to V_{DDPLL}.
		Figure 5-10. PLL Filter — Corrected reference to V_{SSA} to V_{SS}.
		Figure 7-1. Monitor Mode Circuit — Corrected V_{DDPLL} connection.
		Chapter 20 Ordering Information and Mechanical Specifications — Combined ordering information and mechanical specifications. Updated package dimensions to the latest available at time of publication.
October, 2006	5	1.7.2 Analog Power Supply (V_{DDPLL} and V_{SSPLL}) — Reworked for clarity.
March, 2009	6	Figure 1-3. 48-Pin LQFP and QFN Pin Assignment — Corrected pin numbers 37 through 48 Added 48-pin LQFP package information Added 52-pin LQFP package information Added five port B pins for the 52-pin package, and added supporting information In Table 5-1. Numeric Examples, corrected numeric example values In Chapter 6 System Integration Module (SIM), updated functional details In Chapter 7 Monitor Mode (MON), updated and corrected functional details In Chapter 18 Break Module (BRK), corrected break module information In 19.8 Crystal Oscillator Characteristics, corrected crystal characteristics

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Chapter 1
General Description

1.1 Introduction

The MC68HC908JW32 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

1.2 Features

Features of the MC68HC908JW32 include:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- 8-MHz internal bus frequency
- 88-kHz internal RC clock for timebase wakeup
- 32-Kbytes of on-chip FLASH memory with security[1]
- 1-Kbytes of on-chip random-access memory (RAM)
- On-chip programming firmware for use with host PC computer
- Clock generation module (CGM)
- Up to 34 general-purpose 5V input/output (I/O) pins, including:
  - Keyboard interrupts on 8 pins
  - Direct drive for normal LED on 8 pins
  - High current drive for PS/2 connection on 2 pins (with USB module disabled)
- Serial peripheral interface module (SPI)
- PS2 clock generator module
- 16-bit, 2-channel timer interface module (TIM) with selectable rising and falling edges input capture, output compare, PWM capability on each channel, and external clock input option
- Full universal serial bus (USB) specification 2.0 full-speed functions:
  - 12 Mbps data rate
  - On-chip 3.3V regulator
  - Endpoint 0 with 8-byte transmit buffer and 8-byte receive buffer
  - 64 bytes endpoint buffer to share among endpoints 1–4
- System protection features:
  - Optional computer operating properly (COP) reset
  - Optional low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Low-power design (fully static with stop and wait modes)
- Master reset pin with internal pull-up and power-on reset

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH/ROM difficult for unauthorized users.

- External asynchronous interrupt pin with internal pull-up ($\overline{IRQ}$)
- 48-pin quad flat non-leaded package (QFN)

1.3 MCU Block Diagram

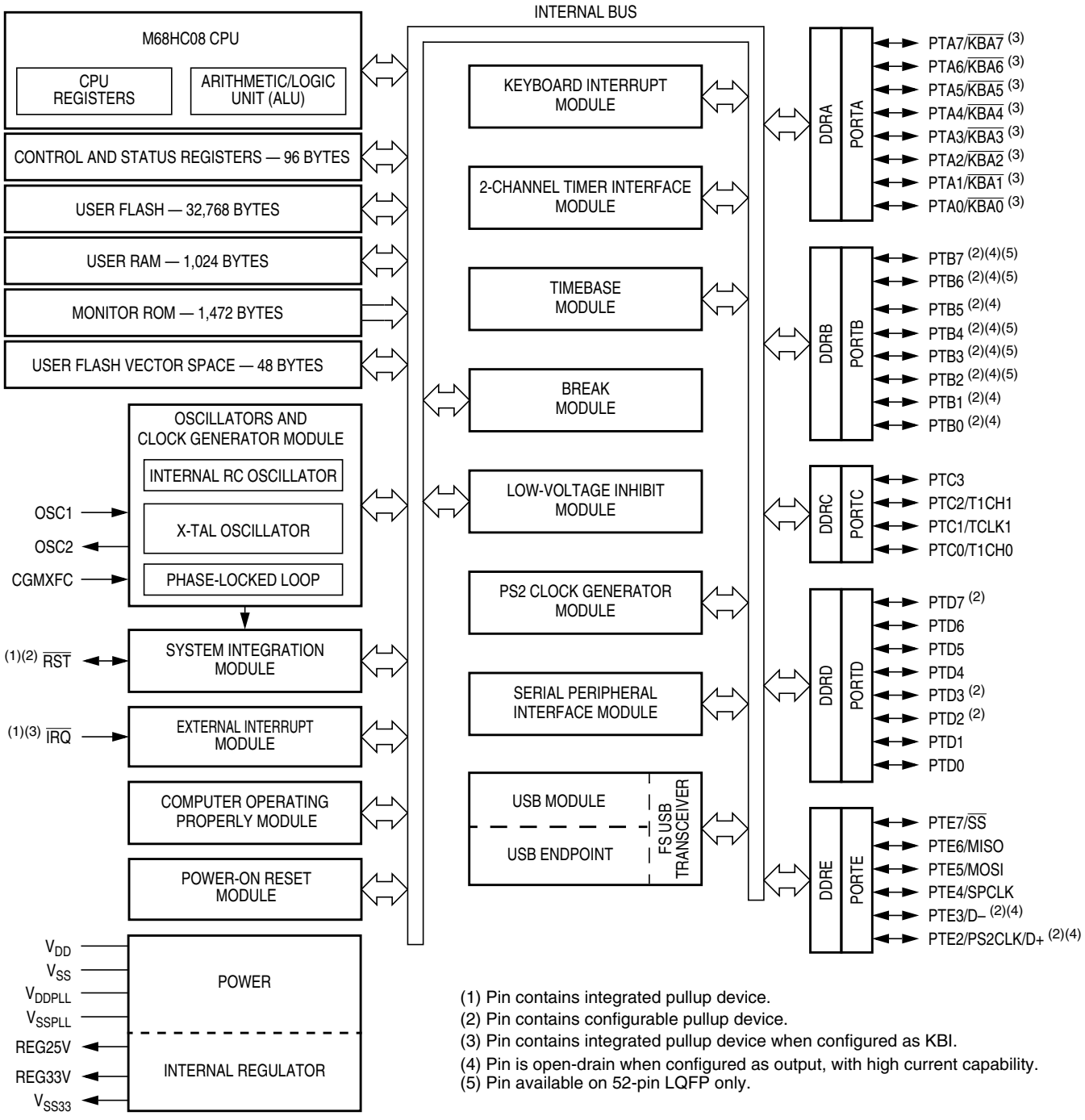


Figure 1-1. MC68HC908JW32 Block Diagram

1.4 Pin Assignments

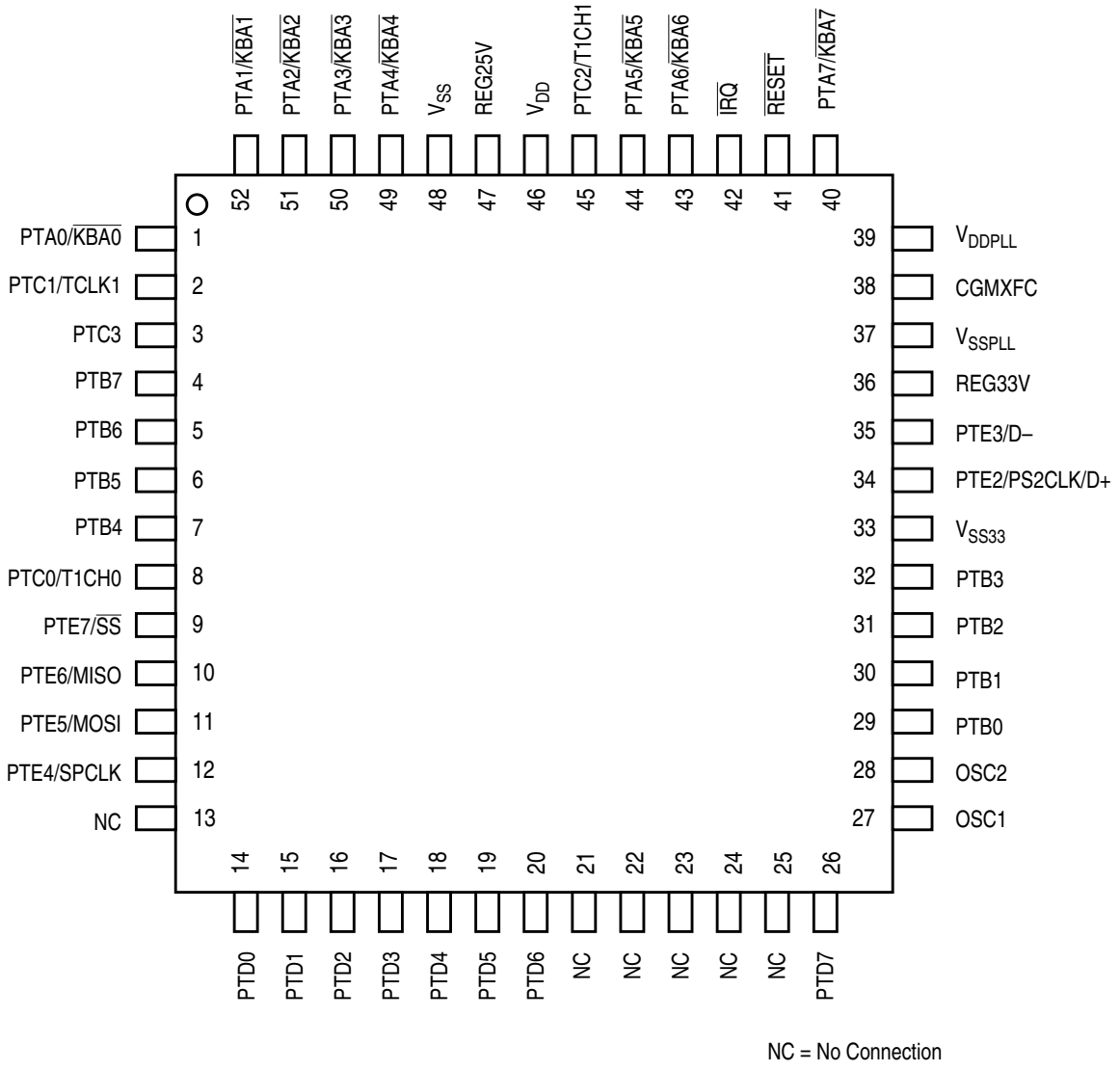


Figure 1-2. 52-Pin LQFP Pin Assignment

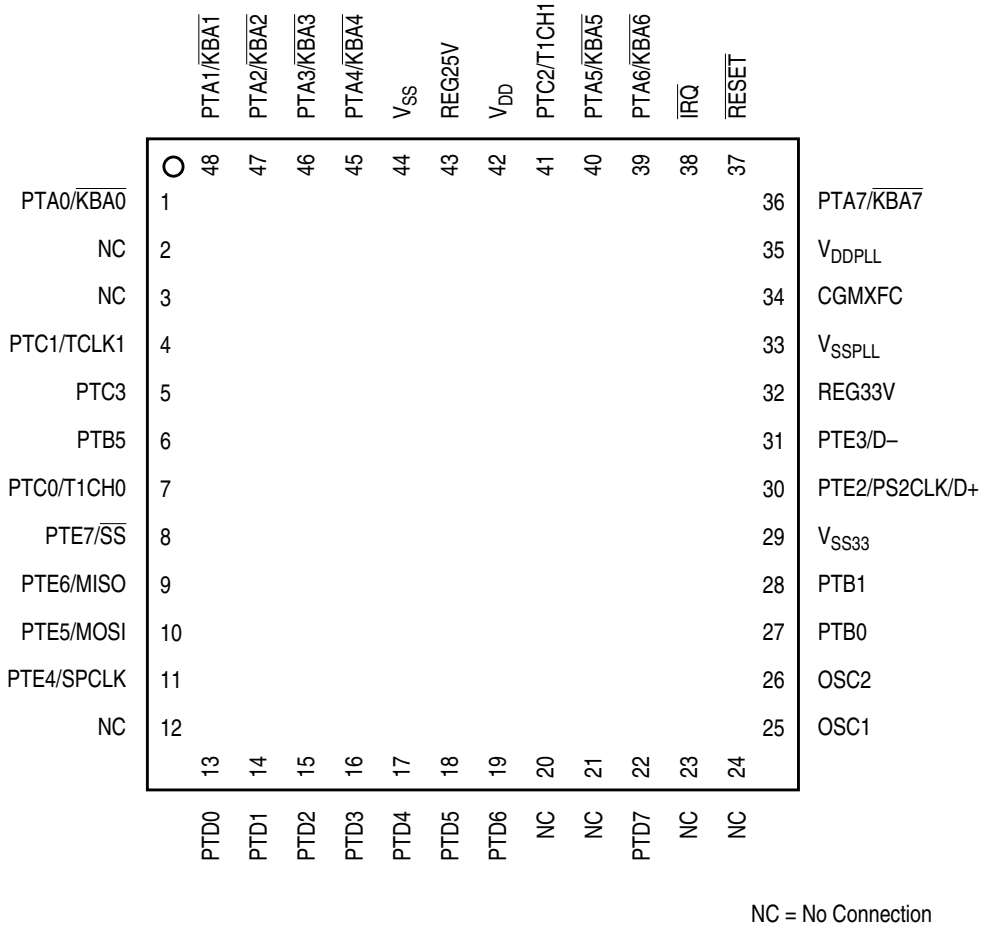


Figure 1-3. 48-Pin LQFP and QFN Pin Assignment

1.5 Clock Tree

Figure 1-4 shows the clock tree diagram for the MC68HC908JW32.

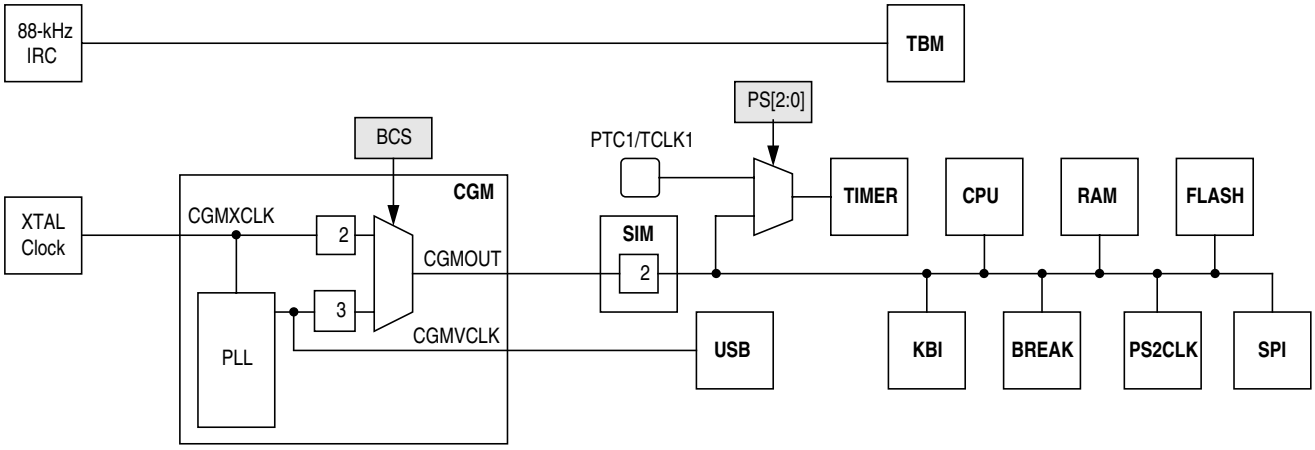


Figure 1-4. Clock Tree Diagram

1.6 Power Management

Figure 1-5 shows the power management diagram for MC68HC908JW32.

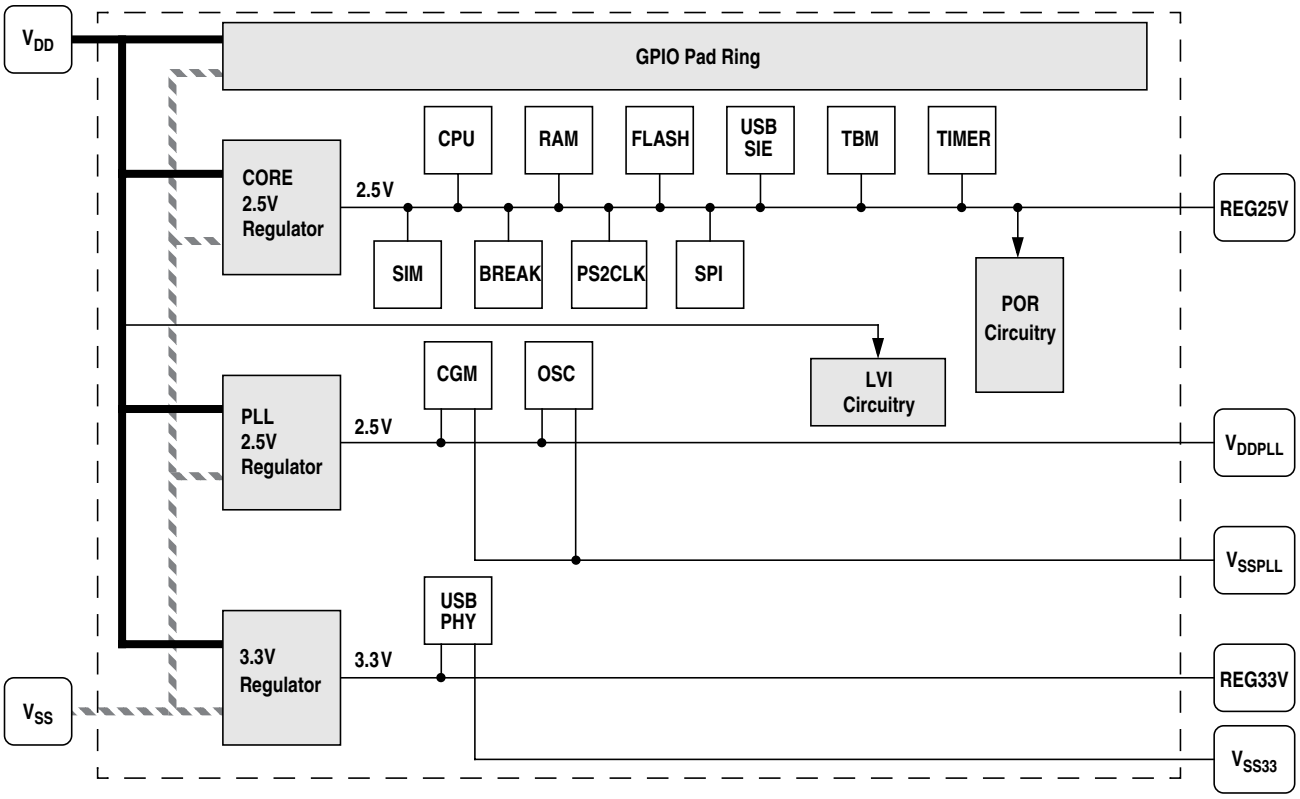


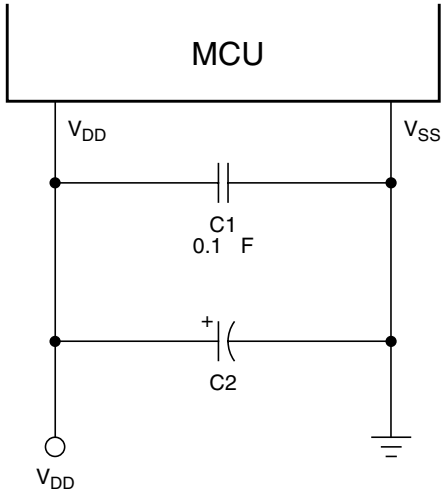
Figure 1-5. Power Management Diagram

1.7 Pin Function

1.7.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as Figure 1-6 shows. Place the C1 bypass capacitor as close to the MCU as possible. Use a high-frequency-response ceramic capacitor for C1. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.



NOTE: Component values shown represent typical applications.

Figure 1-6. Power Supply Bypassing

V_{SS} must be grounded for proper MCU operation.

1.7.2 Analog Power Supply (V_{DDPLL} and V_{SSPLL})

V_{DDPLL} is the internal voltage regulator supply for the CGM module of the device. It is recommended that a decoupling capacitor be connected between the V_{DDPLL} and V_{SSPLL} pins placing it as close to the pins as possible.

1.7.3 Internal Voltage Regulator Supply (REG25V, REG33V, and V_{SS33})

VREG25 is the internal core voltage regulator supply. VREG33 and VSS33 are the internal USB voltage regulator supply.

1.7.4 Oscillator Pins (OSC1 and OSC2)

The OSC1 and OSC2 pins are the connections for the on-chip oscillator circuit.

1.7.5 External Reset Pin ($\overline{\text{RST}}$)

A logic 0 on the $\overline{\text{RST}}$ pin forces the MCU to a known start-up state. $\overline{\text{RST}}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted. A schmitt-trigger and a spike filter is associated with this pin so that the device is more robust to EMC noise.This pin also contains an internal pullup resistor.

1.7.6 External Interrupt Pin ($\overline{\text{IRQ}}$)

$\overline{\text{IRQ}}$ is an asynchronous external interrupt pin. This pin contains an internal pullup resistor.

1.7.7 External Filter Capacitor Pin (CGMXFC)

CGMXFC is an external filter connection for the on-chip PLL.

1.7.8 Port A Input/Output (I/O) Pins (PTA7–PTA0)

PTA7–PTA0 are special function, bidirectional ports pins. These pins are shared with KBI module.

1.7.9 Port B Input/Output (I/O) Pins (PTB7–PTB0)

PTB7–PTB0 are special function, bidirectional ports pins. These pins can be programmable as open-drain output with high current sourcing capability and has built-in programmable pull up resistor.

1.7.10 Port C Input/Output (I/O) Pins (PTC3–PTC0)

PTC0–PTC3 are bidirectional ports pins. PTC0–PTC2 are shared with TIMER channel 0, channel 1 and TCLK1 pins respectively.

1.7.11 Port D Input/Output (I/O) Pins (PTD7–PTD0)

PTD7–PTD0 are bidirectional ports pins. Pullup option are associated with PTD2, 3 and 7. The option is default enabled after reset.

1.7.12 Port E Input/Output (I/O) Pins (PTE7–PTE2)

PTE7–PTE2 are special function, bidirectional ports pins. PTE2–PTE3 are shared with USB 2.0 FS module. PTE2 is shared with PS2 clock module. PTE4–PTE7 are shared with SPI module.