



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



M68HC12B Family

Data Sheet

**M68HC12
Microcontrollers**

M68HC12B
Rev. 9.1
07/2005

freescale.com

M68HC12B Family

Data Sheet

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

<http://freescale.com>

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc.
This product incorporates SuperFlash® technology licensed from SST.

© Freescale Semiconductor, Inc., 2005. All rights reserved.

Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
June, 2001	2.0	Figure 1-7. BDM Tool Connector — Added NC (no connect) designator to pin 3	29
		Figure 18-16. BDM Tool Connector — Added NC designator to pin 3	305
		Table 14-2. Loop Mode Functions — Corrected table header, third column, from DDRS1 to DDS1	195
		WOMS bit description, fifth line, changed (via DDRS0/2) to (via DDS0/2)	195
		SSOE bit description, second line, changed DDRS7 to DDS7	205
		In the table notes following the SPC0 bit description, corrected bit designators from DDRS4, DDRS5, DDRS6, and DDRS7 to DDS4, DDS5, DDS6, and DDS7.	205
September, 2001	3.0	Table 13-3. Prescaler Selection — Added value column and updated prescale factors	172
		19.11 EEPROM Characteristics — Corrected minimum and maximum values for programming and erase times	313
April, 2002	4.0	Document type changed from Advance Information to Technical Data reflecting qualification.	N/A
		Figure 3-9. Condition Code Register (CCR) — Reset value for S bit corrected from U to 1	62
January, 2003	5.0	14.2.3.3 SCI Control Register 2 — Removed erroneous reference to Port S bit 3 in the definition for the transmitter enable bit (TE).	197
		Figure 14-20. Port S Data Register (PORTS) — Removed erroneous pin function for PS3 and PS2.	208
		Reformatted to meet publication standards	N/A
April, 2003	6.0	19.2 Maximum Ratings — Corrected maximum values for VDD, VDDA, VDDX, and VIn	307
		19.7 ATD Maximum Ratings — Corrected maximum values for VRH and VRL	310
		Figure 19-1. Programming Voltage Envelope — Corrected maximum values for VFP and VDD	315
May, 2003	7.0	19.12.1 Programming Voltage Supply Envelope — Added subsection for clarity.	315
		19.12.2 Example V _{FP} Protection Circuitry — Added subsection for clarity.	316
July, 2003	8.0	19.2 Maximum Ratings — Updated values	307
		19.7 ATD Maximum Ratings — Updated values	310
June, 2004	9.0	Table 13-3. Prescaler Selection — Corrected prescaler factor for values 6 and 7	183
July, 2005	9.1	Updated to meet Freescale identity guidelines.	Throughout

List of Chapters

Chapter 1 General Description	19
Chapter 2 Register Block	39
Chapter 3 Central Processor Unit (CPU).	59
Chapter 4 Resets and Interrupts	67
Chapter 5 Operating Modes and Resource Mapping	75
Chapter 6 Bus Control and Input/Output (I/O)	85
Chapter 7 EEPROM	93
Chapter 8 FLASH EEPROM	99
Chapter 9 Read-Only Memory (ROM)	111
Chapter 10 Clock Generation Module (CGM)	113
Chapter 11 Pulse-Width Modulator (PWM)	125
Chapter 12 Standard Timer (TIM).	141
Chapter 13 Enhanced Capture Timer (ECT) Module	159
Chapter 14 Serial Interface	191
Chapter 15 Byte Data Link Communications (BDLC)	213
Chapter 16 msCAN12 Controller	243
Chapter 17 Analog-to-Digital Converter (ATD).	277
Chapter 18 Development Support	289
Chapter 19 Electrical Specifications	307
Chapter 20 Mechanical Specifications	331



List of Chapters

Table of Contents

Chapter 1 General Description

1.1	Introduction	19
1.2	Features	20
1.3	Slow-Mode Clock Divider Advisory	21
1.4	Block Diagrams	22
1.5	Ordering Information	24
1.6	Pinout and Signal Descriptions	24
1.6.1	Pin Assignments	24
1.6.2	Power Supply Pins	24
1.6.2.1	V_{DD} and V_{SS}	24
1.6.2.2	V_{DDX} and V_{SSX}	24
1.6.2.3	V_{DDA} and V_{SSA}	24
1.6.2.4	V_{RH} and V_{RL}	24
1.6.2.5	V_{FP} (MC68HC912B32 and MC68HC912BC32 only)	27
1.6.3	Signal Descriptions	27
1.6.3.1	XTAL and EXTAL	27
1.6.3.2	ECLK	28
1.6.3.3	$\overline{\text{RESET}}$	28
1.6.3.4	$\overline{\text{IRQ}}$	28
1.6.3.5	$\overline{\text{XIRQ}}$	29
1.6.3.6	SMODN, MODA, and MODB	29
1.6.3.7	BKGD	29
1.6.3.8	ADDR15–ADDR0 and DATA15–DATA0	30
1.6.3.9	$\overline{\text{R/W}}$	30
1.6.3.10	$\overline{\text{LSTRB}}$	30
1.6.3.11	IPIPE1 and IPIPE0	30
1.6.3.12	$\overline{\text{DBE}}$	30
1.6.4	Port Signals	32
1.6.4.1	Port A	32
1.6.4.2	Port B	33
1.6.4.3	Port E	33
1.6.4.4	Port DLC	34
1.6.4.5	Port CAN	34
1.6.4.6	Port AD	34
1.6.4.7	Port P	35
1.6.4.8	Port T	35
1.6.4.9	Port S	35
1.6.5	Port Pullup, Pulldown, and Reduced Drive	36

Chapter 2 Register Block

2.1	Introduction	39
2.2	Registers	40

Chapter 3 Central Processor Unit (CPU)

3.1	Introduction	59
3.2	Programming Model	59
3.3	CPU Registers	60
3.3.1	Accumulators A and B	60
3.3.2	Accumulator D	60
3.3.3	Index Registers X and Y	61
3.3.4	Stack Pointer	61
3.3.5	Program Counter	62
3.3.6	Condition Code Register	62
3.4	Data Types	63
3.5	Addressing Modes	63
3.6	Indexed Addressing Modes	64
3.7	Opcodes and Operands	65

Chapter 4 Resets and Interrupts

4.1	Introduction	67
4.2	Exception Priority	67
4.3	Maskable Interrupts	67
4.4	Latching of Interrupts	70
4.5	Interrupt Control and Priority Registers	70
4.5.1	Interrupt Control Register	70
4.5.2	Highest Priority I Interrupt Register	71
4.6	Resets	71
4.6.1	Power-On Reset (POR)	71
4.6.2	External Reset	71
4.6.3	Computer Operating Properly (COP) Reset	71
4.6.4	Clock Monitor Reset	72
4.7	Effects of Reset	72
4.7.1	Operating Mode and Memory Map	72
4.7.2	Clock and Watchdog Control Logic	72
4.7.3	Interrupts	72
4.7.4	Parallel Input/Output (I/O)	72
4.7.5	Central Processing Unit (CPU)	72
4.7.6	Memory	72
4.7.7	Other Resources	73
4.8	Interrupt Recognition	73

Chapter 5 Operating Modes and Resource Mapping

5.1	Introduction	75
5.2	Operating Modes	75
5.2.1	Normal Operating Modes	76
5.2.1.1	Normal Expanded Wide Mode	76
5.2.1.2	Normal Expanded Narrow Mode	76
5.2.1.3	Normal Single-Chip Mode	76
5.2.2	Special Operating Modes	76
5.2.2.1	Special Expanded Wide Mode	76
5.2.2.2	Special Expanded Narrow Mode	76
5.2.2.3	Special Single-Chip Mode	76
5.2.2.4	Special Peripheral Mode	77
5.2.3	Background Debug Mode	77
5.3	Internal Resource Mapping	77
5.4	Mode and Resource Mapping Registers	78
5.4.1	Mode Register	78
5.4.2	Register Initialization Register	80
5.4.3	RAM Initialization Register	80
5.4.4	EEPROM Initialization Register	81
5.4.5	Miscellaneous Mapping Control Register	81
5.5	Memory Map	83

Chapter 6 Bus Control and Input/Output (I/O)

6.1	Introduction	85
6.2	Detecting Access Type from External Signals	85
6.3	Registers	85
6.3.1	Port A Data Register	86
6.3.2	Port A Data Direction Register	86
6.3.3	Port B Data Register	87
6.3.4	Port B Data Direction Register	87
6.3.5	Port E Data Register	88
6.3.6	Port E Data Direction Register	88
6.3.7	Port E Assignment Register	89
6.3.8	Pullup Control Register	91
6.3.9	Reduced Drive of I/O Lines	92

Chapter 7 EEPROM

7.1	Introduction	93
7.2	EEPROM Programmer's Model	93
7.3	EEPROM Control Registers	94
7.3.1	EEPROM Module Configuration Register	94
7.3.2	EEPROM Block Protect Register	95
7.3.3	EEPROM Test Register	95
7.3.4	EEPROM Control Register	96

Chapter 8 FLASH EEPROM

8.1	Introduction	99
8.2	FLASH EEPROM Array	99
8.3	FLASH EEPROM Registers	99
8.3.1	FLASH EEPROM Lock Control Register	100
8.3.2	FLASH EEPROM Module Configuration Register	100
8.3.3	FLASH EEPROM Module Test Register	100
8.3.4	FLASH EEPROM Control Register	102
8.4	Operation	103
8.4.1	Bootstrap Operation Single-Chip Mode	103
8.4.2	Normal Operation	103
8.4.3	Program/Erase Operation	103
8.4.3.1	Read/Write Accesses During Program/Erase	103
8.4.3.2	Program/Erase Verification	104
8.4.3.3	Program/Erase Sequence	104
8.5	Programming the FLASH EEPROM	105
8.6	Erasing the FLASH EEPROM	107
8.7	Program/Erase Protection Interlocks	109
8.8	Stop or Wait Mode	109
8.9	Test Mode	109

Chapter 9 Read-Only Memory (ROM)

9.1	Introduction	111
9.2	ROM Array	111

Chapter 10 Clock Generation Module (CGM)

10.1	Introduction	113
10.2	Block Diagram	113
10.3	Register Map	114
10.4	Clock Selection and Generation	114
10.5	Slow Mode Divider	116
10.6	Clock Functions	116
10.6.1	Computer Operating Properly (COP)	116
10.6.2	Real-Time Interrupt	116
10.6.3	Clock Monitor	116
10.7	Clock Registers	117
10.7.1	Slow Mode Divider Register	117
10.7.2	Real-Time Interrupt Control Register	118
10.7.3	Real-Time Interrupt Flag Register	119
10.7.4	COP Control Register	119
10.7.5	Arm/Reset COP Timer Register	120
10.8	Clock Divider Chains	121

Chapter 11 Pulse-Width Modulator (PWM)

11.1	Introduction	125
11.2	PWM Register Descriptions	128
11.2.1	PWM Clocks and Concatenate Register	128
11.2.2	PWM Clock Select and Polarity Register	129
11.2.3	PWM Enable Register	130
11.2.4	PWM Prescale Counter	131
11.2.5	PWM Scale Register 0	131
11.2.6	PWM Scale Counter 0 Value	131
11.2.7	PWM Scale Register 1	132
11.2.8	PWM Scale Counter 1 Value	132
11.2.9	PWM Channel Counters 0–3	133
11.2.10	PWM Channel Period Registers 0–3	134
11.2.11	PWM Channel Duty Registers 0–3	135
11.2.12	PWM Control Register	136
11.2.13	PWM Special Mode Register	137
11.2.14	Port P Data Register	137
11.2.15	Port P Data Direction Register	138
11.3	PWM Boundary Cases	138
11.4	Using the Output Compare 7 Feature to Generate a PWM	138
11.4.1	PWM Period Calculation	139
11.4.2	Equipment	139
11.4.3	Code Listing	140

Chapter 12 Standard Timer (TIM)

12.1	Introduction	141
12.2	Timer Registers	141
12.2.1	Timer Input Capture/Output Compare Select Register	141
12.3	Block Diagram	142
12.3.1	Timer Compare Force Register	143
12.3.2	Output Compare 7 Mask Register	143
12.3.3	Output Compare 7 Data Register	143
12.3.4	Timer Count Register	144
12.3.5	Timer System Control Register	144
12.3.6	Timer Control Registers	145
12.3.7	Timer Interrupt Mask Registers	146
12.3.8	Timer Interrupt Flag Registers	148
12.3.9	Timer Input Capture/Output Compare Registers	149
12.3.10	Pulse Accumulator Control Register	151
12.3.11	Pulse Accumulator Flag Register	153
12.3.12	16-Bit Pulse Accumulator Count Register	153
12.3.13	Timer Test Register	154
12.3.14	Timer Port Data Register	154
12.3.15	Data Direction Register for Timer Port	155
12.4	Timer Operation in Modes	155

Table of Contents

12.5	Using the Output Compare Function to Generate a Square Wave	156
12.5.1	Sample Calculation to Obtain Period Counts	156
12.5.2	Equipment	156
12.5.3	Code Listing	156

Chapter 13
Enhanced Capture Timer (ECT) Module

13.1	Introduction	159
13.2	Basic Timer Overview	159
13.3	Enhanced Capture Timer Modes of Operation	159
13.3.1	IC Channels	160
13.3.1.1	Non-Buffered IC Channels	160
13.3.1.2	Buffered IC Channels	160
13.3.2	Pulse Accumulators	163
13.3.2.1	Pulse Accumulator Latch Mode	163
13.3.2.2	Pulse Accumulator Queue Mode	163
13.3.3	Modulus Down-Counter	163
13.4	Timer Registers	163
13.4.1	Timer Input Capture/Output Compare Select Register	166
13.4.2	Timer Compare Force Register	166
13.4.3	Output Compare 7 Mask Register	166
13.4.4	Output Compare 7 Data Register	167
13.4.5	Timer Count Registers	168
13.4.6	Timer System Control Register	168
13.4.7	Timer Control Registers	169
13.4.8	Timer Interrupt Mask Registers	171
13.4.9	Main Timer Interrupt Flag Registers	172
13.4.10	Timer Input Capture/Output Compare Registers	173
13.4.11	16-Bit Pulse Accumulator A Control Register	176
13.4.12	Pulse Accumulator A Flag Register	177
13.4.13	Pulse Accumulators Count Registers	178
13.4.14	16-Bit Modulus Down-Counter Control Register	179
13.4.15	16-Bit Modulus Down-Counter Flag Register	180
13.4.16	Input Control Pulse Accumulators Control Register	181
13.4.17	Delay Counter Control Register	181
13.4.18	Input Control Overwrite Register	182
13.4.19	Input Control System Control Register	182
13.4.20	Timer Test Register	183
13.4.21	Timer Port Data Register	184
13.4.22	Data Direction Register for Timer Port	184
13.4.23	16-Bit Pulse Accumulator B Control Register	185
13.4.24	Pulse Accumulator B Flag Register	185
13.4.25	8-Bit Pulse Accumulators Holding Registers	186
13.4.26	Modulus Down-Counter Count Registers	187
13.4.27	Timer Input Capture Holding Registers	187
13.5	Timer and Modulus Counter Operation in Different Modes	189

Chapter 14 Serial Interface

14.1	Introduction	191
14.2	Serial Communication Interface (SCI)	192
14.2.1	Data Format	193
14.2.2	SCI Baud Rate Generation	193
14.2.3	SCI Register Descriptions	194
14.2.3.1	SCI Baud Rate Control Register	194
14.2.3.2	SCI Control Register 1	195
14.2.3.3	SCI Control Register 2	197
14.2.3.4	SCI Status Register 1	198
14.2.3.5	SCI Status Register 2	199
14.2.3.6	SCI Data Register	200
14.3	Serial Peripheral Interface (SPI)	201
14.3.1	SPI Baud Rate Generation	202
14.3.2	SPI Operation	202
14.3.3	\overline{SS} Output	203
14.3.4	Bidirectional Mode (MOMI or SISO)	204
14.3.5	SPI Register Descriptions	204
14.3.5.1	SPI Control Register 1	204
14.3.5.2	SPI Control Register 2	205
14.3.5.3	SPI Baud Rate Register	206
14.3.5.4	SPI Status Register	207
14.3.5.5	SPI Data Register	207
14.4	Port S	208
14.4.1	Port S Data Register	208
14.4.2	Port S Data Direction Register	208
14.4.3	Pullup and Reduced Drive Register for Port S	209
14.5	Serial Character Transmission using the SCI	210
14.5.1	Equipment	210
14.5.2	Code Listing	210
14.6	Synchronous Character Transmission using the SPI	211
14.6.1	Equipment	211
14.6.2	Code Listing	211

Chapter 15 Byte Data Link Communications (BDLC)

15.1	Introduction	213
15.2	Features	213
15.3	Functional Description	213
15.4	BDLC Operating Modes	214
15.4.1	Power Off Mode	215
15.4.2	Reset Mode	215
15.4.3	Run Mode	215
15.5	Power-Conserving Modes	215
15.5.1	BDLC Wait and CPU Wait Mode	216
15.5.2	BDLC Stop and CPU Wait Mode	216

Table of Contents

15.5.3	BDLC Stop and CPU Stop Mode	217
15.6	Loopback Modes	217
15.6.0.1	Digital Loopback Mode	217
15.6.0.2	Analog Loopback Mode	217
15.7	BDLC MUX Interface	218
15.7.1	Rx Digital Filter	218
15.7.1.1	Operation	218
15.7.1.2	Performance	219
15.7.2	J1850 Frame Format	219
15.7.2.1	SOF — Start-of-Frame Symbol	219
15.7.2.2	Data — In-Message Data Bytes	220
15.7.2.3	CRC — Cyclical Redundancy Check Byte	220
15.7.2.4	EOD — End-of-Data Symbol	220
15.7.2.5	IFR — In-Frame Response Bytes	220
15.7.2.6	EOF — End-of-Frame Symbol	220
15.7.2.7	IFS — Interframe Separation Symbol	220
15.7.2.8	BREAK — Break	221
15.7.2.9	IDLE — Idle Bus	221
15.7.3	J1850 VPW Symbols	221
15.7.3.1	Logic 0	222
15.7.3.2	Logic 1	222
15.7.3.3	Normalization Bit (NB)	222
15.7.3.4	Break Signal (BREAK)	222
15.7.3.5	Start-of-Frame Symbol (SOF)	223
15.7.3.6	End-of-Data Symbol (EOD)	223
15.7.3.7	End-of-Frame Symbol (EOF)	223
15.7.3.8	Inter-Frame Separation Symbol (IFS)	223
15.7.3.9	Idle	223
15.7.4	J1850 VPW Valid/Invalid Bits and Symbols	223
15.7.4.1	Invalid Passive Bit	224
15.7.4.2	Valid Passive Logic 0	224
15.7.4.3	Valid Passive Logic 1	224
15.7.4.4	Valid EOD Symbol	224
15.7.4.5	Valid EOF and IFS Symbols	225
15.7.4.6	Idle Bus	225
15.7.4.7	Invalid Active Bit	226
15.7.4.8	Valid Active Logic 1	226
15.7.4.9	Valid Active Logic 0	226
15.7.4.10	Valid SOF Symbol	226
15.7.4.11	Valid BREAK Symbol	227
15.7.5	Message Arbitration	227
15.8	BDLC Protocol Handler	228
15.8.1	Protocol Architecture	228
15.8.2	Rx and Tx Shift Registers	228
15.8.3	Rx and Tx Shadow Registers	228
15.8.4	Digital Loopback Multiplexer	229

15.8.5	State Machine	229
15.8.5.1	4X Mode	229
15.8.5.2	Receiving a Message in Block Mode	229
15.8.5.3	Transmitting a Message in Block Mode	230
15.8.5.4	J1850 Bus Errors	230
15.8.5.5	Summary	231
15.9	BDLC Registers	231
15.9.1	BDLC Control Register 1	231
15.9.2	BDLC Control Register 2	233
15.9.3	BDLC State Vector Register	237
15.9.4	BDLC Data Register	239
15.9.5	BDLC Analog Roundtrip Delay Register	240
15.9.6	Port DLC Control Register	241
15.9.7	Port DLC Data Register	242
15.9.8	Port DLC Data Direction Register	242

Chapter 16 msCAN12 Controller

16.1	Introduction	243
16.2	External Pins	243
16.3	Message Storage	243
16.3.1	Background	244
16.3.2	Receive Structures	245
16.3.3	Transmit Structures	246
16.4	Identifier Acceptance Filter	247
16.5	Interrupts	250
16.5.1	Interrupt Acknowledge	250
16.5.2	Interrupt Vectors	250
16.6	Protocol Violation Protection	251
16.7	Low-Power Modes	251
16.7.1	msCAN12 Sleep Mode	252
16.7.2	msCAN12 Soft-Reset Mode	253
16.7.3	msCAN12 Power-Down Mode	254
16.7.4	Programmable Wakeup Function	254
16.8	Timer Link	254
16.9	Clock System	254
16.10	Memory Map	257
16.11	Programmer's Model of Message Storage	257
16.11.1	Message Buffer Organization	257
16.11.2	Identifier Registers	258
16.11.3	Data Length Register	260
16.11.4	Data Segment Registers	261
16.11.5	Transmit Buffer Priority Register	261
16.12	Programmer's Model of Control Registers	262
16.12.1	msCAN12 Module Control Register 0	262
16.12.2	msCAN12 Module Control Register 1	263
16.12.3	msCAN12 Bus Timing Register 0	264

Table of Contents

16.12.4	msCAN12 Bus Timing Register 1	265
16.12.5	msCAN12 Receiver Flag Register	266
16.12.6	msCAN12 Receiver Interrupt Enable Register	268
16.12.7	msCAN12 Transmitter Flag Register	269
16.12.8	msCAN12 Transmitter Control Register	270
16.12.9	msCAN12 Identifier Acceptance Control Register	270
16.12.10	msCAN12 Receive Error Counter	271
16.12.11	msCAN12 Transmit Error Counter	272
16.12.12	msCAN12 Identifier Acceptance Registers	272
16.12.13	msCAN12 Identifier Mask Registers	273
16.12.14	msCAN12 Port CAN Control Register	275
16.12.15	msCAN12 Port CAN Data Register	275
16.12.16	msCAN12 Port CAN Data Direction Register	276

Chapter 17 Analog-to-Digital Converter (ATD)

17.1	Introduction	277
17.2	Functional Description	277
17.3	ATD Registers	279
17.3.1	ATD Control Register 0	279
17.3.2	ATD Control Register 1	279
17.3.3	ATD Control Register 2	279
17.3.4	ADT Control Register 3	280
17.3.5	ATD Control Register 4	281
17.3.6	ATD Control Register 5	282
17.3.7	ATD Status Registers	284
17.3.8	ATD Test Registers	285
17.3.9	Port AD Data Input Register	286
17.3.10	ATD Result Registers	286
17.4	ATD Mode Operation	287
17.5	Using the ATD to Measure a Potentiometer Signal	287
17.5.1	Equipment	287
17.5.2	Code Listing	287

Chapter 18 Development Support

18.1	Introduction	289
18.2	Instruction Queue	289
18.3	Background Debug Mode (BDM)	290
18.3.1	BDM Serial Interface	290
18.3.2	Enabling BDM Firmware Commands	292
18.3.3	BDM Commands	293
18.3.4	BDM Registers	295
18.3.5	BDM Instruction Register	296
18.3.5.1	Hardware Command	296
18.3.5.2	Firmware Command	297

18.3.6	BDM Status Register	298
18.3.7	BDM Shifter Register	298
18.3.8	BDM Address Register	299
18.3.9	BDM CCR Holding Register	299
18.4	Breakpoints	299
18.4.1	Breakpoint Modes	300
18.4.1.1	SWI Dual Address Mode	300
18.4.1.2	BDM Full Breakpoint Mode	300
18.4.1.3	BDM Dual Address Mode	300
18.4.2	Breakpoint Registers	301
18.4.2.1	Breakpoint Control Register 0	301
18.4.2.2	Breakpoint Control Register 1	302
18.4.2.3	Breakpoint Address Register High	303
18.4.2.4	Breakpoint Address Register Low	303
18.4.2.5	Breakpoint Data Register High	304
18.4.2.6	Breakpoint Data Register Low Byte	304
18.5	Instruction Tagging	304

Chapter 19 Electrical Specifications

19.1	Introduction	307
19.2	Maximum Ratings	307
19.3	Functional Operating Range	308
19.4	Thermal Characteristics	308
19.5	5.0 Volt DC Electrical Characteristics	309
19.6	Supply Current	310
19.7	ATD Maximum Ratings	310
19.8	ATD DC Electrical Characteristics	311
19.9	Analog Converter Operating Characteristics	312
19.10	ATD AC Operating Characteristics (Operating)	313
19.11	EEPROM Characteristics	313
19.12	FLASH EEPROM Characteristics	314
19.12.1	Programming Voltage Supply Envelope	315
19.12.2	Example V_{FP} Protection Circuitry	316
19.13	Pulse-Width Modulator Characteristics	319
19.14	Control Timing	320
19.15	Peripheral Port Timing	325
19.16	Multiplexed Expansion Bus Timing	326
19.17	Serial Peripheral Interface (SPI) Timing	328

Chapter 20 Mechanical Specifications

20.1	Introduction	331
20.2	80-Pin Quad Flat Pack (Case 841B-02)	332



Table of Contents

Chapter 1

General Description

1.1 Introduction

The MC68HC912B32, MC68HC12BE32 and MC68HC(9)12BC32, are 16-bit microcontroller units (MCUs) composed of standard on-chip peripherals. The multiplexed external bus can also operate in an 8-bit narrow mode for interfacing with single 8-bit wide memory in lower-cost systems. There is a slight feature set difference between the four pin-for-pin compatible devices as shown in [Table 1-1](#).

Table 1-1. M68HC12B Series Feature Set Comparisons

Features	MC68HC912B32	MC68HC12BE32	MC68HC912BC32	MC68HC12BC32
CPU12	X	X	X	X
Multiplexed bus	X	X	X	X
32-Kbyte FLASH electrically erasable, programmable read-only memory (EEPROM)	X		X	
32-Kbyte read-only memory (ROM)		X		X
768-byte EEPROM	X	X	X	X
1-Kbyte random-access memory (RAM)	X	X	X	X
Analog-to-digital (A/D) converter	X	X	X	X
Standard timer module (TIM)	X		X	X
Enhanced capture timer (ECT)		X		
Pulse-width modulator (PWM)	X	X	X	X
Asynchronous serial communications interface (SCII)	X	X	X	X
Synchronous serial peripheral interface (SPI)	X	X	X	X
J1850 byte data link communication (BDLC)	X	X		
Controller area network module (CAN)			X	X
Computer operating properly (COP) watchdog timer	X	X	X	X
Slow mode clock divider	X	X	X	X
80-pin quad flat pack (QFP)	X	X	X	X
Single-wire background debug mode (BDM)	X	X	X	X

1.2 Features

Features include:

- 16-bit CPU12:
 - Upwardly compatible with the M68HC11 instruction set
 - Interrupt stacking and programmer's model identical to the M68HC11
 - 20-bit arithmetic logic unit (ALU)
 - Instruction queue
 - Enhanced indexed addressing
 - Fuzzy logic instructions
- Multiplexed bus:
 - Single chip or expanded
 - 16-bit by 16-bit wide or 16-bit by 8-bit narrow modes
- Memory:
 - 32-Kbyte FLASH electrically erasable, programmable read-only memory (EEPROM) with 2-Kbyte erase-protected boot block — MC68HC912B32 and MC68HC912BC32 only
 - 32-Kbyte ROM — MC68HC12BE32 and MC68HC12BC32 only
 - 768-byte EEPROM
 - 1-Kbyte random-access memory (RAM) with single-cycle access for aligned or misaligned read/write
- 8-channel, 10-bit analog-to-digital converter (ATD)
- 8-channel standard timer module (TIM) — MC68HC912B32 and MC68HC(9)12BC32 only:
 - Each channel fully configurable as either input capture or output compare
 - Simple pulse-width modulator (PWM) mode
 - Modulus reset of timer counter
- Enhanced capture timer (ECT) — MC68HC12BE32 only:
 - 16-bit main counter with 7-bit prescaler
 - Eight programmable input capture or output compare channels; four of the eight input captures with buffer
 - Input capture filters and buffers, three successive captures on four channels, or two captures on four channels with a capture/compare selectable on the remaining four
 - Four 8-bit or two 16-bit pulse accumulators
 - 16-bit modulus down-counter with 4-bit prescaler
 - Four user-selectable delay counters for signal filtering
- 16-bit pulse accumulator:
 - External event counting
 - Gated time accumulation
- Pulse-width modulator (PWM):
 - 8-bit, 4-channel or 16-bit, 2-channel
 - Separate control for each pulse width and duty cycle
 - Programmable center-aligned or left-aligned outputs

- Serial interfaces:
 - Asynchronous serial communications interface (SCI)
 - Synchronous serial peripheral interface (SPI)
 - J1850 byte data link communication (BDLC), MC68HC912B32 and MC68HC12BE32 only
 - Controller area network (CAN), MC68HC(9)12BC32 only
- Computer operating properly (COP) watchdog timer, clock monitor, and periodic interrupt timer
- Slow-mode clock divider
- 80-pin quad flat pack (QFP)
- Up to 63 general-purpose input/output (I/O) lines
- Single-wire background debug mode (BDM)
- On-chip hardware breakpoints

1.3 Slow-Mode Clock Divider Advisory

Current versions of the M68HC12B-series devices include a slow-mode clock divider feature. This feature is fully described in [Chapter 10 Clock Generation Module \(CGM\)](#). The register that controls this feature is located at \$00E0. Older device mask sets do not support the slow-mode clock divider feature. This register address is reserved in older devices and provides no function.

Mask sets that do not have the slow-mode clock divider feature on the MC68HC912B32 include: G96P, G86W, and H91F.

Mask sets that do not have the slow-mode clock divider feature on the MC68HC12BE32 include: H54T and J38M.

Mask sets that do not have the slow-mode clock divider feature on the MC68HC(9)12BC32 include: J15G.

1.4 Block Diagrams

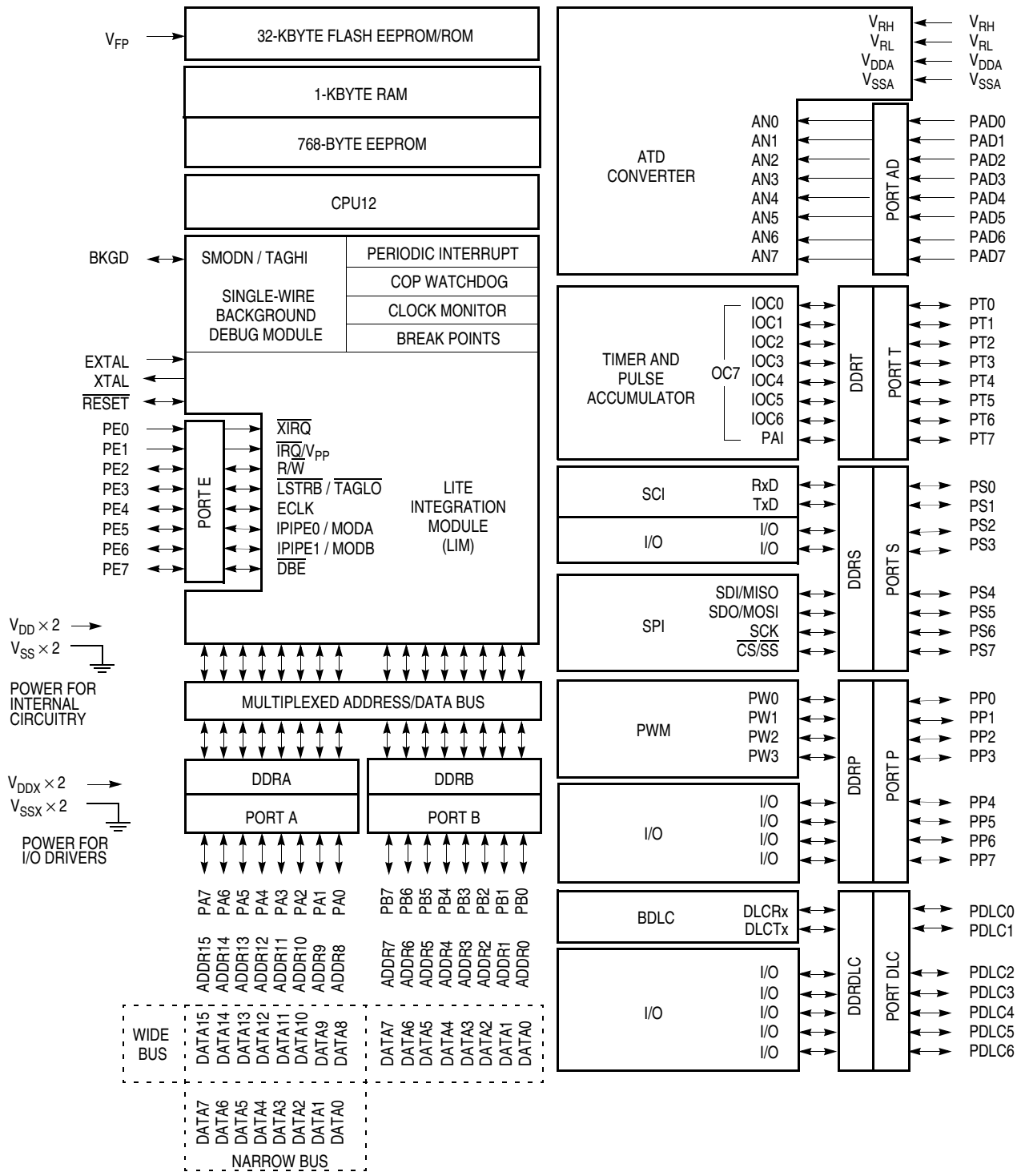


Figure 1-1. Block Diagram for MC68HC912B32 and MC68HC12BE32

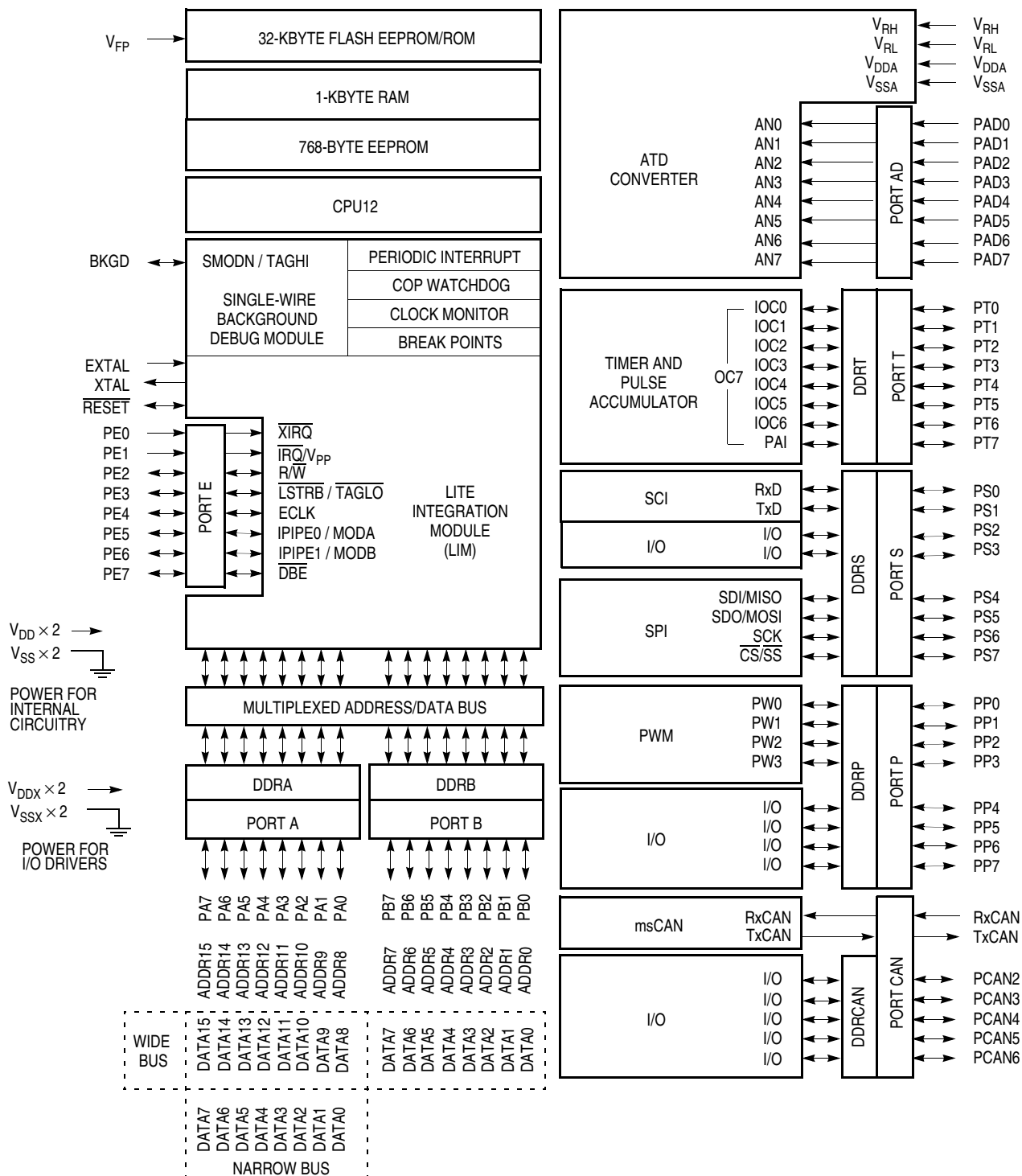


Figure 1-2. Block Diagram for MC68HC(9)12BC32

1.5 Ordering Information

The M68HC12B-series devices are available in 80-pin quad flat pack (QFP) packaging and are shipped in 2-piece sample packs, 84-piece trays, or 420-piece bricks.

Operating temperature range, package type, and voltage requirements are specified when ordering the specific device.

Documents to assist in product selection are available from the Freescale Literature Distribution Center or your local Freescale sales offices.

Product selection guides can also be found on the worldwide web at this URL:

<http://freescale.com>

Evaluation boards, assemblers, compilers, and debuggers are available from Freescale and from third-party suppliers. An up-to-date list of products that support the M68HC12 Family of microcontrollers can be found on the worldwide web at this URL:

<http://freescale.com>

1.6 Pinout and Signal Descriptions

1.6.1 Pin Assignments

The MCU is available in an 80-pin quad flat pack (QFP). [Figure 1-3](#) and [Figure 1-4](#) show the pin assignments. Most pins perform two or more functions, as described in the [1.6.3 Signal Descriptions](#).

1.6.2 Power Supply Pins

The MCU power and ground pins are described here and summarized in [Table 1-2](#).

1.6.2.1 V_{DD} and V_{SS}

V_{DD} and V_{SS} are the internal power supply and ground pins. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

1.6.2.2 V_{DDX} and V_{SSX}

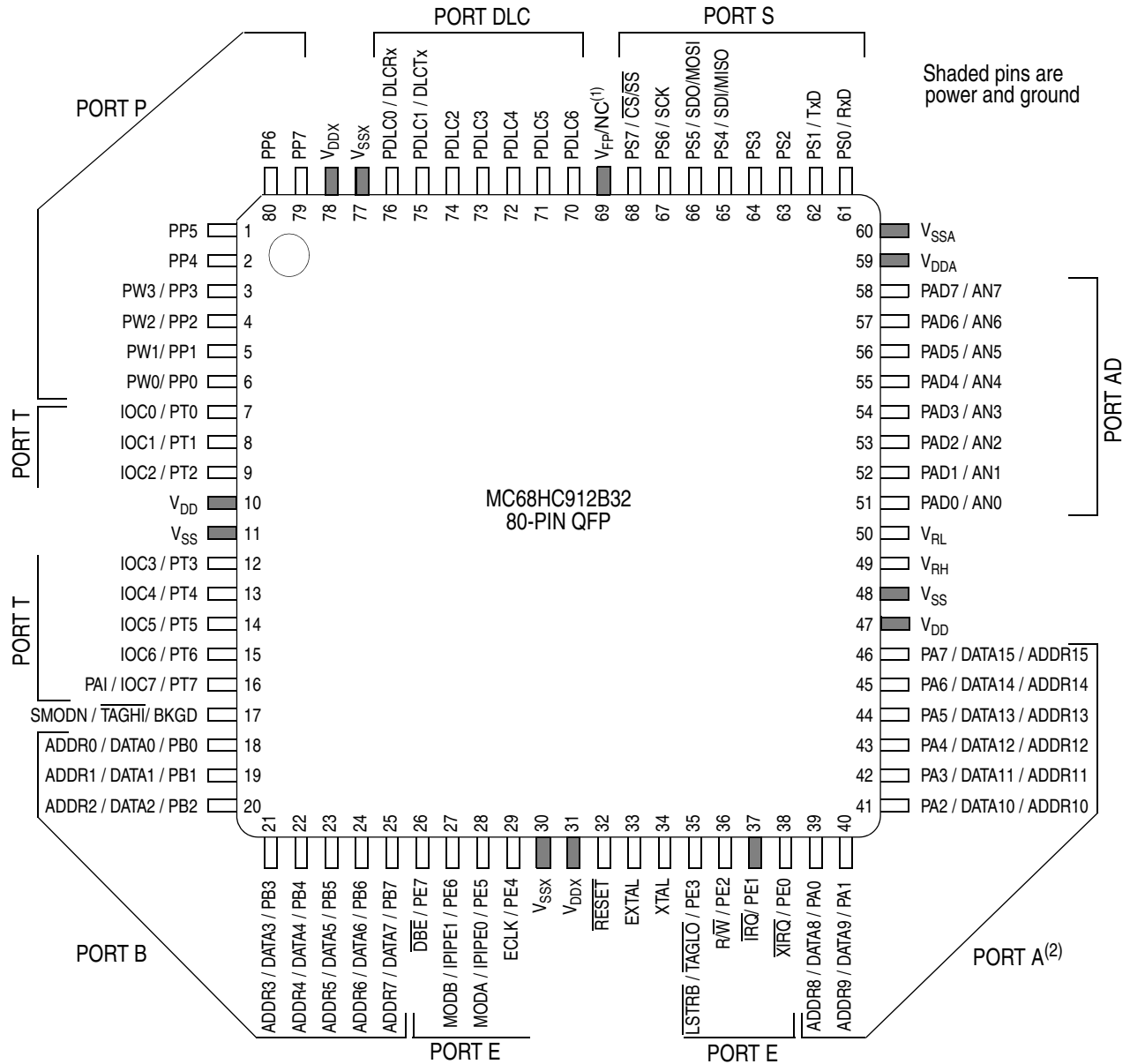
V_{DDX} and V_{SSX} are the external power supply and ground pins. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded.

1.6.2.3 V_{DDA} and V_{SSA}

V_{DDA} and V_{SSA} are the power supply and ground pins for the analog-to-digital converter (ATD). This allows the supply voltage to be bypassed independently.

1.6.2.4 V_{RH} and V_{RL}

V_{RH} and V_{RL} are the reference voltage pins for the ATD.



Notes:

1. Pin 69 is an NC (no connect) on the MC68HC12BE32.
2. In narrow mode, high and low data bytes are multiplexed in alternate bus cycles on port A.

Figure 1-3. Pin Assignments for MC68HC912B32 and MC68HC12BE32 Devices