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Freescale Semiconductor, Inc.

M68HC05 Microcontrollers

MC68HC705C8A
MC68HSC705C8A

Technical Data

MC68HC705C8A/D
Rev. 3, 3/2002

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MC68HC705C8A
MC68HSC705C8A

Technical Data

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Revision History

Date	Revision Level	Description	Page Number(s)
May, 2001	2.1	**1.7 Pin Functions** — Added description of programming voltage (V_{PP}) pin **1.7.2 V_{PP}**	29
		Removed note following **1.7.11 Port D I/O Pins (PD7 and PD5–PD0)**	33
		14.2 Introduction — Updated Motorola contact information	192
March, 2002	3	**14.7 44-Pin Quad Flat Pack (QFP)** — Corrected case outline drawing from Case #824E to Case #824A	195

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Appendix A. MC68HSC705C8A

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Section 1. General Description

1.1 Contents

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1.2 Introduction

The MC68HC705C8A, an enhanced version of the MC68HC705C8, is a member of the low-cost, high-performance M68HC05 Family of 8-bit microcontroller units (MCU). The MC68HSC705C8A, introduced in **Appendix A. MC68HSC705C8A**, is an enhanced, high-speed version of the MC68HC705C8A. The M68HC05 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the M68HC05 central processor unit (CPU) and are available with a variety of subsystems, memory sizes and types, and package types.

1.3 Features

Features of the MC68HC705C8A include:

- M68HC05 central processor unit (CPU)
- On-chip oscillator with crystal/ceramic resonator
- Memory-mapped input/output (I/O)
- Selectable memory configurations
- Selectable programmable and/or non-programmable computer operating properly (COP) watchdog timers
- Selectable port B external interrupt capability
- Clock monitor
- High current drive on pin C7 (PC7)
- 24 bidirectional I/O lines and 7 input-only lines
- Serial communications interface (SCI) system
- Serial peripheral interface (SPI) system
- Bootstrap capability
- Power-saving stop, wait, and data-retention modes
- Single 3.0-volt to 5.5-volt supply (2-volt data-retention mode)
- Fully static operation

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- Software-programmable external interrupt sensitivity
- Bidirectional $\overline{\text{RESET}}$ pin

NOTE: *A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{\text{RESET}}$ is active low. Any reference to voltage, current, or frequency specified in this document will refer to the nominal values. The exact values and their tolerance or limits are specified in* ***Section 13. Electrical Specifications****.*

1.4 Programmable Options

These options are programmable in the mask option registers:

- Enabling of port B pullup devices (see **9.5.2 Mask Option Register 1**)
- Enabling of non-programmable COP watchdog (see **9.5.3 Mask Option Register 2**)

These options are programmable in the option register (see **Figure 1-1**):

- One of four selectable memory configurations
- Programmable read-only memory (PROM) security[1]
- External interrupt sensitivity

Address: $1FDF

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RAM0	RAM1	0	0	SEC*		IRQ	0
Reset:	0	0	0	0	*	U	1	0

*Implemented as an EPROM cell

= Unimplemented U = Unaffected

Figure 1-1. Option Register (Option)

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the PROM difficult for unauthorized users.

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RAM0 — Random-Access Memory Control Bit 0

1 = Maps 32 bytes of RAM into page zero starting at address $0030. Addresses from $0020 to $002F are reserved. This bit can be read or written at any time, allowing memory configuration to be changed during program execution.

0 = Provides 48 bytes of PROM at location $0020–$005F.

RAM1 — Random-Access Memory Control Bit 1

1 = Maps 96 bytes of RAM into page one starting at address $0100. This bit can be read or written at any time, allowing memory configuration to be changed during program execution.

0 = Provides 96 bytes of PROM at location $0100.

SEC — Security Bit

This bit is implemented as an erasable, programmable read-only memory (EPROM) cell and is not affected by reset.

1 = Bootloader disabled; MCU operates only in single-chip mode

0 = Security off; bootloader can be enabled

IRQ — Interrupt Request Pin Sensitivity Bit

IRQ is set only by reset, but can be cleared by software. This bit can be written only once.

1 = $\overline{\text{IRQ}}$ pin is both negative edge- and level-sensitive.

0 = $\overline{\text{IRQ}}$ pin is negative edge-sensitive only.

Bits 5, 4, and 0 — Not used; always read 0

Bit 2 — Unaffected by reset; reads either 1 or 0

1.5 Block Diagram

Figure 1-2 shows the structure of the MC68HC705C8A.

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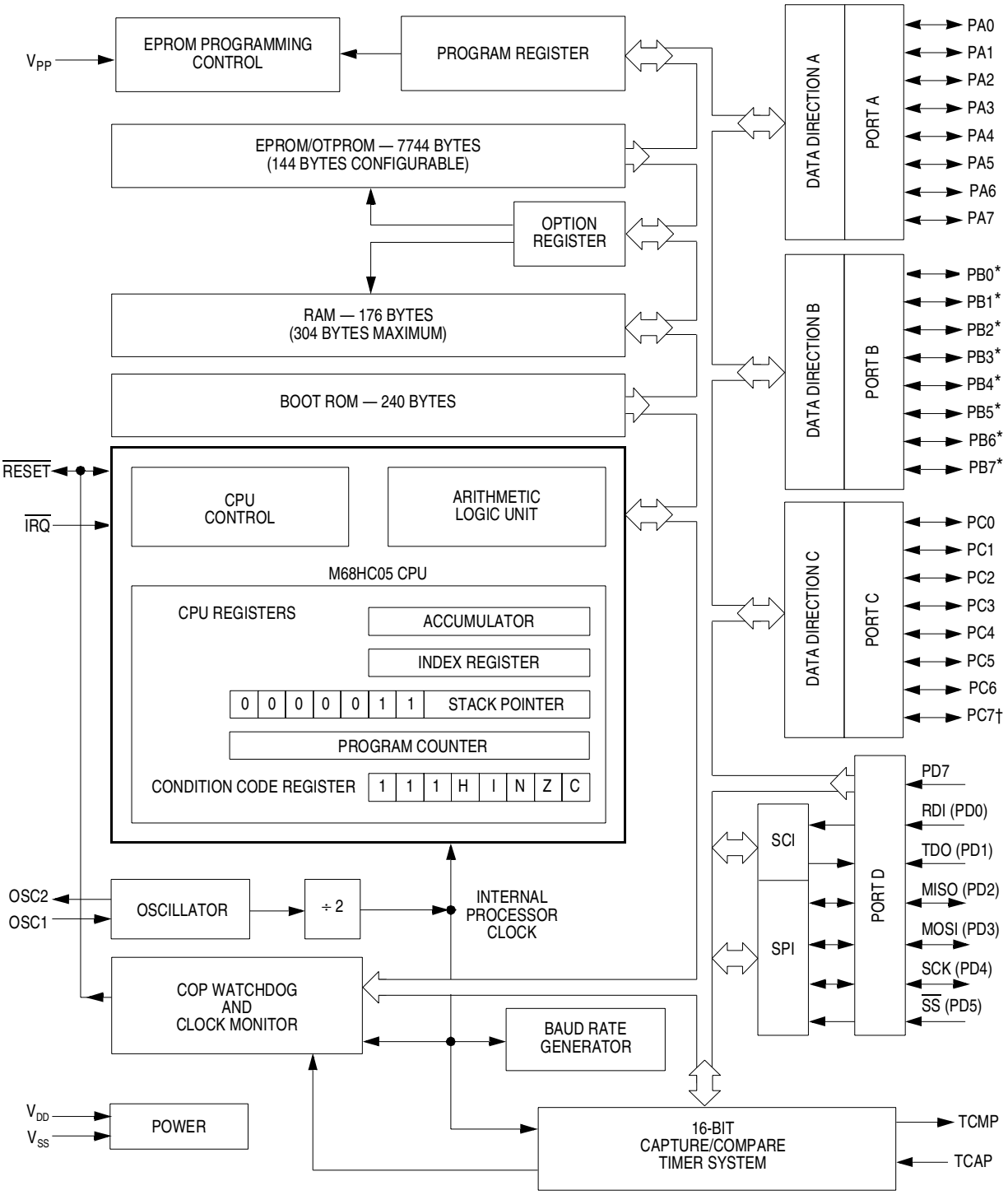

* Port B pins also function as external interrupts.
† PC7 has a high current sink and source capability.

Figure 1-2. MC68HC705C8A Block Diagram

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