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Freescale Semiconductor
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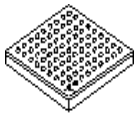
i.MX25 Applications Processor for Consumer and Industrial Products

Silicon Version 1.2

MCIMX25



Package Information
Plastic package
Case 5284 17 x 17 mm, 0.8 mm Pitch
Case 2107 12 x 12 mm, 0.5 mm Pitch

Ordering Information
See Table 1 on page 3 for ordering information.

1 Introduction

The i.MX25 multimedia applications processor has the right mix of high performance, low power, and integration to support the growing needs of the industrial and general embedded markets.

At the core of the i.MX25 is Freescale's fast, proven, power-efficient implementation of the ARM® 926EJ-S™ core, with speeds of up to 400 MHz. The i.MX25 includes support for up to 133 MHz DDR2 memory, integrated 10/100 Ethernet MAC, and two on-chip USB PHYs. The device is suitable for a wide range of applications, including the following:

- Graphical remote controls
- Human Machine Interface (HMI)
- Residential and commercial control panels
- Residential gateway (smart metering)
- Handheld scanners and printers
- Electronic point-of-sale terminals
- Patient-monitoring devices

Features of the i.MX25 processor include the following:

- Advanced power management—The heart of the device is a level of power management throughout the IC that enables the multimedia features and peripherals to achieve minimum system power consumption in active and various low-power modes. Power management techniques allow the designer to deliver a feature-rich product that requires levels of power far lower than typical industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX25 processor is boosted by a 16 KB L1 instruction and data cache system and further enhanced by an LCD controller (with alpha blending), a CMOS image sensor interface, an A/D controller (integrated touchscreen controller), and a programmable Smart DMA (SDMA) controller.
- 128 Kbytes on-chip SRAM—The additional 128 Kbyte on-chip SRAM makes the device ideal for eliminating external RAM in applications with small footprint RTOS. The on-chip SRAM allows the designer to enable an ultra low power LCD refresh.
- Interface flexibility—The device interface supports connection to all common types of external memories: MobileDDR, DDR, DDR2, NOR Flash, PSRAM, SDRAM and SRAM, NAND Flash, and managed NAND.
- Increased security—Because the need for advanced security for tethered and untethered devices continues to increase, the i.MX25 processor delivers hardware-enabled security features that enable secure e-commerce, Digital Rights Management (DRM), information encryption, robust tamper detection, secure boot, and secure software downloads.
- On-chip PHY—The device includes an HS USB OTG PHY and FS USB HOST PHY.
- Fast Ethernet—For rapid external communication, a Fast Ethernet Controller (FEC) is included.
- i.MX25 only supports Little Endian mode.

1.1 Ordering Information

Table 1 provides ordering information for the i.MX25.

Table 1. Ordering Information

Description	Part Number	Silicon Version	Projected Temperature Range (°C)	Package	Ballmap
i.MX253	MCIMX253DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DVM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CVM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253DJM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4	1.1	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CJM4	1.1	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253DJM4A	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4A	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257DJM4AR2	1.2	–20 to +70	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX253	MCIMX253CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX258	MCIMX258CJM4A	1.2	–40 to +85	17 x 17 mm, 0.8 mm pitch, MAPBGA-400	Table 103
i.MX257	MCIMX257CJN4A	1.2	–40 to +85	12 x 12mm, 0.5mm pitch, MAPBGA-347	Table 107

Table 2 shows the functional differences between the different parts in the i.MX25 family.

Table 2. i.MX25 Parts Functional Differences

Features	MCIMX253	MCIMX257	MCIMX258
Core	ARM 926EJ-S	ARM 926EJ-S	ARM 926EJ-S
CPU Speed	400 MHz	400 MHz	400 MHz
L1 I/D Cache	16K I/D	16K I/D	16K I/D
On-chip SRAM	128 KB	128 KB	128 KB
PATA/CE-ATA	Yes	Yes	Yes
LCD Controller	Yes	Yes	Yes
Touchscreen	—	Yes	Yes
CSI	—	Yes	Yes
FlexCAN (2)	—	Yes	Yes
ESAI	—	Yes	Yes
SIM (2)	—	Yes	Yes
Security	—	—	Yes
10/100 Ethernet	Yes	Yes	Yes
HS USB 2.0 OTG + PHY	Yes	Yes	Yes
HS USB 2.0 Host + PHY	Yes	Yes	Yes
12-bit ADC	Yes	Yes	Yes
SD/SDIO/MMC (2)	Yes	Yes	Yes
External Memory Controller	Yes	Yes	Yes
I^2C (3)	Yes	Yes	Yes
SSI/I2S (2)	Yes	Yes	Yes
CSPI (2)	Yes	Yes	Yes
UART (5)	Yes	Yes	Yes

1.2 Block Diagram

Figure 1 shows the simplified interface block diagram.

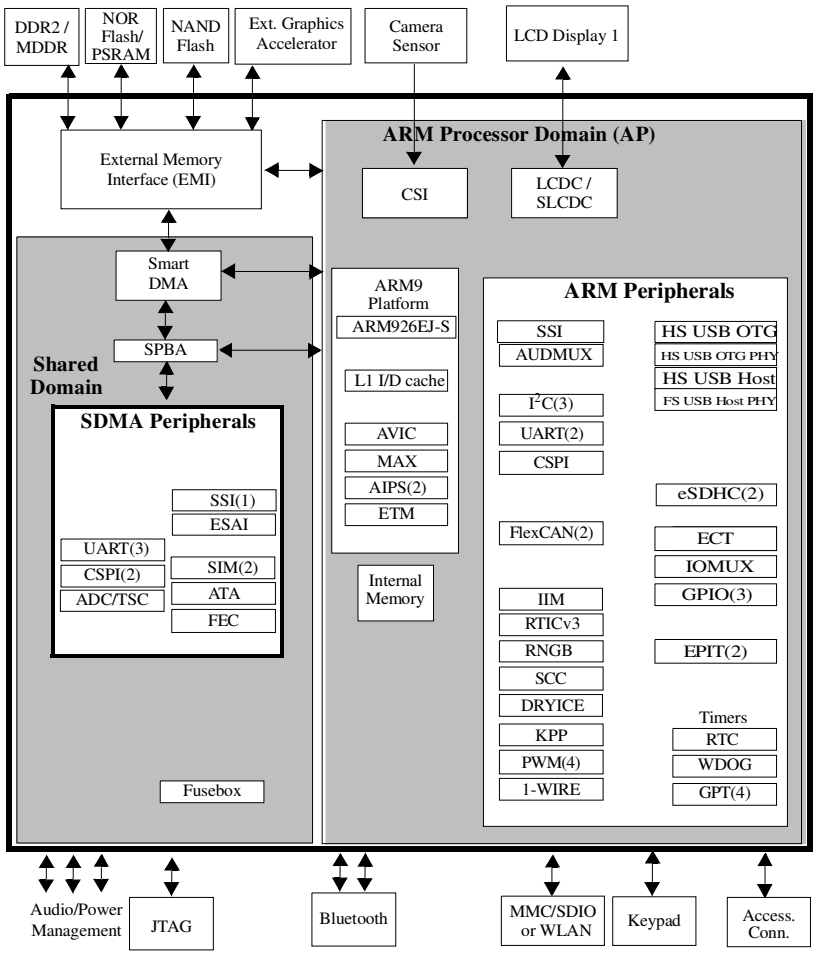


Figure 1. i.MX25 Simplified Interface Block Diagram

2 Features

Table 3 describes the digital and analog modules of the device.

Table 3. i.MX25 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
1-WIRE	1-Wire Interface	Connectivity peripherals	1-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example: Dallas DS2502.
ARM9 or ARM926	ARM926 platform and memory	ARM	The ARM926 Platform consists of the ARM 926EJ-S core, the ETM real-time debug modules, a 5x5 Multi-Layer AHB crossbar switch, and a “primary AHB” complex. It contains the 16 Kbyte L1 instruction cache, 16 Kbyte L1 data cache, 32 Kbyte ROM and 128 Kbyte RAM.
ATA	ATA module	Connectivity peripherals	The ATA module is an AT attachment host interface. Its main use is to interface with IDE hard disc drives and ATAPI optical disc drives. It interfaces with the ATA device over a number of ATA signals.
AUDMUX	Digital audio mux	Multimedia peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals, and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.
CCM	Clock control module	Clocks	This block generates all clocks for the iMX25 system. The CCM also manages the ARM926 Platform's low-power modes (wait, stop, and doze) by disabling peripheral clocks appropriately for power conservation.
CSPI(3)	Configurable serial peripheral interface	Connectivity peripherals	This module is a serial interface equipped with data FIFOs. Each master/slave-configurable SPI module is capable of interfacing to both serial port interface master and slave devices. The CSPI ready (SPI_RDY) and Slave Select (SS) control signals enable fast data communication with fewer software interrupts.
DRYICE	DryIce module	Security	DryIce provides volatile key storage for Point-of-Sale (POS) terminals, and a trusted time source for Digital Rights Management (DRM) schemes. Several tamper-detect circuits are also provided to support key erasure and time invalidation in the event of tampering. Alarms and/or interrupts can also assert if tampering is detected. DryIce also includes a Real Time clock (RTC) that can be used in secure and non-secure applications.
EMI	External memory interface	Connectivity peripherals	The External Memory Interface (EMI) module provides access to external memory for the ARM and other masters. It is composed of four main submodules: • M3IF provides arbitration between multiple masters requesting access to the external memory. • Enhanced SDRAM/LPDDR memory controller (ESDCTL) interfaces to DDR2 and SDR interfaces. • NAND Flash controller (NFC) provides an interface to NAND Flash memories. • Wireless External Interface Memory controller (WEIM) interfaces to NOR Flash and PSRAM.

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EPIT(2)	Enhanced periodic interrupt timer	Timer peripherals	Each Enhanced Periodic Interrupt Timer (EPIT) is a 32-bit set-and-forget timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler to adjust the input clock frequency to the required time setting for the interrupts, and the counter value can be programmed on the fly.
ESAI	Enhanced serial audio interface	Connectivity peripherals	ESAI provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator.
eSDHC(2)	Enhanced multimedia card/ secure digital host controller	Connectivity peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to the SD host controller standard specification version 2.0 • Compatible with the JEDEC MMC system specification version 4.2 • Compatible with the SD memory card specification version 2.0 • Compatible with the SDIO specification version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz and 52 MHz • Up to 200-Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416-Mbps data transfer for MMC cards using eight parallel data lines
FEC	Fast ethernet controller	Connectivity peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10- and 100-Mbps Ethernet networks compliant with IEEE 802.3® standard. An external transceiver interface and transceiver function are required to complete the interface to the media
FlexCAN(2)	Controller area network module	Connectivity peripherals	The Controller Area Network (CAN) protocol is primarily designed to be used as a vehicle serial data bus running at 1 MBps.
GPIO(4)	General purpose I/O modules	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT(4)	General purpose timers	Timer peripherals	Each GPT is a 32-bit free-running or set-and-forget mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in set-and-forget mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
I^2C(3)	I^2C module	Connectivity peripherals	Inter-IC Communication (I^2C) is an industry-standard, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. I^2C is suitable for applications requiring occasional communications over a short distance between many devices. The interface operates up to 100 kbps with maximum bus loading and timing. The I^2C system is a true multiple-master bus, including arbitration and collision detection that prevents data corruption if multiple devices attempt to control the bus simultaneously. This feature supports complex applications with multiprocessor control and can be used for rapid testing and alignment of end products through external connections to an assembly-line computer.
IIM	IC Identification Module	Security	The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, and various control signals requiring a fixed value.
IOMUX	I/O multiplexer	Pins	Each I/O multiplexer provides a flexible, scalable multiplexing solution: • Up to eight output sources multiplexed per pin • Up to four destinations for each input pin • Unselected input paths are held at constant level for reduced power consumption
KPP	Keypad port	Connectivity peripherals	KPP can be used for either keypad matrix scanning or general purpose I/O.
LCDC	LCD Controller	Multimedia peripherals	LCDC provides display data for external gray-scale or color LCD panels. LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.
MAX	ARM platform multilayer AHB crossbar switch	ARM platform	MAX concurrently supports up to five simultaneous connections between master ports and slave ports. MAX allows for concurrent transactions to occur from any master port to any slave port.
PWM(4)	Pulse width modulation	Connectivity peripherals	The Pulse-Width Modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4x16 data FIFO to generate sound.
SDMA	Smart DMA engine	System control	The SDMA provides DMA capabilities inside the processor. It is a shared module that implements 32 DMA channels.
SIM(2)	Subscriber identity module interface	Connectivity peripherals	The SIM is an asynchronous interface designed to facilitate communication with SIM cards or pre-paid phone cards. This module was designed based on the ISO7816 standard; however, the module does require an external companion controller to allow communication to certain smart cards or to pass certain certifications, such as EMV. The SIM supports only 11 and 12ETU cards and can communicate at the default rate, which is obtained at Fi/Di=372/1. An external companion controller is required to support cards aligned on 10.8 or 11.8ETU and to support other rates, such as those obtained at Fi/Di=372/2 and Fi/Di=372/4.
SJC	Secure JTAG interface	System control peripherals	The System JTAG Controller (SJC) provides debug and test control with maximum security.

Table 3. i.MX25 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SLCD	Smart LCD controller	Multimedia peripherals	The SLCDC module transfers data from the display memory buffer to the external display device.
SPBA	Shared peripheral bus arbiter	System control	The SPBA controls access to the shared peripherals. It supports shared peripheral ownership and access rights to an owned peripheral.
SSI(2)	I2S/SSI/AC97 interface	Connectivity peripherals	The SSI is a full-duplex serial port that allows the processor to communicate with a variety of serial protocols, including the Freescale Semiconductor SPI standard and the inter-IC sound bus standard (I2S). The SSIs interface to the AUDMUX for flexible audio routing.
TSC (and ADC)	Touchscreen controller (and A/D converter)	Multimedia peripherals	The touchscreen controller and associated Analog-to-Digital Converter (ADC) together provide a resistive touchscreen solution. The module implements simultaneous touchscreen control and auxiliary ADC operation for temperature, voltage, and other measurement functions.
UART(5)	UART interface	Connectivity peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, one or two stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher maximum baud rate than the 1.875 MHz specified by the TIA/EIA-232-F standard and previous Freescale UART modules. 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA-1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification, the OTG supplement, and the ULPI 1.0 Low Pin Count specification. The module has DMA capabilities for handling data transfer between internal buffers and system memory. An OTG HS PHY and HOST FS PHY are also integrated.

2.1 Special Signal Considerations

Special signal considerations are listed in Table 4. The package contact assignment is found in Section 4, "Package Information and Contact Assignment." Signal descriptions are provided in the reference manual.

Table 4. Signal Considerations

Signal	Description
BAT_VDD	DryIce backup power supply input.
CLK0	Clock-out pin; renders the internal clock visible to users for debugging. The clock source is controllable through CRM registers. This pin can also be configured (through muxing) to work as a normal GPIO.
CLK_SEL	Used to select the ARM clock source from MPLL out or from external EXT_ARMCLK. In normal operation, CLK_SEL should be connected to GND.
EXT_ARMCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.

Table 4. Signal Considerations (continued)

Signal	Description
MESH_C, MESH_D	Wire-mesh tamper detect pins that can be routed at the PCB board to detect attempted tampering of a protected wire. When security measures are implemented, MESH_C should be pulled-up or connected to NVCC_DRYICE and triggers a tamper event when floating or when connected to MESH_D. MESH_D should be pulled-down or connected to GND and triggers an event when floating or connected to MESH_C. These pins can be left unconnected if the DryIce security features are not being used.
NVCC_DRYICE	This is the DryIce power supply output. The supply source is QVDD when the i.MX25 is in run mode. When i.MX25 is in reduced power mode, the DryIce supply source is the BATT_VDD supply. This pin can be used to power external DryIce components (external tamper detect, wire-mesh tamper detect). In order to guarantee the power-loss protection feature which guarantees that RTC and/or secure keys be maintained after power-off an external capacitor no less than 4 µF must be connected to this supply output pin. A 4.7 µF capacitor is recommended.
OSC_BYP	The 32 kHz oscillator bypass-control pin. If this signal is pulled down, then OSC32K_EXTAL and OSC32K_XTAL analog pins should be tied to the external 32.768 kHz crystal circuit. If on the other hand the signal is pulled up, then the external 32 kHz oscillator output clock must be connected to OSC32K_EXTAL analog pin, and OSC32K_XTAL can be no connect (NC).
OSC32K_EXTAL OSC32K_XTAL	These analog pins are connected to an external 32 kHz CLK circuit depending on the state of OSC_BYP pin (see the description of OSC_BYP under the preceding bullet). The 32 kHz reference CLK is required for normal operation.
POWER_FAIL	An interrupt from PMIC, which should be connected to a low-battery detection circuit. This signal is internally connected to an on-chip 100 kΩ pull-down device. If there is no low-battery detection, then users can tie this pin to GND through a pull-down resistor, or leave the signal as NC. This pin can also be configured to work as a normal GPIO.
REF	External ADC reference voltage. REF may be tied to GND if the user plans to only use the internally generated 2.5 V reference supply.
SJC_MOD	Must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.
TAMPER_A, TAMPER _B	DryIce external tamper detect pins, active high. If TAMPER_A or TAMPER_B is connected to NVCC_DRYICE, then external tampering is detected. These pins can be left unconnected if the DryIce security features are not being used.
TEST_MODE	For Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
UPLL_BYPCLK	Primarily for Freescale factory use. There is no internal on-chip pull-up/down on this pin, so it must be externally connected to GND or VDD. Aside from factory use, this pin can also be configured (through muxing) to work as a normal GPIO.
USBPHY1_RREF	Determines the reference current for the USB PHY1 bandgap reference. An external 10 kΩ 1% resistor to GND is required.
USBPHY2_DM USBPHY2_DP	The output impedance of these signals is expected at 10 Ω. It is recommended to also have on-board 33 Ω series resistors (close to the pins).

3 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the i.MX25.

3.1 i.MX25 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC.

3.1.1 DC Absolute Maximum Ratings

Table 5 provides the DC absolute maximum operating conditions.

CAUTION

- Stresses beyond those listed under Table 5 may cause permanent damage to the device.
- Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Table 5 gives stress ratings only—functional operation of the device is not implied beyond the conditions indicated in Table 6.

Table 5. DC Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage	QV_{DD}	–0.5	1.52	V
Supply voltage (level shift i/o)	$V_{DDIOmax}$	–0.5	3.6	V
ESD damage immunity:	V_{esd}			V
Human body model (HBM)		—	2500	
Charge device model (CDM)		—	400	
Machine model (MM)		—	200	
Input voltage range	V_{Imax}	–0.5	NV_{DD} + 0.3	V
Storage temperature range	$T_{storage}$	–40	105	°C

3.1.2 DC Operating Conditions

Table 6 provides the DC recommended operating conditions.

Table 6. DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Core supply voltage (at 266 MHz)	QV_{DD}	1.15	1.34	1.52	V
Core supply voltage (at 400 MHz)	QV_{DD}	1.38	1.45	1.52	V
Coin battery[1] BAT_VDD	V_{DD_BAT}	1.15	—	1.55	V
I/O supply voltage, GPIO NFC,CSI,SDIO	NV_{DD_GPIO1}	1.75	—	3.6	V

Table 6. DC Operating Conditions (continued)

Parameter	Symbol	Min.	Typ.	Max.	Units
I/O supply voltage, GPIO CRM,LCDC,JTAG,MISC	NV_{DD_GPIO2}	3.0	3.3	3.6	—
I/O supply voltage DDR (Mobile DDR mode) EMI1, EMI2	NV_{DD_MDDR}	1.75	—	1.95	V
I/O supply voltage DDR (DDR2 mode) EMI1,EMI2	NV_{DD_DDR2}	1.75	—	1.9	V
I/O supply voltage DDR (SDRAM mode) EMI1,EMI2	NV_{DD_SDRAM}	1.75	—	3.6	V
Supply of USBPHY1 (HS) USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD,USBPHY1_VDDA	$V_{DD\_usbphy1}$	3.17	3.3	3.43	V
Supply of USBPHY2 (FS) USBPHY2_VDD	$V_{DD\_usbphy2}$	3.0	3.3	3.6	V
Supply of OSC24M OSC24M_VDD	V_{DD_OSC24M}	3.0	3.3	3.6	V
Supply of PLL MPLL_VDD,UPLL_VDD	V_{DD_PLL}	1.4	—	1.65	V
Supply of touchscreen ADC NVCC_ADC	V_{DD_tsc}	3.0	3.3	3.6	V
External reference of touchscreen ADC Ref	Vref	2.5	V_{DD_tsc}	V_{DD_tsc}	V
Fusebox program supply voltage FUSE_VDD[2]	$FUSEV_{DD}$ (program mode)	3.3 ± 5%	—	3.6	V
Supply output[3] NVCC_DRYICE	$V_{DD\_}$	1.0	—	1.55	V
Operating ambient temperature	T_A	–40	—	85	°C

1 V_{DD_BAT} must always be powered by battery in security application. In non-security case, V_{DD_BAT} can be connected to QV_{DD}.

2 The fusebox read supply is connected to supply of the full speed USBPHY2_VDD. FUSE_VDD is only used for programming. It is recommended that FUSE_VDD be connected to ground when not being used for programming. See Table 7 for current parameters.

3 NVCC_DRYICE is a supply output. An external capacitor no less than 4 µF must be connected to it. A 4.7 µF capacitor is recommended.

3.1.3 Fusebox Supply Current Parameters

Table 7 lists the fusebox supply current parameters.

Table 7. Fusebox Supply Current Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units
eFuse program current[1] Current to program one eFuse bit The associated VDD_FUSE supply = 3.6 V	$I_{program}$	26	35	62	mA
eFuse read current[2] Current to read an 8-bit eFuse word	I_{read}	—	12.5	15	mA

1 The current $I_{program}$ is during program time ($t_{program}$).

2 The current I_{read} is present for approximately 50 ns of the read access to the 8-bit word.

3.1.4 Interface Frequency Limits

Table 8 provides information for interface frequency limits.

Table 8. Interface Frequency Limits

Parameter	Min.	Typ.	Max.	Units
JTAG: TCK Frequency of Operation	DC	5	10	MHz
OSC24M_XTAL Oscillator	—	24	—	MHz
OSC32K_XTAL Oscillator	—	32.768	—	kHz

Table 9 provides the recommended external crystal specifications.

Table 9. Recommended External Crystal Specifications

	24 MHz	32.768 kHz
Frequency Tolerance	<= ± 30 ppm	<= ± 30 ppm
ESR	< 80 Ω	50 K~60 K
Load Capacitor	8 pF–12 pF	6 pF–8 pF (12 pF–16 pF on each pin)
Shunt Capacitor	< 7 pF	1 pF
Drive Level	> 150 µW	> 1 µW

Table 10 provides the recommended external reference clock oscillator specifications (when reference is used from an external clock source).

Table 10. Recommended External Reference Clock Specifications

	24 MHz	32.768 kHz
V_{OH}	min = 0.7* VDD	min = 0.7* VDD
V_{OL}	max = 0.3* VDD	max = 0.3* VDD
Frequency Tolerance	= 30 ppm	= 30 ppm

Table 10. Recommended External Reference Clock Specifications (continued)

T_{RISE}	1% T_{CLOCK}	1% T_{CLOCK}
T_{FALL}	1% T_{CLOCK}	1% T_{CLOCK}
Duty Cycle	50%	50%

3.1.5 USB_PHY Current Consumption

Table 11 provides information for USB_PHY current consumption.

Table 11. USB PHY Current Consumption[1]

Parameter	Conditions		Typ. (@Typ. Temp)	Max. (@Max. Temp)	Unit
Analog supply USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA (3.3 V)	Full speed	Rx	11.4	—	mA
		Tx	22,6	—	
	High speed	Rx	21.5	—	
		Tx	33.8	—	
	Suspend	—	0.6		µA
Analog supply USBPHY2_VDD (3.3 V)	Full Speed	Rx	120	—	µA
		Tx	25	—	mA
	Low Speed	Rx	252	—	µA
		Tx	5.5	—	mA
All supplies	Suspend		50	100	µA

1 Values must be verified

3.1.6 Power Modes

Table 12 describes the core, clock, and module settings for the different power modes of the processor.

Table 12. i.MX25 Power Mode Settings

Core/Clock/Module	Power Mode				
	Doze	Wait	Stop/Sleep[1]	Run (266 MHz)	Run (400 MHz)
ARM core	Platform clock is off	In wait-for-interrupt mode	—	Active @ 266 MHz	Active @ 400 MHz
Well bias	On	Off	On	Off	Off
MCU PLL	On	On	Off	On	On
USB PLL	Off	Off	Off	On	On
OSC24M	On	On	Off	On	On
OSC32K	On	On	On	On	On
Other modules	Off	Off	Off	On	On

[1] Sleep mode differs from stop mode in that the core voltage is reduced to 1 V.

Table 13 shows typical current consumption for the various power supplies under the various power modes.

Table 13. i.MX25 Power Mode Current Consumption

Power Group	Power Supplies	Voltage Setting	Current Consumption for Power Modes[1]			
			Doze	Wait	Stop	Sleep
NVCC_EMI	NVCC_EMI1 NVCC_EMI2	3.0 V	5 µA	3.15 µA	3.51 µA	3.61 µA
NVCC_CRM	NVCC_CRM	3.0 V	1.15 µA	4.31 µA	0.267 µA	0.32 µA
NVCC_ OTHER	NVCC_SDIO NVCC_CSI NVCC_NFC NVCC_JTAG NVCC_LCDC NVCC_MISC	3.0 V	31.2 µA	29.5 µA	31.7 µA	32.1 µA
NVCC_ADC	NVCC_ADC	3.0 V	163 µA	3.25 µA	1.14 µA	0.871 µA
OSC24M	OSC24M_ VDD	3.0 V	906 µA	903 µA	10.2 µA mA	10.5 µA
PLL_VDD	MPLL_VDD UPLL_VDD	1.4 V	6.83 mA	6.83 mA	38.9 µA	39.1 µA
QVDD	QVDD	1.15 V	8.79 mA	11.28 mA	842 µA	665 µA
USBPHY1_ VDDA	USBPHY1_ VDDA	3.17 V	240 µA	240 µA	241 µA	242 µA
USBPHY1_ VDDA_VBIAS	USBPHY1_ VDDA_VBIAS	3.17 V	0.6 µA	1.46 µA	0.328 µA	0.231 µA
USBPHY1_ UPLL_VDD	USBPHY1_ UPLL_VDD	3.17 V	201 µA	201 µA	191 µA	191 µA
USBPHY2	USBPHY2_ VDD	3.0 V	158 µA	0158 µA	164 µA	164 µA

[1] Values are typical, under typical use conditions.

In the reduced power mode, shown in Table 14, the i.MX25 is powered down, while the RTC clock and the secure keys (in secure-use case), remain operational. BAT_VDD is tied to a battery while all other supplies are turned off.

NOTE

In this low-power mode, i.MX25 cannot be woken up with an interrupt; it must be powered back up before it can detect any events.

Table 14. iMX25 Reduced Power Mode Current Consumption

Power Group	Power Supply	Voltage Setting	Typical Current Consumption
BAT_VDD	BAT_VDD	1.15 V	9.95 µA
		1.55 V	12.6 µA

3.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any i.MX25 board design must comply with the power-up and power-down sequence guidelines given in this section to ensure reliable operation of the device. Recommended power-up and power-down sequences are given in the following subsections.

CAUTION

Deviations from the guidelines in this section may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX25 (worst-case scenario)

NOTE

For security applications, the coin battery must be connected during both power-up and power-down sequences to ensure that security keys are not unintentionally erased.

3.2.1 Power-Up Sequence

For those users that are not using DryIce/SRTC, the following power-up sequence is recommended:

1. Assert power on reset (POR).
2. Turn on QVDD digital logic domain supplies.
3. Turn on NVCCx digital I/O power supplies after QVDD is stable.
4. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed), after all NVCCx digital I/O supplies are stable.
5. Negate the POR signal.

NOTE

- The user is advised to connect FUSEVDD to GND except when fuses are programmed, to prevent unintentional blowing of fuses.
- Other power-up sequences may be possible; however, the above sequence has been verified and is recommended.
- There is a 1 ms minimum time between supplies coming up, and a 1 ms minimum time between POR_B assert and de-assert.
- The dV/dT should be no faster than 0.25 V/µs for all power supplies, to avoid triggering ESD circuit.

Figure 2 shows the power-up sequence diagram. After POR_B is asserted, Core VDD and NVDDx can be powered up. After Core VDD and NVDDx are stable, the analog supplies can be powered up.

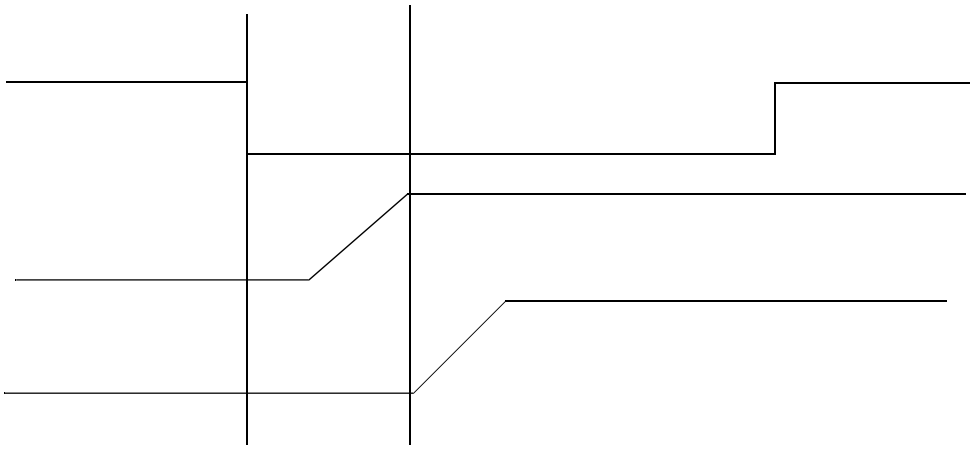


Figure 2. Power-Up Sequence Diagram

3.2.2 Power-Down Sequence

There are no special requirements for the power-down sequence. All power supplies can be shut down at the same time.

3.2.3 SRTC DryIce Power-Up/Down Sequence

In order to guarantee DryIce power-loss protection, including retention of SRTC time data during power down, users must do the following:

- Place a proper capacitor on the NVCC_DRYICE output pin, and
- Implement the below power-up/down sequence

1. Assert power on reset (POR).
2. Turn on NVCC_CRM.
3. Turn on QVDD digital logic domain supplies for not less than 1 ms and not more than 32 ms, after NVCC_CRM reaches 90% of 3.3 V.

NOTE

This is to guarantee that POR is stable already at NVCC_CRM/QVDD power domain interface before QVDD is turned on, and POR instantly propagates to QVDD domain after QVDD is turned on.

4. Turn on other NVCCx digital I/O power supplies for not less than 1 ms and not more than 32 ms, after QVDD reaches 90% of 1.2 V.
5. Turn on all other analog power supplies, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, OSC24M_VDD, MPPLL_VDD, UPLL_VDD, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed) for not less than 1 ms and not more than 32 ms, after NVCCx reaches 90% of 3.3 V.

NOTE

This is to guarantee that analog peripherals can get properly initialized (reset) values from QVDD domain and NVCCx domain.

6. Negate the POR signal for at least 90 µs after all previous steps.

NOTE

- This is to guarantee that both POR logic and clocks are stable inside the i.MX25 chip, before POR is removed.
- The dV/dT should be no faster than 0.25 V/us for all power supplies, to avoid triggering ESD circuit.

In addition, the following power-down sequence is recommended:

1. Turn off power for analog parts, including USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, NVCC_ADC, and FUSEVDD (FUSEVDD is tied to GND if fuses are not programmed).
2. Turn off QVDD.
3. Turn off NVCCx, PLL, OSC, and other powers.

NOTE

The power-down steps can be executed simultaneously, or very shortly one after another.

3.3 Power Characteristics

Table 15 shows values representing maximum current numbers for the i.MX25 under worst case voltage and temperature conditions. These values are derived from the i.MX25 with core clock speed up to 400 MHz. Additionally, no power saving techniques such as clock gating were implemented when measuring these values. Common supplies are bundled according to the i.MX25 power-up sequence requirements. Peak numbers are provided for system designers so that the i.MX25 power supply requirements are satisfied during startup and transient conditions. Freescale recommends that system

current measurements are taken with customer-specific use-cases to reflect the normal operating conditions in the end system.

Table 15. Power Consumption

Power Supply	Voltage (V)	Max Current (mA)
QVDD	1.52	360
NVCC_EMI1, NVCC_EMI2	1.9	30
NVCC_CRM, NVCC_SDIO, NVCC_CSI, NVCC_NFC, NVCC_JTAG, NVCC_LCDC, NVCC_MISC	3.6	110
MPLL_VDD, UPLL_VDD	1.65	20
USBPHY1_VDDA_BIAS, USBPHY1_UPLL_VDD, USBPHY1_VDDA, USBPHY2_VDD, OSC24M_VDD, NVCC_ADC	3.3	40
FUSE_VDD[1]	3.6	62
BATT_VDD	1.55	0.030

[1] The FUSE_VDD rail is connected to ground. it only needs a voltage if the system fuse burning is needed.

The method for obtaining the maximum current is as follows:

1. Measure the worst case power consumption on individual rails using directed test on i.MX25.
2. Correlate the worst case power consumption power measurements with the worst case power consumption simulations.
3. Combine common voltage rails based on the power supply sequencing requirements (add the worst case power consumption on each rail within some test cases from several test cases run, to maximize different rails in the power group).
4. Guard the worst case numbers for temperature and process variation.
5. The sum of individual rails is greater than the real world power consumption, since a real system does not typically maximize the power consumption on all peripherals simultaneously.
6. BATT_VDD current is measured when the system is in reduced power mode maintaining the RTC. When the system is in run mode, QVDD is used to supply the DryIce, so this current becomes negligible. See Table 12, for more details on the power modes.

NOTE

The values mentioned above should not be taken as a typical max run data for specific use cases. These values are Absolute MAX data. Freescale recommends that the system current measurements are taken with customer-specific use-cases to reflect normal operating conditions in the end system.

3.4 Thermal Characteristics

The thermal resistance characteristics for the device are given in Table 16. These values are measured under the following conditions:

- Two-layer substrate
- Substrate solder mask thickness: 0.025 mm
- Substrate metal thicknesses: 0.016 mm
- Substrate core thickness: 0.200 mm
- Core through I.D: 0.118 mm, Core through plating 0.016 mm.
- Flag: Trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold compound: Generic mold compound; k = 0.9 W/m K

Table 16. Thermal Resistance Data

Rating	Condition	Symbol	Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	55	°C/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	33	°C/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	46	°C/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	29	°C/W
Junction to boards[2]	—	$R_{\theta JB}$	22	°C/W
Junction to case (top)[3]	—	$R_{\theta JCtop}$	13	°C/W
Junction to package top[4]	Natural convection	Ψ_{JT}	2	°C/W

1 Junction-to-ambient thermal resistance determined per JEDC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-board thermal resistance determined per JEDC JESD51-8. Thermal test board meets JEDEC specification for this package.

3 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, this thermal characterization parameter is written as Psi-JT.

3.5 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (mDDR), double data rate (DDR2), or synchronous dynamic random access memory (SDRAM)
- General purpose I/O (GPIO)

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output. The association is shown in the “Signal Multiplexing” chapter of the reference manual.

3.5.1 DDR I/O DC Parameters

The DDR pad type is configured by the IOMUXC_SW_PAD_CTL_GRP_DDRTYPE register (see the External Signals and Pin Multiplexing chapter of the *i.MX25 Reference Manual* for details).

3.5.1.1 DDR_TYPE = 00 Standard Setting DDR I/O DC Parameters

Table 17 shows the I/O parameters for mobile DDR. These settings are suitable for mDDR and DDR2 1.8V (± 5%) applications.

Table 17. Mobile DDR I/O DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage	Voh	I_{OH} = –1mA I_{OH} = Specified Drive	OVDD – 0.08 0.8 × OVDD	—	—	V
Low-level output voltage	Vol	I_{OL} = 1mA I_{OL} = Specified Drive	—	—	0.08 0.2 × OVDD	V
High-level output current	I Ioh	Voh = 0.8 × OVDDV Standard Drive High Drive Max. Drive	 –3.6 –7.2 –10.8	—	—	 mA
Low-level output current	I Iol	Vol = 0.2 × OVDDV Standard Drive High Drive Max. Drive	 3.6 7.2 10.8	—	—	 mA
High-level DC CMOS input voltage	VIH	—	0.7 × OVDD	OVDD	OVDD+0.3	V
Low-level DC CMOS input voltage	VIL	—	–0.3	0	0.3 × OVDD	V
Differential receiver VTH+	VTH+	—		—	100	mV
Differential receiver VTH-	VTH-		–100	—	—	mV
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current	Icc-ovdd	VI = OVDD or 0	—	—	990	nA
High-impedance core supply current	Icc-vddi	VI = VDD or 0	—	—	1220	nA

3.5.1.2 DDR_TYPE = 01 SDRAM I/O DC Parameters

Table 18 shows the DC I/O parameters for SDRAM.

Table 18. SDRAM DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage	Voh	Ioh = Specified Drive (Ioh = –4, –8, –12, –16mA)	2.4	—	—	V
Low-level output voltage	Vol	Ioh = Specified Drive (Ioh = 4, 8, 12, 16mA)	—	—	0.4	V
High-level output current	I Ioh	Standard Drive High Drive Max. Drive	–4.0 –8.0 –12.0	—	—	mA
Low-level output current	I Iol	Standard Drive High Drive Max. Drive	4.0 8.0 12.0	—	—	mA
High-level DC input voltage	VIH	—	2.0	—	3.6	V
Low-level DC input voltage	VIL	—	–0.3 V	—	0.8	V
Input current (no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	150 80	nA
High-impedance I/O supply current	Icc-ovdd	VI = OVDD or 0	—	—	1180	nA
High-impedance core supply current	Icc-vddi	VI = VDD or 0	—	—	1220	nA

3.5.1.3 DDR_TYPE = 10 Max Setting DDR I/O DC Parameters

Table 19 shows the I/O parameters for DDR2 (SSTL_18).

Table 19. DDR2 (SSTL_18) I/O DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage	Voh	—	OVDD – 0.28	—	—	V
Low-level output voltage	Vol	—	—	—	0.28	V
Output min. source current[1]	IIoh	—	–13.4	—	—	mA
Output min. sink current[2]	IIol	—	13.4	—	—	mA
DC input logic high	VIH(dc)	—	OVDD/2 + 0.125	—	OVDD + 0.3	V
DC input logic low	VIL(dc)	—	–0.3 V	—	OVDD/2 – 0.125	V
DC input signal voltage[3] (for differential signal)	Vin(dc)	—	–0.3	—	OVDD + 0.3	V
DC differential input voltage[4]	Vid(dc)	—	0.25	—	OVDD+0.6	V

Table 19. DDR2 (SSTL_18) I/O DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Termination voltage[5]	Vtt	—	OVDD/2 – 0.04	OVDD/2	OVDD/2 + 0.04	
Input current[6](no pull-up/down)	IIN	VI = 0 VI = OVDD	—	—	110 60	nA
High-impedance I/O supply current[6]	Icc-ovdd	VI = OVDD or 0	—	—	980	nA
High-impedance core supply current[6]	Icc-vddi	VI = VDD or 0	—	—	1210	nA

1 OVDD = 1.7 V; V_{out} = 1.42 V. (V_{out}-OVDD)/IOH must be less than 21 W for values of V_{out} between OVDD and OVDD-0.28 V.

2 OVDD = 1.7 V; V_{out} = 280 mV. V_{out}/IOL must be less than 21 W for values of V_{out} between 0 V and 280 mV. Simulation circuit for parameters V_{oh} and V_{ol} for I/O cells is below.

3 Vin(dc) specifies the allowable DC excursion of each differential input.

4 Vid(dc) specifies the input differential voltage required for switching. The minimum value is equal to Vih(dc) - Vil(dc).

5 Vtt is expected to track OVDD/2.

6 Minimum condition: BCS model, 1.95 V, and –40 °C. Typical condition: typical model, 1.8 V, and 25 °C. Maximum condition: wcs model, 1.65 V, and 105 °C.

3.5.2 GPIO I/O DC Parameters

Table 20 shows the I/O parameters for GPIO.

Table 20. GPIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
High-level output voltage[1]	Voh	Ioh=–1mA Ioh = Specified Drive	OVDD – 0.15 0.8 × OVDD	—	—	V
Low-level output voltage[1]	Vol	Iol=1mA Iol=Specified Drive	—	—	0.15 0.2 × OVDD	V
High-level output current for slow mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –2.0 –4.0 –8.0	—	—	mA
High-level output current for fast mode	I Ioh	Voh=0.8 × OVDD Standard Drive High Drive Max. Drive	 –4.0 –6.0 –8.0	—	—	mA
Low-level output current for slow mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 2.0 4.0 8.0	—	—	mA
Low-level output current for fast mode	I Iol	Voh=0.2 × OVDD Standard Drive High Drive Max. Drive	 4.0 6.0 8.0	—	—	mA
High-level DC input voltage	VIH	—	0.7 × OVDD	—	OVDD	V
Low-level DC input voltage	VIL	—	–0.3 V	—	0.3 × OVDD	V

Table 20. GPIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Input hysteresis	VHYS	OVDD = 3.3 V OVDD = 1.8V	370 290	—	420 320	mV
Schmitt trigger VT+[1]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[1]	VT–	—	—	—	0.5 × OVDD	V
Pull-up resistor (22 kΩ PU)	Rpu	Vi=0	18.5	22	25.6	kΩ
Pull-up resistor (47 kΩ PU)	Rpu	Vi=0	41	47	55	kΩ
Pull-up resistor (100 kΩ PU)	Rpu	Vi=0	85	100	120	kΩ
Pull-down resistor (100 kΩ PD)	Rpd	VI = OVDD	85	100	120	kΩ
Input current (no pull-up/down)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	100 60 77 50	nA
Input current (22 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	117 0.0001 64 0.0001	—	184 0.0001 104 0.0001	µA
Input current (47 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	54 0.0001 30 0.0001	—	88 0.0001 49 0.0001	µA
Input current (100 kΩ PU)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.0001 23 0.0001	µA
Input current (100 kΩ PD)	IIN	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	25 0.0001 14 0.0001	—	42 0.001 23 0.0001	µA
High-impedance I/O supply current	Icc–ovdd	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	688 688 560 560	nA
High-impedance core supply current	Icc–vddi	VI = 0, OVDD = 3.3 V VI = OVDD = 3.3 V VI = 0, OVDD = 1.8 V VI = OVDD = 1.8 V	—	—	490 490 410 410	nA

[1] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3.6 AC Electrical Characteristics

This section provides the AC parameters for slow and fast I/O.

Figure 3 shows the load circuit for output. Figure 4 through Figure 6 show the output transition time and propagation waveforms.

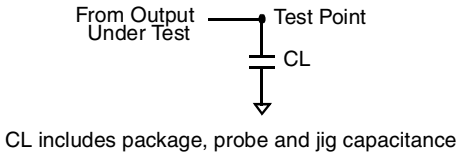


Figure 3. Load Circuit for Output

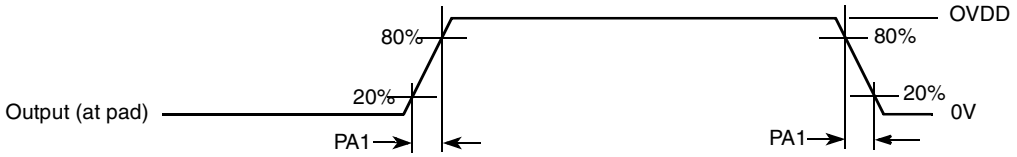


Figure 4. Output Pad Transition Time Waveform

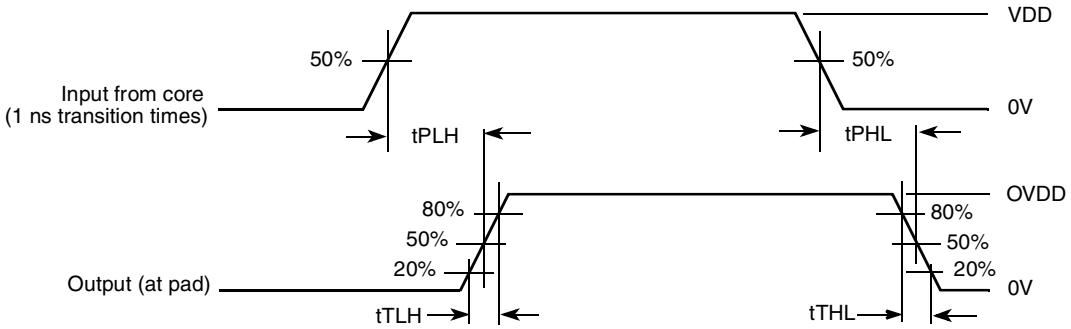


Figure 5. Output Pad Propagation and Transition Time Waveform

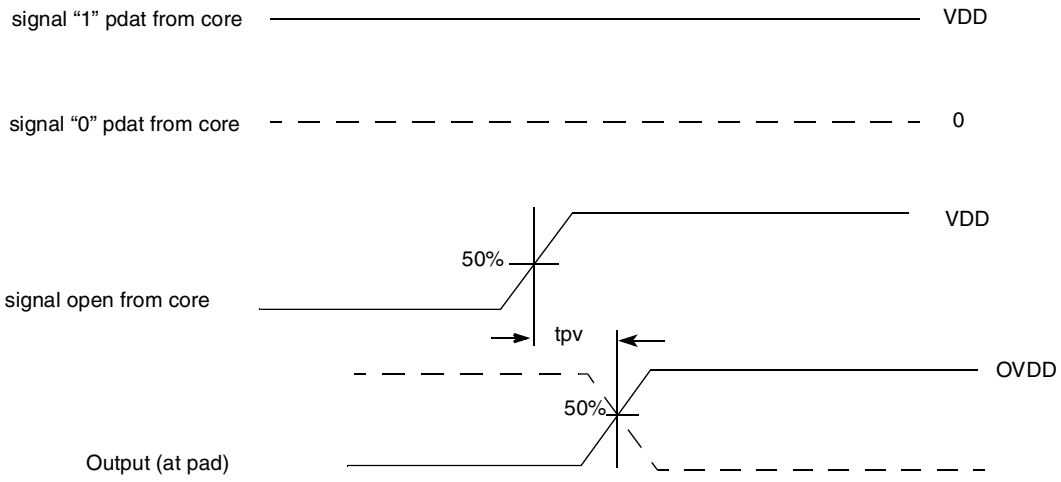


Figure 6. Output Enable to Output Valid