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√RoHS

MCIMX31C and MCIMX31LC
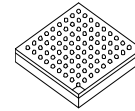
Package Information
Plastic Package
Case 1931 19 x 19 mm, 0.8 mm Pitch

Ordering Information
See Table 1 on page 3 for ordering information.

MCIMX31C and MCIMX31LC

Multimedia Applications Processors for Industrial and Automotive Products

1   Introduction

The MCIMX31C and MCIMX31LC multimedia applications processors represent the next step in low-power, high-performance application processors. Unless otherwise specified, the material in this data sheet is applicable to both the MCIMX31C and MCIMX31LC processors and referred to singularly throughout this document as MCIMX31C. The MCIMX31LC does not include a graphics processing unit (GPU).

Based on an ARM11™ microprocessor core, the MCIMX31C provides the performance with low power consumption required by modern digital devices such as:

* Automotive infotainment and navigation
* Industrial control (human interface)

The MCIMX31C takes advantage of the ARM1136JF-S™ core running at 400 MHz, and is optimized for minimal power consumption using the most advanced techniques for power saving (DVFS, power gating, clock gating). With 90 nm technology and dual-Vt transistors (two threshold voltages), the

Contents

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This document contains information on a new product. Specifications and information herein are subject to change without notice.

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MCIMX31C provides the optimal performance versus leakage current balance.

The performance of the MCIMX31C is boosted by a multi-level cache system, and features peripheral devices such as an MPEG-4 Hardware Encoder (VGA, 30 fps), an Autonomous Image Processing Unit, a Vector Floating Point (VFP11) co-processor, and a RISC-based SDMA controller.

The MCIMX31C supports connections to various types of external memories, such as DDR, NAND Flash, NOR Flash, SDRAM, and SRAM. The MCIMX31C can be connected to a variety of external devices using technology, such as high-speed USB2.0 OTG, ATA, MMC/SDIO, and compact flash.

1.1   Features

The MCIMX31C is designed for automotive and industrial markets where extended operating temperature is required. They provide low-power solutions for high-performance demanding multimedia and graphics applications.

The MCIMX31C is built around the ARM11 MCU core and implemented in the 90 nm technology.

The systems include the following features:

- Multimedia and floating-point hardware acceleration supporting:
  — MPEG-4 real-time encode of up to VGA at 30 fps
  — MPEG-4 real-time video post-processing of up to VGA at 30 fps
  — Video conference call of up to QCIF-30 fps (decoder in software), 128 kbps
  — Video streaming (playback) of up to VGA-30 fps, 384 kbps
  — 3D graphics and other applications acceleration with the ARM® tightly-coupled Vector Floating Point co-processor
  — On-the-fly video processing that reduces system memory load (for example, the power-efficient viewfinder application with no involvement of either the memory system or the ARM CPU)
- Advanced power management
  — Dynamic voltage and frequency scaling
  — Multiple clock and power domains
  — Independent gating of power domains
- Multiple communication and expansion ports including a fast parallel interface to an external graphic accelerator (supporting major graphic accelerator vendors)
- Security

1.2 Ordering Information

Table 1 provides the ordering information for the MCIMX31C.

Table 1. MCIMX31C and MCIMX31LC Ordering Information[1]

Part Number	Silicon Revision	Operating Temperature Range (°C)	Package[2]
MCIMX31CVMN4C**!**	2.0	–40 to 85	
MCIMX31LCVMN4C**!**	2.0	–40 to 85	
MCIMX31CVMN4D**!**	2.0.1	–40 to 85	19 x 19 mm, 0.8 mm pitch, Case 1931
MCIMX31LCVMN4D**!**	2.0.1	–40 to 85	
MCIMX31CJMN4C	2.0.1	–40 to 85	
MCIMX31LCJMN4D	2.0.1	–40 to 85	
MCIMX31CJMN4D	2.0.1	–40 to 85	

[1] Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (**!**)

[2] Case 1931 is RoHS compliant, lead-free, MSL = 3.

1.2.1 Feature Differences Between TO2.0 and TO 2.0.1

The following is a summary of the differences between silicon Revision 2.0 and Revision 2.0.1:

- Revision 2.0.1 - iROM updated to support boot from USB HS and SD/MMC.

1.3 Block Diagram

Figure 1 shows the MCIMX31C simplified interface block diagram.
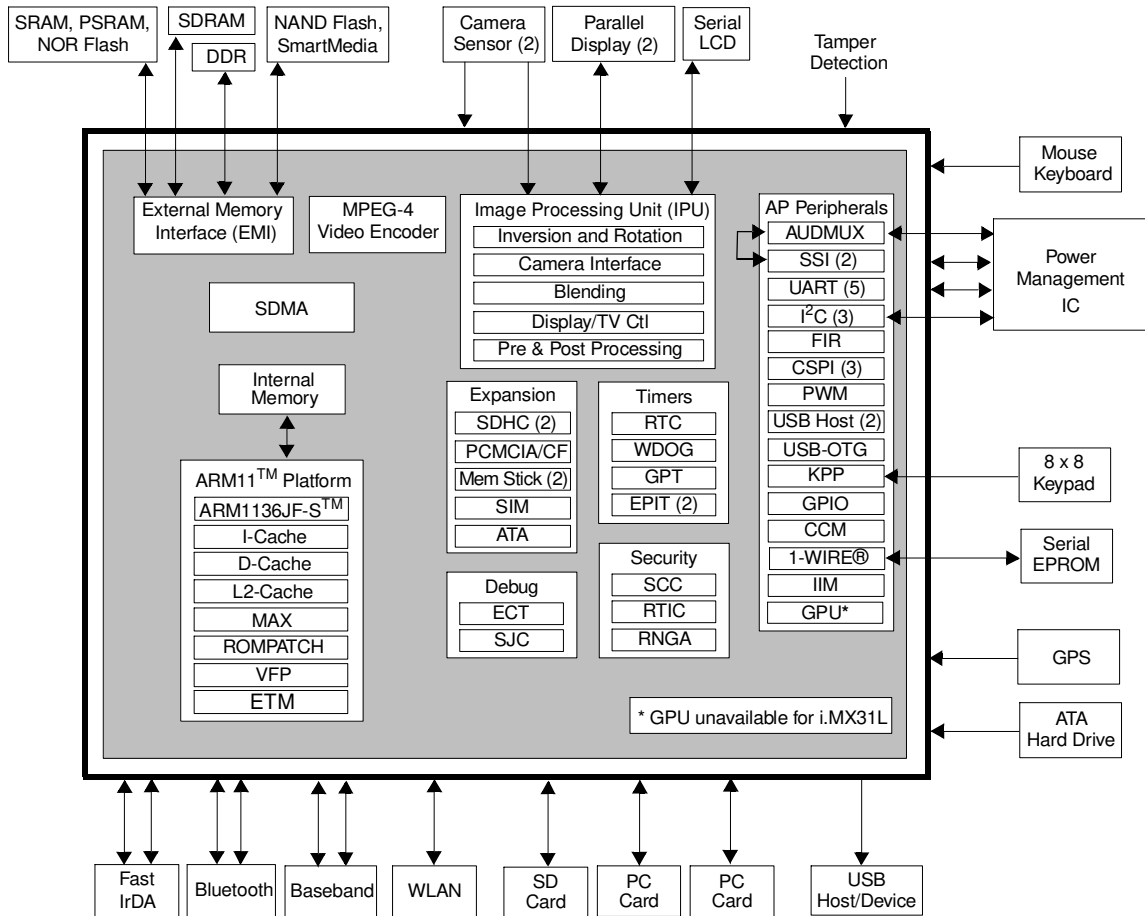
Figure 1. MCIMX31C Simplified Interface Block Diagram

2 Functional Description and Application Information

2.1 ARM11 Microprocessor Core

The CPU of the MCIMX31C is the ARM1136JF-S core based on the ARM v6 architecture. It supports the ARM Thumb® instruction sets, features Jazelle® technology (which enables direct execution of Java byte codes), and a range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.

The ARM1136JF-S processor core features:

- Integer unit with integral EmbeddedICE™ logic
- Eight-stage pipeline
- Branch prediction with return stack
- Low-interrupt latency

- Instruction and data memory management units (MMUs), managed using micro TLB structures backed by a unified main TLB
- Instruction and data L1 caches, including a non-blocking data cache with Hit-Under-Miss
- Virtually indexed/physically addressed L1 caches
- 64-bit interface to both L1 caches
- Write buffer (bypassable)
- High-speed Advanced Micro Bus Architecture (AMBA)™ L2 interface
- Vector Floating Point co-processor (VFP) for 3D graphics and other floating-point applications hardware acceleration
- ETM™ and JTAG-based debug support

2.1.1   Memory System

The ARM1136JF-S complex includes 16 KB Instruction and 16 KB Data L1 caches. It connects to the MCIMX31C L2 unified cache through 64-bit instruction (read-only), 64-bit data read/write (bi-directional), and 64-bit data write interfaces.

The embedded 16K SRAM can be used for audio streaming data to avoid external memory accesses for the low-power audio playback, for security, or for other applications. There is also a 32-KB ROM for bootstrap code and other frequently-used code and data.

A ROM patch module provides the ability to patch the internal ROM. It can also initiate an external boot by overriding the boot reset sequence by a jump to a configurable address.

Table 2 shows information about the MCIMX31C core in tabular form.

Table 2. MCIMX31C Core

Core Acronym	Core Name	Brief Description	Integrated Memory Includes
ARM11 or ARM1136	ARM1136 Platform	The ARM1136™ Platform consists of the ARM1136JF-S core, the ETM real-time debug modules, a 6 x 5 multi-layer AHB crossbar switch (MAX), and a Vector Floating Processor (VFP). The MCIMX31C provides a high-performance ARM11 microprocessor core and highly integrated system functions. The ARM Application Processor (AP) and other subsystems address the needs of the personal, wireless, and portable product market with integrated peripherals, advanced processor core, and power management capabilities.	• 16 Kbyte Instruction Cache • 16 Kbyte Data Cache • 128 Kbyte L2 Cache • 32 Kbyte ROM • 16 Kbyte RAM

2.2   Module Inventory

Table 3 shows an alphabetical listing of the modules in the multimedia applications processor. For extended descriptions of the modules, see the reference manual. A cross-reference is provided to the electrical specifications and timing information for each module with external signal connections.

Table 3. Digital and Analog Modules

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
1-Wire®	1-Wire Interface	Connectivity Peripheral	The 1-Wire module provides bi-directional communication between the ARM11 core and external 1-Wire devices.	4.3.4/20
ATA	Advanced Technology (AT) Attachment	Connectivity Peripheral	The ATA block is an AT attachment host interface. It is designed to interface with IDE hard disc drives and ATAPI optical disc drives.	4.3.5/21
AUDMUX	Digital Audio Multiplexer	Multimedia Peripheral	The AUDMUX interconnections allow multiple, simultaneous audio/voice/data flows between the ports in point-to-point or point-to-multipoint configurations.	4.3.6/30
CAMP	Clock Amplifier Module	Clock	The CAMP converts a square wave/sinusoidal input into a rail-to-rail square wave. The output of CAMP feeds the predivider.	4.3.3/19
CCM	Clock Control Module	Clock	The CCM provides clock, reset, and power management control for the MCIMX31C.	—
CSPI	Configurable Serial Peripheral Interface (x 3)	Connectivity Peripheral	The CSPI is equipped with data FIFOs and is a master/slave configurable serial peripheral interface module, capable of interfacing to both SPI master and slave devices.	4.3.7/30
DPLL	Digital Phase Lock Loop	Clock	The DPLLs produce high-frequency on-chip clocks with low frequency and phase jitters. **Note:** External clock sources provide the reference frequencies.	4.3.8/31
ECT	Embedded Cross Trigger	Debug	The ECT is composed of three CTIs (Cross Trigger Interface) and one CTM (Cross Trigger Matrix—key in the multi-core and multi-peripheral debug strategy.	—
EMI	External Memory Interface	Memory Interface (EMI)	The EMI includes • Multi-Master Memory Interface (M3IF) • Enhanced SDRAM Controller (ESDCTL) • NAND Flash Controller (NFC) • Wireless External Interface Module (WEIM)	— 4.3.9.3/40, 4.3.9.1/32, 4.3.9.2/35
EPIT	Enhanced Periodic Interrupt Timer	Timer Peripheral	The EPIT is a 32-bit "set and forget" timer which starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention.	—
ETM	Embedded Trace Macrocell	Debug/Trace	The ETM (from ARM, Ltd.) supports real-time instruction and data tracing by way of ETM auxiliary I/O port.	4.3.10/48
FIR	Fast InfraRed Interface	Connectivity Peripheral	This FIR is capable of establishing a 0.576 Mbit/s, 1.152 Mbit/s or 4 Mbit/s half duplex link via a LED and IR detector. It supports 0.576 Mbit/s, 1.152 Mbit/s medium infrared (MIR) physical layer protocol and 4Mbit/s fast infrared (FIR) physical layer protocol defined by IrDA, version 1.4.	4.3.11/49

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
Fusebox	Fusebox	ROM	The Fusebox is a ROM that is factory configured by Freescale.	4.3.12/49 See also Table 10
GPIO	General Purpose I/O Module	Pins	The GPIO provides several groups of 32-bit bidirectional, general purpose I/O. This peripheral provides dedicated general-purpose signals that can be configured as either inputs or outputs.	—
GPT	General Purpose Timer	Timer Peripheral	The GPT is a multipurpose module used to measure intervals or generate periodic output.	—
GPU	Graphics Processing Unit	Multimedia Peripheral	The GPU provides hardware acceleration for 2D and 3D graphics algorithms.	—
I^2C	Inter IC Communication	Connectivity Peripheral	The I^2C provides serial interface for controlling the Sensor Interface and other external devices. Data rates of up to 100 Kbits/s are supported.	4.3.13/50
IIM	IC Identification Module	ID	The IIM provides an interface for reading device identification.	—
IPU	Image Processing Unit	Multimedia Peripheral	The IPU processes video and graphics functions in the MCIMX31C and interfaces to video, still image sensors, and displays.	4.3.14/51, 4.3.15/53
KPP	Keypad Port	Connectivity Peripheral	The KPP is used for keypad matrix scanning or as a general purpose I/O. This peripheral simplifies the software task of scanning a keypad matrix.	—
MPEG-4	MPEG-4 Video Encoder	Multimedia Peripherals	The MPEG-4 encoder accelerates video compression, following the MPEG-4 standard	—
MSHC	Memory Stick Host Controller	Connectivity Peripheral	The MSHC is placed in between the AIPS and the customer memory stick to support data transfer from the MCIMX31C to the customer memory stick.	4.3.16/78
PADIO	Pads I/O	Buffers and Drivers	The PADIO serves as the interface between the internal modules and the device's external connections.	4.3.1/16
PCMCIA	PCM	Connectivity Peripheral	The PCMCIA Host Adapter provides the control logic for PCMCIA socket interfaces.	4.3.17/80
PWM	Pulse-Width Modulator	Timer Peripheral	The PWM has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones.	4.3.18/82
RNGA	Random Number Generator Accelerator	Security	The RNGA module is a digital integrated circuit capable of generating 32-bit random numbers. It is designed to comply with FIPS-140 standards for randomness and non-determinism.	—
RTC	Real Time Clock	Timer Peripheral	The RTC module provides a current stamp of seconds, minutes, hours, and days. Alarm and timer functions are also available for programming. The RTC supports dates from the year 1980 to 2050.	—
RTIC	Run-Time Integrity Checkers	Security	The RTIC ensures the integrity of the peripheral memory contents and assists with boot authentication.	—

Table 3. Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Functional Grouping	Brief Description	Section/ Page
SCC	Security Controller Module	Security	The SCC is a hardware component composed of two blocks—the Secure RAM module, and the Security Monitor. The Secure RAM provides a way of securely storing sensitive information.	—
SDHC	Secured Digital Host Controller	Connectivity Peripheral	The SDHC controls the MMC (MultiMediaCard), SD (Secure Digital) memory, and I/O cards by sending commands to cards and performing data accesses to and from the cards.	4.3.19/83
SDMA	Smart Direct Memory Access	System Control Peripheral	The SDMA controller maximizes the system's performance by relieving the ARM core of the task of bulk data transfer from memory to memory or between memory and on-chip peripherals.	—
SIM	Subscriber Identification Module	Connectivity Peripheral	The SIM interfaces to an external Subscriber Identification Card. It is an asynchronous serial interface adapted for Smart Card communication for e-commerce applications.	4.3.20/84
SJC	Secure JTAG Controller	Debug	The SJC provides debug and test control with maximum security and provides a flexible architecture for future derivatives or future multi-cores architecture.	4.3.21/88
SSI	Synchronous Serial Interface	Multimedia Peripheral	The SSI is a full-duplex, serial port that allows the device to communicate with a variety of serial devices, such as standard codecs, Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.	4.3.22/90
UART	Universal Asynchronous Receiver/Transmitter	Connectivity Peripheral	The UART provides serial communication capability with external devices through an RS-232 cable or through use of external circuitry that converts infrared signals to electrical signals (for reception) or transforms electrical signals to signals that drive an infrared LED (for transmission) to provide low speed IrDA compatibility.	—
USB	Universal Serial Bus— 2 Host Controllers and 1 OTG (On-The-Go)	Connectivity Peripherals	• USB Host 1 is designed to support transceiverless connection to the on-board peripherals in Low Speed and Full Speed mode, and connection to the ULPI (UTMI+ Low-Pin Count) and Legacy Full Speed transceivers. • USB Host 2 is designed to support transceiverless connection to the Cellular Modem Baseband Processor. • The USB-OTG controller offers HS/FS/LS capabilities in Host mode and HS/FS in device mode. In Host mode, the controller supports direct connection of a FS/LS device (without external hub). In device (bypass) mode, the OTG port functions as gateway between the Host 1 Port and the OTG transceiver.	4.3.23/98
WDOG	Watchdog Timer Module	Timer Peripheral	The WDOG module protects against system failures by providing a method for the system to recover from unexpected events or programming errors.	—

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3 Signal Descriptions

Signal descriptions are in the reference manual. Special signal considerations are listed following this paragraph. The BGA ball assignment is in Section 5, "Package Information and Pinout," on page 99.

Special Signal Considerations:

- **Tamper detect (GPIO1_6)**

  Tamper detect logic is used to issue a security violation. This logic is activated if the tamper detect input is asserted.

  The tamper detect logic is disabled after reset. After enabling the logic, it is impossible to disable it until the next reset. The GPR[16] bit functions as the tamper detect enable bit.

  GPIO1_6 functions similarly to other I/O with GPIO capabilities regardless of the status of the tamper detect enable bit. (For example, the GPIO1_6 can function as an input with GPIO capabilities, such as sampling through PSR or generating interrupts.)

- **Power ready (GPIO1_5)**

  The power ready input, GPIO1_5, should be connected to an external power management IC power ready output signal. If not used, GPIO1_5 must either be (a) externally pulled-up to NVCC1 or (b) a no connect, internally pulled-up by enabling the on-chip pull-up resistor. GPIO1_5 is a dedicated input and cannot be used as a general-purpose input/output.

- **SJC_MOD**

  SJC_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed, but the value should be much smaller than the on-chip 100 kΩ pull-up.

- **CE_CONTROL**

  CE_CONTROL is a reserved input and must be externally tied to GND through a 1 kΩ resistor.

- **M_REQUEST and M_GRANT**

  These two signals are not utilized internally. The user should make no connection to these signals.

- **Clock Source Select (CLKSS)**

  The CLKSS is the input that selects the default reference clock source providing input to the DPLL. To select CKIH, tie CLKSS to NVCC1. To select CKIL, tie CLKSS to ground. After initialization, the reference clock source can be changed (initial setting is overwritten) by programming the PRCS bits in the CCMR.

4 Electrical Characteristics

This section provides the device-level and module-level electrical characteristics for the MCIMX31C.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 4 for a quick reference to the individual tables and sections.

Table 4. MCIMX31C Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 5, "Absolute Maximum Ratings"	on page 10
Table 6, "Thermal Resistance Data—19 × 19 mm Package"	on page 10
Table 7, "Operating Ranges"	on page 12
Table 8, "Specific Operating Ranges for Silicon Revision 2.0 and 2.0.1"	on page 12
Table 9, "Interface Frequency"	on page 13
Section 4.1.1, "Supply Current Specifications"	on page 14
Section 4.2, "Supply Power-Up/Power-Down Requirements and Restrictions"	on page 15

CAUTION

Stresses beyond those listed under Table 5, "Absolute Maximum Ratings," on page 10 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 7, "Operating Ranges," on page 12 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Voltage (Core)	$QVCC_{max}$	−0.5	1.47	V
Supply Voltage (I/O)	$NVCC_{max}$	−0.5	3.1	V
Input Voltage Range	V_{Imax}	−0.5	NVCC +0.3	V
Storage Temperature	$T_{storage}$	−40	125	^{o}C
ESD Damage Immunity:				
Human Body Model (HBM)	V_{esd}	—	H1C[1]	V
Machine Model (MM)		—	200	
Charge Device Model (CDM)		—	C2[2]	
Offset voltage allowed in run mode between core supplies.	V_{core_offset}[3]	—	15	mV

[1] HBM ESD classification level according to the AEC-Q100-002-Rev-D standard.

[2] Integrated circuit CDM ESD classification level according to the AEC-Q100-011-Rev-B standard.

[3] The offset is the difference between all core voltage pair combinations of QVCC, QVCC1, and QVCC4.

Table 6 provides the thermal resistance data for the 19 × 19 mm, 0.8 mm pitch package.

Table 6. Thermal Resistance Data—19 × 19 mm Package

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (natural convection)	Single layer board (1s)	$R_{\theta JA}$	46	°C/W	1, 2, 3
Junction to Ambient (natural convection)	Four layer board (2s2p)	$R_{\theta JA}$	29	°C/W	1, 2, 3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	38	°C/W	1, 2, 3

Table 6. Thermal Resistance Data—19 × 19 mm Package (continued)

Rating	Board	Symbol	Value	Unit	Notes
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	25	°C/W	1, 2, 3
Junction to Board	—	$R_{\theta JB}$	19	°C/W	1, 3
Junction to Case (Top)	—	$R_{\theta JCtop}$	10	°C/W	1, 4
Junction to Package Top (natural convection)	—	Ψ_{JT}	2	°C/W	1, 5

NOTES

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 7 provides the operating ranges.

NOTE

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.

Table 7. Operating Ranges

Symbol	Parameter	Min	Max	Units
QVCC, QVCC1, QVCC4	Core Operating Voltage[1],[2]			V
	$0 \le f_{ARM} \le 400$ MHz	1.22	1.47	
	State Retention Voltage[3]	0.95	—	
NVCC1, NVCC3–10	I/O Supply Voltage, except DDR[4]	1.75	3.1	V
NVCC2, NVCC21, NVCC22	I/O Supply Voltage, DDR only	1.75	1.95	V
FVCC, MVCC, SVCC, UVCC	PLL (Phase-Locked Loop) and FPM (Frequency Pre-multiplier) Supply Voltage[5]	1.3	1.47	V
IOQVDD	On-device Level Shifter Supply Voltage	1.6	1.9	V
FUSE_VDD	Fusebox read Supply Voltage[6]	—	—	V
	Fusebox write (program) Supply Voltage[7]	3.0	3.3	V
T_A	Operating Ambient Temperature Range	–40	85	°C
T_j	Operating Junction Temperature Range	—	105	°C

[1] Measured at package balls, including peripherals, ARM, and L2 cache supplies (QVCC, QVCC1, QVCC4, respectively).

[2] The core voltage must be higher than 1.38V to avoid corrupted data during transfers from the USB HS. Please refer to Errata file ENGcm02610 ID

[3] The SR voltage is applied to QVCC, QVCC1, and QVCC4 after the device is placed in SR mode. The Real-Time Clock (RTC) is operational in State Retention (SR) mode.

[4] Overshoot and undershoot conditions (transitions above NVCC and below GND) on I/O must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

[5] PLL voltage must not be altered after power-up, otherwise the PLL will be unstable and lose lock. To minimize inducing noise on the PLL supply line, source the voltage from a low-noise, dedicated supply. PLL parameters in Table 28, "DPLL Specifications," on page 31, are guaranteed over the entire specified voltage range.

[6] In read mode, FUSE_VDD can be floated or grounded.

[7] Fuses might be inadvertently blown if written to while the voltage is below this minimum.

Table 8. Specific Operating Ranges for Silicon Revision 2.0 and 2.0.1

Symbol	Parameter	Min	Max	Units
FUSE_VDD	Fusebox read Supply Voltage[1]	—	—	V
	Fusebox write (program) Supply Voltage[2]	3.0	3.3	V

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[1] In read mode, FUSE_VDD should be floated or grounded.

[2] Fuses might be inadvertently blown if written to while the voltage is below the minimum.

Table 9 provides information for interface frequency limits. For more details about clocks characteristics, see Section 4.3.8, "DPLL Electrical Specifications" on page 31 and Section 4.3.3, "Clock Amplifier Module (CAMP) Electrical Characteristics" on page 19.

Table 9. Interface Frequency

ID	Parameter	Symbol	Min	Typ	Max	Units
1	JTAG TCK Frequency	f_{JTAG}	DC	5	10	MHz
2	CKIL Frequency[1]	f_{CKIL}	32	32.768	38.4	kHz
3	CKIH Frequency[2]	f_{CKIH}	15	26	75	MHz

[1] CKIL must be driven by an external clock source to ensure proper start-up and operation of the device. CKIL is needed to clock the internal reset synchronizer, the watchdog, and the real-time clock.

[2] DPTC functionality, specifically the voltage/frequency relation table, is dependent on CKIH frequency. At the time of publication, standard tables used by Freescale OSs provided for a CKIH frequency of 26 MHz only. Any deviation from this frequency requires an update to the OS. For more details, refer to the particular OS user's guide documentation. DPTC/DVFS are not supported for $fARM \leq 400MHz$.

Table 10 shows the fusebox supply current parameters.

Table 10. Fusebox Supply Current Parameters

Ref. Num	Description	Symbol	Minimum	Typical	Maximum	Units
1	eFuse Program Current.[1] Current to program one eFuse bit: efuse_pgm = 3.0V	$I_{program}$	—	35	60	mA

[1] The current $I_{program}$ is during program time ($t_{program}$).

4.1.1 Supply Current Specifications

Table 11 shows the core current consumption for –40°C to 85°C for Silicon Revision 2.0 and 2.0.1 for the MCIMX31C.

Table 11. Current Consumption for –40°C to 85°C[1, 2] for Silicon Revision 2.0 and 2.0.1

Mode	Conditions	QVCC (Peripheral)		QVCC1 (ARM)		QVCC4 (L2)		FVCC + MVCC + SVCC + UVCC (PLL)		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Deep Sleep	• QVCC = 0.95 V • ARM and L2 caches are power gated (QVCC1 = QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.20	9.00	—	—	—	—	0.04	0.14	mA
State Retention	• QVCC and QVCC1 = 0.95 V • L2 caches are power gated (QVCC4 = 0 V) • All PLLs are off, VCC = 1.4 V • ARM is in well bias • FPM is off • 32 kHz input is on • CKIH input is off • CAMP is off • TCK input is off • All modules are off • No external resistive loads • RNGA oscillator is off	0.20	9.00	0.15	3.50	—	—	0.04	0.14	mA
Wait	• QVCC,QVCC1, and QVCC4 = 1.22 V • ARM is in wait for interrupt mode • MAX is active • L2 cache is stopped but powered • MCU PLL is on (400 MHz), VCC = 1.4 V • USB PLL and SPLL are off, VCC = 1.4 V • FPM is on • CKIH input is on • CAMP is on • 32 kHz input is on • All clocks are gated off • All modules are off (by programming CGR[2:0] registers) • RNGA oscillator is off • No external resistive loads	7.00	19.00	3.00	100.00	0.03	0.90	4.00	6.00	mA

[1] Typical column: TA = 25°C

[2] Maximum column: TA = 85°C

4.2 Supply Power-Up/Power-Down Requirements and Restrictions

Any MCIMX31C board design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in any or all of the following situations:

- Cause excessive current during power-up phase
- Prevent the device from booting
- Cause irreversible damage to the MCIMX31C (worst-case scenario)

4.2.1 Powering Up

The Power On Reset ($\overline{POR}$) pin must be kept asserted (low) throughout the power-up sequence. Power-up logic must guarantee that all power sources reach their target values prior to the release (de-assertion) of $\overline{POR}$. Figure 2 and Figure 3 show two options of the power-up sequence.

NOTE

Stages need to be performed in the order shown; however, *within* each stage, supplies can be powered up in any order. For example, supplies IOQVDD, NVCC1, and NVCC3 through NVCC10 do not need to be powered up in the order shown.

CAUTION

NVCC6 and NVCC9 must be at the same voltage potential. These supplies are connected together on-chip to optimize ESD damage immunity.
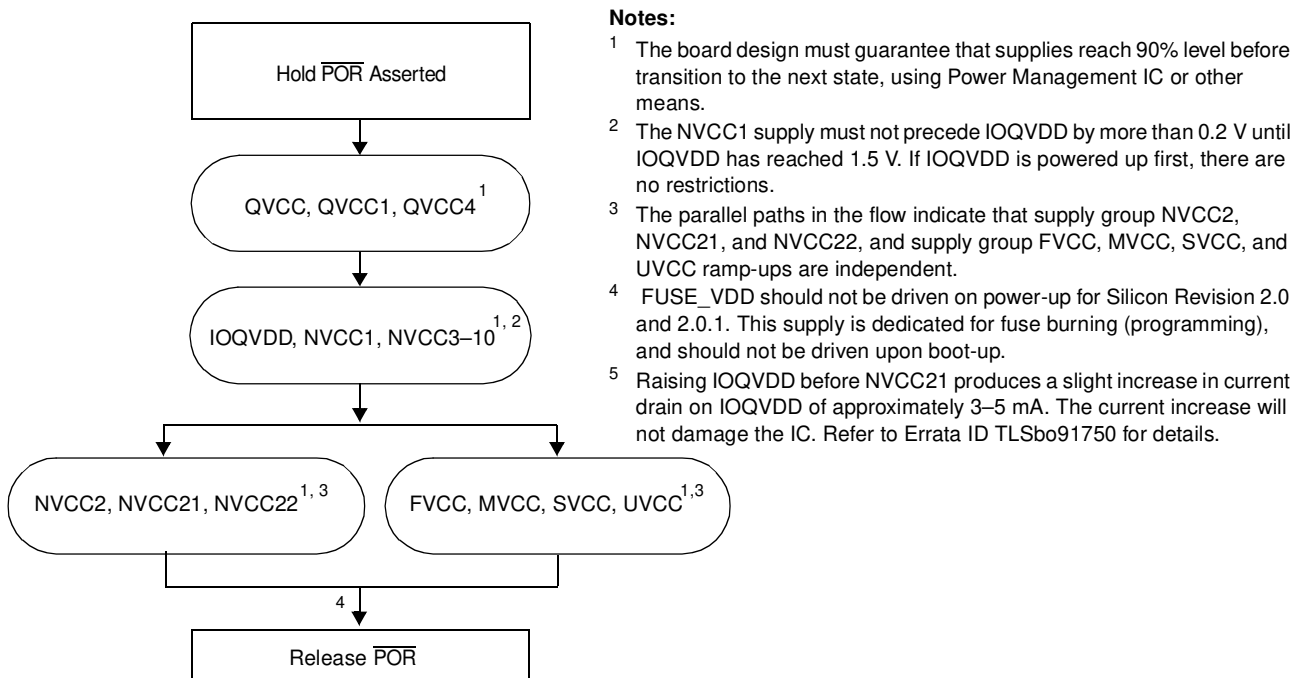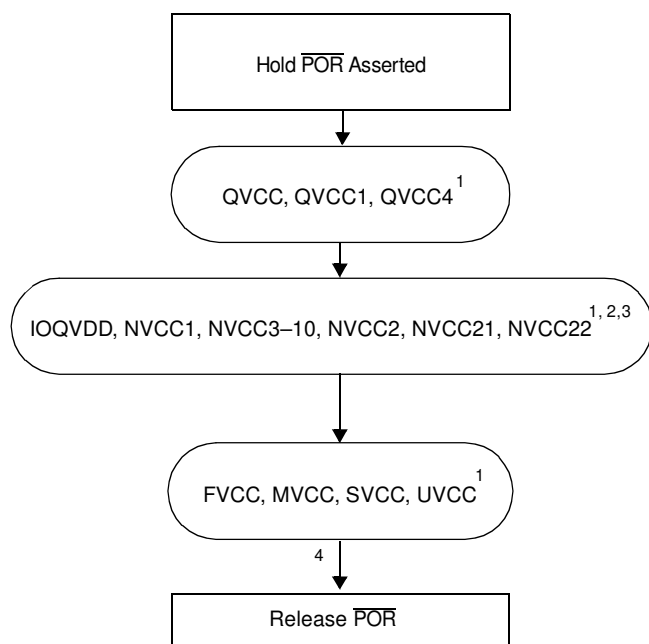

Notes:

[1] The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.

[2] The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.

[3] The parallel paths in the flow indicate that supply group NVCC2, NVCC21, and NVCC22, and supply group FVCC, MVCC, SVCC, and UVCC ramp-ups are independent.

[4] FUSE_VDD should not be driven on power-up for Silicon Revision 2.0 and 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.

[5] Raising IOQVDD before NVCC21 produces a slight increase in current drain on IOQVDD of approximately 3–5 mA. The current increase will not damage the IC. Refer to Errata ID TLSbo91750 for details.

Figure 2. Option 1 Power-Up Sequence for Silicon Revision 2.0 and 2.0.1

Notes:
[1] The board design must guarantee that supplies reach 90% level before transition to the next state, using Power Management IC or other means.
[2] The NVCC1 supply must not precede IOQVDD by more than 0.2 V until IOQVDD has reached 1.5 V. If IOQVDD is powered up first, there are no restrictions.
[3] Raising NVCC2, NVCC21, and NVCC22 at the same time as IOQVDD does not produce the slight increase in current drain on IOQVDD (as described in Figure 2, Note 5).
[4] FUSE_VDD should not be driven on power-up for Silicon Revision2.0 and 2.0.1. This supply is dedicated for fuse burning (programming), and should not be driven upon boot-up.

Figure 3. Option 2 Power-Up Sequence (Silicon Revision 2.0 and 2.0.1)

4.2.2 Powering Down

The power-down sequence should be completed as follows:

1. Lower the FUSE_VDD supply (when in write mode).
2. Lower the remaining supplies.

4.3 Module-Level Electrical Specifications

This section contains the MCIMX31C electrical information including timing specifications, arranged in alphabetical order by module name.

4.3.1 I/O Pad (PADIO) Electrical Specifications

This section specifies the AC/DC characterization of functional I/O of the MCIMX31C. There are two main types of I/O: regular and DDR. In this document, the "Regular" type is referred to as GPIO.

4.3.1.1 DC Electrical Characteristics

The MCIMX31C I/O parameters appear in Table 12 for GPIO. See Table 7, "Operating Ranges," on page 12 for temperature and supply voltage ranges.

NOTE

The term NVCC in this section refers to the associated supply rail of an input or output. The association is shown in the Signal Multiplexing chapter of the reference manual. NVCC for Table 12 refers to NVCC1 and NVCC3–10; QVCC refers to QVCC, QVCC1, and QVCC4.

Table 12. GPIO DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	I_{OH} = −1 mA	NVCC −0.15	—	—	V
		I_{OH} = specified Drive	0.8*NVCC	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA	—	—	0.15	V
		I_{OL} = specified Drive	—	—	0.2*NVCC	V
High-level output current, slow slew rate	I_{OH_S}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive	 −2 −4 −8	—	—	mA
High-level output current, fast slew rate	I_{OH_F}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive	 −4 −6 −8	—	—	mA
Low-level output current, slow slew rate	I_{OL_S}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive	 2 4 8	—	—	mA
Low-level output current, fast slew rate	I_{OL_F}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive	 4 6 8	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	—	NVCC	V
Low-Level DC input voltage	V_{IL}	—	0	—	0.3*QVCC	V
Input Hysteresis	V_{HYS}	Hysteresis enabled	0.25	—	—	V
Schmitt trigger VT+	$V_T +$	Hysteresis enabled	0.5*QVCC	—	—	V
Schmitt trigger VT−	$V_T -$	Hysteresis enabled	—	—	0.5*QVCC	V
Pull-up resistor (100 kΩ PU)	R_{PU}[1]	—	—	100	—	kΩ
Pull-down resistor (100 kΩ PD)	R_{PD}[1]	—	—	100	—	
Input current (no PU/PD)	I_{IN}	V_I = NVCC or GND	—	—	±1	µA
Input current (100 kΩ PU)	I_{IN}	V_I = 0	—	—	25	µA µA
Input current (100 kΩ PD)	I_{IN}	V_I = NVCC	—	—	28	µA
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

[1] Not a precise value. Measurements made on small sample size have shown variations of ±50% or more.

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The MCIMX31C I/O parameters appear in Table 13 for DDR (Double Data Rate). See Table 7, "Operating Ranges," on page 12 for temperature and supply voltage ranges.

NOTE

NVCC for Table 13 refers to NVCC2, NVCC21, and NVCC22.

Table 13. DDR (Double Data Rate) I/O DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	V_{OH}	I_{OH} = −1 mA	NVCC −0.12	—	—	V
		I_{OH} = specified Drive	0.8*NVCC	—	—	V
Low-level output voltage	V_{OL}	I_{OL} = 1 mA	—	—	0.08	V
		I_{OL} = specified Drive	—	—	0.2*NVCC	V
High-level output current	I_{OH}	V_{OH}=0.8*NVCC Std Drive High Drive Max Drive DDR Drive[1]	— −3.6 −7.2 −10.8 −14.4	—	—	mA
Low-level output current	I_{OL}	V_{OL}=0.2*NVCC Std Drive High Drive Max Drive DDR Drive[1]	— 3.6 7.2 10.8 14.4	—	—	mA
High-Level DC input voltage	V_{IH}	—	0.7*NVCC	NVCC	NVCC+0.3	V
Low-Level DC input voltage	V_{IL}	—	−0.3	0	0.3*NVCC	V
Tri-state leakage current	I_{OZ}	V_I = NVCC or GND I/O = High Z	—	—	±2	µA

[1] Use of DDR Drive can result in excessive overshoot and ringing.

4.3.2 AC Electrical Characteristics

Figure 4 depicts the load circuit for outputs. Figure 5 depicts the output transition time waveform. The range of operating conditions appears in Table 14 for slow general I/O, Table 15 for fast general I/O, and Table 16 for DDR I/O (unless otherwise noted).

CL includes package, probe and fixture capacitance
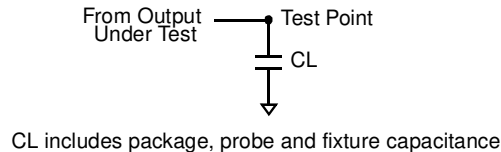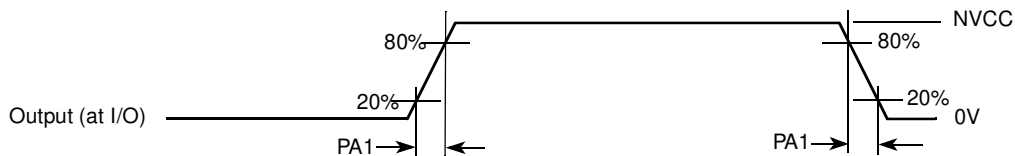
Figure 4. Load Circuit for Output

Figure 5. Output Transition Time Waveform

Table 14. AC Electrical Characteristics of Slow[1] General I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.92 1.5	1.95 2.98	3.17 4.75	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	1.52 2.75	—	4.81 8.42	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	2.79 5.39	—	8.56 16.43	ns

[1] Fast/slow characteristic is selected per GPIO (where available) by "slew rate" control. See reference manual.

Table 15. AC Electrical Characteristics of Fast[1] General I/O [2]

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.68 1.34	1.33 2.6	2.07 4.06	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.91 1.79	1.77 3.47	2.74 5.41	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.36 2.68	2.64 5.19	4.12 8.11	ns

[1] Fast/slow characteristic is selected per GPIO (where available) by "slew rate" control. See reference manual.
[2] Use of GPIO in fast mode with the associated NVCC > 1.95 V can result in excessive overshoot and ringing.

Table 16. AC Electrical Characteristics of DDR I/O

ID	Parameter	Symbol	Test Condition	Min	Typ	Max	Units
PA1	Output Transition Times (DDR Drive)[1]	tpr	25 pF 50 pF	0.51 0.97	0.82 1.58	1.28 2.46	ns
	Output Transition Times (Max Drive)	tpr	25 pF 50 pF	0.67 1.29	1.08 2.1	1.69 3.27	ns
	Output Transition Times (High Drive)	tpr	25 pF 50 pF	.99 1.93	1.61 3.13	2.51 4.89	ns
	Output Transition Times (Std Drive)	tpr	25 pF 50 pF	1.96 3.82	3.19 6.24	4.99 9.73	ns

[1] Use of DDR Drive can result in excessive overshoot and ringing.

4.3.3 Clock Amplifier Module (CAMP) Electrical Characteristics

This section outlines the Clock Amplifier Module (CAMP) specific electrical characteristics. Table 17 shows clock amplifier electrical characteristics.

Table 17. Clock Amplifier Electrical Characteristics for CKIH Input

Parameter	Min	Typ	Max	Units
Input Frequency	15	—	75	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	(VDD [1] – 0.25)	—	3	V
Sinusoidal Input Amplitude	0.4 [2]	—	VDD	Vp-p
Duty Cycle	45	50	55	%

[1] VDD is the supply voltage of CAMP. See reference manual.
[2] This value of the sinusoidal input will be measured through characterization.

4.3.4   1-Wire Electrical Specifications

Figure 6 depicts the RPP timing, and Table 18 lists the RPP timing parameters.
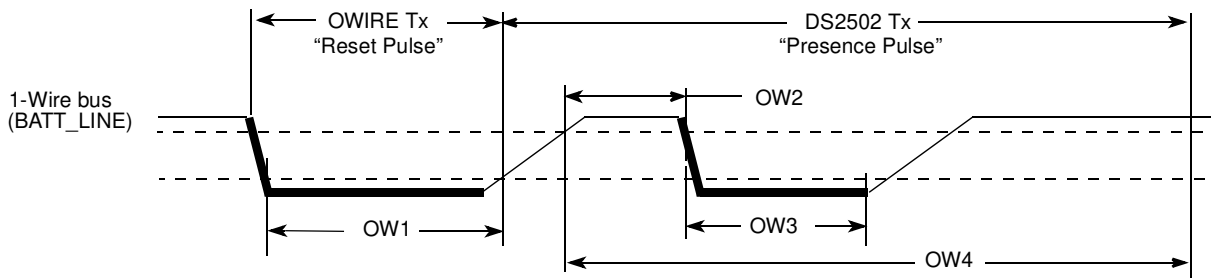
Figure 6. Reset and Presence Pulses (RPP) Timing Diagram

Table 18. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Units
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 7 depicts Write 0 Sequence timing, and Table 19 lists the timing parameters.
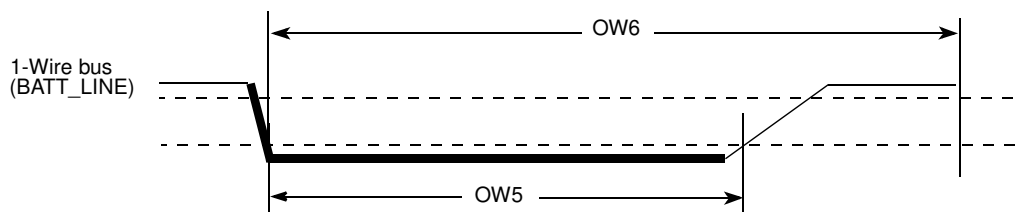
Figure 7. Write 0 Sequence Timing Diagram

Table 19. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Units
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

Figure 8 depicts Write 1 Sequence timing, Figure 9 depicts the Read Sequence timing, and Table 20 lists the timing parameters.
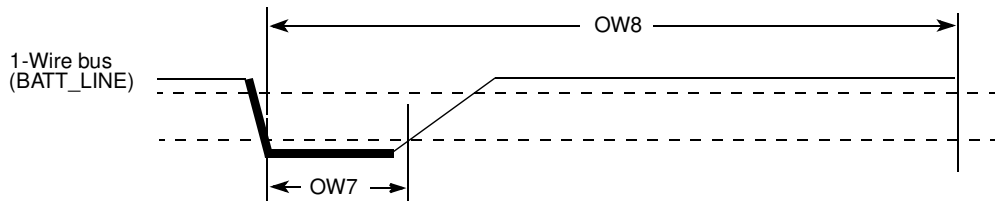
Figure 8. Write 1 Sequence Timing Diagram
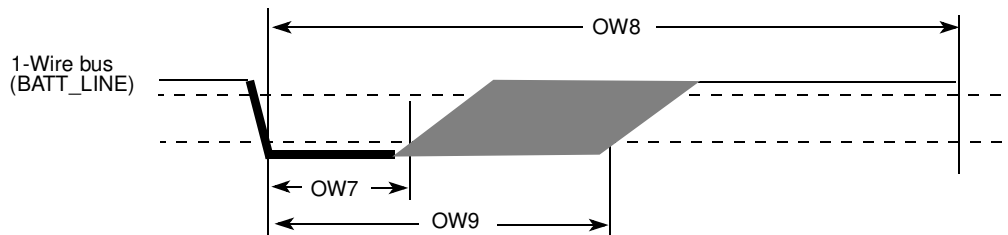
Figure 9. Read Sequence Timing Diagram

Table 20. WR1/RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Units
OW7	Write 1 / Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.3.5 ATA Electrical Specifications (ATA Bus, Bus Buffers)

This section discusses ATA parameters. For a detailed description, refer to the ATA specification.

The user needs to use level shifters for 3.3 Volt or 5.0 Volt compatibility on the ATA interface.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-5) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

4.3.5.1   Timing Parameters

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the ATA interface on silicon, the bus buffer used, the cable delay and cable skew. Table 21 shows ATA timing parameters.

Table 21. ATA Timing Parameters

| Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (ipg_clk_ata)	peripheral clock frequency
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4 UDMA5	 15 ns 10 ns 7 ns 5 ns 4 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4 UDMA5	 5.0 ns 4.6 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	transceiver
tbuf	Max buffer propagation delay	transceiver
tcable1	Cable propagation delay for ata_data	cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	cable

Name	Description	Value/ Contributing Factor[1]
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	cable

[1] Values provided where applicable.

4.3.5.2 PIO Mode Timing

Figure 10 shows timing for PIO read, and Table 22 lists the timing parameters for PIO read.
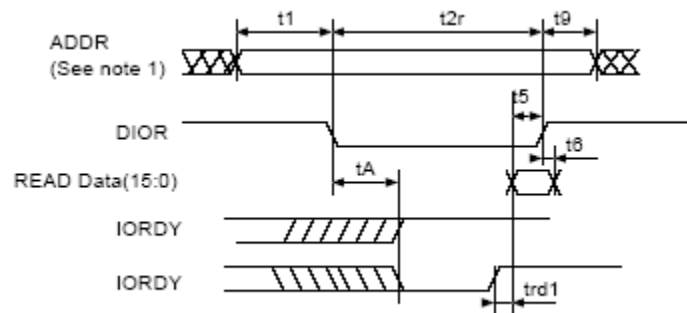
Figure 10. PIO Read Timing Diagram

Table 22. PIO Read Timing Parameters

ATA Parameter	Parameter from **Figure 10**	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r * T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)*T – (tsu + thi) (time_pio_rdx – 0.5) * T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9

Figure 11 shows timing for PIO write, and Table 23 lists the timing parameters for PIO write.

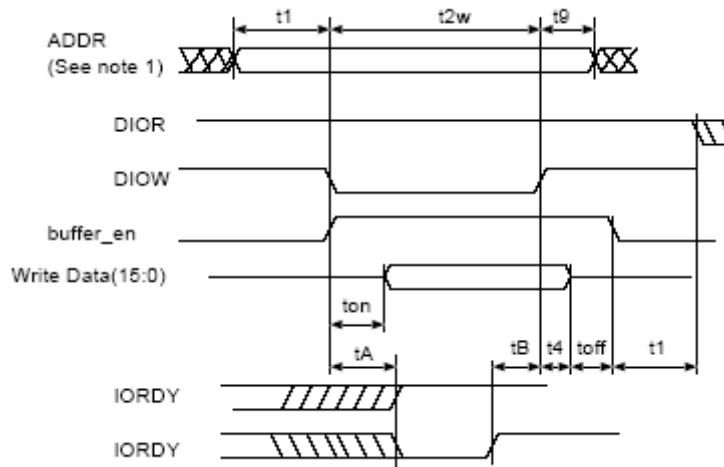**Figure 11. Multiword DMA (MDMA) Timing**

Table 23. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 11	Value	Controlling Variable
t1	t1	t1 (min) = time_1 * T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w * T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 * T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)* T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 * T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) * T – (tco + tsui + tcable2 + tcable2 + 2*tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) * T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough.	—
—	—	Avoid bus contention when switching buffer off by making toff long enough.	—

Figure 12 shows timing for MDMA read, Figure 13 shows timing for MDMA write, and Table 24 lists the timing parameters for MDMA read and write.
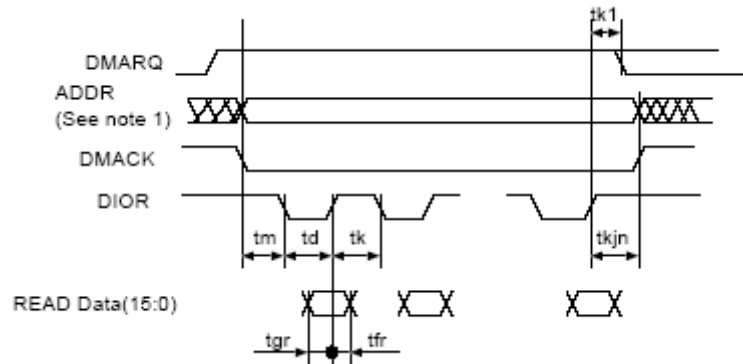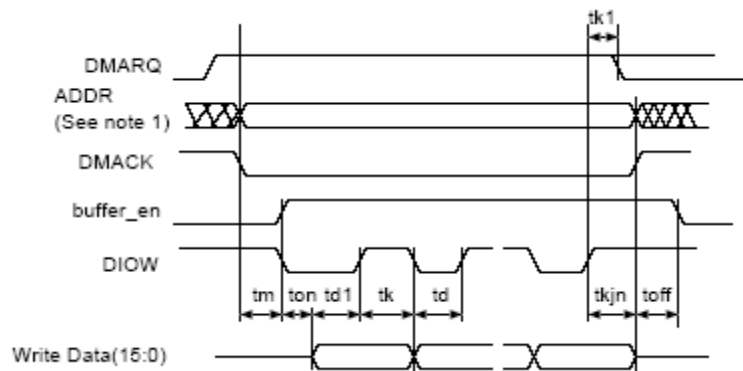
Figure 12. MDMA Read Timing Diagram

Figure 13. MDMA Write Timing Diagram

Table 24. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from **Figure 12**, **Figure 13**	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m * T − (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d * T − (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k * T − (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) * T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td − te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d * T − (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k * T − (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k−2)*T − (tsu + tco + 2*tbuf + 2*tcable2)	time_d, time_k
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) * T − (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on * T − tskew1 toff = time_off * T − tskew1	—

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