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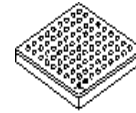
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MCIMX50



Package Information

Plastic Package

Case 416 MAPBGA 13 x 13 mm, 0.5 mm pitch
Case 416 PoPBGA 13 x 13 mm, 0.5 mm pitch
Case 400 MAPBGA 17 x 17 mm, 0.8 mm pitch

i.MX50 Applications Processors for Consumer Products

Ordering Information

See [Table 1 on page 7](#) for ordering information.

1 Introduction

The i.MX50 applications processors are multimedia-focused products offering high-performance processing optimized for lowest power consumption. The i.MX50 processors are Freescale Energy Efficiency Solutions products.

The i.MX50 is optimized for portable multimedia applications and features Freescale's advanced implementation of the ARM Cortex-A8[®] core, which operates at speeds as high as 1 GHz. The i.MX50 provides a powerful display architecture, including a 2D Graphics Processing Unit (GPU) and Pixel Processing Pipeline (ePXP). Additionally, the i.MX50 includes a complete integration of the electrophoretic display function. The i.MX50 supports DDR2, LPDDR2, and LPDDR1 DRAM at clock rate up to 266 MHz to enable a range of performance and power trade-offs.

The flexibility of the i.MX50 architecture allows it to be used in a variety of applications. As the heart of the

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Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.



application chipset, the i.MX50 provides a rich set of interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, and displays.

1.1 Product Overview

The i.MX50 is designed to enable high-tier portable applications by satisfying the performance requirements of advanced operating systems and applications.

1.1.1 Dynamic Performance Scaling

Freescale's dynamic voltage and frequency scaling (DVFS) allows the device to run at much lower voltage and frequency with ample processing capacity for tasks, such as audio decode, resulting in significant power reduction.

1.1.2 Multimedia Processing Powerhouse

The multimedia performance of the i.MX50 processor ARM Cortex-A8 core is boosted by a multi-level cache system, a NEON™ coprocessor with SIMD media processing architecture and 32-bit single-precision floating point support, and two vector floating point coprocessors. The system is further enhanced by a programmable smart DMA (SDMA) controller.

1.1.3 Powerful Display System

The i.MX50 includes support for both standard LCD displays as well as electrophoretic displays (e-paper). The display subsystem consists of the following modules:

- Electrophoretic Display Controller (EPDC) (i.MX508 only)
The EPDC is a feature-rich, low power, and high-performance direct-drive active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT architectures. The goal of the EPDC is to provide an efficient SoC integration of this functionality for e-paper applications, allowing a significant bill of materials cost savings over an external solution while reaching much higher levels of performance and lower power. The EPDC module is defined in the context of an optimized hardware/software partitioning and works in conjunction with the ePXP (see [Section 1.1.4, “Graphics Accelerators”](#)).
- Enhanced LCD Controller Interface (eLCDIF)
The eLCDIF is a high-performance LCD controller interface that supports a rich set of modes and allows interoperability with a wide variety of LCD panels, including DOTCK/RGB and smart panels. The module also supports synchronous operation with the ePXP to allow the processed frames to be passed from the ePXP to the eLCDIF through an on-chip SRAM buffer. The eLCDIF can support up to 32-bit interfaces.

1.1.4 Graphics Accelerators

Integrated graphics accelerators offload processing from the ARM processor, enabling high performance graphic applications at minimum power.

- Pixel Processing Pipeline (ePXP)

The ePXP is a high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma mapping, and rotation. The ePXP is enhanced with features specifically for grayscale applications working in conjunction with the electrophoretic display controller to form a full grayscale display solution. In addition, the ePXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated LCD controller (eLCDIF).

- Graphics acceleration

The i.MX50 provides a 2D graphics accelerator with performance up to 200 Mpix/s.

1.1.5 Multilevel Memory System

The multilevel memory system of the i.MX50 is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The i.MX50 supports many types of external memory devices, including DDR2, LPDDR2, LPDDR1, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC) and OneNAND™, and managed NAND including eMMC up to rev. 4.4.

1.1.6 Smart Speed™ Technology

The i.MX50 device has power management throughout the SOC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart Speed technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than industry expectations.

1.1.7 Interface Flexibility

The i.MX50 supports connection to a variety of interfaces, including an LCD controller for displays, two high-speed USB on-the-go-capable PHYs, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (for example, UART, I²C, and I²S serial audio).

1.1.8 Advanced Security

The i.MX50 delivers hardware-enabled security features, such as High-Assurance Boot 4 (HAB4) for signed/authenticated firmware images, basic DRM support with random private keys and AES encryption/decryption, and storage and programmability of on-chip fuses.

1.2 Features

The i.MX50 applications processor is based on the ARM Cortex-A8 platform and has the following features:

- MMU, L1 instruction cache, and L1 data cache
- Unified L2 cache
- 800 MHz or 1 GHz target frequency of the core (including NEON, VFPv3, and L1 cache)

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- NEON coprocessor (SIMD Media Processing Architecture) and Vector Floating Point (VFP-Lite) coprocessor supporting VFPv3

The memory system consists of the following components:

- Level 1 cache:
 - Instruction (32 Kbyte)
 - Data (32 Kbyte)
- Level 2 cache:
 - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
 - Boot ROM, including HAB (96 Kbyte)
 - Internal multimedia/shared, fast access RAM (128 Kbyte)
- External memory interfaces:
 - 16/32-bit DDR2-533, LPDDR2-533, or LPDDR1-400 up to a total of 2 GByte
 - 8-bit NAND SLC/MLC Flash with up to 100 MHz synchronous clock rate and up to 32-bit hardware ECC for 1 Kbyte block size
 - 16/32-bit NOR Flash with a dedicated 16-bit muxed-mode interface. I/O muxing logic selects EIMv2 port as primary muxing at system boot.
 - 16-bit PSRAM, Cellular RAM
 - Managed NAND, including eMMC up to rev 4.4

The i.MX50 introduces a next generation system bus fabric architecture that aggregates various sub-system buses and masters for access to system peripherals and memories. The various bus-systems and components are as follows:

- 64-bit AXI Fabric (266 MHz)—This bus-fabric is the SoC's central bus aggregation point.
 - Provides access to all slave targets in the SoC:
 - ROM (ROMCP)
 - On-chip RAM (OCRAM)
 - External DRAM (DRAM MC)
 - External static RAM (EIM)
 - Interrupt controller (TZIC)
 - Decode into the AHB MAX crossbar second level AHB fabric.
 - Provides arbitration to the following masters in the system:
 - ARM CPU complex
 - Pixel processing pipeline (ePXP)
 - Electrophoretic display controller (EPDC)
 - eLCDIF LCD display controller
 - DCP Crypto engine
 - BCH ECC engine
 - MAX AHB crossbar

- GPU 2D
- SDMA
- USBOH1 (USB OTG and host controller complex)
- FEC Ethernet controller
- MAX AHB crossbar (133 MHz)—This connects the various AHB bus sub-segments in the system and provides decode into the following slaves:
 - IP-Bus 1 (66 MHz)—This bus segment contains peripherals accessible by the ARM core and without DMA capability
 - IP-Bus 2 (66 MHz)—This bus segment contains peripherals accessible by the ARM core and without DMA capability
 - APBH DMA bridge (133 MHz)—The APBH DMA bridge is a master to the MAX for its memory-side DMA operations. The APBH bus is an AMBA APB slave bus providing peripheral access to many of the high-speed IP blocks on the i.MX50.
- IP-Bus 3 (66 MHz)—This third peripheral bus segment contains peripherals accessible by the ARM core and SDMA and as such houses peripherals with DMA capability. The IP-Bus 3 can be accessed by the ARM CPU through IP-Bus 1 and SPBA.
- Quality of service controller (QoSC)—This provides both soft and dynamic arbitration/priority control. The QoS works in conjunction with the critical display modules such as the eLCDIF and EPDC to provide dynamic priority control, based on real-time metrics.

The i.MX50 makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption, while freeing up the CPU core for other tasks.

The i.MX50 incorporates the following hardware accelerators:

- GPU2Dv1—2D Graphics accelerator, OpenVG 1.1, 200 Mpix/s performance
- eXP—enhanced PiXel Processing Pipeline off loading key pixel processing operations required to support both LCD and EPD display applications

The i.MX50 includes the following interfaces to external devices:

NOTE

Not all the interfaces are available simultaneously depending on I/O multiplexer configuration.

- Displays:
 - EPDC (i.MX508 Only)—Supporting direct-driver TFT backplanes beyond 2048 × 1536 at 106 Hz refresh (or 4096 × 4096 at 20 Hz)
 - eLCDIF—Supporting beyond SXGA + (1400 × 1050) at 60 Hz resolutions with up to a 32-bit display interface
 - On the i.MX508, both displays can be active simultaneously. If both displays are active, the eLCDIF only provides a 16-bit interface due to pin muxing.
- Expansion cards:
 - Four SD/MMC card

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- USB:
 - One High Speed (HS) USB 2.0 OTG-capable port with integrated HS USB PHY
 - One High Speed (HS) USB 2.0 host port with integrated HS USB PHY
- Miscellaneous interfaces:
 - One-wire (OWIRE) port
 - Two I2S/SSI/AC97 ports, supporting up to 1.4 Mbps each connected to the Audio Multiplexer (AUDMUX) providing four external ports
 - Five UART RS232 ports, up to 4.0 Mbps each
 - Two eCSPI (Enhanced CSPI) ports, up to 66 Mbps each plus CSPI port, up to 16.6 Mbps
 - Three I²C ports, supporting 400 kbps
 - Fast Ethernet controller IEEE 802.3, 10/100 Mbps
 - Key pad port (KPP)
 - Two pulse width modulators (PWM)
 - GPIO with interrupt capabilities
 - Secure JTAG controller (SJC)

The system supports efficient and smart power control and clocking:

- Supporting DVFS techniques for low power modes, including auto slow architecture
- Power gating-SRPG (state retention power gating) for ARM core and NEON
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip 32 kHz and 24 MHz oscillators
- A total of four PLLs with the fourth PLL providing up to eight independently controllable outputs, improving the ease of clocking control, especially for display and connectivity modules

Security functions are enabled and accelerated by the following hardware:

- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features
- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches
- Advanced high assurance boot (A-HAB)—HAB with the next embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization

1.3 Ordering Information

Table 1 provides the ordering information.

Table 1. Ordering Information

Part Number	Maximum ARM CLK Frequency	Mask Set	Features	Temperature Range (°C)		Package ¹
				T _{ambient}	T _{junction}	
MCIMX508CVK1B	1 GHz	N78A	Full Specification	0 to 70	0 to 90	13 x 13 mm, 0.5 mm pitch BGA Case: 416 MAPBGA
MCIMX508CVM1B	1 GHz	N78A	Full Specification	0 to 70	0 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA
MCIMX508CVK8B	800 MHz	N78A	Full Specification	0 to 70	0 to 90	13 x 13 mm, 0.5 mm pitch BGA Case: 416 MAPBGA
MCIMX508CZK8B	800 MHz	N78A	Full Specification	0 to 70	0 to 90	13 x 13 mm, 0.5 mm pitch BGA Case: 416 PoPBGA
MCIMX508CVM8B	800 MHz	N78A	Full Specification	0 to 70	0 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA
MCIMX507CVM1B	1 GHz	N78A	No GPU	0 to 70	0 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA
MCIMX507CVK1B	1 GHz	N78A	No GPU	0 to 70	0 to 90	13 x 13 mm, 0.5 mm pitch BGA Case: 416 MAPBGA
MCIMX507CVM8B	800 MHz	N78A	No GPU	0 to 70	0 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA
MCIMX507CVK8B	800 MHz	N78A	No GPU	0 to 70	0 to 90	13 x 13 mm, 0.5 mm pitch BGA Case: 416 MAPBGA
MCIMX503CVK8B	800 MHz	N78A	No EPD controller	0 to 70	0 to 90	13 x 13 mm, 0.5 mm pitch BGA Case: 416 MAPBGA
MCIMX503CVM8B	800 MHz	N78A	No EPD controller	0 to 70	0 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA
MCIMX503EVM8B	800 MHz	N78A	No EPD controller, Extended Temperature	-20 to 70	-20 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA
MCIMX502CVK8B	800 MHz	N78A	No GPU, no EPD controller	0 to 70	0 to 90	13 x 13 mm, 0.5 mm pitch BGA Case: 416 MAPBGA
MCIMX502CVM8B	800 MHz	N78A	No GPU, no EPD controller	0 to 70	0 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA
MCIMX502EVM8B	800 MHz	N78A	No GPU, no EPD controller, Extended Temperature	-20 to 70	-20 to 90	17 x 17 mm, 0.8 mm pitch BGA Case: 400 MAPBGA

¹ Case MAPBGA is RoHS compliant, lead-free MSL (Moisture Sensitivity Level) 3.

1.4 Part Number Feature Comparison

Table 2 provides an overview of the feature differences between the i.MX50 part numbers.

Table 2. Part Number Feature Comparison

Part Number	Disabled Features	Comments
MCIMX508	None	
MCIMX507	GPU	
MCIMX503	EPDC	The i.MX503 has the same ball map and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX503, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.
MCIMX502	GPU, EPDC	The i.MX502 has the same ball map and IOMUX as the i.MX508. The EPDC pins still exist on the i.MX502, but because the EPDC block is disabled, those pins cannot be used for EPDC functionality (ALT0) and must be configured in the IOMUX with another ALT-mode setting.

1.5 Package Feature Comparison

Table 3 provides an overview of the feature and pin differences between the i.MX50 packages.

Table 3. Package Feature Comparison

Package	Dimensions	I/O Pin Differences Versus 416 MAPBGA	Notes on Package Differences
416 MAPBGA	13 x 13 mm, 0.5 mm pitch	—	<ul style="list-style-type: none"> USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the 416 MAPBGA package substrate. USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the 416 MAPBGA package substrate.
416 PoPBGA	13 x 13 mm, 0.5 mm pitch	<p>Deleted Pins: DRAM_A10 DRAM_A11 DRAM_A12 DRAM_A13 DRAM_A14 DRAM_CAS DRAM_OPEN DRAM_OPENFB DRAM_RAS DRAM_SDBA0 DRAM_SDBA1 DRAM_SDBA2 DRAM_SDCLK_1 DRAM_SDCLK_1_B DRAM_SDODT0 DRAM_SDODT1 DRAM_SDWE DRAM_OPEN DRAM_OPENFB</p> <p>Added Pins: POP_EMMC_RST POP_LPDDR2_ZQ0 POP_LPDDR2_ZQ1 POP_LPDDR2_1.8V POP_NAND_VCC</p>	<ul style="list-style-type: none"> The i.MX50 PoPBGA package supports 168-FBGA LPDDR2 DRAM memory only. It is not possible to support LPDDR1 or DDR2 on the i.MX50 PoPBGA. i.MX50 PoPBGA was designed to accommodate a combined LPDDR2 / eMMC PoP memory. The PoP eMMC device uses the SD3_DATA[7:0], SD3_CLK, and SD3_CMD pins. Because the PoP eMMC I/O and memory supplies are tied together on the substrate, 1.8 V eMMC I/O operation is not supported for the PoP eMMC device. POP_NAND_VCC and NVCC_NANDF must use a 3 V supply. The NVCC_EMI_DRAM power pins supply 1.2 V power to the i.MX50 DRAM controller as well as the PoP LPDDR2 DRAM. Additional PoP package pin descriptions may be found in the Special Signals Considerations section (Table 5). On the PoPBGA package, the DRAM Address, Data, and clock pins are routed to the bottom balls for Freescale test purposes only. It is recommended that these bottom DRAM pins are left unconnected on the customer PCB. USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the 416 PoPBGA package substrate. USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the 416 PoPBGA package substrate.
400 MAPBGA	17 x 17 mm, 0.8 mm pitch	<p>Deleted Pins: DRAM_SDCLK_1 DRAM_SDCLK_1_B DRAM_A14 DRAM_SDODT1 UART2_CTS UART2_RTS</p>	<ul style="list-style-type: none"> USB_OTG_VDDA25 and USB_H1_VDDA25 are independent and NOT shorted together on the 400 MAPBGA package substrate. USB_OTG_VDDA33 and USB_H1_VDDA33 are independent and NOT shorted together on the 400 MAPBGA package substrate.

2 Architectural Overview

The following sections provide an architectural overview of the i.MX50 processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX50 processor system.

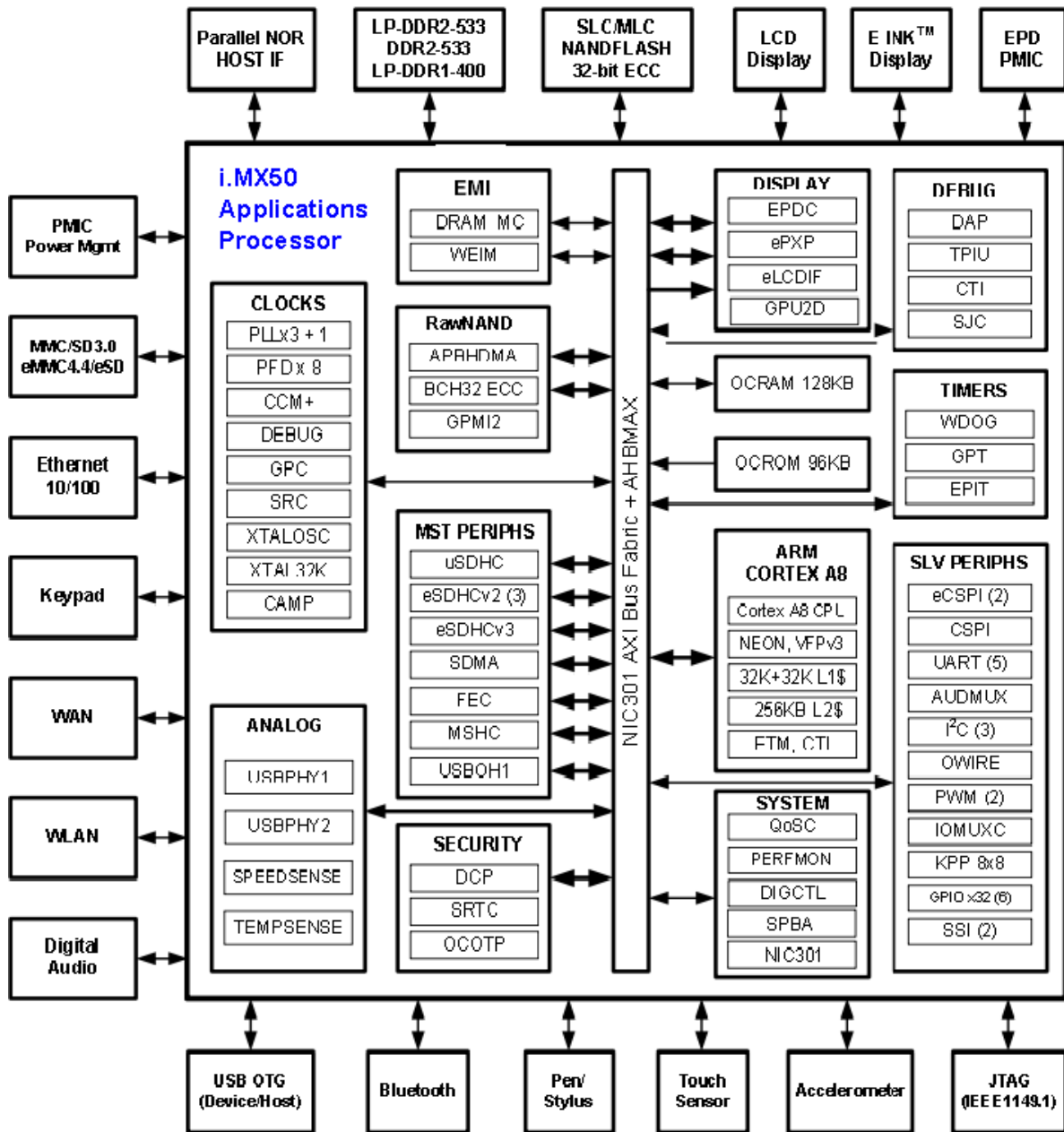


Figure 1. i.MX50 System Block Diagram

NOTE

The numbers in brackets indicate the number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

3 Modules List

The i.MX50 processor contains a variety of digital and analog modules that are described in [Table 4](#) in alphabetical order.

Table 4. i.MX50 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM Cortex-A8	ARM Cortex-A8 Platform	ARM	The ARM Cortex-A8 Core Platform consists of the ARM Cortex-A8 processor and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON coprocessor with SIMD media processing architecture, register file with 32 × 64-bit general-purpose registers, an Integer execute pipeline (ALU, Shift, MAC), dual, single-precision floating point execute pipeline (FADD, FMUL), load/store and permute pipeline, and a non-pipelined vector floating point (VFP Lite) coprocessor supporting VFPv3.
EPDC	Electrophoretic Display Controller	Display Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels supporting a wide variety of TFT backplanes.
eXPX	enhanced PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations such as color-space conversion, alpha blending, gamma-mapping, and rotation. The eXPX is enhanced with features specifically for grayscale applications. In addition, the eXPX supports traditional pixel/frame processing paths for still-image and video processing applications allowing it to interface with the integrated LCD controller (eLCDIF).
eLCDIF	enhanced LCD Interface	Display Peripherals	The eLCDIF is a high-performance LCD controller interface supporting a rich set of modes allowing inter operability with a wide variety of LCD panels, including DOTCK/RGB and smart panels. The module also supports a synchronous operation with the eXPX to allow the processed frames to be passed from the eXPX to the eLCDIF through an on-chip SRAM buffer. The eLCDIF can support up to 32-bit interfaces.
AUDMUX	Digital Audio Mux	Slave Connectivity Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1 and SSI2) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has six ports (two internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CAMP-1	Clock Amplifier	Clocks, Resets, and Power Control	Clock Amplifier

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for system power management. The system includes four PLLs.
CSPI eCSPI-1 eCSPI-2	Configurable SPI, Enhanced CSPI	Slave Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rate up to 66.5 Mbit/s (for eCSPI, master mode). It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
DAP TPIU CTI	Debug System	System Control Peripherals	The Debug System provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, three cross-system triggers (CTI), counters, and sequencers. Debug access port (DAP)—The DAP provides real-time access for the debugger without halting the core to System memory and peripheral registers. All debug configuration registers and Debugger access to JTAG scan chains.
DRAM MC	DRAM Memory Controller	External Memory Interface	The DRAM MC consists of a DRAM memory controller and PHY, supporting LPDDR2, DDR2, and LPDDR1 memories with clock frequencies up to 266 MHz with 32-bit interface. It is tightly linked with the system bus fabric and employs advanced arbitration mechanism to maximize DRAM bandwidth efficiency.
EIM	Static Memory Controller	External Memory Interface	The EIM is an external static memory and generic host interface. It supports up to a 32-bit interface (through pin-muxing) or a dedicated 16-bit muxed interface. It can be used to interface to PSRAMs (sync and async), NOR-flash or any external memory mapped peripheral.
BCH32/GPMI2	Raw NAND System with ECC	RawNAND and SSP Peripherals	The i.MX50 contains a fully hardware accelerated raw NAND flash solution supporting SLC and MLC devices. The system consists of the GPMI2 module, which is driven by the APBH DMA engine to perform the NAND flash interface function (supporting up to ONFI2.1). Coupled with the GPMI2 is the BCH32 hardware error-correction engine which is an AXI bus-master and supports up to 32-bits of correction over block sizes up to 1 Kbyte (that is, supports up to 2 Kbyte code-size).
System Fabric and QoS	System Fabric and QoS	System Peripherals	In order to aggregate the multitude of masters and memory mapped devices, the i.MX50 contains a next-generation AMBA3 AXI bus fabric. In addition, the i.MX50 contains a Quality of Service Controller IP (QoSC) which allows both soft priority control and dynamic priority elevation. Software priority control works for all masters but dynamic hardware control only works for EPDC and eLCDIF.
EPIT	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit <i>set and forget</i> timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eSDHCv3-3 (eMMC 4.4)	Ultra-High-Speed Multi-Media Card/ Secure Digital card host controller, ver. 3	Master Connectivity Peripherals	Ultra High-Speed eSDHC, enhanced to support eMMC 4.4 standard specification, for 832 Mbps. IP is backward compatible to eSDHCv2 IP. See complete features listing in eSDHCv2 entry below. Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port).
eSDHCv2-1 eSDHCv2-2 eSDHCv2-4	Enhanced Multi-Media Card/ Secure Digital Host Controller, ver. 2		In Enhanced Multi-Media Card/Secure Digital Host Controller the Ports 1, 2, and 4 are compatible with the <i>MMC System Specification</i> version 4.3, full support The generic features of the eSDHCv2 module, when serving as SD/MMC host, include the following: <ul style="list-style-type: none"> • Can be configured either as SD/MMC controller • Supports eSD and eMMC standard, for SD/MMC embedded type cards • Conforms to <i>SD Host Controller Standard Specification</i> version 2.0, full support • Compatible with the SD Memory Card Specification version 1.1 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: <ul style="list-style-type: none"> —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full/High speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines
FEC	Fast Ethernet Controller	Master Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6	General Purpose I/O Modules	Slave Connectivity Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit <i>free-running</i> or <i>set and forget</i> mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU2Dv1	Graphics Processing Unit-2D, ver. 1	Display Peripherals	The GPU2Dv1 provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution.
I ² C-1 I ² C-2 I ² C-3	I ² C Interface	Connectivity Peripherals	I ² C provides serial interface for controlling peripheral devices. Data rates of up to 400 kbps are supported.
OCOTP Controller	On-chip OTP controller	Security Peripherals	The on-chip one-time -programmable (OCOTP) ROM serves the functions of hardware and software capability bits, Freescale operations and unique-ID, the customer-programmable cryptography key, and storage of various ROM and general purpose configuration bits.
IOMUXC	IOMUX Control	Slave Connectivity Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
KPP	Keypad Port	Slave Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: <ul style="list-style-type: none"> • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
OWIRE	One-Wire Interface	Slave Connectivity Peripherals	One-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example, Dallas DS2502.
PWM-1 PWM-2	Pulse Width Modulation	Slave Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
RAM 128 Kbytes	Internal RAM	Internal Memory	The On-Chip Memory controller (OCRAM) module, is an interface between the system's AXI bus, to the internal (on-chip) SRAM memory module. It is used for controlling the 128 Kbyte multimedia RAM, through a 64-bit AXI bus.
ROM 96 Kbytes	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. The ROM Controller supports ROM Patching.

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	Master Connectivity Peripherals	<p>The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by offloading various cores in dynamic data routing. The SDMA features list is as follows:</p> <ul style="list-style-type: none"> • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle uni-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API is available
SJC	Secure JTAG Controller	System Control Peripherals	<p>The Secure JTAG Controller provides a mechanism for regulating JTAG access, preventing unauthorized JTAG usage while allowing JTAG access for manufacturing tests and software debugging.</p> <p>The i.MX50 JTAG port provides debug access to several hardware blocks including the ARM processor and the system bus, therefore, it must be accessible for initial laboratory bring-up, manufacturing tests and troubleshooting, and for software debugging by authorized entities. However, if the JTAG port is left unsecured it provides a method for executing unauthorized program code, getting control over secure applications, and running code in privileged modes.</p> <p>The Secure JTAG controller provides three different security modes that can be selected through an e-fuse configuration to prevent unauthorized JTAG access.</p>
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	<p>SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.</p>
SRTC	Secure Real Time Clock	Security Peripherals	<p>The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC. The NVCC_SRTC can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR marks the event (security violation indication).</p>

Table 4. i.MX50 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2	I2S/SSI/AC97 Interface	Slave Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX50 processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.
Temperature Monitor	Temp Sensor	Analog	The temperature sensor is an internal module to the i.MX50 that monitors the die temperature.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface, ver. 2	Slave Connectivity Peripherals	Each of the UARTv2 modules supports the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps)
USB-OH-1	USB 2.0 High-Speed OTG-capable and Host ports	Master Connectivity Peripherals	USB-OH-1 supports USB2.0 HS/FS/LS, and contains: <ul style="list-style-type: none"> • One high-speed OTG-capable module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY
WDOG-1	Watch Dog	Timer Peripherals	The Watchdog (WDOG) timer module protects against system failures by providing a method of escaping from unexpected events or programming errors. The WDOG Timer supports two comparison points during each counting period. Each of the comparison points is configurable to invoke an interrupt to the ARM core, and a second point invokes an external event on the WDOG line.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module combined with an external 24 MHz crystal with load capacitors implements a crystal oscillator.

3.1 Special Signal Considerations

Table 5 lists special signal considerations for the i.MX50. The signal names are listed in alphabetical order. The package contact assignments are found in Section 5, “Package Information and Contact Assignments.” The signal descriptions are defined in the *MCIMX50 Applications Processor Reference Manual* (MCIMX50RM).

Table 5. Special Signal Considerations

Signal Name	Remarks
BOOT_MODE0, BOOT_MODE1	These two input pins are sampled out of reset and set the boot mode. For Internal boot, they should be set to 00. For Internal Fuse Only boot, they should be set to 10. For USB downloader, they should be set to 11. The BOOTMODE pins are in the NVCC_RESET domain and include an internal 100K pull-up resistor at start-up.
BOOT_CONFIG1[7:0], BOOT_CONFIG2[7:0], BOOT_CONFIG3[7:0]	These 24 pins are the GPIO boot override pins and may be driven at power up to select the boot mode. They are sampled 4 x CKIL clock cycles after POR is de-asserted. Consult the “System Boot” chapter of the Reference Manual for more details. Note that these are not dedicated pins: the BOOT_CONFIG pins appear over 24 pins of the EIM interface.
BT_LPB_FREQ[1:0]	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the BT_LPB_FREQ[1:0] pins will be sampled to determine the ARM core frequency. Consult the “System Boot” chapter of the Reference Manual for more details. Note that these are not dedicated pins: BT_LPB_FREQ0 appears on SSI_TXFS and BT_LPB_FREQ1 appears on SSI_TXC.
CHGR_DET_B	This is the USB Charger Detect pin. It is an open drain output pin that expects a 100 K pull-up. This pin is asserted low when a USB charger is detected on the OTG PHY DP and DM. This detection occurs with the application of VBUS. This pin is a raw sensor output and care must be taken to follow the system timings outlined in the USB charger specification Rev 1.1. The maximum current leakage at this pin is 8.5 μ A. This pin can be controlled by software control as well. If not used, this pin should be tied to ground or left floating.
CKIH	This is an input to the CAMPs (Clock Amplifiers), which include on-chip AC-coupling precluding the need for external coupling capacitors. The CAMPs are enabled by default, but the main clocks feeding the on-chip clock tree are sourced from XTAL/EXTAL by default. Optionally, the use of a low jitter external oscillators to feed CKIH (while not required) can be an advantage if low jitter or special frequency clock sources are required by modules sourced by CKIH. See CCM chapter in the <i>MCIMX50 Applications Processor Reference Manual</i> (MCIMX50RM) for details on the respective clock trees. After initialization, the CAMPs may be disabled if not used by programming the CCR CAMPx_EN field. If disabled, the on-chip CAMP output is low and the input is irrelevant. CKIH is on the NVCC_JTAG power domain, so the input clock amplitude should not exceed NVCC_JTAG. If unused, the user should tie CKIH to GND for best practice.
CKIL/ECKIL	The user must tie a fundamental mode 32.768 K crystal across ECKIL and CKIL. The target ESR should be 50 K or less. The bias resistor for the amplifier is integrated and approximately 14 M Ω . The target load capacitance for the crystal is approximately 10 pF. The load capacitors on the board should be slightly less than double this value after taking parasitics into account. While driving in an external 32 KHz signal into ECKIL, CKIL should be left floating so that it biases. A differential amplifier senses these two pins to propagate the clock inside the i.MX508. Care must be taken to minimize external leakages on ECKIL and CKIL. If they are significant to the 14 M Ω feedback or 1 μ A, then loss of oscillation margin or cessation of oscillation may result.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_OPEN, DRAM_OPENFB (for 416 MAPBGA and 400 MAPBGA)	These pins are the echo gating output and feedback pins used by the DRAM PHY to bound a window around the DQS transition. For an application using a single DRAM device, these pins should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (DRAM_SDCLK0 + DRAM_SDQS0). For an application using two DRAM devices, they should be routed so that the trace length (DRAM_OPEN + DRAM_OPENFB) = trace length (AVG(DRAM_SDCLK0+DRAM_SDCLK1) + AVG (DRAM_SDQS0_to_Device0 + DRAM_SDQS0_to_Device1)). This connection is required for LPDDR1, LPDDR2, and DDR2. For the i.MX50 PoP package, these signals are connected on the substrate.
DRAM_SDOdT0 (for 416 MAPBGA and 400 MAPBGA), DRAM_SDOdT1 (for 416 MAPBGA only)	These pins are the On-die termination outputs from the i.MX50. For DDR2, these pins should be connected to the DDR2 DRAM ODT pins. For LPDDR1 and LPDDR2, these pins should be left floating. Note that both SDOdT pins are removed on the 416 PoPBGA package, and only SDOdT0 exists on the 400 MAPBGA package.
DRAM_CALIBRATION	This pin is the ZQ calibration used to calibrate DRAM Ron and ODT. For LPDDR2, this pin should be connected to ground through a 240 Ω 1% resistor. For DDR2 and LPDDR1, this pin should be connected to ground through a 300 Ω 1% resistor.
JTAG_MOD	This input has an internal 100K pull-up, by default. Note that JTAG_MOD is referenced as SJC_MOD in the <i>MCIMX50 Applications Processor Reference Manual</i> (MCIMX50RM) - both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. If JTAG port is not needed, the internal pull-up can be disabled in order to reduce supply current to the pin.
JTAG_TCK	This input has an internal 100K pull-down. This pin is in the NVCC_JTAG domain.
JTAG_TDI	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TDO	This is a 3-state output with an internal gate keeper enable to prevent a floating condition. An external pull-up or pull-down resistor on JTAG_TDO is detrimental and should be avoided. This pin is in the NVCC_JTAG domain.
JTAG_TMS	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
JTAG_TRSTB	This input has an internal 47K pull-up to NVCC_JTAG. This pin is in the NVCC_JTAG domain.
NC	These signals are No Connect (NC) and should be floated by the user.
LOW_BATT_GPIO	If the LOW_BATT_GPIO (UART4_TXD) is asserted at power up, the i.MX50 will boot up at a lower ARM clock frequency to reduce system power. The actual ARM clock frequency used when LOW_BATT_GPIO is asserted is determined by the BT_LPB_FREQ[1:0] pins (220 MHz to 55.3 MHz). The polarity of the LOW_BATT_GPIO is active high by default, but may be set to active low by setting the LOW_BATT_GPIO_LEVEL OTP bit. See the “System Boot” chapter of the Reference Manual for more details. Note that this is not a dedicated pin: LOW_BATT_GPIO appears on the UART4_TXD pin.
PMIC_STBY_REQ	This output may be driven high when the i.MX50 enters the STOP mode to notify the PMIC to enter its low power standby state. This output is in the NVCC_SRTC domain.
PMIC_ON_REQ	This output from the i.MX50 can instruct the PMIC to turn on when the i.MX50 only has NVCC_SRTC power. This may be useful for an alarm application, as it allows the i.MX50 to turn off all blocks except for the RTC and then power on again at a specified time. This output is in the NVCC_SRTC domain.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
PMIC_RDY	This input may be used by a PMIC to signal to the i.MX50 that the PMIC supply outputs are at operating levels when resuming from STOP mode. The PMIC_RDY input is pin muxed on ALT3 of the I2C3_SCL pin and is in the NVCC_MISC domain.
POP_EMMC_RST (416 PoPBGA Only)	This pin is the PoP eMMC 4.4 Reset pin. The customer may connect this on their PCB to any free GPIO, or just leave floating for non-4.4 eMMC. This pin does not connect to the i.MX50 die.
POP_LPDDR2_ZQ0/ZQ1 (416 PoPBGA Only)	These pins connect to the PoP LPDDR2 DRAM ZQ pins and should be connected on the customer PCB to a 240 Ω 1% resistor to ground if used. These pins do not connect to the i.MX50 die.
POP_LPDDR2_1.8V (416 PoPBGA Only)	These pins are the 1.8 V supply for the PoP LPDDR2 DRAM. These pins do not connect to the i.MX50 die.
POP_NAND_VCC (416 PoPBGA Only)	This is the 3.3V I/O and memory supply for the PoP eMMC. Note that most eMMC can operate with a 1.8V I/O or a 3.3V I/O voltage. However, because we tied the eMMC memory and I/O domains together, you can't use the 1.8 V I/O option for the PoP eMMC, only 3.3 V I/O.
POR_B	This POWER-ON RESET input is a cold reset negative logic input that resets all modules and logic in the IC. The POR_B pin should have an external 68 K pull-up to NVCC_RESET and a 1 μ F capacitor to ground. Note: The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: <ul style="list-style-type: none"> • Test logic (JTAG, IOMUXC, DAP) • SRTC • Cold reset logic of WDOG—Some WDOG logic is only reset by POR_B. See WDOG chapter in the <i>MCIMX50 Applications Processor Reference Manual (MCIMX50RM)</i> for details.
SSI_EXT1_CLK, SSI_EXT2_CLK	The SSI_EXT1_CLK and SSI_EXT2_CLK outputs are recommended for generating a clock output from the i.MX50. Use of the CKO1 and CKO2 clock outputs is not recommended, as the large number of combinational logic muxes on those signals will impact jitter and duty-cycle. Note that these two clock outputs do not have dedicated pins: SSI_EXT1_CLK is IOMUX ALT3 on the OWIRE pin, and SSI_EXT2_CLK is IOMUX ALT3 of the EPITO pin.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
USB_H1_GPANAIO, USB_OTG_GPANAIO	These signals are reserved for Freescale manufacturing use only. Users should float these outputs.
USB_H1_RREFEXT, USB_OTG_RREFEXT	These signals determine the reference current for the USB PHY bandgap reference. An external 6.04 k Ω 1% resistor to GND is required. This resistor should be connected through a short (low impedance connection) and placed away from other noisy regions. If USB_H1 is not used, the H1 RREFEXT resistor may be eliminated and the pin left floating. If USB_OTG is not used, the OTG RREFEXT resistor may be eliminated and the pin left floating.

Table 5. Special Signal Considerations (continued)

Signal Name	Remarks
USB_H1_VBUS, USB_OTG_VBUS	These inputs are used by the i.MX50 to detect the presence and level of USB 5 V. If either VBUS input pin is connected to an external USB connector, there is a possibility that a fast 5 V edge rate during a cable attach could trigger the VBUS input ESD protection, which could result in damage to the i.MX50 silicon. To prevent this, the system should use some circuitry to prevent the 5 V edge rate from exceeding 5.25 V / 1 μ s. Freescale recommends the use of a low pass filter consisting of 100 Ω resistor in series and a 1 μ F capacitor close to the i.MX50 pin. In the case when the USB interface is connected on an on-board USB device (for example, 3G modem), the corresponding USB_VBUS pin may be left floating.
VREF	This pin is the DRAM MC reference voltage input. For LPDDR2 and DDR2, this pin should be connected to $\frac{1}{2}$ of NVCC_EMI_DRAM. For LPDDR1, this pin should be left floating. The user may generate VREF using a precision external resistor divider. Use a 1 k Ω 0.5% resistor to GND and a 1 k Ω 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 μ F capacitor.
WDOG_B	This output can be used to reset the system PMIC when the i.MX50 processor is locked up. This output is in the NVCC_MISC domain.
WDOG_RST_B_DEB	This output may be used to drive out the internal system reset signal to the system reset controller. This is only intended for debug purposes.
XTAL/EXTAL	These pins are the 24 MHz crystal driver as well as the external 24 MHz clock input. If using these pins to directly drive a 24 MHz crystal: <ul style="list-style-type: none"> • The user should tie a 24 MHz fundamental-mode crystal across XTAL and EXTAL. • The crystal must be rated for a maximum drive level of 100 μW or higher. • The recommended crystal ESR (equivalent series resistance) is 80 Ω or less. If using these pins as a clock input from an external 24 MHz oscillator: <ul style="list-style-type: none"> • The crystal may be eliminated and EXTAL driven directly driven by the external oscillator. The clock signal level on EXTAL must swing from NVCC_SRTC to GND. • In this configuration, the XTAL pin must be floated and the COSC_EN bit (bit 12 in the CCR register in the Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. • Note there are strict jitter requirements if using an external oscillator in a USB application: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics of the i.MX50 processor.

NOTE

These electrical specifications are preliminary. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications are published after thorough characterization and device qualifications have been completed.

4.1 Chip-Level Conditions

This section provides the chip-level electrical characteristics for the IC. See [Table 6](#) for a quick reference to the individual tables and sections.

Table 6. i.MX50 Chip-Level Conditions

For these characteristics, see	Topic appears ...
Absolute Maximum Ratings	on page 21
13 x 13 mm MAPBGA Package Thermal Resistance Data	on page 22
13 x 13 mm PoPBGA Package Thermal Resistance Data	on page 23
17 x 17 mm MAPBGA Package Thermal Resistance Data	on page 23
Operating Ranges	on page 24
Operating Frequencies	on page 26
Supply Current	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under [Table 7](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in [Table 11](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral core supply voltage	VCC	-0.3	1.5	V
ARM core supply voltage	VDDGP	-0.3	1.35	V
Bandgap and 480 MHz PLL supply	VDD3P0	-0.5	3.6	V
PLL digital supplies	VDD1P2	-0.3	1.35	V
PLL analog supplies	VDD1P8	-0.3	2.25	V
Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	VDD2P5	-0.5	2.85	V
Memory array supply	VDDA/VDDAL1	-0.5	1.35	V
Supply voltage (HVIO)	Supplies denoted as I/O supply	-0.5	3.6	V
Supply voltage (GPIO, LVIO)	Supplies denoted as I/O supply	-0.5	3.3	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD + 0.3 ¹	V
USB VBUS	VBUS			V
DC		—	6.00	
Transient (t<30ms, duty cycle < 0.05%)		—	7.00	

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity:	V_{esd}			V
Human Body Model (HBM)		—	2000	
Charge Device Model (CDM)		—	500	
Storage temperature range	T_{STORAGE}	-40	125	°C

¹ The term OVDD in this section refers to the associated supply rail of an input or output. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance Data

4.1.2.1 13 x 13 mm MAPBGA Package Thermal Resistance Data

Table 8 provides thermal resistance data for a 13 x 13 mm MAPBGA package.

Table 8. 13 x 13 mm MAPBGA Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection) ^{1, 2}	Single layer board (1s)	$R_{\theta\text{JA}}$	51	°C/W
Junction to Ambient (natural convection) ^{1, 2, 3}	Four layer board (2s2p)	$R_{\theta\text{JA}}$	28	°C/W
Junction to Ambient (at 200 ft/min) ^{1, 3}	Single layer board (1s)	$R_{\theta\text{JMA}}$	40	°C/W
Junction to Ambient (at 200 ft/min) ^{1, 3}	Four layer board (2s2p)	$R_{\theta\text{JMA}}$	24	°C/W
Junction to Board ⁴	—	$R_{\theta\text{JB}}$	14	°C/W
Junction to Case ⁵	—	$R_{\theta\text{JC}}$	9	°C/W
Junction to Package Top (natural convection) ⁶	—	Ψ_{JT}	2	°C/W

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per JEDEC JESD51-2 with the single layer board horizontal. The thermal test board meets JESD51-9 specification.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.2.2 13 x 13 mm PoPBGA Package Thermal Resistance Data

Table 9 provides thermal resistance data for a 13 x 13 mm PoPBGA package.

Table 9. 13 x 13 mm PoPBGA Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection) ^{1, 2}	Single layer board (1s)	$R_{\theta JA}$	57	°C/W
Junction to Ambient (natural convection) ^{1, 2, 3}	Four layer board (2s2p)	$R_{\theta JA}$	31	°C/W
Junction to Ambient (at 200 ft/min) ^{1, 3}	Single layer board (1s)	$R_{\theta JMA}$	46	°C/W
Junction to Ambient (at 200 ft/min) ^{1, 3}	Four layer board (2s2p)	$R_{\theta JMA}$	28	°C/W
Junction to Board ⁴	—	$R_{\theta JB}$	18	°C/W
Junction to Case ⁵	—	$R_{\theta JC}$	6	°C/W
Junction to Package Top (natural convection) ⁶	—	Ψ_{JT}	2	°C/W

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- ² Per JEDEC JESD51-2 with the single layer board horizontal. The thermal test board meets JESD51-9 specification.
- ³ Per JEDEC JESD51-6 with the board horizontal.
- ⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- ⁵ Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).
- ⁶ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.2.3 17 x 17 mm MAPBGA Package Thermal Resistance Data

Table 10 provides thermal resistance data for a 17 x 17 mm MAPBGA package.

Table 10. 17 x 17 mm MAPBGA Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection) ^{1, 2}	Single layer board (1s)	$R_{\theta JA}$	53	°C/W
Junction to Ambient (natural convection) ^{1, 2, 3}	Four layer board (2s2p)	$R_{\theta JA}$	30	°C/W
Junction to Ambient (at 200 ft/min) ^{1, 3}	Single layer board (1s)	$R_{\theta JMA}$	44	°C/W
Junction to Ambient (at 200 ft/min) ^{1, 3}	Four layer board (2s2p)	$R_{\theta JMA}$	26	°C/W
Junction to Board ⁴	—	$R_{\theta JB}$	19	°C/W
Junction to Case ⁵	—	$R_{\theta JC}$	8	°C/W
Junction to Package Top (natural convection) ⁶	—	Ψ_{JT}	2	°C/W

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- ² Per JEDEC JESD51-2 with the single layer board horizontal. The thermal test board meets JESD51-9 specification.

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- ³ Per JEDEC JESD51-6 with the board horizontal.
- ⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- ⁵ Thermal resistance between the die and the case top surface as measured by using the cold plate method (MIL SPEC-883 Method 1012.1).
- ⁶ Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Table 11 provides the operating ranges of the i.MX50 processor.

Table 11. i.MX50 Operating Ranges

Symbol	Parameter	Minimum ¹	Nominal ²	Maximum ¹	Unit
VDDGP	ARM core supply voltage $f_{\text{ARM}} = 1 \text{ GHz}$	1.20	1.275	1.35	V
	ARM core supply voltage $400 < f_{\text{ARM}} \leq 800 \text{ MHz}$	0.95	1.05	1.15	V
	ARM core supply voltage $167 < f_{\text{ARM}} \leq 400 \text{ MHz}$	0.85	0.95	1.15	V
	ARM core supply voltage $24 \leq f_{\text{ARM}} \leq 167 \text{ MHz}$	0.8	0.9	1.15	V
	ARM core supply voltage Stop mode	0.75	0.85	1.15	V
VCC	Peripheral supply voltage Low Performance mode (LPM). The DDR clock rate is 24 MHz.	1 ³	1.05	1.275	V
	Peripheral supply voltage Reduced Performance mode (RPM). The DDR clock rate is 133 MHz.	1 ³	1.05	1.275	V
	Peripheral supply voltage High Performance mode (HPM). The clock frequencies are derived from AHB bus using 133 MHz and AXI bus using 266 MHz (as needed). The DDR clock rate is 266 MHz.	1.175	1.225	1.275	V
	Peripheral supply voltage Stop mode	0.9 ³	0.95	1.275	V
VDDA/VDDAL1	Memory arrays voltage—Run mode $24 \leq f_{\text{ARM}} \leq 800 \text{ MHz}$	1.15	1.20	1.275	V
	Memory arrays voltage—Run mode $f_{\text{ARM}} = 1 \text{ GHz}$	1.25	1.30	1.35	V
	Memory arrays voltage—Stop mode	0.9	0.95	1.275	V
VDD3P0	Bandgap and 480 MHz PLL supply	2.7	3.0	3.3	V
VDD2P5	Efuse, 24 MHz oscillator, 32 kHz oscillator mux supply	2.375	2.5	2.625	V
VDD1P2	PLL digital supplies	1.15	1.2	1.32	V
VDD1P8	PLL analog supplies	1.75	1.8	1.95	V

Table 11. i.MX50 Operating Ranges (continued)

Symbol	Parameter	Minimum ¹	Nominal ²	Maximum ¹	Unit
NVCC_JTAG	GPIO digital power supplies	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR supply DDR2/LPDDR1 range	1.71	1.8	1.95	V
	DDR supply LPDDR2 range	1.14	1.2	1.3	V
VREF	DRAM Reference Voltage Input		1/2 NVCC_EMI_DRAM		
VDDO25	EMI Pad Predriver supply	2.375	2.5	2.625	V
NVCC_NANDF NVCC_SD1 NVCC_SD2 NVCC_KEYPAD NVCC_EIM NVCC_EPDC NVCC_LCD NVCC_MISC NVCC_SPI NVCC_SSI NVCC_UART	High voltage I/O (HVIO) supplies HVIO_L HVIO_H	1.65 2.7	1.875 3.0	1.95 3.3	V
NVCC_SRTC	SRTC core and I/O supply (LVIO)	1.1	1.2	1.3	V
NVCC_RESET	LVIO	1.65	1.875 or 2.775	3.1	V
USB_H1_VDDA25 USB_OTG_VDDA25 ⁴	USB_PHY analog supply	2.25	2.5	2.75	V
USB_H1_VDDA33 USB_OTG_VDDA33 ⁵	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 7 and Table 78 for details. This is not a power supply.	—	—	—	—
T _A	Ambient Temperature, Consumer	0	—	70	°C
T _A	Extended Ambient Temperature, Consumer	-20	—	70	°C
T _j	Junction Temperature, Consumer	0	—	90	°C
T _j	Extended Junction Temperature, Consumer	-20	—	90	°C

¹ Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

² The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

³ VCC minimum voltage is 1.02 V for extended temperature (-20°C) devices.

⁴ USB_OTG_VDDA25 and USB_H1_VDDA25 are shorted together on the 416 MAPBGA and 416 PoPBGA package substrates.

⁵ USB_OTG_VDDA33 and USB_H1_VDDA33 are shorted together on the 416 MAPBGA and 416 PoPBGA package substrates.