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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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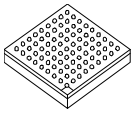
RoHS

IMX51



Package Information
Plastic Package
Case 2058 13 x 13 mm, 0.5 mm pitch
Case 2017 19 x 19 mm, 0.8 mm pitch

i.MX51 Applications Processors for Consumer and Industrial Products

Ordering Information
See Table 1 on page 3 for ordering information.

1 Introduction

The i.MX51 multimedia applications processors represent Freescale Semiconductor's latest addition to a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The i.MX51 processors feature Freescale's advanced and power-efficient implementation of the ARM Cortex™-A8 core, which operates at speeds as high as 800 MHz. Up to 200 MHz DDR2 and mobile DDR DRAM clock rates are supported. These devices are suitable for applications such as the following:

- Netbooks (web tablets)
- Nettops (Internet desktop devices)
- Mobile Internet devices (MID)
- Portable media players (PMP)
- Portable navigation devices (PND)
- High-end PDAs
- Gaming consoles
- Automotive navigation and entertainment (see automotive data sheet, IMX51AEC)

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Features include the following:

- **Smart Speed Technology**—The heart of the i.MX51 processors is a level of power management throughout the device that enables the rich suite of multimedia features and peripherals to achieve minimum system power consumption in both active and various low-power modes. Smart Speed Technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than typical industry expectations.
- **Applications Processor**—The i.MX51 processors boost the capabilities of high-tier portable applications by providing for the ever-increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) allows the device run at much lower voltage and frequency with sufficient MIPS for tasks such as audio decode resulting in significant power reduction.
- **Multimedia Powerhouse**—The multimedia performance of the i.MX51 processors is boosted by a multi-level cache system and further enhanced by a Multi-Standard Hardware Video Codec, autonomous Image Processing Unit, SD and HD720p Triple Video (TV) Encoder with triple video DAC, Neon (including Advanced SIMD, 32-bit Single-Precision floating point support and Vector Floating Point co-processor), and a programmable smart DMA (SDMA) controller.
- **Powerful Graphics Acceleration**—Graphics is the key to mobile game navigation, web browsing, and other applications. The i.MX51 processors provide two independent, integrated Graphics Processing Units: OpenGL ES 2.0 3D graphics accelerator (27 Mtri/s, 166 Mpix/s) and OpenVG 1.1 2D graphics accelerator (166 Mpix/s).
- **Interface Flexibility**—The i.MX51 processor interface supports connection to all popular types of external memories: DDR2, Mobile DDR, NOR Flash, PSRAM, Cellular RAM, NAND Flash (MLC and SLC), and OneNAND. Designers seeking to provide products that deliver a rich multimedia experience find a full suite of on-chip peripherals: LCD controller and CMOS sensor interface, High-Speed USB On-The-Go with PHY, and three High-Speed USB hosts, multiple expansion card ports (High-Speed MMC/SDIO Host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, I^2S serial audio, and SIM card, among others).
- **Increased Security**—Because the need for advanced security for mobile devices continues to increase, the i.MX51 processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the MX51 security features contact your Freescale representative.

1.1 Ordering Information

Table 1 provides the ordering information.

Table 1. Ordering Information[1]

Part Number[2,]	Mask Set	Features	Case Temperature Range (°C)	Package[3]
MCIMX512CJM6C	M77X	No hardware video codecs No hardware graphics accelerators	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX512DJM8C	M77X	No hardware video codecs No hardware graphics accelerators	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX513CJM6C	M77X	No hardware graphics accelerators	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX513DJM8C	M77X	No hardware graphics accelerators	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515CJM6C	M77X	Full specification	–40 to 95	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515DJM8C	M77X	Full specification	–20 to 85	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX515DVK8C!	M77X	Full specification	–20 to 85	13 x 13 mm, 0.5 mm pitch BGA Case 2058

1 For Junction Temperature (Tj) maximum ratings, see Table 11, "Absolute Maximum Ratings," on page 18.

2 Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: Indicated by the Icon (!)

3 Case 2017 and Case 2058 are RoHS compliant, lead-free, MSL = 3.

1.2 Block Diagram

Figure 1 shows the functional modules of the processor.

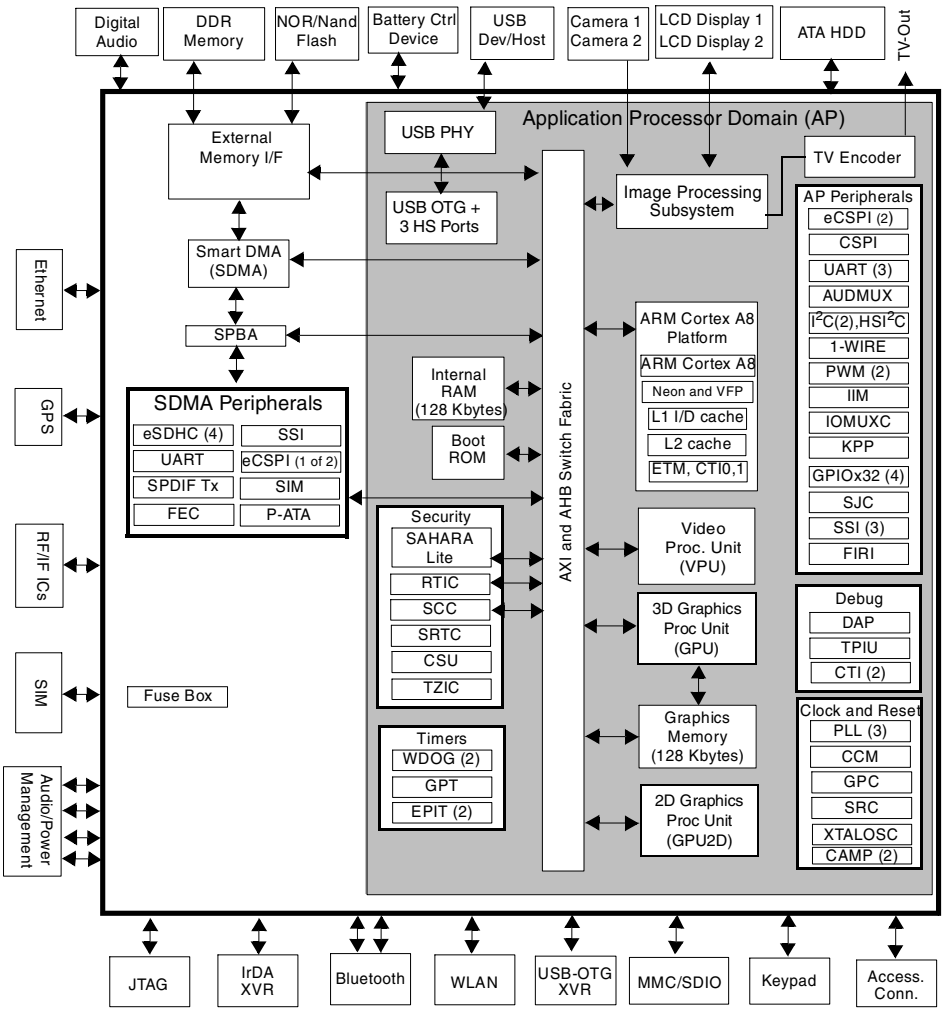


Figure 1. Functional Block Diagram

2 Features

The i.MX51 processor contains a large number of digital and analog modules that are described in Table 2.

Table 2. i.MX51 Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
1-WIRE	1-Wire Interface	Connectivity Peripherals	1-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example: Dallas DS2502.
ARM Cortex™-A8	ARM Cortex™-A8 Platform	ARM	The ARM Cortex™-A8 Core Platform consists of the ARM Cortex™-A8 processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the Level 2 Cache Controller, 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, and a 256 Kbyte L2 cache. The platform also contains an Event Monitor and Debug modules. It also has a NEON co-processor with SIMD media processing architecture, register file with 32 × 64-bit general-purpose registers, an Integer execute pipeline (ALU, Shift, MAC), dual, single-precision floating point execute pipeline (FADD, FMUL), load/store and permute pipeline and a Non-Pipelined Vector Floating Point (VFP) co-processor (VFPv3).
Audio Subsystem	Audio Subsystem	Multimedia Peripherals	The elements of the audio subsystem are three Synchronous Serial Interfaces (SSI1-3), a Digital Audio Mux (AUDMUX), and Digital Audio Out (SPDIF TX). See the specific interface listings in this table.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for system power management. The modules include three PLLs and a Frequency Pre-Multiplier (FPM).
CSPI-1, eCSPI-2 eCSPI-3	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 66.5 Mbit/s (for eCSPI, master mode). It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX51 platform, and for sharing security information between the various security modules. The Security Control Registers (SCR) of the CSU are set during boot time by the High Assurance Boot (HAB) code and are locked to prevent further writing.
Debug System	Debug System	System Control	The Debug System provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, cross-system triggers, counters, and sequencers.

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EMI	External Memory Interface	Connectivity Peripherals	The EMI is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels: fast memories (Mobile DDR, DDR2) channel, slow memories (NOR-FLASH/PSRAM/NAND-FLASH and so on) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) Channel. In order to increase the bandwidth performance, the EMI separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EMI features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (Read or Write) was the last access • Flexible bank interleaving • Supports 16/32-bit Mobile DDR up to 200 MHz SDCLK (mDDR400) • Supports 16/32-bit (Non-Mobile) DDR2 up to 200 MHz SDCLK (DDR2-400) • Supports up to 2 Gbit Mobile DDR memories • Supports 16-bit (in muxed mode only) PSRAM memories (sync and async operating modes), at slow frequency, for debugging purposes • Supports 32-bit NOR-Flash memories (only in muxed mode), at slow frequencies for debugging purposes • Supports 4/8-ECC, page sizes of 512 Bytes, 2 Kbytes and 4 Kbytes • NAND-Flash (including MLC) • Multiple chip selects • Enhanced Mobile DDR memory controller, supporting access latency hiding • Supports watermarking for security (Internal and external memories) • Supports Samsung OneNAND™ (only in muxed I/O mode)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
eSDHC-1 eSDHC-2 eSDHC-3	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to SD Host Controller Standard Specification version 2.0 • Compatible with the MMC System Specification version 4.2 • Compatible with the SD Memory Card Specification version 2.0 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eSDHC-4 (muxed with P-ATA)	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	Can be configured as eSDHC (see above) and is muxed with the P-ATA interface.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
FIRI	Fast Infra-Red Interface	Connectivity Peripherals	Fast Infra-Red Interface
GPIO-1 GPIO-2 GPIO-3 GPIO-4	General Purpose I/O Modules	System Control Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU	Graphics Processing Unit	Multimedia Peripherals	The GPU provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution. It supports color representation up to 32 bits per pixel. The GPU with its 128 KByte memory enables high performance mobile 3D and 2D vector graphics at rates up to 27 Mtriangles/sec, 166 Mpixels/sec, 664 Mpixels/sec (Z).
GPU2D	Graphics Processing Unit-2D Ver. 1	Multimedia Peripherals	The GPU2D provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution.
I^2C-1 I^2C-2 HS-I^2C	I^2C Interface	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 Kbps are supported by two of the I^2C ports. Data rates of up to 3.4 Mbps (I^2C Specification v2.1) are supported by the HS-I^2C. **Note:** See the errata for the HS-I^2C in the i.MX51 Chip Errata. The two standard I^2C modules have no errata.

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IIM	IC Identification Module	Security	The IC Identification Module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
IPU	Image Processing Unit	Multimedia Peripherals	IPU enables connectivity to displays and image sensors, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces. • Legacy Interfaces • Analog TV interfaces (through a TV encoder bridge) The processing includes: • Support for camera control • Image enhancement: color adjustment and gamut mapping, gamma correction and contrast enhancement, sharpening and noise reduction • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Synchronization and control capabilities, allowing autonomous operation. • Hardware de-interlacing support
KPP	Keypad Port	Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
P-ATA (Muxed with eSDHC-4	Parallel ATA	Connectivity Peripherals	The P-ATA block is an AT attachment host interface. Its main use is to interface with hard disc drives and optical disc drives. It interfaces with the ATA-5 (UDMA-4) compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side. This is muxed with eSDHC-4 interfaces.
PWM-1 PWM-2	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
RAM 128 Kbytes	Internal RAM	Internal Memory	Unified RAM, can be split between Secure RAM and Non-Secure RAM
ROM 36 Kbytes	Boot ROM	Internal Memory	Supports secure and regular Boot Modes

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
RTIC	Real Time Integrity Checker	Security	Protecting read-only data from modification is one of the basic elements in trusted platforms. The Run-Time Integrity Checker v3 (RTICv3) module, is a data monitoring device responsible for ensuring that memory content is not corrupted during program execution. The RTICv3 mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The RTICv3's purpose is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement, and assist with boot authentication.
SAHARA Lite	SAHARA security accelerator Lite	Security	SAHARA (Symmetric/Asymmetric Hashing and Random Accelerator) is a security co-processor. It implements symmetric encryption algorithms, (AES, DES, 3DES, and RC4), public key algorithms, hashing algorithms (MD5, SHA-1, SHA-224, and SHA-256), and a hardware random number generator. It has a slave IP bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.
SCC	Security Controller	Security	The Security Controller is a security assurance hardware module designed to safely hold sensitive data such as encryption keys, digital right management (DRM) keys, passwords, and biometrics reference data. The SCC monitors the system's alert signal to determine if the data paths to and from it are secure—that is, cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCC also features a Key Encryption Module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex™-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API are available
SIM	Subscriber Identity Module Interface	Connectivity Peripherals	The SIM is an asynchronous interface with additional features for allowing communication with Smart Cards conforming to the ISO 7816 specification. The SIM is designed to facilitate communication to SIM cards or pre-paid phone cards.

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SJC	Secure JTAG Interface	System Control Peripherals	JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX51 processor incorporates a mechanism for regulating JTAG access. The i.MX51Secure JTAG Controller provides four different JTAG security modes that can be selected via e-fuse configuration.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Only the transmitter functionality is supported.
SRTC	Secure Real Time Clock	Security	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication).
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX51 processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two timeslots are being used simultaneously.
TVE	TV Encoder	Multimedia	The TVE is implemented in conjunction with the Image Processing Unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports the following analog video outputs: composite, S-video, and component video up to HD720p/1080i.
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone Interrupt Controller (TZIC) collects interrupt requests from all i.MX51 sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.

Table 2. i.MX51 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
UART-1 UART-2 UART-3	UART Interface	Connectivity Peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7 or 8 bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and previous Freescale UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USB	USB 2.0 High-Speed OTG and 3x Hosts	Connectivity Peripherals	USB-OTG contains one high-speed OTG module, which is internally connected to the on-chip HS USB PHY. There are an additional three high-speed host modules that require external USB PHYs.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing such as rotation and mirroring. VPU Features: • MPEG-4 decode: 720p, 30 fps, simple profile and advanced simple profile • MPEG-4 encode: D1, 25/30 fps, simple profile • H.263 decode: 720p, 30 fps, profile 3 • H.263 encode: D1, 25/30 fps, profile 3 • H.264 decode: 720p, 30 fps, baseline, main, and high profile • H.264 encode: D1, 25/30 fps, baseline profile • MPEG-2 decode: 720p, 30 fps, MP-ML • MPEG-2 encode: D1, 25/30 fps, MP-ML (in software with partial acceleration in hardware) • VC-1 decode: 720p, 30 fps, simple, main, and advanced profile • DivX decode: 720p, 30 fps versions 3, 4, and 5 • RV10 decode: 720p, 30 fps • MJPEG decode: 32 Mpix/s • MJPEG encode: 64 Mpix/s
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. This situation should be avoided, as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module allows connectivity to an external crystal.

2.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX51. The signal names are listed in alphabetical order. The package contact assignments are found in Section 5, "Package Information and Contact Assignments." Signal descriptions are defined in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM).

Table 3. Special Signal Considerations

Signal Name	Remarks
CKIH1, CKIH2	Inputs feeding CAMPs (Clock Amplifiers) that have on-chip ac coupling precluding the need for external coupling capacitors. The CAMPs are enabled by default, but the main clocks feeding the on-chip clock tree are sourced from XTAL/EXTAL by default. Optionally, the use of a low jitter external oscillators to feed CKIH1 or CKIH2 (while not required) can be an advantage if low jitter or special frequency clock sources are required by modules driven by CKIH1 or CKIH2. See CCM chapter in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details on the respective clock trees. After initialization, the CAMPs could be disabled (if not used) by CCM registers (CCR CAMPx_EN field). If disabled, the on-chip CAMP output is low; the input is irrelevant. If unused, the user should tie CKIH1/CKIH2 to GND for best practice.
CLK_SS	Clock Source Select is the input that selects the default reference clock source providing input to the DPLLs. To use a reference in the megahertz range per Table 8, tie CLK_SS to GND to select EXTAL/XTAL. To use a reference in the kilohertz range per Table 59, tie CLK_SS to NVCC_PER3 to select CKIL. After initialization, the reference clock source can be changed (initial setting is overwritten). **Note:** Because this input has a keeper circuit, Freescale recommends tying this input to directly to GND or NVCC_PER3. If a series resistor is used its value must be $\leq$ 4.7 kΩ.
COMP	The user should bypass this reference with an external 0.1 µF capacitor tied to GND. If TV OUT is not used, float the COMP contact and ensure the DACs are powered down. **Note:** Previous engineering samples required this reference to be bypassed to a positive supply.
FASTR_ANA and FASTR_DIG	These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND.
GPANAIO	This signal is reserved for Freescale manufacturing use only. Users should float this output.
GPIO_NAND	This is a general-purpose input/output (GPIO3_12) on the NVCC_NANDF_A power rail.
IOB, IOG, IOR, IOB_BACK, IOG_BACK, and IOR_BACK	These signals are analog TV outputs that should be tied to GND when not being used.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM). Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed.
NC	These signals are No Connect (NC) and should be floated by the user.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
PMIC_INT_REQ	When using the MC13892 power management IC, the PMIC_INT_REQ high-priority interrupt input on i.MX51 should be either floated or tied to NVCC_SRTC_POW with a 4.7 kΩ to 68 kΩ resistor. This avoids a continuous current drain on the real-time clock backup battery due to a 100 kΩ on-chip pull-up resistor. PMIC_INT_REQ is not used by the Freescale BSP (board support package) software. The BSP requires that the general-purpose INT output from the MC13892 be connected to the i.MX51 GPIO input GPIO1_8 configured to cause an interrupt that is not high-priority. The original intent was for PMIC_INT_REQ to be connected to a circuit that detects when the battery is almost depleted. In this case, the I/O must be configured as alternate mode 0 (ALT0 = power fail).
POR_B	This cold reset negative logic input resets all modules and logic in the IC. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Memory repair – Configuration of memory repair per fuse settings • Cold reset logic of WDOG – Some WDOG logic is only reset by POR_B. See WDOG chapter in *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details.
RREFEXT	Determines the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required.
SGND, SVCC, and SVDDGP	These sense lines provide the ability to sense actual on-chip voltage levels on their respective supplies. SGND monitors differentials of the on-chip ground versus an external power source. SVCC monitors on-chip VCC, and SVDDGP monitors VDDGP. Freescale recommends connection of the SVCC and SVDDGP signals to the feedback inputs of switching power-supplies or to test points.
STR	This signal is reserved for Freescale manufacturing use. The user should float this signal.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.
VREF	When using VREF with DDR-2 I/O, the nominal 0.9 V reference voltage must be half of the NVCC_EMI_DRAM supply. The user must tie VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% VREF tolerance (per the DDR-2 specification) is maintained when four DDR-2 ICs plus the i.MX51 are drawing current on the resistor divider. **Note:** When VREF is used with mDDR this signal must be tied to GND.
VREFOUT	This signal determines the Triple Video DAC (TVDAC) reference voltage. The user must tie VREFOUT to an external 1.05 kΩ 1% resistor to GND.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
VREG	This regulator is no longer used and should be floated by the user.
XTAL/EXTAL	The user should tie a fundamental-mode crystal across XTAL and EXTAL. The crystal must be rated for a maximum drive level of 100 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. Freescale BSP (Board Support Package) software requires 24 MHz on EXTAL. The crystal can be eliminated if an external 24 MHz oscillator is available. In this case, EXTAL must be directly driven by the external oscillator and XTAL is floated. The EXTAL signal level must swing from NVCC_OSC to GND. If the clock is used for USB, then there are strict jitter requirements: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY. The COSC_EN bit in the CCM (Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. COSC_EN is bit 12 in the CCR register of the CCM.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	100 kΩ pull-down
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_DE_B	Input/open-drain output	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3 IOMUX Configuration for Boot Media

The information provided in this section describes the contacts assigned for each type of bootable media. It also includes data about the clocks used during boot flow and their frequencies. Signals that can be multiplexed appear in tables throughout this section. See the IOMUXC chapter in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details about how to program the IOMUX controller.

3.1 NAND

The NAND Flash Controller (NFC) signals are not configured in the IOMUX. The NFC interface uses dedicated contacts on the IC.

3.2 SD/MMC IOMUX Pin Configuration

Table 5 shows the SD/MMC IOMUX pin configuration.

Table 5. SD/MMC IOMUX Pin Configuration

Signal	eSDHC1	eSDHC2	eSDHC3	eSDHC4
CLK	SD1_CLK.alt0	SD2_CLK.alt0	NANDF_RDY_INT.alt5	NANDF_CS2.alt5
CMD	SD1_CMD.alt0	SD2_CMD.alt0	NANDF_CS7.alt5	NANDF_RB1.alt5
DAT0	SD1_DATA0.alt0	SD2_DATA0.alt0	NANDF_WE_B.alt2	NANDF_CS3.alt5
DAT1	N/A[1]	N/A	N/A	N/A
DAT2	N/A	N/A	N/A	N/A
CD/DAT3	SD1_DATA3.alt0	SD2_DATA3.alt0	NANDF_RB0.alt5	NANDF_CS6.alt5
DAT4	N/A	N/A	N/A	N/A
DAT5	N/A	N/A	N/A	N/A
DAT6	N/A	N/A	N/A	N/A
DAT7	N/A	N/A	N/A	N/A

1 N/A in the ROM code indicates the pins are not available.

Only DAT0 is available when the SD/MMC is used for boot. The remaining lines (DAT1–DAT7) are not available.

3.3 I^2C IOMUX Pin Configuration

The contacts assigned to the signals used by the three I^2C modules is shown in Table 6.

Table 6. I^2C IOMUX Pin Configuration

Signal	HSI^{2}C	I^{2}C1	I^{2}C2
SDA	I2C1_DAT.alt0	I2C1_DAT.alt0	GPIO1_3.alt2
SCL	I2C1_CLK.alt0	I2C1_CLK.alt0	GPIO1_2.alt2

3.4 eCSPI/CSPI IOMUX Pin Configuration

The contacts assigned to the signals used by the three SPI modules is shown in Table 7.

Table 7. SPI IOMUX Pin Configuration

Signal	eCSPI1	eCSPI2	CSPI
MISO	CSPI1_MISO.alt0	NANDF_RB3.alt2	USBH1_NXT.alt1
MOSI	CSPI1_MOSI.alt0	NANDF_D15.alt2	USBH1_DIR.alt1
RDY	CSPI1_RDY.alt0	NANDF_RB1.alt2	USBH1_STP.alt1
SCLK	CSPI1_SCLK.alt0	NANDF_RB2.alt2	USBH1_CLK.alt1
SS0	N/A[1]	N/A	N/A
SS1	N/A	N/A	USBH1_DATA5.alt1
SS2	N/A	N/A	N/A
SS3	N/A	N/A	N/A

1 N/A in the ROM code indicates the pins are not available.

3.5 Wireless External Interface Module (WEIM)

The WEIM interface signals are not configured in the IOMUX. The WEIM interface uses dedicated contacts on the IC.

3.6 UART IOMUX Pin Configuration

The contacts assigned to the signals used by the three UART modules are shown in Table 8.

Table 8. UART IOMUX Pin Configuration

Signal	UART1	UART2	UART3
TXD	UART1_TXD.alt0	UART2_TXD.alt0	UART3_TXD.alt1
RXD	UART1_RXD.alt0	UART2_RXD.alt0	UART3_RXD.alt1
CTS	UART1_CTS.alt0	USBH1_DATA0.alt1	KEY_COL5.alt2
RTS	UART1_RTS.alt0	USBH1_DATA3.alt1	KEY_COL4.alt2

3.7 USB-OTG IOMUX Pin Configuration

The interface signals of the UTMI PHY are not configured in the IOMUX. The UTMI PHY interface uses dedicated contacts on the IC.

Table 9. ULPI PHY IOMUX Pin Configuration

Signal	ULPI PHY
USB_PWR	GPIO1_8.alt1
USB_OC	GPIO1_9.alt1

Table 9. ULPI PHY IOMUX Pin Configuration (continued)

Signal	ULPI PHY
USBOTG_CLK	EIM_CS4.alt2
USBOTG_NXT	EIM_CS3.alt2
USBOTG_STP	EIM_CS2.alt2
USBOTG_DAT0	EIM_D24.alt2
USBOTG_DAT1	EIM_D25.alt2
USBOTG_DAT2	EIM_D26.alt2
USBOTG_DAT3	EIM_D27.alt2
USBOTG_DAT4	EIM_D28.alt2
USBOTG_DAT5	EIM_D29.alt2
USBOTG_DAT6	EIM_D30.alt2
USBOTG_DAT7	EIM_D31.alt2

NOTE

USB OTG ULPI port is not supported and it is not functional. On-chip PHY is always used for the OTG port.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX51 processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 10 for a quick reference to the individual tables and sections.

Table 10. i.MX51 Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 11, “Absolute Maximum Ratings”	on page 18
Table 12, “Thermal Resistance Data”	on page 18
Table 13, “i.MX51 Operating Ranges”	on page 19
Table 14, “Interface Frequency”	on page 21

CAUTION

Stresses beyond those listed under Table 11 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 13 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 11. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral Core Supply Voltage	VCC	–0.3	1.35	V
ARM Core Supply Voltage	VDDGP	–0.3	1.15	V
Supply Voltage (UHVIO, I^2C)	Supplies denoted as I/O Supply	–0.5	3.6	V
Supply Voltage (except UHVIO, I^2C)	Supplies denoted as I/O Supply	–0.5	3.3	V
USB VBUS	VBUS	—	5.25	V
Input/Output Voltage Range	V_{in}/V_{out}	–0.5	OVDD + 0.3[1]	V
ESD Damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage Temperature Range	$T_{STORAGE}$	–40	125	°C
Junction Temperature (MCIMX51xD—Consumer)	T_J	—	105	°C
Junction Temperature (MCIMX51xC—Industrial)	T_J	—	105	°C

1 The term OVDD in this section refers to the associated supply rail of an input or output. The association is described in Table 128 and Table 131. The maximum range can be superseded by the DC tables.

Table 12 provides the thermal resistance data.

Table 12. Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Case[1], 19 x 19 mm package	—	$R_{\theta JC}$	6	°C/W
Junction to Case[1], 13 x 13 mm package	—	$R_{\theta JC}$	6	°C/W

1 Rjc-x per JEDEC 51-12: The junction-to-case thermal resistance. The “x” indicates the case surface where T_{case} is measured and through which 100% of the junction power is forced to flow due to the cold plate heat sink fixture placed either at the top (T) or bottom (B) of the package, with no board attached to the package.

Table 13 shows the i.MX51 operating ranges.

Table 13. i.MX51 Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP MCIMX51xD products (Consumer)	ARM core supply voltage $0 \leq f_{ARM} \leq 167$ MHz	0.8	0.85	1.15	V
	ARM core supply voltage $167 < f_{ARM} \leq 800$ MHz	1.05	1.1	1.15	V
	ARM core supply voltage Stop mode	0.8	0.85	1.15	V
VDDGP MCIMX51xC products (Industrial)	ARM core supply voltage $0 < f_{ARM} \leq 600$ MHz	0.95	1.0	1.10	V
	ARM core supply voltage Stop mode	0.90	0.95	1.05	V
VCC MCIMX51xD products (Consumer)	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage Low Performance Mode (LPM) The clock frequencies are derived from AXI and AHB buses at 44 MHz and a DDR clock rate of DDR Clock/3. DDR2 does not support frequencies below 125 MHz per JEDEC.	1.00	1.05	1.275	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.275	V
VCC MCIMX51xC products (Industrial)	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage—Stop mode	0.90	0.95	1.275	V
VDDA	Memory arrays voltage—Run Mode	1.15	1.20	1.275	V
	Memory arrays voltage—Stop Mode	0.9	0.95	1.275	V
VDD_DIG_PLL_A VDD_DIG_PLL_B	PLL Digital supplies	1.15	1.2	1.35	V
VDD_ANA_PLL_A VDD_ANA_PLL_B	PLL Analog supplies	1.75	1.8	1.95	V

Table 13. i.MX51 Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
NVCC_EMI NVCC_PER5 NVCC_PER10 NVCC_PER11 NVCC_PER12 NVCC_PER13 NVCC_PER14	GPIO EMI Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_IPUx[3] NVCC_PER3 NVCC_PER8 NVCC_PER9	GPIO IPU Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR and Fuse Read Supply	1.65	1.8	1.95	V
VDD_FUSE[4]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF_x[5] NVCC_PER15 NVCC_PER17	Ultra High voltage I/O (UHVIO) supplies	—			V
	UHVIO_L	1.65	1.875	1.95	
	UHVIO_H	2.5	2.775	3.1	
	UHVIO_UH	3.0	3.3	3.6	
NVCC_USBPHY NVCC_OSC	USB_PHY analog supply, oscillator analog supply[6]	2.25	2.5	2.75	V
TVDAC_DHVDD, NVCC_TV_BACK, AHVDDRGB	TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V
NVCC_HS4_1 NVCC_HS4_2 NVCC_HS6 NVCC_HS10	HS-GPIO additional digital power supplies	1.65	—	3.1	V
NVCC_I2C	I^2C and HS-I^2C I/O Supply[7]	1.65	1.875	1.95	V
		2.7	3.0	3.3	
NVCC_SRTC_ POW	SRTC Core and I/O Supply (LVIO)	1.1	1.2	1.3	V
VDDA33	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 11 and Table 126 for details. This is not a power supply.	—	—	—	—
T_C	Case Temperature (MCIMX51xD—Consumer)	–20	—	85	°C
	Case Temperature (MCIMX51xC—Industrial)	–40	—	95	°C

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 The NVCC_IPUx rails are isolated from one another. This allows the connection of different supply voltages for each one. For example, NVCC_IPU2 can operate at 1.8 V while NVCC_IPU4 operates at 3.0 V.

4 In Read mode, Freescale recommends VDD_FUSE be floated or grounded. Tying VDD_FUSE to a positive supply (3.0 V–3.3 V) increases the possibility of inadvertently blowing fuses and is not recommended.

5 The NAND Flash supplies are composed of three groups: A, B, and C. Each group can be powered with a different supply voltage. For example, NVCC_NANDF_A = 1.8 V, NVCC_NANDF_B = 3.0 V, NVCC_NANDF_C = 2.7 V.

6 The analog supplies should be isolated in the application design. Use of series inductors is recommended.

7 Operation of the HS-I^{2}C and I^{2}C is not guaranteed when operated between the supply voltages of 1.95 to 2.7 V.

Table 14. Interface Frequency

Parameter Description	Symbol	Min	Max	Unit
JTAG: TCK Operating Frequency	f_{tck}	See Table 99, "JTAG Timing," on page 132		MHz
CKIL: Operating Frequency	f_{ckil}	See Table 74, "FPM Specifications," on page 82		kHz
CKIH: Operating Frequency	f_{ckih}	See Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 48		MHz
XTAL Oscillator	f_{xtal}	22	27	MHz

4.1.1 Supply Current

Table 15 shows the fuse supply current.

Table 15. Fuse Supply Current[1]

Description	Symbol	Min	Typ	Max	Unit
eFuse Program Current.[2] Current required to program one eFuse bit: The associated VDD_FUSE supply per Table 13.	$I_{program}$	—	60	120	mA

1 The read current of approximately 5 mA is derived from the DDR supply (NVCC_EMI_DRAM).

2 The current $I_{program}$ is only required during program time.

Table 16 shows the current core consumption (not including I/O) of the i.MX51.

Table 16. i.MX51 Stop Mode Current and Power Consumption

Mode	Condition	Supply	Nominal	Unit
Stop Mode • External reference clocks gated • Power gating for ARM and processing units • Stop mode voltage	VDDGP = 0.85 V, VCC = 0.95 V, VDDA = 0.95 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered down (SBYOS bit asserted) No external resistive loads that cause current flow Standby voltage allowed (VSTBY bit is asserted) T_A = 25 °C	VDDGP	0.18	mA
		VCC	0.35	
		VDDA	0.15	
		NVCC_OSC	0.012	
		Total	0.66	mW

Table 16. i.MX51 Stop Mode Current and Power Consumption (continued)

Mode	Condition	Supply	Nominal	Unit
Stop Mode • External reference clocks gated • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.2 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled. USBPHY PLL off External (MHz) crystal and on-chip oscillator powered down (SBYOS bit asserted) No external resistive loads that cause current flow T_A = 25°C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	0.012	
		Total	1.09	mW
Stop Mode • External reference clocks enabled • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.20 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	1.5	
		Total	4.8	mW
Stop Mode • External reference clocks enabled • No power gating for ARM and processing units • HPM voltage	VDDGP = 1.1 V, VCC = 1.225 V, VDDA = 1.2 V All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	50	mA
		VCC	2	
		VDDA	1.15	
		NVCC_OSC	1.5	
		Total	63	mW

4.1.2 USB PHY Current Consumption

Table 17 shows the USB PHY current consumption.

Table 17. USB PHY Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog Supply VDDA33 (3.3 V)	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	
Analog Supply NVCC_USBPHY (2.5 V)	Full Speed	RX	6.5	7	mA
		TX	6.5	7	
	High Speed	RX	12	13	
		TX	21	22	
Digital Supply VCC (1.2 V)	Full Speed	RX	6	7	mA
		TX	6	7	
	High Speed	RX	6	7	
		TX	6	7	
VDDA33 + NVCC_USBPHY + VCC	Suspend		50	100	µA

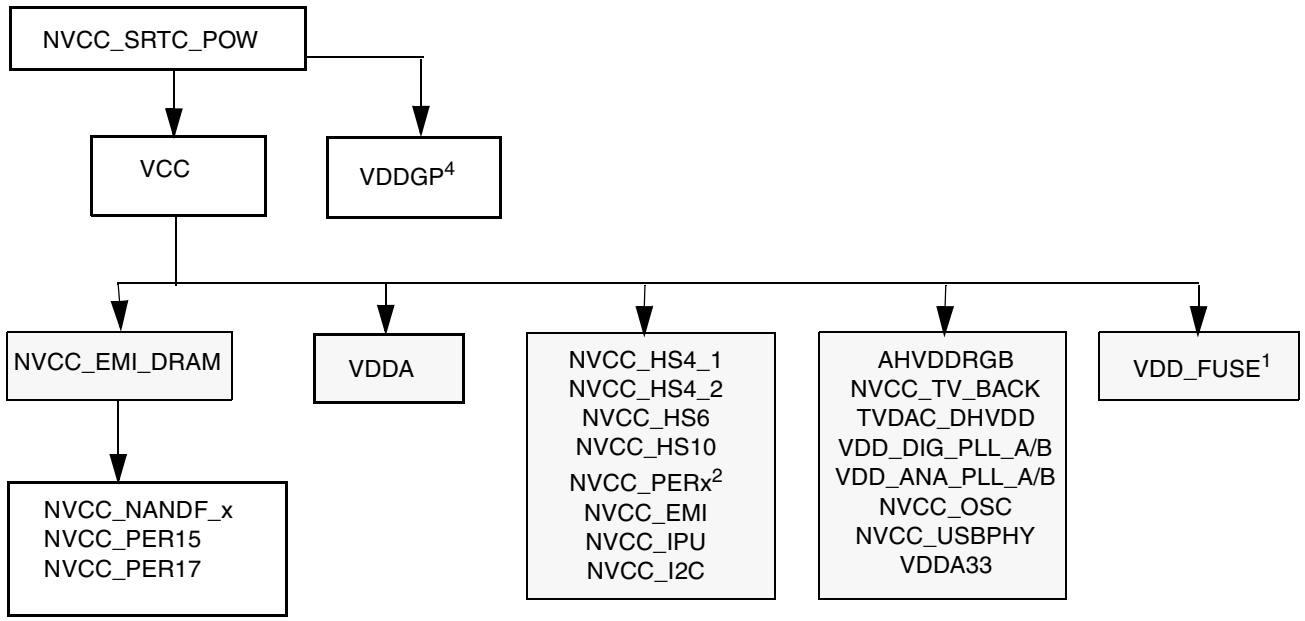
4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX51 processor (worst-case scenario)

4.2.1 Power-Up Sequence

Figure 2 shows the power-up sequence.



1. VDD_FUSE should only be powered when writing.
2. NVCC_PERx refers to NVCC_PER 3, 5, 8, 9, 10, 11, 12, 13, 14.
3. No power-up sequence dependencies exist between the supplies shown in the block diagram shaded in gray.
4. There is no requirement for VDDGP to be preceded by any other power supply other than NVCC_SRTC_POW.
5. If all of the UHVIO supplies (NVCC_NANDFx, NVCC_PER15 and NVCC_PER17) are less than 2.75 V then there is no requirement on the power up sequence order between NVCC_EMI_DRAM and the UHVIO supplies. However, if the voltage is 2.75 V and above, then NVCC_EMI_DRAM needs to power up before the UHVIO supplies as shown here.

Figure 2. Power-Up Sequence

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.

For more information on power up, see i.MX51 Power-Up Sequence (AN4053).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIO/HSGPIO)
- Double Data Rate 2 (DDR2)
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- High-Speed I^2C and I^2C
- Enhanced Secure Digital Host Controller (eSDHC)

NOTE

The term OVDD in this section refers to the associated supply rail of an input or output. The association is shown in Table 128 and Table 131.

4.3.1 GPIO/HSGPIO DC Parameters

The parameters in Table 18 are guaranteed per the operating ranges in Table 13, unless otherwise noted.

Table 18. GPIO/HSGPIO DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Iout = -1 mA	OVDD –0.15	—	OVDD + 0.3	V
Low-level output voltage	Vol	Iout = 1mA	—	—	0.15	V
High-level output current	Ioh	Vout = 0.8×OVDD Low drive Medium drive High drive Max drive	 –1.9 –3.7 –5.2 –6.6	—	—	mA
Low-level output current	Iol	Vout = 0.2×OVDD Low drive Medium drive High drive Max drive	 1.9 3.7 5.2 6.6	—	—	mA
High-Level DC input voltage[1]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1]	VIL	—	0	—	0.3×OVDD	V
Input Hysteresis	VHYS	OVDD = 1.875 OVDD = 2.775	0.25	0.34 0.45	—	V
Schmitt trigger VT+[1, 2]	VT+	—	0.5OVDD	—	—	V
Schmitt trigger VT-[1, 2]	VT-	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	—	—	See Note [3]	—
Input current (22 kΩ Pull-up)	Iin	Vin = 0	—	—	161	µA
Input current (47 kΩ Pull-up)	Iin	Vin = 0	—	—	76	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0	—	—	36	µA
Input current (100 kΩ Pull-down)	Iin	Vin = OVDD	—	—	36	µA
Keeper Circuit Resistance	—	OVDD = 1.875V OVDD = 2.775V	— —	22 17	— —	kΩ

[1] To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

[2] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

[3] I/O leakage currents are listed in Table 25.