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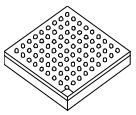
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: IMX53IEC
Rev. 6, 03/2013

MCIMX53xC

i.MX53 Applications Processors for Industrial Products

Silicon Version 2.1



Package Information
Plastic Package
Case TEPBGA-2 19 x 19 mm, 0.8 mm pitch

Ordering Information
See Table 1 on page 2

1 Introduction

The i.MX53 processor features ARM Cortex™-A8 core, which operates at clock speeds as high as 800 MHz. It provides DDR2/LVDDR2-800, LPDDR2-800, or DDR3-800 DRAM memories.

The flexibility of the i.MX53 architecture allows for its use in a wide variety of applications. As the heart of the application chipset, the i.MX53 processor provides all the interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, camera sensors, and dual displays.

Features of the i.MX53 processor include the following:

- Applications processor—The i.MX53xD processors boost the capabilities of high-tier portable applications by satisfying the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks such as audio decode.

- Multilevel memory system—The multilevel memory system of the i.MX53 is based on the L1 instruction and data caches, L2 cache, internal and external memory. The i.MX53 supports many types of external memory devices, including DDR2, low voltage DDR2, LPDDR2, DDR3, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND including eMMC up to rev 4.4.
- Smart speed technology—The i.MX53 device has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product requiring levels of power far lower than industry expectations.
- Multimedia powerhouse—The multimedia performance of the i.MX53 processor ARM core is boosted by a multilevel cache system, Neon (including advanced SIMD, 32-bit single-precision floating point support) and vector floating point coprocessors. The system is further enhanced by a multi-standard hardware video codec, autonomous image processing unit (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration— The i.MX53 processors provide two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator (33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance) and an OpenVG™ 1.1 2D graphics accelerator (200 Mpix/s).
- Interface flexibility—The i.MX53 processor supports connection to a variety of interfaces, including LCD controller for two displays and CMOS sensor interface, high-speed USB on-the-go with PHY, plus three high-speed USB hosts, multiple expansion card ports (high-speed MMC/SDIO host and others), 10/100 Ethernet controller, and a variety of other popular interfaces (PATA, UART, I^2C, and I^2S serial audio, among others).
- Advanced security—The i.MX53 processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. For detailed information about the i.MX53 security features contact a Freescale representative.

The i.MX53 application processor is a follow-on to the i.MX51, with improved performance, power efficiency, and multimedia capabilities.

1.1 Functional Part Differences and Ordering Information

shows the functional differences between the different parts in the i.MX53 family.

Table 1 provides ordering information.

Table 1. Ordering Information

Part Number	Mask Set	CPU Frequency	Notes	Package[1]
MCIMX537CVV8C	N78C	800 MHz	—	19 x 19 mm, 0.8 mm pitch BGA Case TEPBGA-2

[1] Case TEPBGA-2 is RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

1.2 Features

The i.MX53 multimedia applications processor (AP) is based on the ARM Platform, which has the following features:

- MMU, L1 instruction and L1 data cache
- Unified L2 cache
- Maximum frequency of the core (including Neon, VFPv3 and L1 cache): 800 MHz
- Neon coprocessor (SIMD media processing architecture) and vector floating point (VFP-Lite) coprocessor supporting VFPv3
- TrustZone

The memory system consists of the following components:

- Level 1 cache:
  - Instruction (32 Kbyte)
  - Data (32 Kbyte)
- Level 2 cache:
  - Unified instruction and data (256 Kbyte)
- Level 2 (internal) memory:
  - Boot ROM, including HAB (64 Kbyte)
  - Internal multimedia/shared, fast access RAM (128 Kbyte)
  - Secure/non-secure RAM (16 Kbyte)
- External memory interfaces:
  - 16/32-bit DDR2-800, LV-DDR2-800 or DDR3-800 up to 2 Gbyte
  - 32-bit LPDDR2
  - 8/16-bit NAND SLC/MLC Flash, up to 66 MHz, 4/8/14/16-bit ECC
  - 8/16-bit NOR Flash, PSRAM, and cellular RAM.
  - 32-bit multiplexed mode NOR Flash, PSRAM & cellular RAM.
  - 8-bit Asynchronous (DTACK mode) EIM interface.
  - All EIM pins are muxed on other interfaces (data with NFC pins). I/O muxing logic selects EIM port, as primary muxing at system boot.
  - Samsung OneNAND™ and managed NAND including eMMC up to rev 4.4 (in muxed I/O mode)

The i.MX53 system is built around the following system on chip interfaces:

- 64-bit AMBA AXI v1.0 bus—used by ARM platform, multimedia accelerators (such as VPU, IPU, GPU3D, GPU2D) and the external memory controller (EXTMC) operating at 200 MHz.
- 32-bit AMBA AHB 2.0 bus—used by the rest of the bus master peripherals operating at 133 MHz.
- 32-bit IP bus—peripheral bus used for control (and slow data traffic) of the most system peripheral devices operating at 66 MHz.

The i.MX53 makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption while freeing up the CPU core for other tasks.

The i.MX53 incorporates the following hardware accelerators:

- VPU, version 3—video processing unit
- GPU3D—3D graphics processing unit, OpenGL ES 2.0, version 3, 33 Mtri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance, 256 Kbyte RAM memory
- GPU2D—2D graphics accelerator, OpenVG 1.1, version 1, 200 Mpix/s performance,
- IPU, version 3M—image processing unit
- ASRC—asynchronous sample rate converter

The i.MX53 includes the following interfaces to external devices:

NOTE

Not all interfaces are available simultaneously, depending on I/O multiplexer configuration.

- Hard disk drives:
  - PATA, up to U-DMA mode 5, 100 MByte/s
  - SATA II, 1.5 Gbps
- Displays:
  - Five interfaces available. Total rate of all interfaces is up to 180 Mpixels/s, 24 bpp. Up to two interfaces may be active at once.
  - Two parallel 24-bit display ports. The primary port is up to 165 Mpix/s (for example, UXGA at 60 Hz).
  - LVDS serial ports: one dual channel port up to 165 Mpix/s or two independent single channel ports up to 85 MP/s (for example, WXGA at 60 Hz) each.
  - TV-out/VGA port up to 150 Mpix/s (for example, 1080p60).
- Camera sensors:
  - Two parallel 20-bit camera ports. Primary up to 180-MHz peak clock frequency, secondary up to 120-MHz peak clock frequency.
- Expansion cards:
  - Four SD/MMC card ports: three supporting 416 Mbps (8-bit i/f) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4).
- USB
  - High-speed (HS) USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - High-speed host with integrated on-chip high-speed PHY
    - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB
- Miscellaneous interfaces:
  - One-wire (OWIRE) port

- Three I2S/SSI/AC97 ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
- Five UART RS232 ports, up to 4.0 Mbps each. One supports 8-wire, the other four support 4-wire.
- Two high speed enhanced CSPI (ECSPI) ports plus one CSPI port
- Three I^2C ports, supporting 400 kbps
- Fast Ethernet controller, IEEE1588 V1 compliant, 10/100 Mbps
- Two controller area network (FlexCAN) interfaces, 1 Mbps each
- Sony Phillips Digital Interface (SPDIF), Rx and Tx
- Key pad port (KPP)
- Two pulse-width modulators (PWM)
- GPIO with interrupt capabilities

The system supports efficient and smart power control and clocking:

- Supporting DVFS (dynamic voltage and frequency scaling) technique for low power modes
- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHz external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware/features:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)
- Secure JTAG controller (SJC)—Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features
- Secure real-time clock (SRTC)—Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches
- Real-time integrity checker, version 3 (RTICv3)—RTIC type1, enhanced with SHA-256 engine
- SAHARAv4 Lite—Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2)—Improved SCC with AES engine, secure/non-secure RAM and support for multiple keys as well as TZ/non-TZ separation
- Central security unit (CSU)—Enhancement for the IIM (IC Identification Module). CSU is configured during boot by eFUSEs, and determines the security level operation mode as well as the TrustZone (TZ) policy
- Advanced High Assurance Boot (A-HAB)—HAB with the following embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization
- Tamper detection mechanism—Provides evidence of any physical attempt to remove the device cover. Upon detection of such an attack, sensitive information can immediately be erased.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX53 processor system.

2.1 Block Diagram

Figure 1 shows the functional modules in the i.MX53 processor system.

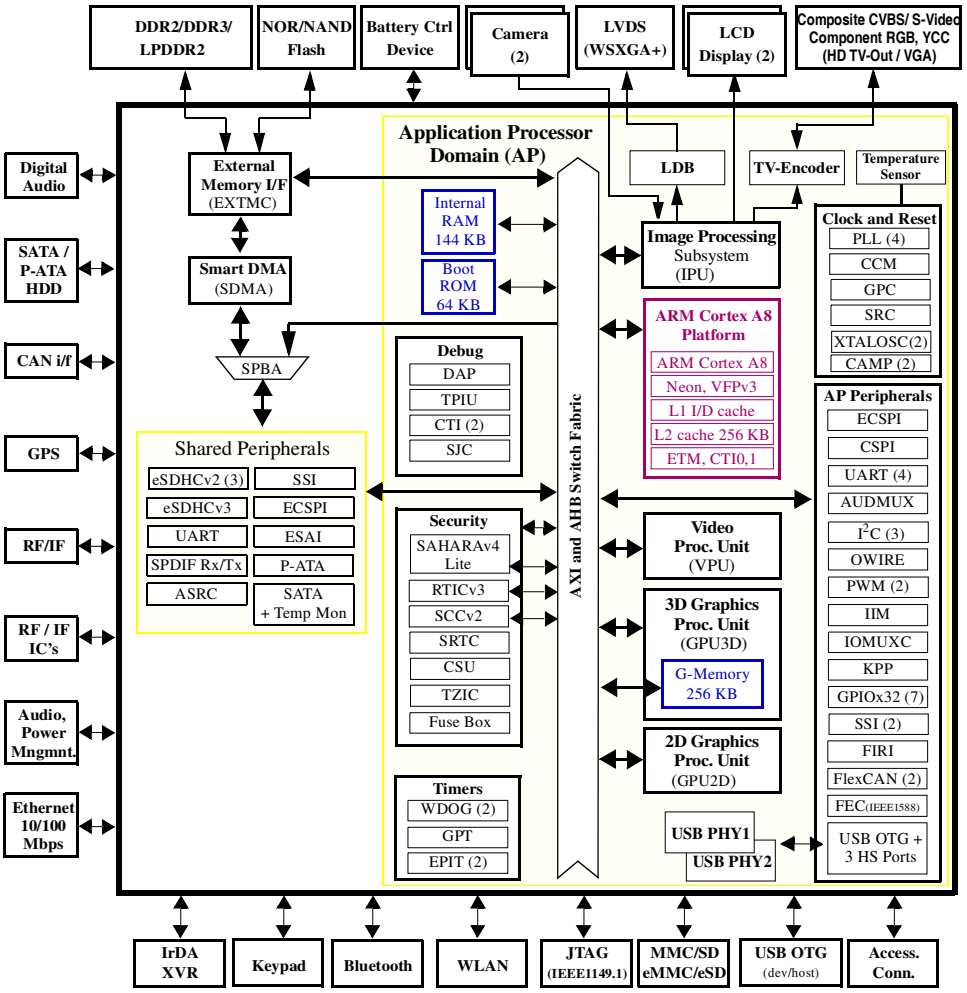


Figure 1. i.MX53 System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (2) indicates two separate PWM peripherals.

3 Modules List

The i.MX53 processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX53 Digital and Analog Blocks

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Cortex™ A8 platform consists of the ARM processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, Level 2 cache controller and a 256 Kbyte L2 cache. The platform also contains an event monitor and debug modules. It also has a NEON coprocessor with SIMD media processing architecture, a register file with 32/64-bit general-purpose registers, an integer execute pipeline (ALU, Shift, MAC), dual single-precision floating point execute pipelines (FADD, FMUL), a load/store and permute pipeline and a non-pipelined vector floating point (VFP Lite) coprocessor supporting VFPv3.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The asynchronous sample rate converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120 dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Multiplexer	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CAMP-1 CAMP-2	Clock Amplifier	Clocks, Resets, and Power Control	Clock amplifier
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, as well as for system power management. The system includes four PLLs.
CSPI ECSPI-1 ECSPI-2	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced synchronous serial interface, with data rates 16-60 Mbit/s. It is configurable to support master/slave modes. In Master mode it supports four slave selects for multiple peripherals.
CSU	Central Security Unit	Security	The central security unit (CSU) is responsible for setting comprehensive security policy within the i.MX53 platform, and for sharing security information between the various security modules. The security control registers (SCR) of the CSU are set during boot time by the high assurance boot (HAB) code and are locked to prevent further writing.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DEBUG	Debug System	System Control	The debug system provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, three cross-system triggers (CTI), counters, and sequencers. debug access port (DAP)— The DAP provides real-time access for the debugger without halting the core to system memory, peripheral register, debug configuration registers and JTAG scan chains.
EXTMC	External Memory Controller	Connectivity Peripherals	The EXTMC is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels, fast memories (DDR2/DDR3/LPDDR2) channel, slow memories (NOR-FLASH / PSRAM / NAND-FLASH etc.) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) channel. In order to increase the bandwidth performance, the EXTMC separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EXTMC Features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (read or write) was the last access • Flexible bank interleaving • Support 16/32-bit DDR2-800 or DDR3-800 or LPDDR2. • Support up to 2 GByte DDR memories. • Support NFC, EIM signal muxing scheme. • Support 8/16/32-bit Nor-Flash/PSRAM memories (sync and async operating modes), at slow frequency. (8-bit is not supported on D[23]-D[16]). • Support 4/8/14/16-bit ECC, page sizes of 512-B, 2-KB and 4-KB Nand-Flash (including MLC) • Multiple chip selects (up to 4). • Enhanced DDR memory controller, supporting access latency hiding • Support watermark for security (internal and external memories)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The enhanced serial audio interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The ESAI has 12 pins for data and clocking connection to external devices.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESDHCV3-3	Ultra-High-Speed eMMC / SD Host Controller	Connectivity Peripherals	Ultra high-speed eMMC / SD host controller, enhanced to support eMMC 4.4 standard specification, for 832 MBps. • Port 3 is specifically enhanced to support eMMC 4.4 specification, for double data rate (832 Mbps, 8-bit port). ESDHCV3 is backward compatible to ESDHCV2 and supports all the features of ESDHCV2 as described below.
ESDHCV2-1 ESDHCV2-2 ESDHCv2-4	Enhanced Multi-Media Card / Secure Digital Host Controller		Enhanced multimedia card / secure digital host controller • Ports 1, 2, and 4 are compatible with the “MMC System Specification” version 4.3, full support and supporting 1, 4 or 8-bit data. The generic features of the eSDHCv2 module, when serving as SD / MMC host, include the following: • Can be configured either as SD / MMC controller • Supports eSD and eMMC standard, for SD/MMC embedded type cards • Conforms to SD Host Controller Standard Specification, version 2.0, full support. • Compatible with the SD Memory Card Specification, version 1.1 • Compatible with the SDIO Card Specification, version 1.2 • Designed to work with SD memory, miniSD memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full/high speed mode. • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using 4 parallel data lines • Up to 416 Mbps data transfer for MMC cards using 8 parallel data lines
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet media access controller (MAC) is designed to support both 10 Mbps and 100 Mbps Ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX53 also consists of HW assist for IEEE1588™ standard. See, TSU and CE_RTC (IEEE1588) section for more details.
FIRI	Fast Infrared Interface	Connectivity Peripherals	Fast infrared interface
FLEXCAN-1 FLEXCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The controller area network (CAN) protocol was primarily, but not exclusively, designed to be used as a vehicle serial data bus. Meets the following specific requirements of this application: real-time processing, reliable operation in the EXTMC environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN is a full implementation of the CAN protocol specification, Version 2.0 B (ISO 11898), which supports both standard and extended message frames at 1 Mbps.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3D	Graphics Processing Unit	Multimedia Peripherals	The GPU, version 3, provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution. It supports color representation up to 32 bits per pixel. GPU enables high-performance mobile 3D and 2D vector graphics at rates up to 33 Mtriangles/s, 200 Mpix/s, 800 Mpix/s (z).
GPU2D	Graphics Processing Unit-2D	Multimedia Peripherals	The GPU2D version 1, provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD1080 resolution.
I2C-1 I2C-2 I2C-3	I^2C Controller	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 kbps are supported.
IIM	IC Identification Module	Security	The IC identification module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module. IIM interfaces to the electrical fuse array (split to banks). Enabled to set up boot modes, security levels, security keys and many other system parameters. i.MX53A consists of 4 x 256-bit + 1 x 128-bit fuse-banks (total 1152 bits) through IIM interface.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
IPU	Image Processing Unit	Multimedia Peripherals	Version 3M IPU enables connectivity to displays, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces: • Legacy parallel interfaces • Single/dual channel LVDS display interface • Analog TV or VGA interfaces The processing includes: • Image enhancement—color adjustment and gamut mapping, gamma correction and contrast enhancement • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Hardware de-interlacing support • Synchronization and control capabilities, allowing autonomous operation.
KPP	Keypad Port	Connectivity Peripherals	The KPP supports an 8 × 8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS display bridge is used to connect the IPU (image processing unit) to external LVDS display interface. LDB supports two channels; each channel has following signals: • 1 clock pair • 4 data pairs On-chip differential drivers are provided for each pair.
OWIRE	One-Wire Interface	Connectivity Peripherals	One-wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example, Dallas DS2502.
PATA	Parallel ATA	Connectivity Peripherals	The PATA block is a AT attachment host interface. Its main use is to interface with hard disk drives and optical disc drives. It interfaces with the ATA-6 compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side.
PWM-1 PWM-2	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
INTRAM	Internal RAM	Internal Memory	Internal RAM, shared with VPU. The on-chip memory controller (OCRAM) module, is an interface between the system's AXI bus, to the internal (on-chip) SRAM memory module. It is used for controlling the 128 KB multimedia RAM, through a 64-bit AXI bus.
BOOTROM	Boot ROM	Internal Memory	Supports secure and regular boot modes. The ROM controller supports ROM patching.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
RTIC	Run-Time Integrity Checker	Security	Protecting read only data from modification is one of the basic elements in trusted platforms. The run-time integrity checker, version 3 (RTIC) block is a data-monitoring device responsible for ensuring that the memory content is not corrupted during program execution. The RTIC mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The purpose of the RTIC is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement and assist with boot authentication.
SAHARA	SAHARA Security Accelerator	Security	SAHARA (symmetric/asymmetric hashing and random accelerator), version 4, is a security coprocessor. It implements symmetric encryption algorithms, (AES, DES, 3DES, RC4 and C2), public key algorithms (RSA and ECC), hashing algorithms (MD5, SHA-1, SHA-224 and SHA-256), and a hardware true random number generator. It has a slave IP Bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.
SATA	Serial ATA	Connectivity Peripherals	SATA HDD interface, includes the SATA controller and the PHY. It is a complete mixed-signal IP solution for SATA HDD connectivity.
SCCv2	Security Controller, ver. 2	Security	The security controller is a security assurance hardware module designed to safely hold sensitive data, such as encryption keys, digital right management (DRM) keys, passwords and biometrics reference data. The SCCv2 monitors the system's alert signal to determine if the data paths to and from it are secure, that is, it cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCCv2 also features a key encryption module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (copy mode) • Up to 8-word buffer for configurable burst transfers to / from the EXTMC • Support of byte swapping and CRC calculations • A library of scripts and API is available

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SECRAM	Secure / Non-secure RAM	Internal Memory	Secure / non-secure Internal RAM, controlled by SCC.
SJC	Secure JTAG Interface	System Control Peripherals	JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX53 processor incorporates a mechanism for regulating JTAG access. SJC provides four different JTAG security modes that can be selected through an e-fuse configuration.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (shared peripheral bus arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Both transmitter and receiver functionalists are supported.
SRTC	Secure Real Time Clock	Security	The SRTC incorporates a special system state retention register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized separately even if all other supply rails are shut down. This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication).
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX53A processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX for mapping to external ports. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8 x 24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two time slots are being used simultaneously.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IPTP	IEEE1588 Precision Time Protocol	Connectivity Peripherals	The IEEE 1588-2002 (version 1) standard defines a precision time protocol (PTP) - which is a time-transfer protocol that enables synchronization of networks (for example, Ethernet), to a high degree of accuracy and precision. The IEEE1588 hardware assist is composed of the two blocks: time stamp unit and real time clock, which provide the timestamping protocol's functionality, generating and reading the needed timestamps. The hardware-assisted implementation delivers more precise clock synchronization at significantly lower CPU load compared to purely software implementations.
Temperature Monitor	(Part of SATA Block)	System Control Peripherals	The temperature sensor is an internal module to the i.MX53 that monitors the die temperature. The monitor is capable in generating SW interrupt, or trigger the CCM, to reduce the core operating frequency.
TVE	TV Encoder	Multimedia	The TV encoder, version 2.1 is implemented in conjunction with the image processing unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports composite PAL/NTSC, VGA, S-video, and component up to HD1080p analog video outputs.
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone interrupt controller (TZIC) collects interrupt requests from all i.MX53 sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UART blocks supports the following serial data transmit/receive protocols and configurations: • 7 or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable bit-rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 Mbps, which is specified by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USB	USB Controller	Connectivity Peripherals	USB supports USB2.0 480 MHz, and contains: • One high-speed OTG sub-block with integrated HS USB PHY • One high-speed host sub-block with integrated HS USB PHY • Two identical high-speed Host modules The high-speed OTG module, which is internally connected to the HS USB PHY, is equipped with transceiver-less logic to enable on-board USB connectivity without USB transceivers All the USB ports are equipped with standard digital interfaces (ULPI, HS IC-USB) and transceiver-less logic to enable onboard USB connectivity without USB transceivers.

Table 2. i.MX53 Digital and Analog Blocks (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU) version 3, which covers many SD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing such as rotation and mirroring. VPU Features: • MPEG-2 decode, Mail-High profile, up to 1080i/p resolution, 40 Mbps bit rate • MPEG4/XviD decode, SP/ASP profile, up to 1080 i/p resolution, 40 Mbps bit rate • H.263 decode, P0/P3 profile, up to 16CIF resolution, 20 Mbps bit rate • H.264 decode, BP/MP/HP profile, up to 1080 i/p resolution, 40 Mbps bit rate • VC1 decode, SP/MP/AP profile, up to 1080 i/p resolution, 40 Mbps bit rate • RV10 decode, 8/9/2010 profile, up to 1080 i/p resolution, 40 Mbps bit rate • DivX decode, 3/4/5/6 profile, up to 1080 i/p resolution, 40 Mbps bit rate • MJPEG decode, Baseline profile, up to 8192 x 8192 resolution, 40 Mpixel/s bit rate for 4:4:4 format • MPEG4 encode, Simple profile, up to 720p resolution, 12 Mbps bit rate[1] • H.263 encode, P0/P3 profile, up to 4CIF resolution, 8 Mbps bit rate[1] • H.264 encode, Baseline profile, up to 720p resolution, 14 Mbps bit rate[1] • MJPEG encode, Baseline profile, up to 8192 x 8192 resolution, 80 Mpixel/s bit rate for 4:2:2 format
WDOG-1	Watch Dog	Timer Peripherals	The watch dog timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. This situation should be avoided, as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
XTALOSC	24 MHz Crystal Oscillator	Clocking	Provides a crystal oscillator amplifier that supports a 24 MHz external crystal
XTALOSC_ 32K	32.768 kHz Crystal Oscillator I/F	Clocking	Provides a crystal oscillator amplifier that supports a 32.768 kHz external crystal.

[1] VPU can generate higher bit rate than the maximum specified by the corresponding standard.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX53 Reference Manual. Special signal considerations information is contained in Chapter 1 of *i.MX53 System Development User's Guide* (MX53UG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX53 processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 3 for a quick reference to the individual tables and sections.

Table 3. i.MX53 Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	Table 4 on page 16
TEPBGA-2 Package Thermal Resistance Data	Table 5 on page 17
i.MX53 Operating Ranges	Table 6 on page 18
External Clock Sources	Table 7 on page 20
Maximal Supply Currents	Table 8 on page 20
USB Interface Current Consumption	Table 9 on page 23

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 4 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges table is not implied.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral Core Supply Voltage	VCC	-0.3	1.35	V
ARM Core Supply Voltage	VDDGP	-0.3	1.4	V
Supply Voltage UHVIO	Supplies denoted as I/O Supply	-0.5	3.6	V
Supply Voltage for non UHVIO	Supplies denoted as I/O Supply	-0.5	3.3	V
USB VBUS	VBUS	—	5.25	V

Table 4. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63[1]	V
Input/Output Voltage Range	V_{in}/V_{out}	-0.5	OVDD +0.3[2]	V
ESD Damage Immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage Temperature Range	$T_{STORAGE}$	-40	150	°C

1 USB_DN and USB_DP can tolerate 5 V for up to 24 hours.

2 The term OVDD in this section refers to the associated supply rail of an input or output. The association is described in Table 111 on page 148. The maximum range can be superseded by the DC tables.

4.1.2 Thermal Resistance

4.1.2.1 TEPBGA-2 Package Thermal Resistance

Table 5 provides the TEPBGA-2 package thermal resistance data.

Table 5. TEPBGA-2 Package Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Ambient (natural convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	28	°C/W
Junction to Ambient (natural convection)[1, 2, 3]	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	21	°C/W
Junction to Ambient (at 200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W
Junction to Board[4]	—	$R_{\theta JB}$	6	°C/W
Junction to Case[5]	—	$R_{\theta JC}$	4	°C/W
Junction to Package Top (natural convection)[6]	—	Ψ_{JT}	4	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4.1.3 Operating Ranges

Table 6 provides the operating ranges of i.MX53 processor.

Table 6. i.MX53 Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP[3]	ARM core supply voltage $f_{ARM} \leq 400$ MHz	0.9	0.95	1.15	V
	ARM core supply voltage $f_{ARM} \leq 800$ MHz	1.05	1.1	1.15	V
	ARM core supply voltage Stop mode	0.8	0.85	1.15	V
VCC	Peripheral supply voltage[4]	1.25	1.3	1.35	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.35	V
VDDA[5]	Memory arrays voltage	1.25	1.30	1.35	V
	Memory arrays voltage—Stop mode	0.9	0.95	1.35	V
VDDAL1[5]	L1 Cache Memory arrays voltage	1.25	1.30	1.35	V
	L1 Cache Memory arrays voltage—Stop mode	0.9	0.95	1.35	V
VDD_DIG_PLL[6]	PLL Digital supplies—external regulator option	1.25	1.3	1.35	V
VDD_ANA_PLL[7]	PLL Analog supplies—external regulator option	1.75	1.8	1.95	V
NVCC_CKIH	ESD protection of the CKIH pins, FUSE read Supply and 1.8V bias for the UHVIO pads	1.65	1.8	1.95	V
NVCC_LCD NVCC_JTAG	GPIO digital power supplies	1.65	1.8 or 2.775	3.1	V
NVCC_LVDS	LVDS interface Supply	2.375	2.5	2.75	V
NVCC_LVDS_BG	LVDS Band Gap Supply	2.375	2.5	2.75	V
NVCC_EMI_DRAM	DDR Supply DDR2 range	1.7	1.8	1.9	V
	DDR Supply LPDDR2 range	1.14	1.2	1.3	
	DDR Supply LV-DDR2 range	1.47	1.55	1.63	
		1.42	1.5	1.58	
	DDR Supply DDR3 range	1.42	1.5	1.58	
VDD_FUSE[8]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF NVCC_SD1 NVCC_SD2 NVCC_PATA NVCC_KEYPAD NVCC_GPIO NVCC_FEC NVCC_EIM_MAIN NVCC_EIM_SEC NVCC_CSI	Ultra High voltage I/O (UHVIO) supplies:				V
	• UHVIO_L	1.65	1.8	1.95	
	• UHVIO_H	2.5	2.775	3.1	
	• UHVIO_UH	3.0	3.3	3.6	

Table 6. i.MX53 Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
TVDAC_DHVDD[9] TVDAC_AHVDDRGB[9]	TVE digital and analog power supply, TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V
	For GPIO use only, when TVE is not in use	1.65	1.8 or 2.775	3.1	V
NVCC_SRTC_POW	SRTC Core and slow I/O Supply (GPIO)[10]	1.25	1.3	1.35	V
NVCC_RESET	LVIO	1.65	1.8 or 2.775	3.1	V
USB_H1_VDDA25 USB_OTG_VDDA25 NVCC_XTAL	USB_PHY analog supply, oscillator amplifier analog supply[11]	2.25	2.5	2.75	V
USB_H1_VDDA33 USB_OTG_VDDA33	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 4 on page 16 and Table 104 on page 141 for details. Note that this is not a power supply.	—	—	—	—
VDD_REG[12]	Power supply input for the integrated linear regulators	2.37	2.5	2.63	V
VP	SATA PHY core power supply	1.25	1.3	1.35	V
VPH	SATA PHY I/O supply voltage	2.25	2.5	2.75	V
T_J	Junction temperature	-40	105[13]	125	°C

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 A voltage transition is allowed for the required supply ramp up to the nominal value prior to achieving a clock speed increase. Similarly, to accommodate a frequency reduction, a voltage transition is allowed for a supply ramp down to the nominal value after the frequency is decreased.

4 For BSDL mode, the minimum operating temperature is 20 °C and the maximum operating temperature is the maximum temperature specified for the particular part grade.

5 VDDA and VDDAL1 can be driven by the VDD_DIG_PLL internal regulator using external connections. When operating in this configuration, the regulator is still operating at the default 1.2 V, as bootup start. During bootup initialization, software should increase this regulator voltage to match VCC (1.3 V nominal) in order to reduce internal leakage current.

6 By default, VDD_DIG_PLL is driven from internal on-die 1.2 V linear regulator (LDO). In this case, there is no need driving this supply externally. LDO output to VDD_DIG_PLL should be configured by software after power-up to 1.3 V output. A bypass capacitor of minimal value 22 µF should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.

7 By default, the VDD_ANA_PLL is driven from internal on-die 1.8 V linear regulator (LDO). In this case there is no need driving this supply externally. A bypass capacitor of minimal value 22 µF should be connected to this pad in any case whether it is driven internally or externally. Use of the on-chip LDO is preferred. See i.MX53 System Development User's Guide.

8 After fuses are programmed, Freescale strongly recommends the best practice of reading the fuses to verify that they are written correctly. In Read mode, VDD_FUSE should be floated or grounded. Tying VDD_FUSE to a positive supply (3.0 V–3.3 V) increases the possibility of inadvertently blowing fuses and is not recommended in read mode.

9 If not using the TVE module or other pads in this power domain for the product, the TVDAC_DHVDD and TVDAC_AHVDDRGB can be kept floating or tied to GND—the recommendation is to float.

10 GPIO pad operational at low frequency

[11] The analog supplies should be isolated in the application design. Use of series inductors is recommended.

[12] VDD_REG is power supply input for the integrated linear regulators of VDD_ANA_PLL and VDD_DIG_PLL when they are configured to the internal supply option. VDDR_REG still has to be tied to 2.5 V supply when VDD_ANA_PLL and VDD_DIG_PLL are configured for external power supply mode although in this case it is not used as supply source.

[13] Lifetime of 87,600 hours based on 105 ^{o}C junction temperature at nominal supply voltages.

4.1.4 External Clock Sources

The i.MX53 device has four external input system clocks, a low frequency (CKIL), a high frequency (XTAL), and two general purpose CKIH1 and CKIH2 clocks.

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

CKIH1 and CKIH2 provide additional clock source option for peripherals that require specific and accurate frequencies.

Table 7 shows the interface frequency requirements. See Chapter 1 of *i.MX53 System Development User's Guide* (MX53UG) for additional clock and oscillator information.

Table 7. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
CKIL Oscillator[1]	f_{ckil}	—	32.768[2]/32.0	—	kHz
CKIH1, CKIH2 Operating Frequency	f_{ckih1}, f_{ckih2}	See Table 32, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 44			MHz
XTAL Oscillator	f_{xtal}	22	24	27	MHz

[1] External oscillator or a crystal with internal oscillator amplifier.

[2] Recommended nominal frequency 32.768 kHz.

4.1.5 Maximal Supply Currents

Table 8 represents the maximal momentary current transients on power lines, and should be used for power supply selection. Maximal currents higher by far than the average power consumption of typical use cases. For typical power consumption information, see i.MX53 power consumption application note.

Table 8. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDGP	800 MHz ARM clock	1450	mA
VCC		800	mA
VDDA+VDDAL1		100	mA
VDD_DIG_PLL		10	mA

Table 8. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
VP		20	mA
VDD_ANA_PLL		10	mA
NVCC_XTAL		25	mA
VDD_REG		325	mA
VDD_FUSE	Fuse Write Mode operation	120	mA
NVCC_EMI_DRAM[1]	1.8V (DDR2)	800	mA
	1.5V (DDR3)	650	mA
	1.2V (LPDDR2)	250	mA
TVDAC_DHVDD + TVDAC_AHVDDRGB		200	mA
NVCC_SRTC_POW		50[2]	µA
USB_H1_VDDA25 + USB_OTG_VDDA25		50	mA
USB_H1_VDDA33 + USB_OTG_VDDA33		20	mA
VPH		60	mA
NVCC_CKIH		Use maximal I/O Eq[3], N=4	
NVCC_CSI		Use maximal I/O Eq[3], N=20	
NVCC_EIM_MAIN		Use maximal I/O Eq[3], N=39	
NVCC_EIM_SEC		Use maximal I/O Eq[3], N=16	
NVCC_FEC		Use maximal I/O Eq[3], N=11	
NVCC_GPIO		Use maximal I/O Eq[3], N=13	
NVCC_JTAG		Use maximal I/O Eq[3], N=6	
NVCC_KPAD		Use maximal I/O Eq[3], N=11	
NVCC_LCD		Use maximal I/O Eq[3], N=29	
NVCC_LVDS		Use maximal I/O Eq[3], N=20	
NVCC_LVDS_BG		Use maximal I/O Eq[3], N=1	
NVCC_NANDF		Use maximal I/O Eq[3], N=8	
NVCC_PATA		Use maximal I/O Eq[3], N=29	
NVCC_REST		Use maximal I/O Eq[3], N=5	

Table 8. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_SD1		Use maximal I/O Eq[3], N=6	
NVCC_SD2		Use maximal I/O Eq[3], N=6	

[1] The results are based on calculation assuming the following conditions:
—Four 16-bit DDR devices
—Heavy use profile
—On-Die Termination (ODT) of 50 Ω for DDR2 and 40 Ω for DDR3
—Dual rank termination schema
—Command and Address line termination to NVCC_EMI_DRAM/2 voltage
These numbers include both i.MX53 DDR controller I/O current consumption and DDR memory I/O power consumption for data and DQS lines.

[2] 50 μA current is the worst case for fast silicon at 125 °C. The typical current is 3 μA for typical silicon at 25 °C.

[3] General Equation for estimated, maximal power consumption of an I/O power supply:
Imax = N x C x V x (0.5 x F)
Where:
N - Number of I/O pins supplies by the power line
C - Equivalent external capacitive load
V - I/O voltage
(0.5 x F) - Data change rate. Up to 0.5 of the clock rate (F).

4.1.6 USB-OH-3 (OTG + 3 Host ports) Module and the Two USB PHY (OTG and H1) Current Consumption

Table 9 shows the USB interface current consumption.

Table 9. USB Interface Current Consumption

Parameter	Conditions		Typical at 25 °C	Max	Unit
Analog Supply 3.3 V USB_H1_VDDA33 USB_OTG_VDDA33	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	
Analog Supply 2.5 V USB_H1_VDDA25 USB_OTG_VDDA25	Full Speed	RX	6.5	7	mA
		TX	6.5	7	
	High Speed	RX	12	13	
		TX	21	22	
Digital Supply VCC (1.2 V)	Full Speed	RX	8	—	mA
		TX	8	—	
	High Speed	RX	8	—	
		TX	8	—	

4.2 Power Supply Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX53 processor (worst-case scenario)

4.2.1 Power-Up Sequence

The following observations should be considered:

- The consequent steps in power up sequence should not start before the previous step supplies have been stabilized within 90-110% of their nominal voltage, unless stated otherwise.
- NVCC_SRTC_POW should remain powered ON continuously, to maintain internal real-time clock status. Otherwise, it has to be powered ON together with VCC, or preceding VCC.
- The VCC should be powered ON together, or any time after NVCC_SRTC_POW.
- NVCC_CKIH should be powered ON after VCC is stable and before other I/O supplies (NVCC_xxx) are powered ON.

- I/O Supplies (NVCC_xxx) below or equal to 2.8 V nom./3.1 V max. should not precede NVCC_CKIH. They can start powering ON during NVCC_CKIH ramp-up, before it is stabilized. Within this group, the supplies can be powered-up in any order.
  Alternatively, the on-chip regulator VDD_ANA_PLL can be used to power NVCC_CKIH and NVCC_RESET. In this case, the sequence defined in the "Interfacing the i.MX53 Processor with LTC3589-1" section of the *i.MX53 System Development User's Guide* (MX53UG) must be followed.
- I/O Supplies (NVCC_xxx) above 2.8 V nom./3.1 V max. should be powered ON only after NVCC_CKIH is stable.
- In case VDD_DIG_PLL and VDD_ANA_PLL are powered ON from internal voltage regulator (default case for i.MX53), there are no related restrictions on VDD_REG, as it is used as their internal regulators power source.
  If VDD_DIG_PLL and VDD_ANA_PLL are powered on externally, to reduce current leakage during the power-up, it is recommended to activate the VDD_REG before or at the same time with VDD_DIG_PLL and VDD_ANA_PLL. If this sequencing is not possible, make sure that the 2.5 V VDD_REG supply shut-off output impedance is higher than 1 kΩ when it is inactive.
- VDD_REG supply is required to be powered ON to enable DDR operation. It must be powered on after VCC and before NVCC_EMI_DRAM. The sequence should be:

  VCC →VDD_REG →NVCC_EMI_DRAM

- VDDA and VDDAL1 can be powered ON anytime before POR_B, regardless of any other power signal.
- VDDGP can be powered ON anytime before POR_B, regardless of any other power signal.
- VP and VPH can be powered up together, or anytime after, the VCC. VP and VPH should come before POR.
- TVDAC_DHVDD and TVDAC_AHVDDRGB should be powered from the same regulator. This is due to ESD diode protection circuit, that may cause current leakage if one of the supplies is powered ON before the other.

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage.

Figure 2 shows the power-up sequence diagram.

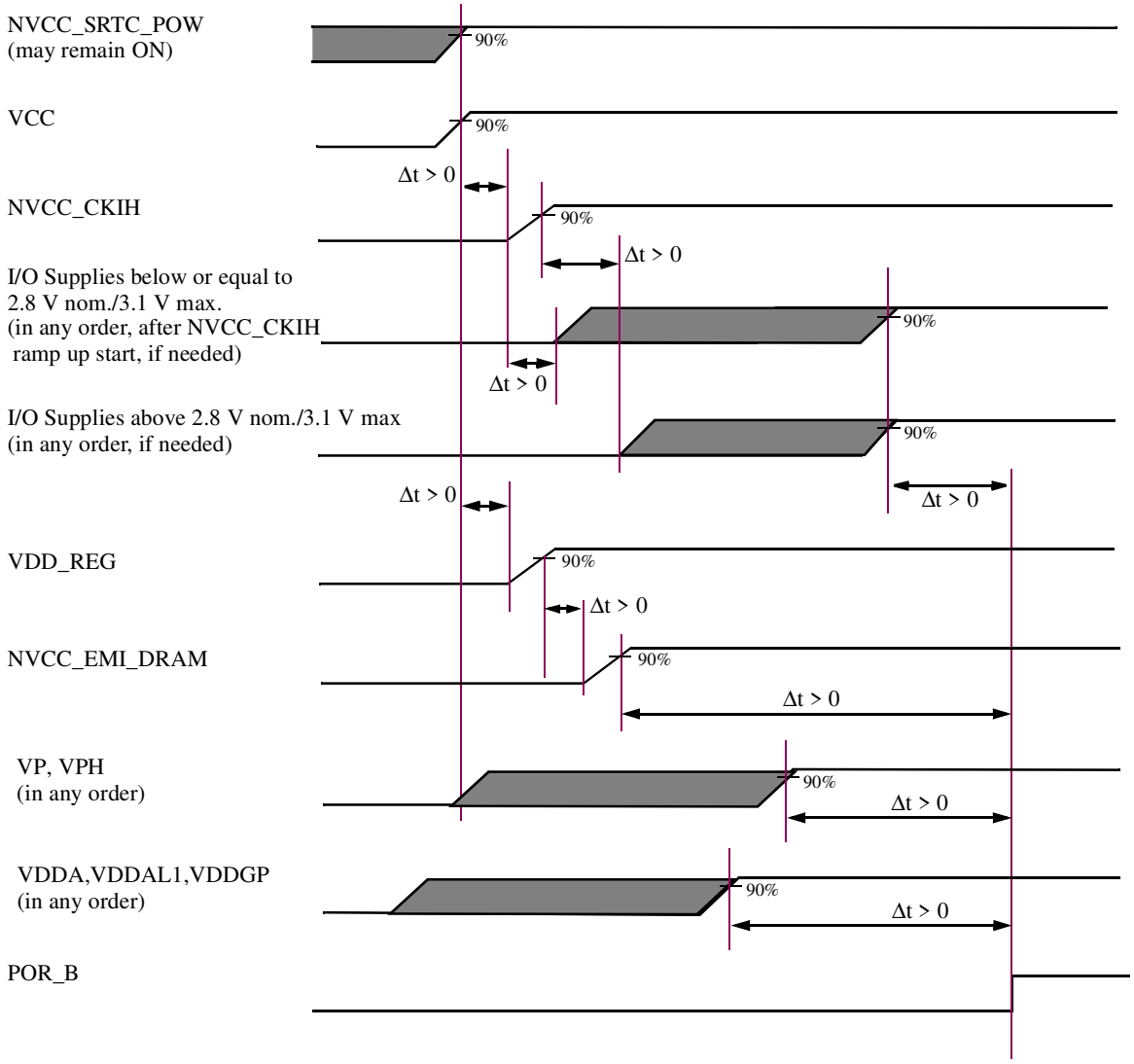


Figure 2. Power-Up Detailed Sequence

1 If fuse writing is required, VDD_FUSE should be powered ON after NVCC_CKIH is stable.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the parts that use both 1.8 V and the 3.3 V supply).

NOTE

For further details on power-up sequence, see the “Setting up Power Management” chapter of *i.MX53 System Development User’s Guide* (MX53UG).