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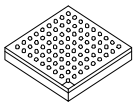
i.MX 6SoloLite Applications Processors for Consumer Products



Package Information
Plastic Package
13 x 13 mm, 0.5 mm pitch

Ordering Information
See Table 1 on page 3

1 Introduction

The i.MX 6SoloLite processor represents Freescale's latest achievement in integrated multimedia applications processors, which are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The processor features Freescale's advanced implementation of the a single ARM Cortex™-A9 core, which operates at speeds up to 1 GHz. It includes 2D graphics processor and integrated power management. The processor provides a 32-bit DDR3-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6SoloLite processor is specifically useful for applications, such as:

- Color and monochrome eReaders
- Entry level tablets
- Barcode scanners

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The i.MX 6SoloLite processor features:

- Applications processor—The processor enhances the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, and managed NAND, including eMMC up to rev 4.4.
- Smart speed technology—The processor has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: 2D BLit engine, a 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—The processor supports connections to a variety of interfaces: LCD controller, CMOS sensor interface (parallel), high-speed USB on-the-go with PHY, high-speed USB host PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100 Mbps Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Electronic Paper Display Controller—The processor integrates EPD controller that supports E-INK color and monochrome with up to 2048 x 1536 resolution at 106 Hz refresh, 4096 x 4096 resolution at 20 Hz refresh and 5-bit grayscale (32-levels per color channel). The processor also integrates an EPD controller that supports SiPix monochrome panels.
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6SoloLite security reference manual. Contact your local Freescale representative for more information.
- Integrated power management—The processor integrates linear regulators and generate internally all the voltage levels for different domains. This significantly simplifies system power management structure.
- GPIO with interrupt capabilities—The new GPIO pad design supports configurable dual voltage rails at 1.8V and 3.3V supplies. The pad is configurable to interface at either voltage level.

1.1 Ordering Information

Table 1 shows the orderable part numbers covered by this datasheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in Table 1, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Orderable Part Numbers

Part Number[1]	Mask Set	Options	Speed Grade	Temperature (Tj)	Package[2]
MCIMX6L8DVN10AA	N20G	With GPU, E-ink	1 GHz	0 to +95C	13x13mm, 0.5mm pitch BGA
MCIMX6L7DVN10SA	N20G	With Sipix	1 GHz	0 to +95C	13x13mm, 0.5mm pitch BGA
MCIMX6L3EVN10AA	N20G	With GPU	1 GHz	-40 to +105C	13x13mm, 0.5mm pitch BGA
MCIMX6L2EVN10AA	N20G		1 GHz	-40 to +105C	13x13mm, 0.5mm pitch BGA

1 Part numbers with a PC prefix indicate non-production engineering parts.

2 Case 2240 is RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

Figure 1 describes the part number nomenclature so that users can identify the characteristics of the specific part number they have (for example, Cores, Frequency, Temperature Grade, Fuse options, Silicon revision).

Ensure that you have the right datasheet for your specific part by checking the Temperature Grade (Junction) field and matching it to the right datasheet. If you have questions, see freescale.com/imx6series or contact your Freescale representative.

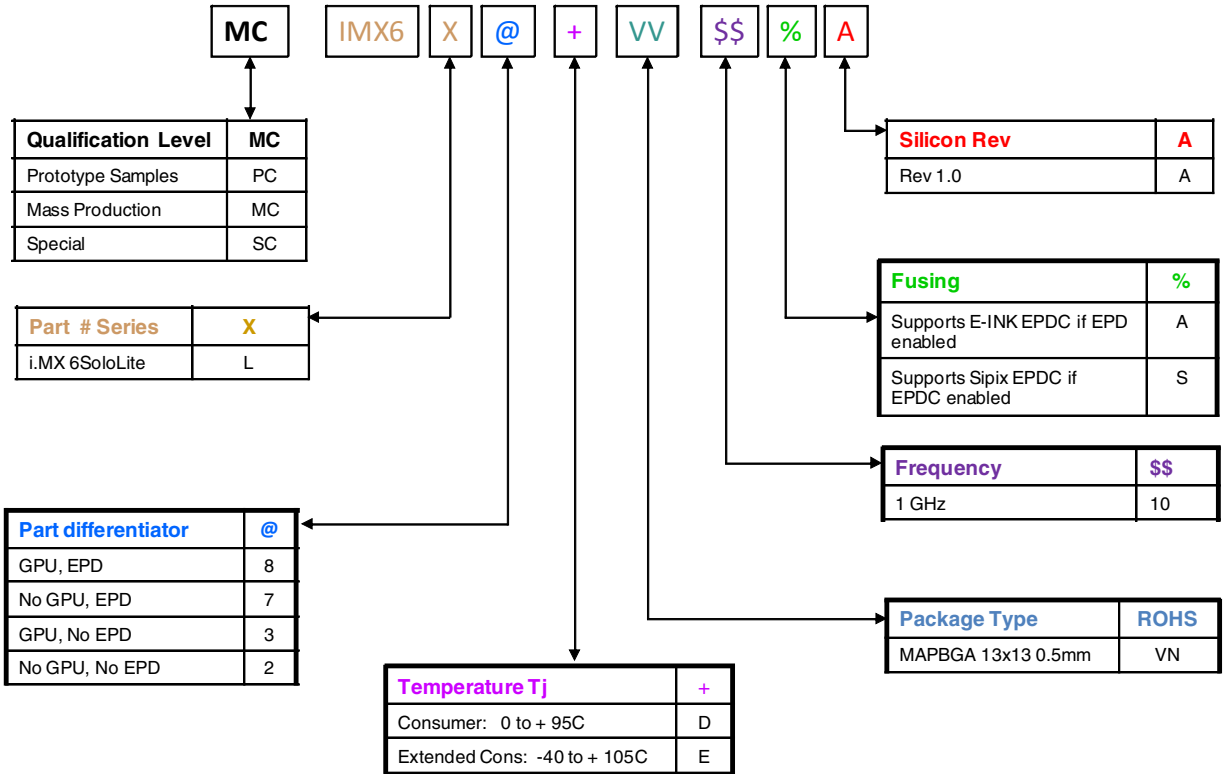

Figure 1. Part Number Nomenclature—i.MX 6SoloLite

1.2 Features

The i.MX 6SoloLite processor is based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex-A9 MPCore CPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per Table 9, "Operating Ranges," on page 21
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (256 KByte)
- On-Chip Memory:
  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
- External memory interfaces:
  - 16-bit, and 32-bit DDR3-800, and LPDDR2-800 channels
  - 16/32-bit NOR Flash.
  - 16/32-bit PSRAM, Cellular RAM (32 bits or less)

Each i.MX 6SoloLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total three interfaces are available.
  - LCD, 24bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz)

  - EPDC, color, and monochrome E-INK, up to 1650x2332 resolution and 5-bit grayscale
  - SPDC, color, and monochrome SiPix panels
- Camera sensors:
  - Parallel Camera port (up to 16 bit)
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - Two High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - One USB 2.0 (480 Mbps) hosts:
    - One HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Miscellaneous IPs and interfaces:
  - Three I^2S/SSI/AC97 supported
  - Five UARTs, up to 4.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
  - Four eCSPI (Enhanced CSPI)
  - Three I^2C, supporting 400 kbps
  - Ethernet Controller, 10/100 Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Two Watchdog timers (WDOG)
  - Audio MUX (AUDMUX)

The i.MX 6SoloLite processor integrates advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SoloLite processor uses dedicated HW accelerators to meet the targeted multimedia performance. The use of HW accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6SoloLite processor incorporates the following hardware accelerators:

- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Orderable Part Numbers," on page 3. Functions, such as 2D hardware graphics acceleration, E-Ink or SiPix may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SoloLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SoloLite processor system.

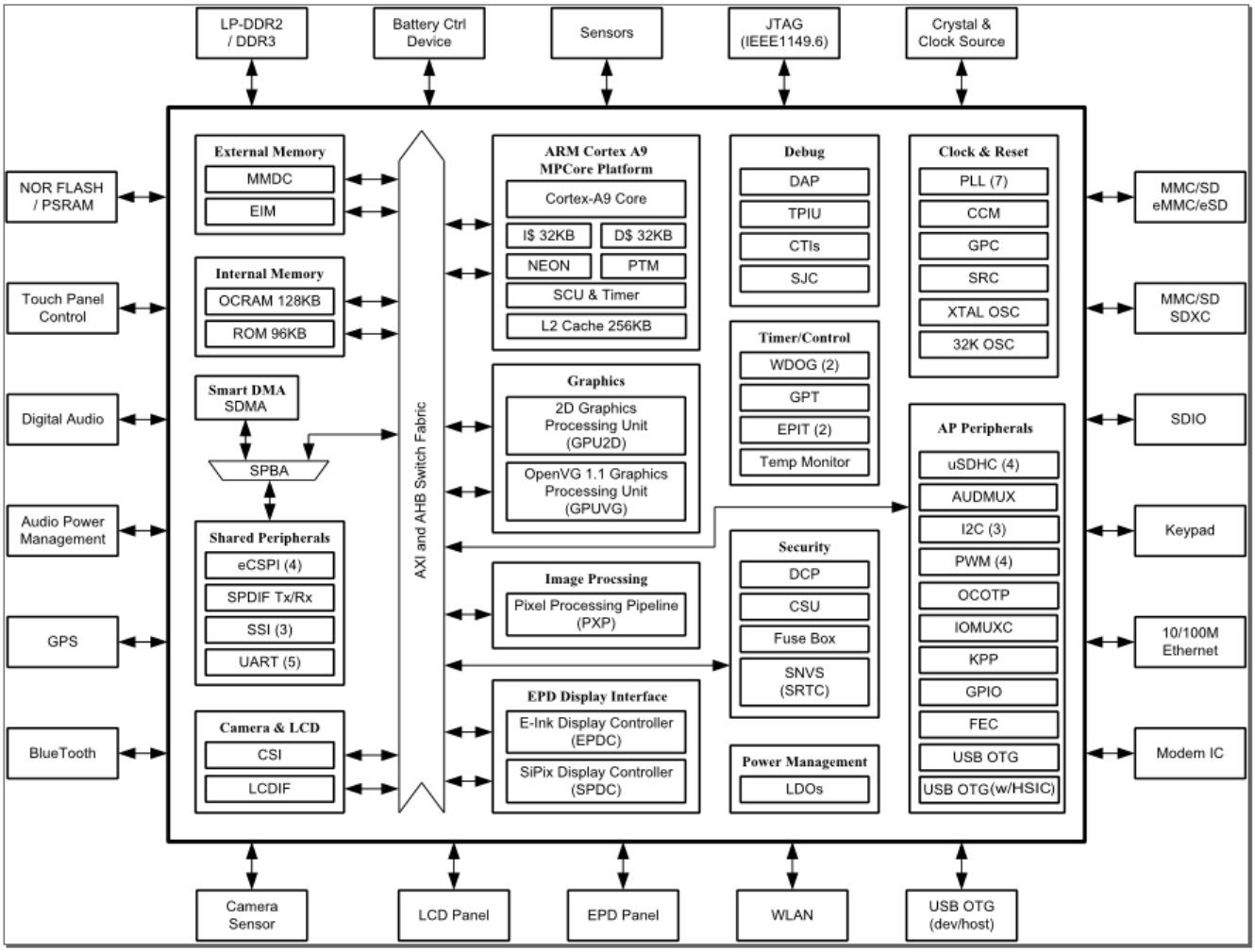

Figure 2. i.MX 6SoloLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6SoloLite processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6SoloLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
128x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6SoloLite processor consists of 2-128x8-bit fuse box accessible through OCOTP_CTRL interface.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of a Cortex-A9 core version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloLite platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-1 CTI-2 CTI-3 CTI-4 CTI-5	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E-INK™ EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPUVGv2	Vector Graphics Processing Unit ver2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD Interface	Multimedia Peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32-bit DDR3-800 or LPDDR2-800 • Supports up to 2 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SoloLite processor, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD. either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Softwareitching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloLite processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDC	Electrophoretic Display Controller	Peripherals	The SPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive SiPix™ EPD panels, supporting a wide variety of TFT backplanes.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions. The Temperature sensor IP for detecting die temperature. The temperature read out does not reflect case or ambient temperature, but the proximity of the temperature sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH2A	2x USB 2.0 High Speed OTG and 1x HS Hosts	Connectivity Peripherals	USBO2H contains: • One Two high-speed OTG module with integrated HS USB PHY • One identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. HW reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support HW reset • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system’s security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6SoloLite processor. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are provided in the i.MX 6SoloLite reference manual.

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/CLK1_N	One general purpose differential high speed clock Input/output is provided. It could be used to: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the i.MX 6SoloLite reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximal clock out frequency range supported is 528 MHz. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the CLK1 input/output could be disabled (if not used). If unused, the CLK1_N/P pair may be left floating.
DRAM_VREF	When using DRAM_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DRAM_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DRAM_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6SoloLite are drawing current on the resistor divider. It is recommended to use regulated power supply for "big" memory configurations (more that eight devices).
GPANAIO	This signal is reserved for Freescale manufacturing use only. User must leave this connection floating.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6SoloLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common Software debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be floated by the user.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
ONOFF	In normal mode may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to Software controllable power down). Long above ~5s connection to GND causes “forced” OFF.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low)
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO floating.
TEST_MODE	TEST_MODE is for Freescale factory use. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. level and the frequency should be <32 MHz under typical conditions. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typically 80 Ω is recommended. Freescale BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is floated. The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2 V. This clock is used as a reference for USB, PCIe, and SATA, so there are strict frequency tolerance and jitter requirements. See the XTALOSC chapter and relevant interface specifications chapters of the i.MX 6SoloLite reference manual, for details.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper

Table 4. JTAG Controller Interface Summary (continued)

JTAG	I/O Type	On-Chip Termination
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
CCM	CLK1_N, CLK1_P	Float
USB	USB_H1_DN, USB_H1_DP, USB_H1_VBUS, USB_OTG_CHD_B, USB_OTG_DN, USB_OTG_DP, USB_OTG_VBUS	Float

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloLite processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SoloLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 18
BGA Case 2240 Package Thermal Resistance	on page 18
Operating Ranges	on page 21
External Clock Sources	on page 22
Maximal Supply Currents	on page 23
Low Power Mode Supply Currents	on page 24
USB PHY Current Consumption	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max[1]	Unit
Core supply voltages	VDD_ARM_IN VDD_SOC_IN VDD_PU_IN	-0.3	1.5	V
Internal supply voltages	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD[2]+0.3	V
ESD Immunity (HBM)	Vesd_CDM	—	2000	V
ESD Immunity (CDM)	Vesd_CDM	—	500	V
Storage temperature range	$T_{STORAGE}$	-40	150	°C

1 Exceeding maximum may result in breakdown, or reduction in IC life time, performance, and/or reliability.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 8 provides the MAPBGA package thermal resistance data.

Table 8. Package Thermal Resistance Data

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient[1] (natural convection)	Single layer board (1s)	$R_{\theta JA}$	51	°C/W
	Four layer board (2s2p)	$R_{\theta JA}$	28	°C/W

Table 8. Package Thermal Resistance Data (continued)

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[2]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	9	°C/W
Junction to Package Top[4]	Natural Convection	Ψ_{JT}	2	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Figure 3 shows major power systems blocks and internal/external connections for the i.MX 6Sololite proessor.

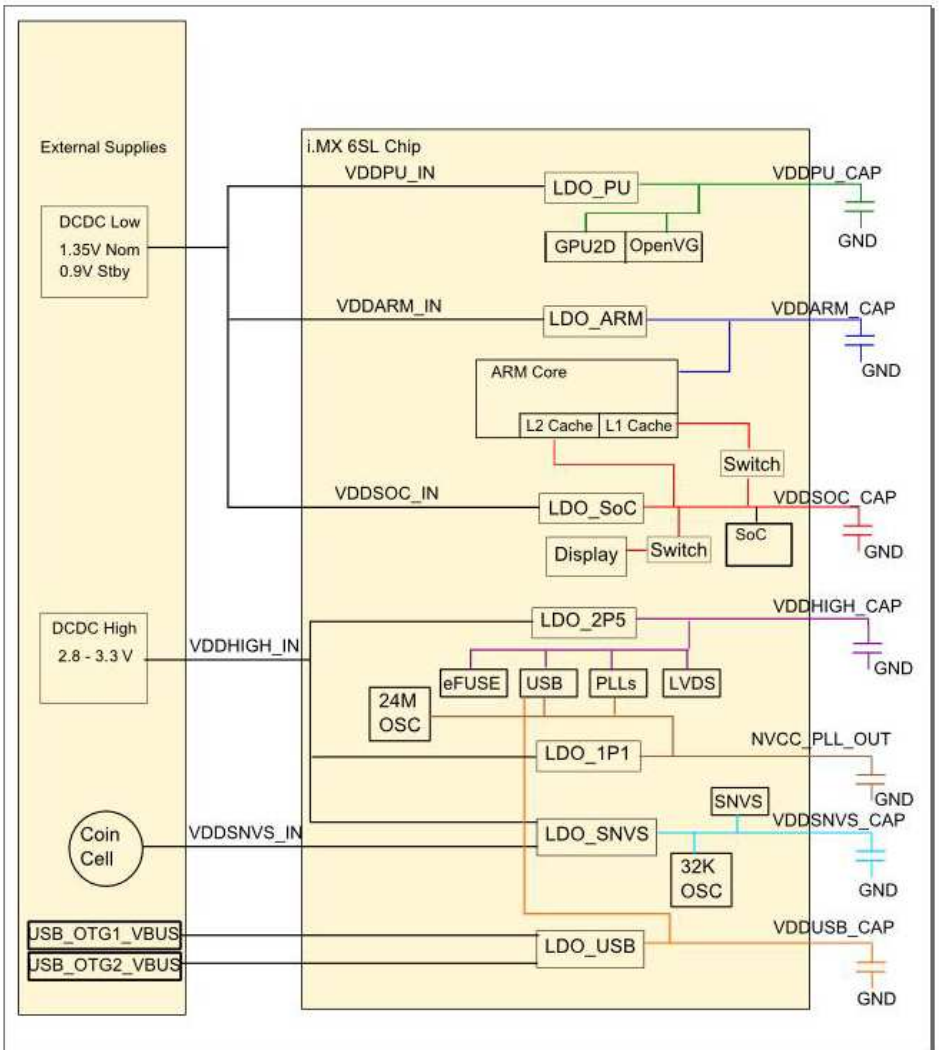

Figure 3. i.MX 6SoloLite SoC Power Block Diagram

Table 9 provides the operating ranges of the i.MX 6SoloLite processor.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375[2]		1.5	V	LDO output set at 1.250V minimum for operation up to 996MHz.
		1.275[2]		1.5	V	LDO output set at 1.150V minimum for operation up to 792MHz
		1.075[2]		1.5	V	LDO output set at 0.95V minimum for operation up to 396MHz
		1.075[2]		1.5	V	LDO output set at 0.950V minimum for operation up to 192MHz
		1.050[2]		1.5	V	LDO output set at 0.9250V minimum for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.275[2,4]		1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.250		1.3	V	LDO bypassed for operation up to 996 MHz.
		1.150		1.3	V	LDO bypassed for operation up to 792 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 396 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 192MHz
		0.925		1.3	V	LDO bypassed for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.15[4]		1.3	V	
Standby/DSM Mode	VDD_ARM_IN	0.9		1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 24.
	VDD_SOC_IN VDD_PU_IN	0.9		1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN[5]	2.8		3.3	V	Must match the range of voltges that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.8		3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4		5.25	V	
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supplies[6]	NVCC33_IO	2.8	3.0	3.3	V	Worst case, assuming all SOC I/O operating at 1.8V. NVCC33_IO must always be greater than NVCC18_IO.
	NVCC18_IO	1.62	1.8	1.98	V	
	NVCC_1P2V		1.2			
Junction temperature	T_J	0		95	°C	Consumer
Junction temperature	T_J	-40		105		Extended Consumer

1 Applying the maximum voltage results in maximum power consumption and heat generation. Freescale recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDD_ARM_IN and VDDSOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

3 VDD_SOC_CAP and VDD_PU_CAP must be equal.

4 VDDSOC and VDDPU output voltage must be set to this rule: VDDARM-VDDSOC/PU<50mV

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

4.1.4 External Clock Sources

Each i.MX 6SoloLite processor has two external input system clocks: a low frequency (RTC_XTAL) and a high frequency (XTAL).

The RTC_XTAL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and Watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTAL, in case accuracy is not important.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

Table 10 shows the interface frequency requirements.

Table 10. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTAL Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTAL Oscillator[4,2]	f_{xtal}		24		MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6SoloLite Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	1 GHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	1 GHz ARM clock	650	mA
VDD_PU_IN	1 GHz ARM clock	150	mA
VDD_HIGH_IN	—	30[1]	mA
VDD_SNVS_IN	—	250[2]	µA

Table 11. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
USB_OTG1_VBUS USB_OTG2_VBUS	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	—[4]	
NVCC33_IO	N=156	Use maximal IO Equation[5]	
NVCC18_IO	N=156	Use maximal IO Equation[5]	
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination.
See the i.MX 6SoloLite Power Consumption Measurement Application Note or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximal power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 12 shows the current core consumption (not including I/O) of i.MX 6SoloLite processor in selected low power modes.

Table 12. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.375 V)	4	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN(3.0 V)	9	
		Total	44.9	mW

Table 12. Stop Mode Current and Power Consumption (continued)

STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN (3.0 V)	4.5	
		Total	29.3	mW
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	0.1	
		VDD_HIGH_IN (3.0 V)	4.0	
		Total	25.9	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	1.0	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	3	
		Total	10.1	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	0.75	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	0.15	
		Total	1.3	mW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.