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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

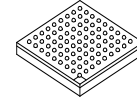
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# i.MX 6Dual/6Quad Applications Processors Consumer - PoP

**MCIMX6Q5ExxxxD**  
**MCIMX6Q7CxxxxD**  
**MCIMX6Q5ExxxxE**  
**MCIMX6Q7CxxxxE**  
**MCIMX6D5ExxxxD**  
**MCIMX6D7CxxxxD**  
**MCIMX6D5ExxxxE**  
**MCIMX6D7CxxxxE**



**Package Information**  
Plastic Package  
12 x 12 mm, 0.4 mm pitch

Ordering Information
See <a href="#">Table 1</a>

## 1 Introduction

The i.MX 6Dual/6Quad processors are part of a growing family of multimedia-focused products that offer high performance processing and are optimized for lowest power consumption.

The i.MX 6Dual/6Quad processors feature advanced implementation of the quad ARM<sup>®</sup> Cortex<sup>®</sup>-A9 core, which operates at speeds up to 800 MHz. They include 2D and 3D graphics processors, 1080p video processing, and integrated power management. Each processor provides a 2 × 32-bit LPDDR2-800 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth<sup>®</sup>, GPS, hard drive, displays, and camera sensors.

The i.MX 6Dual/6Quad processors are specifically useful for applications such as the following:

- High-end mobile Internet devices (MID)
- High-end PDAs
- High-end portable media players (PMP) with HD video capability

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## Introduction

- Gaming consoles
- Portable navigation devices (PND)

The i.MX 6Dual/6Quad processors offers numerous advanced features, such as:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. The Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon® MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES .0 3D graphics accelerator with four shaders (up to MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I<sup>2</sup>C, and I<sup>2</sup>S serial audio, SATA-II, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDL SRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.



## 1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this data sheet. This table does not include all possible orderable part numbers. The latest part numbers are available on [nxp.com/imx6series](http://nxp.com/imx6series). If your desired part number is not listed in the table, or you have questions about available parts, see [nxp.com/imx6series](http://nxp.com/imx6series) or contact your NXP representative.

**Table 1. Orderable Part Numbers**

Part Number	Quad/Dual CPU	Options	Speed Grade	Temperature Grade	Package
MCIMX6Q5EZK08AD	i.MX 6Quad	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q5EZK08AE	i.MX 6Quad	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q7CZK08AD	i.MX 6Quad	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6Q7CZK08AE	i.MX 6Quad	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D5EZK08AD	i.MX 6Dual	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D5EZK08AE	i.MX 6Dual	MLB not supported	800 MHz	Extended Commercial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D7CZK08AD	i.MX 6Dual	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)
MCIMX6D7CZK08AE	i.MX 6Dual	MLB not supported	800 MHz	Industrial	12 mm x 12 mm, 0.4 mm pitch, FCPBGA, Package on Package (PoP)

Figure 1 describes the part number nomenclature to identify the characteristics of the specific part number you have (for example, cores, frequency, temperature grade, fuse options, silicon revision). Figure 1 applies to the i.MX 6Dual/6Quad.

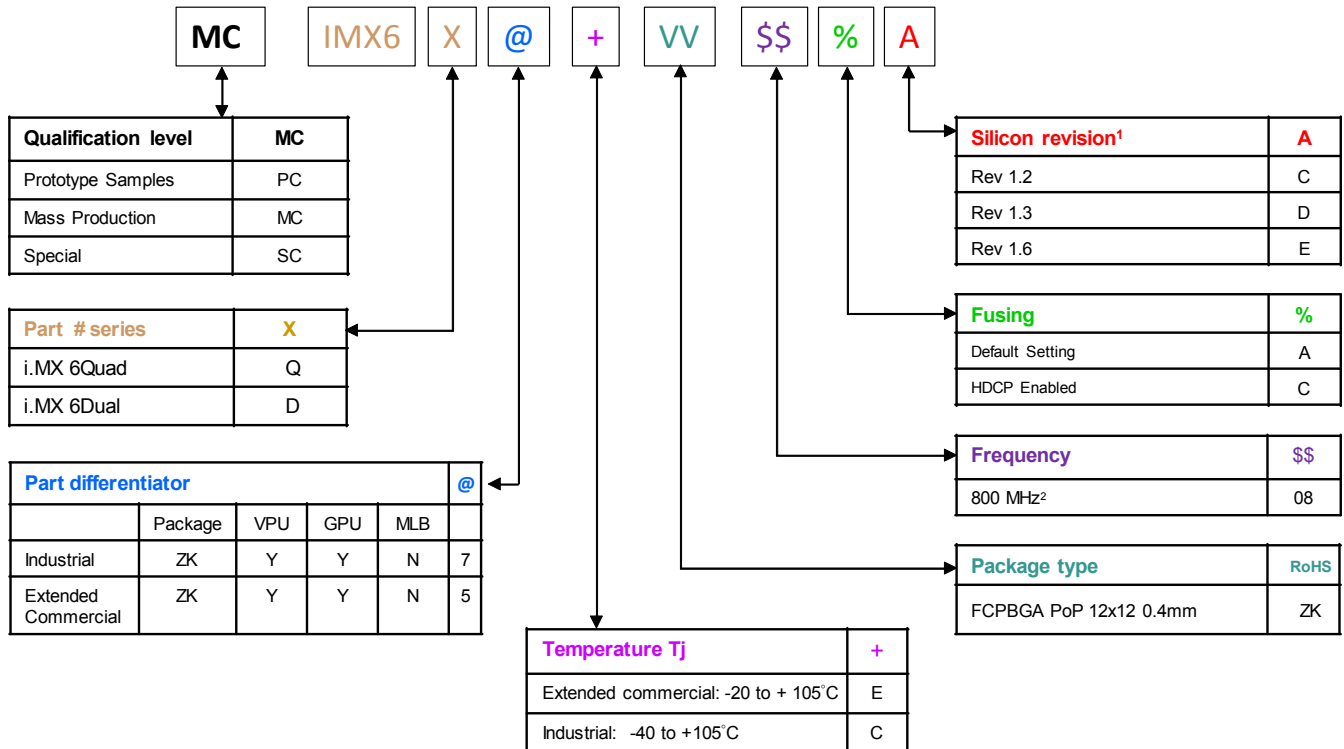
The two characteristics that identify which data sheet a specific part applies to are the part number series field and the temperature grade (junction) field:

- The i.MX 6Dual/6Quad Automotive and Infotainment Applications Processors data sheet (IMX6DQAEC) covers parts listed with “A (Automotive temp)”
- The i.MX 6Dual/6Quad Applications Processors for Consumer Products data sheet (IMX6DQCEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)”

## Introduction

- The i.MX 6Dual/6Quad Applications Processors for Consumer Products data sheet (IMX6DQCPOPEC) covers parts listed with “D (Commercial temp)” or “E (Extended Commercial temp)” and that uses the Package-on-Package.
- The i.MX 6Dual/6Quad Applications Processors for Industrial Products data sheet (IMX6DQIEC) covers parts listed with “C (Industrial temp)”

Ensure that you have the right data sheet for your specific part by checking the temperature grade (junction) field and matching it to the right data sheet. If you have questions, see [nxp.com/imx6series](http://nxp.com/imx6series) or contact your NXP representative.



**Figure 1. Part Number Nomenclature—i.MX 6Dual PoP and 6Quad PoP**

## 1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU processor (with TrustZone<sup>®</sup>)
- The core configuration is symmetric, where each core includes:

- 32 KByte L1 Instruction Cache
- 32 KByte L1 Data Cache
- Private Timer and Watchdog
- Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per [Table 6](#).
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

- Boot ROM, including HAB (96 KB)
- Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
- Secure/non-secure RAM (16 KB)
- External memory interfaces:
  - 2 × 32-bit, LPDDR2-800 channels supporting DDR interleaving mode
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
  - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps
- Displays—Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
  - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
  - LVDS serial ports—One port up to 170 Mpixels/sec (for example, WUXGA at 60 Hz) or two ports up to 85 MP/sec each
  - HDMI 1.4 port
  - MIPI/DSI, two lanes at 1 Gbps

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- Camera sensors:
  - Parallel Camera port (up to 20 bit and up to 240 MHz peak)
  - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6Dual/6Quad processor has four lanes.
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed PHY
    - Two HS hosts with integrated High Speed Inter-Chip (HS-IC) USB PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - SSI block capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I<sup>2</sup>S mode
  - ESAI is capable of supporting audio sample frequencies up to 260 kHz in I2S mode with 7.1 multi channel outputs
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while the other four support 4-wire. This is due to the SoC IOMUX limitation, because all UART IPs are identical.
  - Five eCSPI (Enhanced CSPI)
  - Three I2C, supporting 400 kbps
  - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000<sup>1</sup> Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

- Two Controller Area Network (FlexCAN), 1 Mbps each
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPU)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES .0)
- GPU2Dv2—2D Graphics Processing Unit (BitBlit)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSES and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

### 1.3 Signal Naming Convention

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Standardized Signal Name Map* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.



## Introduction

The signal names of the i.MX6 series of products are standardized to align the signal names within the family and across the documentation. Benefits of this standardization are as follows:

- Signal names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- Signal names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This standardization applies only to signal names. The ball names are preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

## 2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

### 2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

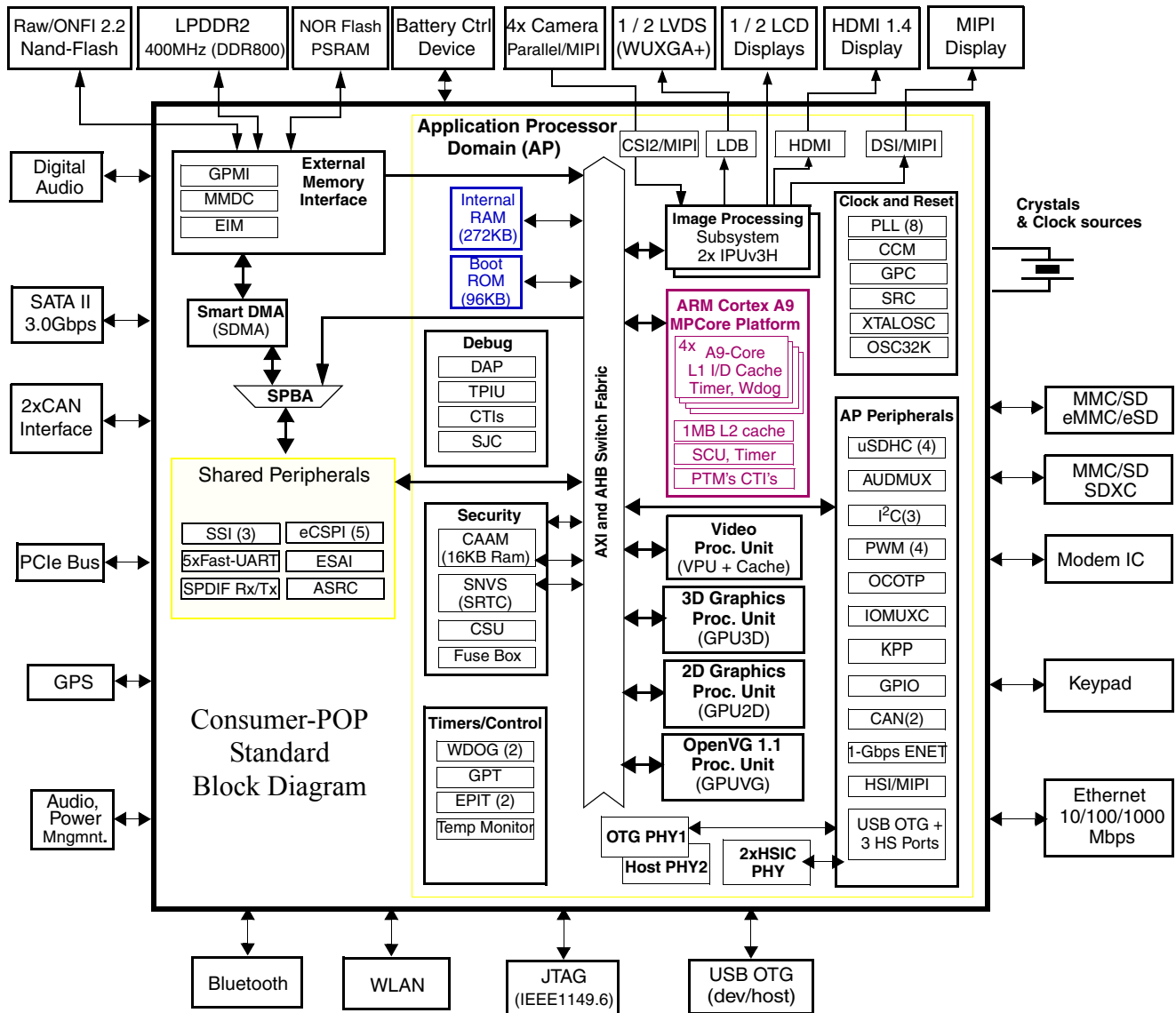


Figure 2. i.MX 6Dual/6Quad Consumer Grade System Block Diagram

#### NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

### 3 Modules List

The i.MX 6Dual/6Quad processors contain a variety of digital and analog modules. [Table 2](#) describes these modules in alphabetical order.

**Table 2. i.MX 6Dual/6Quad Modules List**

Block Mnemonic	Block Name	Subsystem	Brief Description
512 x 8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Dual/6Quad processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	System Control Peripherals	DMA controller used for GPMI2 operation.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of 4x (four) Cortex-A9 cores version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC error correction for NAND Flash controller (GPMI).
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Dual/6Quad processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	MIPI CSI-2 Interface	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports up to 1 Gbps for up to 3 data lanes and up to 800 Mbps for 4 data lanes.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Dual/6Quad platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: <ul style="list-style-type: none"> <li>• System memory and peripheral registers</li> <li>• All debug configuration registers</li> </ul> The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Dual/6Quad processor has two such modules, one for each IPU.
DSI	MIPI DSI interface	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
eCSPI1-5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX 6Dual/6Quad processors also consist of hardware assist for IEEE 1588 standard. For details, see the ENET chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM). <p><b>Note:</b> The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).</p>
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

**Table 2. i.MX 6Dual/6Quad Modules List (continued)**

Block Mnemonic	Block Name	Subsystem	Brief Description
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC error correction for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver. 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPU3Dv4	Graphics Processing Unit-3D, ver. 4	Multimedia Peripherals	The GPU2Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1



Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tessellation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I <sup>2</sup> C-1 I <sup>2</sup> C-2 I <sup>2</sup> C-3	I <sup>2</sup> C Interface	Connectivity Peripherals	I <sup>2</sup> C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: <ul style="list-style-type: none"> <li>• Parallel Interfaces for both display and camera</li> <li>• Single/dual channel LVDS display interface</li> <li>• HDMI transmitter</li> <li>• MIPI/DSI transmitter</li> <li>• MIPI/CSI-2 receiver</li> </ul> The processing includes: <ul style="list-style-type: none"> <li>• Image conversions: resizing, rotation, inversion, and color space conversion</li> <li>• A high-quality de-interlacing filter</li> <li>• Video/graphics combining</li> <li>• Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement</li> <li>• Support for display backlight reduction</li> </ul>
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: <ul style="list-style-type: none"> <li>• Open drain design</li> <li>• Glitch suppression circuit design</li> <li>• Multiple keys detection</li> <li>• Standby key press detection</li> </ul>
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: <ul style="list-style-type: none"> <li>• One clock pair</li> <li>• Four data pairs</li> </ul> Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: <ul style="list-style-type: none"> <li>• Supports dual x32 for LPDDR2-800</li> <li>• Supports up to 4 GByte DDR memory space</li> </ul>

**Table 2. i.MX 6Dual/6Quad Modules List (continued)**

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRM memory controllers.
ROM 96 KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	<p>The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:</p> <ul style="list-style-type: none"> <li>• Powered by a 16-bit Instruction-Set micro-RISC engine</li> <li>• Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels</li> <li>• 48 events with total flexibility to trigger any combination of channels</li> <li>• Memory accesses including linear, FIFO, and 2D addressing</li> <li>• Shared peripherals between ARM and SDMA</li> <li>• Very fast context-switching with 2-level priority based preemptive multi-tasking</li> <li>• DMA units with auto-flush and prefetch capability</li> <li>• Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address)</li> <li>• DMA ports can handle unit-directional and bi-directional flows (copy mode)</li> <li>• Up to 8-word buffer for configurable burst transfers</li> <li>• Support of byte-swapping and CRC calculations</li> <li>• Library of Scripts and API is available</li> </ul>
SJC	System JTAG Controller	System Control Peripherals	<p>The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards.</p> <p>The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.</p>
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	<p>The SSI is a full-duplex synchronous interface, which is used on the processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.</p>

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> <li>• 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)</li> <li>• Programmable baud rates up to 5 MHz</li> <li>• 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud</li> <li>• IrDA 1.0 support (up to SIR speed of 115200 bps)</li> <li>• Option to operate as 8-pins full UART, DCE, or DTE</li> </ul>
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: <ul style="list-style-type: none"> <li>• One high-speed OTG module with integrated HS USB PHY</li> <li>• One high-speed Host module with integrated HS USB PHY</li> <li>• Two identical high-speed Host modules connected to HSIC USB ports.</li> </ul>

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	<p>i.MX 6Dual/6Quad specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:</p> <ul style="list-style-type: none"> <li>• Conforms to the SD Host Controller Standard Specification version 3.0</li> <li>• Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41 including high-capacity (size &gt; 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports #3 and #4 only.</li> <li>• Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2TB.</li> <li>• Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10</li> <li>• Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00</li> </ul> <p>All four ports support:</p> <ul style="list-style-type: none"> <li>• 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max)</li> <li>• 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)</li> </ul> <p>However, the SoC-level integration and I/O muxing logic restrict the functionality to the following:</p> <ul style="list-style-type: none"> <li>• Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card Detection” and “Write Protection” pads and do not support hardware reset.</li> <li>• Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset.</li> <li>• All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.</li> </ul>
VDOA	VDOA	Multimedia Peripherals	The Video Data Order Adapter (VDOA) is used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for complete list of VPU's decoding/encoding capabilities.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.



Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: <ul style="list-style-type: none"> <li>• Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency</li> <li>• Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency</li> <li>• Multiple chip selects</li> </ul>
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

### 3.1 Special Signal Considerations

The package contact assignments can be found in [Section 6, “Package Information and Contact Assignments.”](#) Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual (IMX6DQRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

### 3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, “Unused analog interfaces,” of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

## 4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Dual/6Quad processors.

### 4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the SoC. See [Table 3](#) for a quick reference to the individual tables and sections.

**Table 3. i.MX 6Dual/6Quad Chip-Level Conditions**

For these characteristics, ...	Topic appears ...
<a href="#">Absolute Maximum Ratings</a>	<a href="#">on page 20</a>
<a href="#">PoP Package Thermal Resistance</a>	<a href="#">on page 21</a>
<a href="#">Operating Ranges</a>	<a href="#">on page 22</a>
<a href="#">External Clock Sources</a>	<a href="#">on page 24</a>
<a href="#">Maximum Measured Supply Currents</a>	<a href="#">on page 26</a>
<a href="#">Low Power Mode Supply Currents</a>	<a href="#">on page 27</a>
<a href="#">USB PHY Current Consumption</a>	<a href="#">on page 29</a>
<a href="#">SATA Typical Power Consumption</a>	<a href="#">on page 29</a>
<a href="#">PCIe 2.0 Maximum Power Consumption</a>	<a href="#">on page 30</a>
<a href="#">HDMI Maximum Power Consumption</a>	<a href="#">on page 31</a>

#### 4.1.1 Absolute Maximum Ratings

##### CAUTION

Stresses beyond those listed under [Table 4](#) may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

## Electrical Characteristics

**Table 4. Absolute Maximum Ratings**

Parameter Description	Symbol	Min	Max	Unit
Core supply input voltage (LDO enabled)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.6	V
Core supply input voltage (LDO bypass)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.4	V
Core supply output voltage (LDO enabled)	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP NVCC_PLL_OUT	-0.3	1.4	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.7	V
DDR I/O supply voltage	NVCC_DRAM	-0.4	1.975 (See note 1)	V
GPIO I/O supply voltage	NVCC_CSI NVCC_EIM NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD NVCC_JTAG	-0.5	3.7	V
HDMI, PCIe, and SATA PHY high (VPH) supply voltage	HDMI_VPH PCIE_VPH SATA_VPH	-0.3	2.85	V
HDMI, PCIe, and SATA PHY low (VP) supply voltage	HDMI_VP PCIE_VP SATA_VP	-0.3	1.4	V
LVDS and MIPI I/O supply voltage (2.5V supply)	NVCC_LVDS_2P5 NVCC_MIPI	-0.3	2.85	V
PCIe PHY supply voltage	PCIE_VPTX	-0.3	1.4	V
RGMI I/O supply voltage	NVCC_RGMII	-0.5	2.725	V
SNVS IN supply voltage (Secure Non-Volatile Storage and Real Time Clock)	VDD_SNVS_IN	-0.3	3.4	V
USB I/O supply voltage	USB_H1_DN USB_H1_DP USB_OTG_DN USB_OTG_DP USB_OTG_CHD_B	-0.3	3.73	V
USB VBUS supply voltage	USB_H1_VBUS USB_OTG_VBUS	—	5.35	V
$V_{in}/V_{out}$ input/output voltage range (non-DDR pins)	$V_{in}/V_{out}$	-0.5	OVDD+0.3 (See note 2)	V
$V_{in}/V_{out}$ input/output voltage range (DDR pins)	$V_{in}/V_{out}$	-0.5	OVDD+0.4 (See notes 1 & 2)	V
ESD immunity (HBM)	$V_{esd\_HBM}$	—	2000	V
ESD immunity (CDM)	$V_{esd\_CDM}$	—	500	V
Storage temperature range	$T_{storage}$	-40	150	°C

<sup>1</sup> The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC\_DRAM exceeds 1.575V.

<sup>2</sup> OVDD is the I/O supply voltage.

## 4.1.2 Thermal Resistance

### NOTE

Per JEDEC JESD51-2, the intent of thermal resistance measurements is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

### 4.1.2.1 FCPBGA Package Thermal Resistance

### 4.1.2.2 PoP Package Thermal Resistance

Table 5 provides the PoP package thermal resistance data.

**Table 5. PoP Package Thermal Resistance Data**

Rating	Board	Symbol	Value	Unit
Junction to Ambient <sup>1</sup> (natural convection)	Single layer board (1s)	$R_{\theta JA}$	41	°C/W
	Four layer board (2s2p)	$R_{\theta JA}$	26	°C/W
Junction to Ambient <sup>1</sup> (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	33	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	22	°C/W
Junction to Board <sup>2</sup>	—	$R_{\theta JB}$	13	°C/W
Junction to Case <sup>3</sup> (Top)	—	$R_{\theta JCtop}$	2	°C/W

<sup>1</sup> Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

<sup>2</sup> Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

<sup>3</sup> Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

### 4.1.3 Operating Ranges

Table 6 provides the operating ranges of the i.MX 6Dual/6Quad processors.

**Table 6. Operating Ranges**

Parameter Description	Symbol	Min	Typ	Max <sup>1</sup>	Unit	Comment <sup>2</sup>
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN <sup>3</sup>	1.275 <sup>4</sup>	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP <sup>5</sup> ) of 1.150 V minimum for operation up to 792 MHz.
		1.05 <sup>4</sup>	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN <sup>6</sup>	1.350 <sup>4</sup>	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275 <sup>4,7</sup>	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed <sup>8</sup>	VDD_ARM_IN VDD_ARM23_IN <sup>3</sup>	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925	—	1.3	V	LDO bypassed for operation up to 396 MHz.
	VDD_SOC_IN	1.225	—	1.3	V	264 MHz < VPU ≤ 352 MHz.
		1.15	—	1.3	V	VPU ≤ 264 MHz.
Standby/DSM Mode	VDD_ARM_IN VDD_ARM23_IN <sup>3</sup>	0.9	—	1.3	V	See Table 9, “Stop Mode Current and Power Consumption,” on page 27.
		VDD_SOC_IN	0.9	—	1.3	
VDD_HIGH internal Regulator	VDD_HIGH_IN <sup>9</sup>	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN <sup>9</sup>	2.8	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
Supply for RGMII I/O power group <sup>10</sup>	NVCC_RGMII	1.15	—	2.625	V	<ul style="list-style-type: none"> <li>• 1.15 V – 1.30 V in HSIC 1.2 V mode</li> <li>• 1.43 V – 1.58 V in RGMII 1.5 V mode</li> <li>• 1.70 V – 1.90 V in RGMII 1.8 V mode</li> <li>• 2.25 V – 2.625 V in RGMII 2.5 V mode</li> </ul>



Table 6. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max <sup>1</sup>	Unit	Comment <sup>2</sup>
GPIO supplies <sup>10</sup>	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDE, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	Isolation between the NVCC_EIMx and NVCC_SDx different supplies allow them to operate at different voltages within the specified range. Example: NVCC_EIM1 can operate at 1.8 V while NVCC_EIM2 operates at 3.3 V.
	NVCC_LVDS_2P5 <sup>11</sup> NVCC_MIPI	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.3	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.3	V	—
SATA Supply voltages	SATA_VP	0.99	1.1	1.3	V	—
	SATA_VPH	2.25	2.5	2.75	V	—
Junction temperature Extended Commercial	T <sub>J</sub>	-20	—	105	°C	See <i>i.MX 6Dual/6Quad Product Lifetime Usage Estimates Application Note, AN4724</i> , for information on product lifetime (power-on years) for this processor.
Junction temperature Industrial	T <sub>J</sub>	-40	—	105	°C	See <i>i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note, AN4724</i> , for information on product lifetime (power-on years) for this processor.

<sup>1</sup> Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V<sub>min</sub> + the supply tolerance). This results in an optimized power/speed ratio.

<sup>2</sup> See the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the \*\_CAP supply outputs.

<sup>3</sup> For Quad core system, connect to VDD\_ARM\_IN. For Dual core system, may be shorted to GND together with VDD\_ARM23\_CAP to reduce leakage.

<sup>4</sup> VDD\_ARM\_IN and VDD\_SOC\_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

<sup>5</sup> VDD\_ARM\_CAP must not exceed VDD\_CACHE\_CAP by more than +50 mV. VDD\_CACHE\_CAP must not exceed VDD\_ARM\_CAP by more than 200 mV.

<sup>6</sup> VDD\_SOC\_CAP and VDD\_PU\_CAP must be equal.

<sup>7</sup> In LDO enabled mode, the internal LDO output set points must be configured such that the:

VDD\_ARM LDO output set point does not exceed the VDD\_SOC LDO output set point by more than 100 mV.

VDD\_SOC LDO output set point is equal to the VDD\_PU LDO output set point.

The VDD\_ARM LDO output set point can be lower than the VDD\_SOC LDO output set point, however, the minimum output set points shown in this table must be maintained.

## Electrical Characteristics

- <sup>8</sup> In LDO bypassed mode, the external power supply must ensure that VDD\_ARM\_IN does not exceed VDD\_SOC\_IN by more than 100 mV. The VDD\_ARM\_IN supply voltage can be lower than the VDD\_SOC\_IN supply voltage. The minimum voltages shown in this table must be maintained.
- <sup>9</sup> To set VDD\_SNVS\_IN voltage with respect to Charging Currents and RTC, see the *Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG)*.
- <sup>10</sup> All digital I/O supplies (NVCC\_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.
- <sup>11</sup> This supply also powers the pre-drivers of the DDR I/O pins; therefore, it must always be provided, even when LVDS is not used.

### 4.1.4 External Clock Sources

Each i.MX 6Dual/6Quad processor has two external input system clocks: a low frequency (RTC\_XTALI) and a high frequency (XTALI).

The RTC\_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, that can be used instead of RTC\_XTALI when accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

#### NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC\_XTALI reference. If the internal oscillator is used instead, careful consideration should be given to the timing implications on all of the SoC modules dependent on this clock.

Table 7 shows the interface frequency requirements.

**Table 7. External Input Clock Frequency**

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator <sup>1,2</sup>	f <sub>ckil</sub>	—	32.768 <sup>3</sup> /32.0	—	kHz
XTALI Oscillator <sup>4,2</sup>	f <sub>xtal</sub>	—	24	—	MHz

<sup>1</sup> External oscillator or a crystal with internal oscillator amplifier.

<sup>2</sup> The required frequency stability of this clock source is application dependent. For recommendations, see the *Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG)*.

<sup>3</sup> Recommended nominal frequency 32.768 kHz.

<sup>4</sup> External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 7 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC\_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25  $\mu$ A more I<sub>dd</sub> than crystal oscillator
  - Approximately  $\pm$ 50% tolerance

- No external component required
- Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, an internal ring oscillator is used. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator.
  - If no external crystal is present, then the ring oscillator is used.

The decision to choose a clock source should be based on real-time clock use and precision timeout.

#### 4.1.5 Maximum Measured Supply Currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use case that requires maximum supply current is not a realistic use case.

To help illustrate the effect of the application on power consumption, data was collected while running industry standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Description of test conditions:

- The Power Virus data shown in [Table 8](#) represent a use case designed specifically to show the maximum current consumption possible for the ARM core complex. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited, if any, practical use case, and be limited to an extremely low duty cycle unless the intention was to specifically cause the worst case power consumption.
- EEMBC CoreMark: Benchmark designed specifically for the purpose of measuring the performance of a CPU core. More information available at [www.eembc.org/coremark](http://www.eembc.org/coremark). Note that this benchmark is designed as a core performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a computationally-intensive application rather than the Power Virus.
- 3DMark Mobile 2011: Suite of benchmarks designed for the purpose of measuring graphics and overall system performance. More information available at [www.rightware.com/benchmarks](http://www.rightware.com/benchmarks). Note that this benchmark is designed as a graphics performance benchmark, not a power benchmark. This use case is provided as an example of power consumption that would be typical in a very graphics-intensive application.
- Devices used for the tests were from the high current end of the expected process variation.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in [Table 8](#), however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6Dual/6Quad Power Consumption Measurement Application Note (AN4509)* for more details on typical power consumption under various use case definitions.