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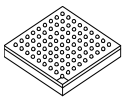
NXP Semiconductors
Data Sheet: Technical Data

Document Number: IMX6ULLIEC
Rev. 1.2, 11/2017

MCIMX6Y0CVM05AA MCIMX6Y0CVM05AB
MCIMX6Y1CVM05AA MCIMX6Y1CVM05AB
MCIMX6Y1CVK05AA MCIMX6Y1CVK05AB
MCIMX6Y2CVM05AA MCIMX6Y2CVM05AB
MCIMX6Y2CVM08AA MCIMX6Y2CVM08AB
MCIMX6Y2CVK08AB

i.MX 6ULL Applications Processors for Industrial Products



Package Information
Plastic Package
MAPBGA 14 x 14 mm, 0.8 mm pitch
MAPBGA 9 x 9 mm, 0.5 mm pitch

Ordering Information
See Table 1 on page 3

1 i.MX 6ULL Introduction

The i.MX 6ULL processors represent NXP's latest achievement in integrated multimedia-focused products offering high performance processing with a high degree of functional integration, targeted towards the growing market of connected devices.

The i.MX 6ULL is a high performance, ultra efficient processor family with featuring NXP's advanced implementation of the single Arm Cortex®-A7 core, which operates at speeds of up to 792 MHz. i.MX 6ULL includes integrated power management module that reduces the complexity of external power supply and simplifies the power sequencing. Each processor in this family provides various memory interfaces, including LPDDR2, DDR3, DDR3L, Raw and Managed NAND flash, NOR flash, eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.

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The i.MX 6ULL processors are specifically useful for applications such as:

- Telematics
- Audio playback
- Connected devices
- IoT Gateway
- Access control panels
- Human Machine Interfaces (HMI)
- Portable medical and health care
- IP phones
- Smart appliances
- eReaders

The features of the i.MX 6ULL processors include:

- Single-core Arm Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, an Electrophoretic Display (EPD) controller, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- 2x Ethernet interfaces—2x 10/100 Mbps Ethernet controllers.
- Human-machine interface—Each processor supports one digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: two high-speed USB on-the-go with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), two 12-bit ADC modules with up to 10 total input channels and two CAN ports.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, AES-128 encryption, SHA-1, SHA-256 HW acceleration engine, and secure software downloads. The security features are discussed in the *i.MX 6ULL Security Reference Manual* (IMX6ULLSRM).

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6ULL features, see Section 1.2, “Features"”.

1.1 Ordering Information

Table 1 provides examples of orderable part numbers covered by this data sheet.

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y0CVM05AA MCIMX6Y0CVM05AB	Features supports: • 528 MHz, industrial grade for general purpose • No security • No LCD/CSI • No CAN • Ethernet x1 • USB OTG x1 • ADC x1 • UART x4 • SAI x1 • No ESAI • Timer x2 • PWM x4 • I2C x2 • SPI x2	14 x 14 mm, 0.8 pitch MAPBGA	-40 to +105
MCIMX6Y1CVM05AA MCIMX6Y1CVM05AB	Features supports: • 528 MHz, industrial grade for general purpose • Basic security • No LCD/CSI • CAN x1 • Ethernet x1 • USB OTG x2 • ADC x1 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14 mm, 0.8 pitch MAPBGA	-40 to +105

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y1CVK05AA MCIMX6Y1CVK05AB	Features supports: • 528 MHz, industrial grade for general purpose • Basic security • No LCD/CSI • CAN x1 • Ethernet x1 • USB OTG x2 • ADC x1 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	9 x 9 mm, 0.5 pitch MAPBGA	-40 to +105
MCIMX6Y2CVM05AA MCIMX6Y2CVM05AB	Features supports: • 528 MHz, industrial grade for general purpose • Basic security • With LCD/CSI • CAN x2 • Ethernet x2 • USB OTG x2 • ADC x2 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14mm, 0.8 pitch MAPBGA	-40 to +105

Table 1. Ordering Information

Part Number	Feature	Package	Junction Temperature T_j (°C)
MCIMX6Y2CVM08AA MCIMX6Y2CVM08AB	Features supports: • 792 MHz, industrial grade for general purpose • Basic security • With LCD/CSI • CAN x2 • Ethernet x2 • USB OTG x2 • ADC x2 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	14 x 14 mm, 0.8 pitch MAPBGA	-40 to +105
MCIMX6Y2CVK08AB	Features supports: • 792 MHz, industrial grade for general purpose • Basic security • With LCD/CSI • CAN x2 • Ethernet x2 • USB OTG x2 • ADC x2 • UART x8 • SAI x3 • ESAI x1 • Timer x4 • PWM x8 • I2C x4 • SPI x4	9 x 9 mm, 0.5 pitch MAPBGA	-40 to +105

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number they have (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 6ULL Applications Processors for Industrial Products Data Sheet (IMX6ULLIEC) covers parts listed with a “C (Industrial temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there will be any questions, visit the web page NXP.com/imx6series or contact a NXP representative for details.

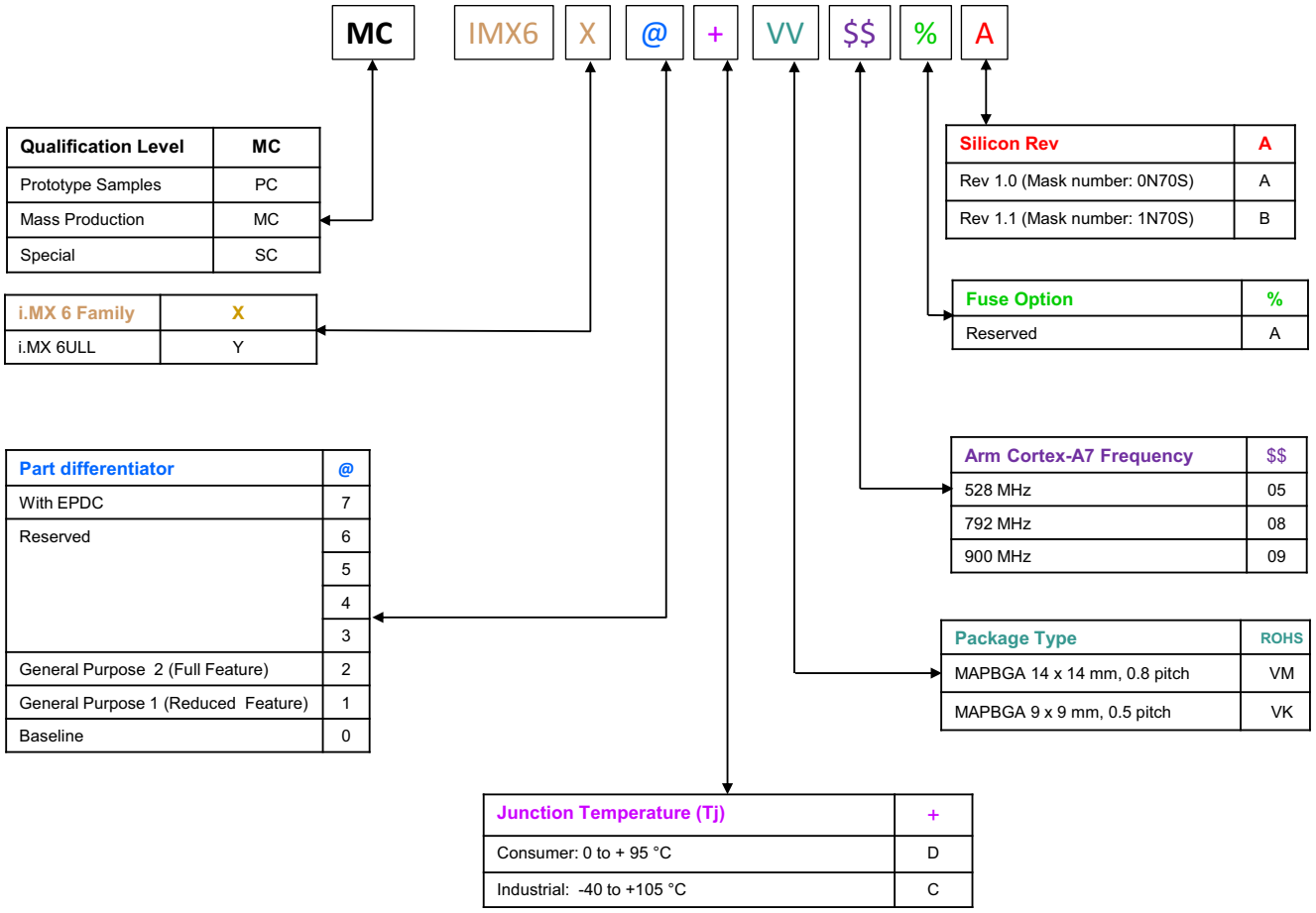

Figure 1. Part Number Nomenclature—i.MX 6ULL

1.2 Features

The i.MX 6ULL processors are based on Arm Cortex-A7 MPCore™ Platform, which has the following features:

- Supports single Arm Cortex-A7 MPCore (with TrustZone) with:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A7 NEON Media Processing Engine (MPE) Co-processor
- General Interrupt Controller (GIC) with 128 interrupts support
- Global Timer
- Snoop Control Unit (SCU)
- 128 KB unified I/D L2 cache
- Single Master AXI bus interface output of L2 cache

- Frequency of the core (including Neon and L1 cache), as per Table 10, "Operating Ranges," on page 24.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
  - 32 double-precision VFPv3 floating point registers

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia/shared, fast access RAM (OCRAM, 128 KB)
- External memory interfaces: The i.MX 6ULL processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
  - 16-bit LP-DDR2-800, 16-bit DDR3-800 and DDR3L-800
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bits.
  - 16/8-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

Each i.MX 6ULL processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays:
  - One parallel display port, support max 85 MHz display clock and up to WXGA (1366 x 768) at 60 Hz
  - Support 24-bit, 18-bit, 16-bit, and 8-bit parallel display
  - Electrophoretic display controller support direct-driver for E-Ink EPD panel, with up to 2048x1536 resolution at 106 Hz
- Camera sensors:
  - One parallel camera port, up to 24 bit and 133.3 MHz pixel clock
  - Support 24-bit, 16-bit, 10-bit, and 8-bit input
  - Support BT.656 interface
- Expansion cards:
  - Two MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
    - 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)

- USB:
  - Two high speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
- Miscellaneous IPs and interfaces:
  - Three I2S/SAI/AC97, up to 1.4 Mbps each
  - ESAI
  - Sony Philips Digital Interface Format (SPDIF), Rx and Tx
  - Eight UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - Support RTS/CTS for hardware flow control
  - Four eCSPI (Enhanced CSPI), up to 52 Mbps each
  - Four I^2C, supports 400 kbps
  - Two 10/100 Ethernet Controller (IEEE1588 compliant)
  - Eight Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - One Quad SPI to connect to serial NOR flash
  - Two Flexible Controller Area Network (FlexCAN)
  - Three Watchdog timers (WDOG)
  - 8-bit/10-bit/12-bit/16-bit camera interface
  - Two 12-bit Analog to Digital Converters (ADC) with up to 10 input channels in total

The i.MX 6ULL processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Use Voltage Sensor for monitoring the die voltage
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for Arm and NEON
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6ULL processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6ULL processors incorporate the following hardware accelerators:

- PXP—Pixel Processing Pipeline for image resize, rotation, overlay and CSC. Off loading key pixel processing operations are required to support the LCD display applications.
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- Arm TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock, both active tamper and passive tamper detection logic has up to 10 tamper inputs. Voltage monitor, temperature monitor, and clock frequency monitor protects the secure key storage.
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: AES-128 encryption, SHA-1, and SHA-256 HW acceleration engine, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions, such as display and camera interfaces, connectivity interfaces.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6ULL processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6ULL processor system.

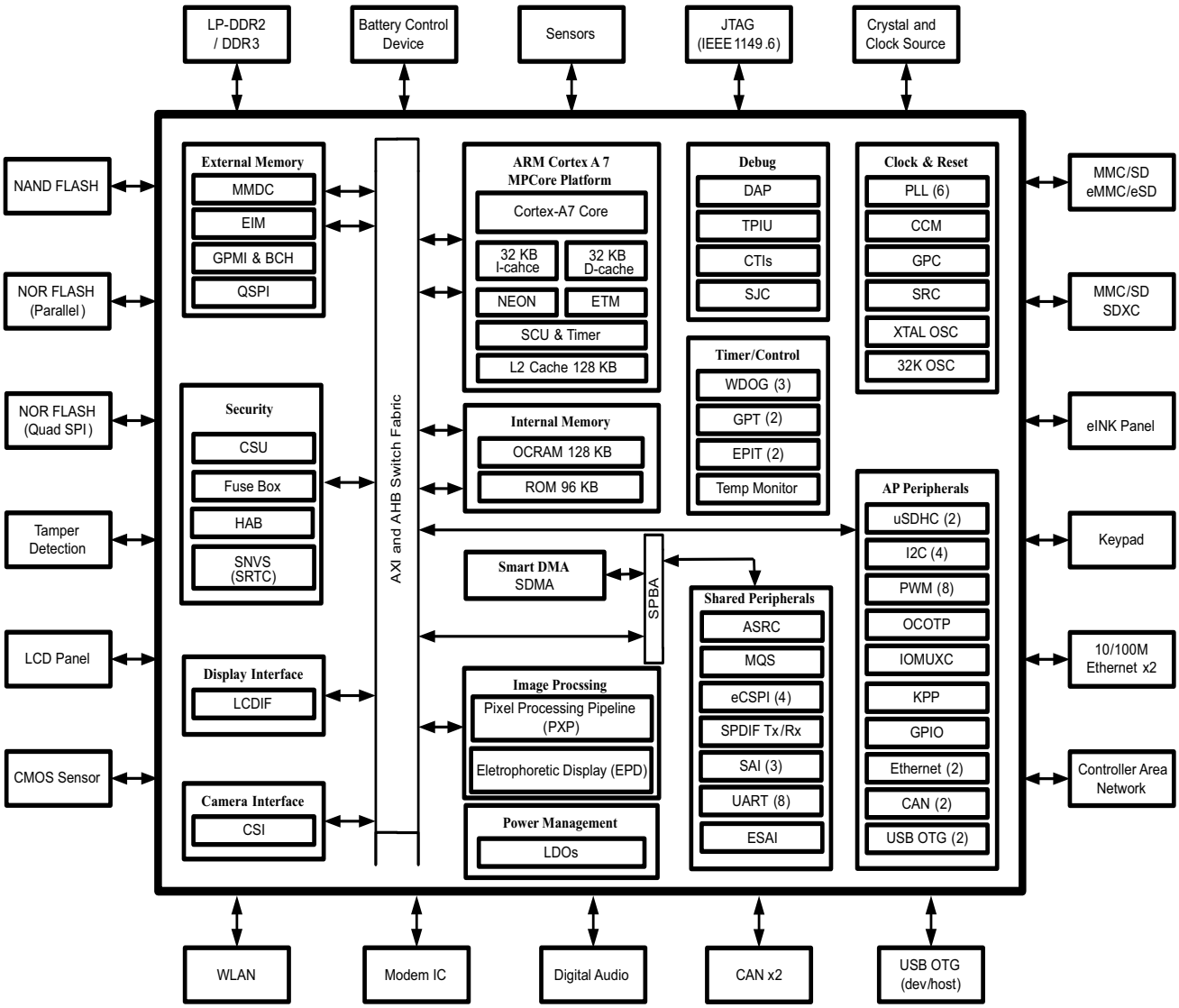

Figure 2. i.MX 6ULL System Block Diagram

3 Modules List

The i.MX 6ULL processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6ULL Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
ADC1 ADC2	Analog to Digital Converter	—	The ADC is a 12-bit general purpose analog to digital converter.
Arm	Arm Platform	Arm	The Arm Core Platform includes 1x Cortex-A7 core. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
BCH	Binary-BCH ECC Processor	System Control Peripherals	The BCH module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia Peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6ULL platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A7 Core Platform.

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPDC	Electrophoretic Display Controller	Multimedia Peripherals	The EPDC is a feature-rich, low power, and high performance direct-drive active matrix EPD controller. It is specially designed to drive E-INK^{TM} EPD panels, supporting a wide variety of TFT backplanes.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Purpose Memory Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices and 40-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.
GPT1 GPT2	General Purpose Timer	Timer peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD interface	Connectivity peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.
MQS	Medium Quality Sound	Multimedia Peripherals	MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM7 PWM8	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	Pixel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.
RNGB	Random Number Generator	Security	Random number generating module.
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module acts as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between Arm and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6ULL processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6ULL SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
System Counter	—	—	The system counter module is a programmable system counter which provides a shared time base to the Cortex A series cores as part of Arm's generic timer architecture. It is intended for use in application where the counter is always powered on and supports multiple, unrelated clocks.

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TSC	Touch Screen	Touch Controller	With touch controller to support 4-wire and 5-wire resistive touch panel.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by Arm) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4 UART5 UART6 UART7 UART8	UART Interface	Connectivity Peripherals	Each of the UARTv2 module supports the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 5 Mbps. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud
uSDHC1 uSDHC2	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6ULL specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 Two ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as interfaces to on-board peripherals. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface).

Table 2. i.MX 6ULL Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
USB	Universal Serial Bus 2.0	Connectivity Peripherals	USBO2 (USB OTG1 and USB OTG2) contains: • Two high-speed OTG 2.0 modules with integrated HS USB PHYs • Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0
WDOG1 WDOG3	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.
WDOG2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6ULL processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments"." Signal descriptions are provided in the *i.MX 6ULL Reference Manual* (IMX6ULLRM).

Table 3. Special Signal Considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N	One general purpose differential high speed clock Input/output is provided. It can be used: • To feed external reference clock to the PLLs and further to the modules inside SoC. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the *i.MX 6ULL Reference Manual* (IMX6ULLRM) for details on the respective clock trees. Alternatively one may use single ended signal to drive CLK1_P input. In this case corresponding CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. After initialization, the CLK1 input/output can be disabled (if not used). If unused, either or both of the CLK1_N/P pairs may remain unconnected.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required, system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO unconnected.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALO must be directly driven by the external oscillator and XTALI is disconnected. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when two DDR3 ICs plus the i.MX 6ULL are drawing current on the resistor divider.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6ULL reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be disconnected by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for NXP factory use. The user must tie this pin directly to GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused
CCM	CCM_CLK1_N, CCM_CLK1_P	Not connect
USB	USB_OTG1_CHD_B, USB_OTG1_DN, USB_OTG1_DP, USB_OTG1_VBUS, USB_OTG2_DN, USB_OTG2_DP, USB_OTG2_VBUS	Not connect
ADC	ADC_VREFH	Tie to VDDA_ADC_3P3
	VDDA_ADC_3P3	VDDA_ADC_3P3 must be powered even if the ADC is not used.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6ULL processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6ULL Chip-Level Conditions

For these characteristics	Topic appears
Absolute Maximum Ratings	on page 22
Thermal Resistance	on page 22
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximum Supply Currents	on page 27
Power Modes	on page 28
USB PHY Current Consumption	on page 31

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core Supply Voltage	VDDSOC_IN	-0.3	1.6	V
Internal Supply Voltage	VDDARM_CAP VDDSOC_CAP	-0.3	1.4	V
GPIO Supply Voltage	NVCC_CSI NVCC_ENET NVCC_GPIO NVCC_UART NVCC_LCD NVCC_NAND NVCC_SD1	-0.5	3.7	V
DDR IO Supply Voltage	NVCC_DRAM	-0.4	1.975[1]	V
VDD_SNVS_IN Supply Voltage	VDD_SNVS_IN	-0.3	3.6	V
VDDHIGH_IN Supply voltage	VDD_HIGH_IN	-0.3	3.7	V
USB VBUS	USB_OTG1_VBUS USB_OTG2_VBUS	—	5.5	V
Input voltage on USB_OTG_DP and USB_OTG_DN pins	USB_OTG1_DP/USB_OTG1_DN USB_OTG2_DP/USB_OTG2_DN	-0.3	3.63	V
Input/Output Voltage Range	$V_{in/Vout}$	-0.5	OVDD+0.3[2]	V
ESD damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	Vesd	 — —	 2000 500	V
Storage Temperature Range	TSTORAGE	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575 V.

2 OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 14 x 14 mm (VM) Package Thermal Resistance

Table 8 displays the 14 x 14 mm (VM) package thermal resistance data.

Table 8. 14 x 14 (VM) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural convection	Single-layer board (1s)	$R_{\theta JA}$	58.4	°C/W	1,2
Junction to Ambient Natural convection	Four-layer board (2s2p)	$R_{\theta JA}$	37.6	°C/W	1,2,3

Table 8. 14 x 14 (VM) Thermal Resistance Data (continued)

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	48.6	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	32.9	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	21.8	°C/W	4
Junction to Case	—	$R_{\theta JC}$	19.3	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	2.3	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB}	12.0	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB

4.1.2.2 9 x 9 MM (VK) Package Thermal Resistance

Table 9 displays the 9 x 9 MM (VK) thermal resistance data.

Table 9. 9 x 9 MM (VK) Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Ambient Natural Convection	Single-layer board (1s)	$R_{\theta JA}$	65.6	°C/W	1,2
Junction to Ambient Natural Convection	Four-layer board (2s2p)	$R_{\theta JA}$	36.2	°C/W	1,2,3
Junction to Ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	51.2	°C/W	1,3
Junction to Ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	31.8	°C/W	1,3
Junction to Board	—	$R_{\theta JB}$	17.1	°C/W	4
Junction to Case	—	$R_{\theta JC}$	14.5	°C/W	5
Junction to Package Top	Natural Convection	Ψ_{JT}	0.6	°C/W	6
Junction to Package Bottom	Natural Convection	Ψ_{JB_CSB}	11.1	°C/W	7

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistances between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7 Thermal resistance between the die and the central solder balls on the bottom of the package based on simulation.

4.1.3 Operating Ranges

Table 10 provides the operating ranges of the i.MX 6ULL processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6ULL Reference Manual* (IMX6ULLRM).

Table 10. Operating Ranges

Parameter Description	Symbol	Operating Conditions	Min	Typ	Max[1]	Unit	Comment
Run Mode: LDO Enabled	VDD_SOC_IN	A7 core at 792 MHz	1.325	—	1.5	V	VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point (VDD_ARM_CAP and VDD_SOC_CAP) for correct supply voltage regulation.
		A7 core at 528 MHz and below	1.275	—	1.5		
	VDD_ARM_CAP	A7 core at 792 MHz	1.2		1.26	V	—
		A7 core at 528 MHz	1.15	—	1.26		
		A7 core at 396 MHz	1.00	—	1.26		
		A7 core at 198 MHz	0.925	—	1.26		
	VDD_SOC_CAP	—	1.15	—	1.26	V	—
Run Mode: LDO Bypassed	VDD_SOC_IN	A7 core operations at 528 MHz or below.	1.15	—	1.26	V	A7 core operation above 528 MHz is not supported when LDO is bypassed.

Table 10. Operating Ranges (continued)

Low Power Run Mode: LDO Enabled	VDD_SOC_IN	—	1.275	—	1.5	V	VDD_SOC_IN must be 125 mV higher than the LDO Output Set Point (VDD_ARM_CAP and VDD_SOC_CAP) for correct supply voltage regulation.
	VDD_SOC_CAP	All PLL bypassed, all clocks running at 24 MHz or below	0.925	—	1.26	V	—
	VDD_ARM_CAP		0.925	—	1.26	V	
Low Power Run Mode: LDO Bypassed	VDD_SOC_IN	All PLL bypassed, all clocks running at 24 MHz or below	0.925	—	1.26	V	—
SUSPEND (DSM) Mode	VDD_SOC_IN	—	0.9	—	1.26	V	Refer to Table 15 Low Power Mode Current and Power Consumption on page -29
VDD_HIGH internal regulator	VDD_HIGH_IN[2]	—	2.80	—	3.6	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[2, 3]	—	2.40	—	3.6	V	Can be combined with VDDHIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS	—	4.40	—	5.5	V	—
	USB_OTG2_VBUS	—	4.40	—	5.5	V	—
DDR I/O supply	NVCC_DRAM	LPDDR2	1.14	1.2	1.3	V	—
		DDR3L	1.28	1.35	1.45	V	—
		DDR3	1.43	1.5	1.575	V	—
	NVCC_DRAM2P5	—	2.25	2.5	2.75	V	—
GPIO supplies	NVCC_CSI[2]	—	1.65	1.8, 2.8, 3.3	3.6	V	All digital I/O supplies (NVCC_xxxx) must be powered (unless otherwise specified in this data sheet) under normal conditions whether the associated I/O pins are in use or not.
	NVCC_ENET[2]						
	NVCC_GPIO[2]						
	NVCC_UART[2]						
	NVCC_LCD[2]						
	NVCC_NAND[2]						
	NVCC_SD1[2]						
A/D converter	VDDA_ADC_3P3[2]	—	3.0	3.15	3.6	V	VDDA_ADC_3P3 must be powered when chip is in RUN mode, IDLE mode, or SUSPEND mode. VDDA_ADC_3P3 should not be powered when chip is in SNVS mode.