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NXP Semiconductors
Data Sheet: Technical Data

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MCIMX7D*x*D*xxxxx*D
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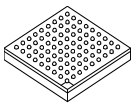
i.MX 7Dual Family of Applications Processors Datasheet



Package Information
Plastic Package
BGA 12 x 12 mm, 0.4 mm pitch
BGA 19 x 19 mm, 0.75 mm pitch

Ordering Information
See Table 1 on page 3

1 i.MX 7Dual introduction

The i.MX 7Dual family of processors represents NXP's latest achievement in high-performance processing for low-power requirements with a high degree of functional integration. These processors are targeted towards the growing market of connected and portable devices.

The i.MX 7Dual family of processors features advanced implementation of the ARM® Cortex®-A7 core, which operates at speeds of up to 1 GHz and 1.2 GHz, depending on the part number. The i.MX 7Dual family provides up to 32-bit DDR3/DDR3L/LPDDR2/LPDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

The i.MX 7Dual family of processors is specifically useful for applications such as:

- Audio
- Connected devices
- Access control panels
- Human-machine interfaces (HMI)
- Portable medical and health care
- IP phones
- Smart appliances
- Point of Sale
- eReaders
- Wearables
- Home energy management systems

The features of the i.MX 7Dual family of processors include the following:

- ARM Cortex-A7 plus ARM Cortex-M4—Heterogeneous Multicore Processing architecture enables the device to run an open operating system like Linux/Android on the Cortex-A7 core and an RTOS like FreeRTOS™ on the Cortex-M4 core.
- Two ARM Cortex-A7 cores—The processor enhances the capabilities of portable, connected applications by fulfilling the ever-increasing MIPS needs of operating systems and applications at lowest power consumption levels per MHz.
- Multilevel memory system—The multilevel Cortex-A7 memory system is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, DDR3L, LPDDR2 and LPDDR3, NOR Flash, NAND Flash (MLC and SLC), QSPI Flash, and managed NAND, including eMMC rev.
- Power efficiency—Power management implemented throughout the IC enables features and peripherals to consume minimum power in both active and various low-power modes.
- Multimedia—The multimedia performance is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) coprocessor, a programmable smart DMA (SDMA) controller.
- Up to two Gigabit Ethernet with AVB—10/100/1000 Mbps Ethernet controllers supporting IEEE Std 1588 time synchronization.
- Electronic Paper Display Controller (EPDC)—The processor integrates an EPD controller that supports E Ink color and monochrome panels with up to 2048 x 1536 resolution at 106 Hz refresh, 4096 x 4096 resolution at 20 Hz refresh, and 5-bit grayscale (32-levels per color channel).
- Human-machine interface (HMI)—i.MX 7Dual processor provides up to two separate display interfaces (parallel display and two-lane MIPI-DSI), CMOS sensor interface (two-lane MIPI-CSI and parallel).
- Interface flexibility—i.MX 7Dual processor supports connections to a variety of interfaces: two high-speed USB on-the-go modules with PHY, High-Speed Inter-Chip USB, multiple expansion card ports (high-speed MMC/SDIO host and other), two Gigabit Ethernet controllers with support for Ethernet AVB, PCIe-II, two 12-bit ADCs with a total of 8 single-ended inputs, two CAN ports, and a variety of other popular interfaces (such as UART, I^2C, and I^2S).

- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 7Dual security reference manual.
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different power domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 7Dual features, see Section 1.2, "Features."

1.1 Ordering information

Table 1 provides examples of orderable sample part numbers covered by this data sheet.

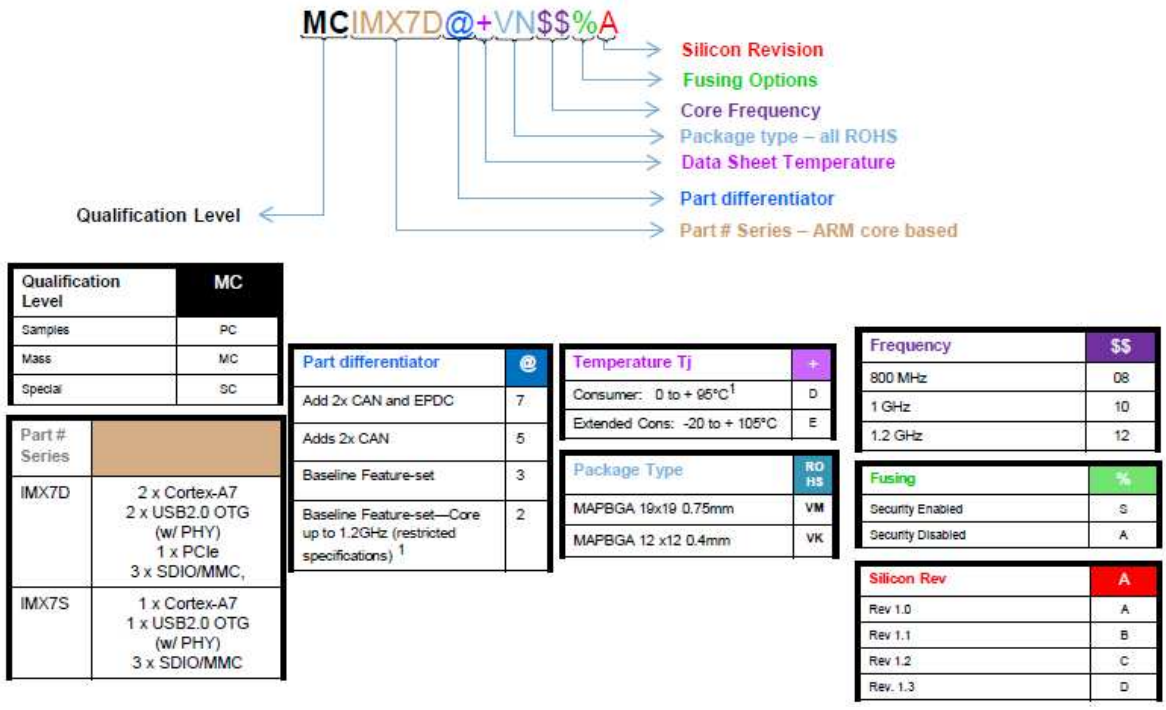
Table 1. Orderable parts

Part Number	Options	Cortex-A7 CPU Speed Grade	Qualification Tier	Temperature (T_j)	Package
MCIMX7D7DVK10SD	EPDC, CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Consumer[1]	0 to +95°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D7DVM10SD	EPDC, CAN 2 x Gigabit Ethernet 10 tamper pins 2 x ADC	1 GHz	Consumer[1]	0 to +95°C	19x19 mm 0.75 mm pitch BGA
MCIMX7D5EVM10SD	No EPDC, CAN 2 x Gigabit Ethernet 10 tamper pins 2 x ADC	1 GHz	Industrial[2]	-20 to 105°C	19x19 mm 0.75 mm pitch BGA
MCIMX7D3DVK10SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Consumer[1]	0 to +95°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D3EVK10SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1 x ADC	1 GHz	Industrial[2]	–20 to +105°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D2DVK12SD	No EPDC, No CAN 2 x Gigabit Ethernet 4 tamper pins 1x ADC	1.2 GHz	Consumer	0 to 85°C	12x12 mm 0.4 mm pitch BGA
MCIMX7D2DVM12SD	No EPDC, No CAN 2x Gigabit Ethernet 10 tamper pins 2x ADC	1.2 GHz	Consumer	0 to 85°C	19x19mm 0.75 mm pitch BGA

1 Consumer qualification grade assumes 5-year lifetime with 50% duty cycle.

2 Industrial qualification grade assumes 10-year lifetime with 100% duty cycle.

Figure 1 describes the part number nomenclature so that the users can identify the characteristics of the specific part number.



[1] Restricted electrical specifications for parts with CPU maximum frequency of 1.2 GHz:

- Temperature range 0 to 85 degrees C (see Table 1)
- VDD_ARM requirements (see Table 9)

Figure 1. Part number nomenclature—i.MX 7Dual family of processors

1.2 Features

The i.MX 7Dual family of processors is based on ARM Cortex-A7 MPCore™ Platform, which has the following features:

- Two ARM Cortex-A7 Cores (with TrustZone® technology)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - NEON MPE (media processing engine) coprocessor

The ARM Cortex-A7 Core complex shares:

- General interrupt controller (GIC) with 128 interrupt support
- Global timer
- Snoop control unit (SCU)
- 512 KB unified I/D L2 cache

- Two master AXI bus interfaces output of L2 cache
- Frequency of the core (including NEON and L1 cache), as per Table 9.
- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The ARM Cortex-M4 platform:

- Cortex-M4 CPU core
- MPU (memory protection unit)
- FPU (floating-point unit)
- 16 KByte instruction cache
- 16 KByte data cache
- 64 KByte TCM (tightly-coupled memory)

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (256 KB of total OCRAM)
  - Secure/nonsecure RAM (32 KB)
- External memory interfaces: The i.MX 7Dual family of processors supports the latest, high-volume, cost effective DRAM, NOR, and NAND Flash memory standards.
  - Up to 32-bit LP-DDR2-1066, DDR3-1066, DDR3L-1066, and LPDDR3-1066
  - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 62 bits.
  - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.

Each i.MX 7Dual processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Available interfaces.
  - One parallel 24-bit display port
  - One EPD port
  - One MIPI DSI port
- Camera sensors:
  - One parallel Camera port (up to 24 bit and up to 133 MHz peak)
  - One MIPI-CSI port
- Expansion cards:
  - Three MMC/SD/SDIO card ports all supporting the following. Moreover, the third port can support HS400.

  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards, up to 208 MHz
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS200 and HS400 DDR modes
- USB:
  - Two high-speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - One high-speed USB 2.0 (480 Mbps) host with integrated HSIC USB (high-speed inter-chip USB) PHY
- Expansion PCI Express port (PCIe) v. 2.1 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting root complex operations and endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - Three instances of SAI supporting up to three I^2S and AC97 ports
  - Seven UARTs, up to 4.0 Mbps:
    - Providing RS232 interface
    - Supporting 9-bit RS485 Multidrop mode
  - Four eCSPI (Enhanced CSPI)
  - Four I^2C, supporting 400 kbps
  - Two 1-gigabit Ethernet controllers (designed to be compatible with IEEE Std 1588), 10/100/1000 Mbps with AVB support
  - Four pulse width modulators (PWM)
  - System JTAG controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 key pad port (KPP)
  - One quad SPI
  - Four watchdog timers (WDOG)
  - One (12 x 12 mm) or two (19 x 19 mm) 2-channel, 12-bit analog-to-digital converters (ADC)—effective number of bits (ENOB) can vary (typically 9–10 bits) depending on the system implementation and the condition of the power/ground noise condition

The i.MX 7Dual family of processors integrates advanced power management unit and controllers:

- PMU (power-management unit), multiple LDO supplies, for on-chip resources
- Temperature sensor for monitoring the die temperature
- Software state retention and power gating for ARM and NEON
- Support for various levels of system power modes
- Flexible clock gating control scheme

The i.MX 7Dual family of processors uses dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 7Dual family of processors incorporates the following hardware accelerators:

- PXP—PiXel processing pipeline for imagine resize, rotation, overlay and CSC. Off loading key pixel processing operations are required to support the LCD and EPDC display applications.
- EPDC

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone technology including separation of interrupts and memory mapping
- SJC—System JTAG controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic acceleration and assurance module, containing cryptographic and hash engines supporting DPA (differential power analysis) protection, 32 KB secure RAM, and true and pseudo random number generator (NIST certified).
- SNVS—Secure non-volatile storage, including secure real time clock
- CSU—Central security unit. Enhancement for the IC identification module (IIM). Configured during boot and by eFuses and determines the security-level operation mode as well as the TrustZone policy.
- A-HAB—Advanced high-assurance boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, SRK revocation mechanism, warm boot, CSU, and TrustZone initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1. Functions, such as display and camera interfaces, connectivity interfaces, may not be enabled for specific part numbers.

2 Architectural overview

The following subsections provide an architectural overview of the i.MX 7Dual processor system.

2.1 Block diagram

Figure 2 shows the functional modules in the i.MX 7Dual processor system.

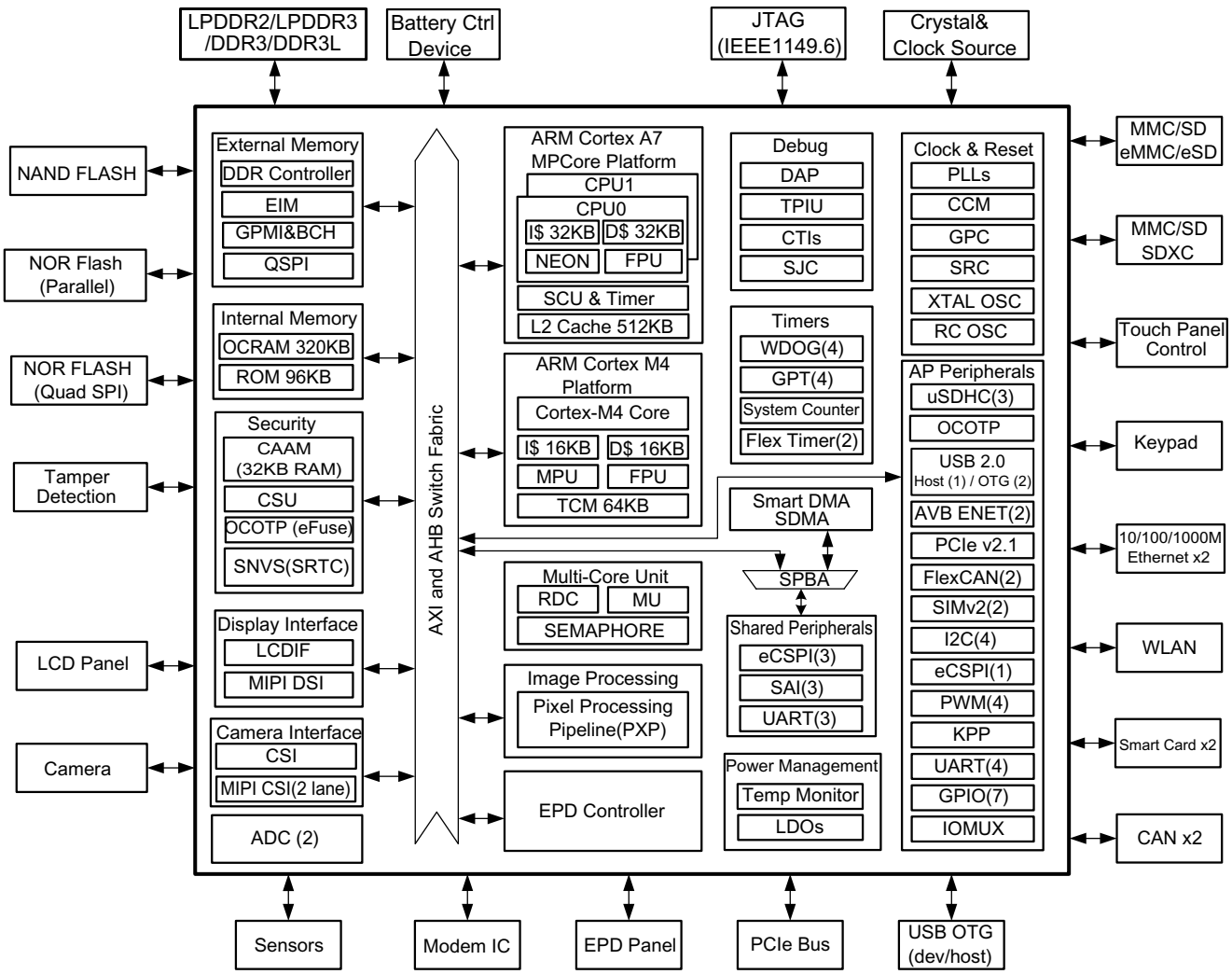


Figure 2. i.MX 7Dual System block diagram

3 Modules list

The i.MX 7Dual family of processors contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 7Dual modules list

Block Mnemonic	Block Name	Subsystem	Brief Description
ADC1 ADC2	Analog to Digital Converter		The ADC is a 12-bit general purpose analog to digital converter (ADC2 is not available in the 12x12 package).
ARM	ARM Platform	ARM	The ARM Core Platform includes two Cortex-A7 coresand 1x Cortex-M4. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
BCH	Binary-BCH ECC Processor	System control peripherals	The BCH module provides up to 62-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, entropy source generator, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certifiable by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). CAAM also implements a Secure Memory mechanism. In i.MX 7Dual processors, the security memory provided is 32 KB.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, resets, and power control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	Parallel CSI	Multimedia peripherals	The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
CSU	Central Security Unit	security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 7Dual platform.
DAP	Debug Access Port	System control peripherals	The DAP provides real-time access for the debugger without halting the core to access: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains.

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support for 16-bit (in Muxed I/O mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support for 16-bit (in muxed and non-muxed I/O modes) NOR-Flash memories, at slow frequency • Multiple chip selects
ENET1 ENET2	Ethernet Controller	Connectivity peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details.
EPDC	Electrophoretic Display Controller	Connectivity peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E Ink™ EPD panels, supporting a wide variety of TFT backplanes. Various levels of flexibility and programmability have been introduced, as well as hardware support for different E Ink image enhancing algorithms, such as Regal D waveform support.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
FLEXTIMER1 FLEXTIMER2	Flexible Timer Module	Timer Peripherals	Provide input signal capture and PWM support
GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7	General Purpose I/O Modules	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPMI	General Purpose Memory Interface	Connectivity peripherals	The GPMI module supports up to 8x NAND devices and 62-bit ECC encryption/decryption for NAND Flash Controller (GPMI2). GPMI supports separate DMA channels for each NAND device.

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPT	General Purpose Timer	Timer peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
I2C1 I2C2 I2C3 I2C4	I^2C Interface	Connectivity peripherals	I^2C provide serial interface for external devices. Data rates of up to 320 kbps are supported.
IOMUXC	IOMUX Control	System control peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD interface	Multimedia peripherals	The LCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability. The LCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface).
MIPI-CSI (two-lane)	MIPI Camera Interface	Multimedia peripherals	This module provides a two-lane MIPI camera interface operating up to a maximum bit rate of 1.5 Gbps.
MIPI DSI (two-lane)	MIPI Display Interface	Connectivity peripherals	This module provides a two-lane MIPI display interface operating up to a maximum bit rate of 1.5 Gbps.
DDRC	DDR Controller	Connectivity peripherals	The DDR Controller has the following features: • Supports 16/32-bit DDR3/DDR3L, LPDDR3, and LPDDR2-1066 • Supports up to 2 Gbyte DDR memory space
MQS	Medium-quality sound module	Multimedia peripherals	MQS is used to generate 2-channel, medium-quality, PWM-like audio, via two standard digital GPIO pins. The electronic specification is the same as the GPIO digital output.

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 7Dual processors, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
PCIe	PCI Express 2.0	Connectivity peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power Management Unit	Data path	Integrated power management unit. Used to provide power to various SoC domains.
PWM1 PWM2 PWM3 PWM4	Pulse Width Modulation	Connectivity peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
PXP	PiXel Processing Pipeline	Display peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with the integrated EPD.

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module act as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	Synchronous Audio Interface	Connectivity peripherals	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I^2S, AC97, TDM, and codec/DSP interfaces.
SDMA	Smart Direct Memory Access	System control peripherals	The SDMA is a multichannel flexible DMA engine. It helps in maximizing system performance by offloading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unidirectional and bidirectional flows (Copy mode) • Up to 8-word buffer for configurable burst transfers for EMIv2.5 • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SIMv2-1 SIMv2-2	Smart Card	Connectivity peripherals	Smart card interface designed to be compatible with ISO7816.

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SJC	System JTAG Controller	System control peripherals	The SJC provides JTAG interface (designed to be compatible with JTAG TAP standards) to internal logic. The i.MX 7Dual family of processors uses JTAG port for production, testing, and system debugging. Additionally, the SJC provides BSR (Boundary Scan Register) standard support, designed to be compatible with IEEE 1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 7Dual SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
TEMPSENSOR	Temperature Sensor	System control peripherals	Temperature sensor
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART1 UART2 UART3 UART4 UART5 UART6 UART7	UART Interface	Connectivity peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 Mbps. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC1 uSDHC2 uSDHC3	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity peripherals	i.MX 7Dual SoC characteristics: All the MMC/SD/SDIO controller IPs are based on the uSDHC IP. They are designed to be: • Fully compatible with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2. • Fully compatible with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications v 3.0 including high-capacity SDXC cards up to 2 TB. • Fully compatible with SDIO command/response sets and interrupt/Read-Wait mode as defined in the SDIO Card Specification, Part E1, v. 3.0 All the ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS200 and HS400. However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • uSDHC1 and uSDHC2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • uSDHC3 is primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for uSDHC1 and uSDHC2 in 4-bit configuration (SD interface). uSDHC3 is placed in his own independent power domain.
USBOTG2	2x USB 2.0 High Speed OTG and HSIC USB	Connectivity peripherals	USBOTG2 contains: • Two high-speed OTG modules with integrated HS USB PHYs • One high-speed Host module connected to HSIC USB port.

Table 2. i.MX 7Dual modules list(continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG1 WDOG3 WDOG4	Watchdog	Timer peripherals	The Watch dog timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG2 (TrustZone)	Watchdog (TrustZone technology)	Timer peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping Normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.

3.1 Special signal considerations

Table 3 lists special signal considerations for the i.MX 7Dual family of processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package information and contact assignments." Signal descriptions are provided in the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

Table 3. Special signal considerations

Signal Name	Remarks
CCM_CLK1_P/ CCM_CLK1_N CCM_CLK2	One general purpose differential high speed clock input/output and one single-ended clock input are provided. Either or both of them can be used: • To feed an external reference clock to the PLLs and to the modules inside the SoC, for example, as an alternate reference clock for PCIe, Video/Audio interfaces and so forth. • To output the internal SoC clock to be used outside the SoC as either a reference clock or as a functional clock for peripherals; for example, it can be used as an output of the PCIe master clock (root complex use) See the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM) for details on the respective clock trees. The CCM_CLK1_* inputs/outputs are an LVDS differential pair. Alternatively, a single-ended signal may be used to drive CCM_CLK1_P input. In this case corresponding CCM_CLK1_N input should be tied to the constant voltage level equal to 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See the LVDS pad electrical specification for further details. CCM_CLK2 is a single-ended input referenced to ground. After initialization: • The CCM_CLK1_* inputs/outputs can be disabled if not used. Any of the unused CCM_CLK1_* pins may be left floating. • The CCM_CLK2 input should be grounded if not used.
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (100 k ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. It is recommended to use the configurable load capacitors provided in the IP instead of adding them externally. To hit the exact oscillation frequency, the configurable capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 M). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level. In the case when a high-accuracy realtime clock is not required, the system may use internal low frequency oscillator. It is recommended to connect RTC_XTALI to ground and keep RTC_XTALO floating. This will however result in increased power consumption, because the internal oscillator uses higher power than the RTC oscillator. Thus for lowest power configuration it is recommended to always install a crystal.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO.

Table 3. Special signal considerations(continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 7Dual are drawing current on the resistor divider. It is recommended to use regulated power supply for “big” memory configurations (more than eight devices)
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
PCIE_VPH/PCIE_VPH_TX/ PCIE_VPH_RX	Short these pins to VDDA_PHY1P8 if using PCIe. User can tie these pins to ground if not using PCIe.
PCIE_VP/PCIE_VP_TX/PC IE_VP_RX	Short these pins to VDDD_1P0CAP if using PCIe. User can tie these pins to ground with a 10 KΩ resistor if not using PCIe.
VDDA_MIPI_1P8	Short these pins to VDDA_PHY_1P8 if using MIPI. User can leave these pins floating or grounded if not using MIPI.
VDD_MIPI_1P0	Short these pins to VDDD_1P0_CAP if using MIPI. User can leave these pins floating or grounded if not using MIPI.
GPANAIO	This signal is reserved for manufacturing use only. User must leave this connection floating.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM). Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to high configures the JTAG interface to a mode compatible with the IEEE 1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	Do not connect. These signals are reserved and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	In Normal mode, may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for factory use. This signal is internally connected to an on-chip pull-down device. The user must tie this signal to GND.

Table 3. Special signal considerations(continued)

Signal Name	Remarks
PCIE_REXT	The impedance calibration process requires connection of reference resistor 4.7 KΩ 1% precision resistor on PCIE_REXT pad to ground.
USB_OTG1_REXT/USB_OTG2_REXT	The bias generation and impedance calibration process for the USB OTG PHYs requires connection of 200 Ω (1% precision) reference resistors on each of the USB_OTG1_REXT and USB_OTG2_REXT pads to ground.
USB_OTG1_CHD_B	An external pullup resistor with value in range from 10 kΩ to 100 kΩ should be connected between open-drain output USB_OTG1_CHD_B and supply VDD_USB_OTG1_3P3_IN for 3.3 V signaling. Optionally, a similarly valued pullup resistor could be connected instead between USB_OTG1_CHD_B and an unrelated supply up to 1.8 V, but in that case the output is only valid when both that supply and VDD_USB_OTG1_3P3_IN are powered.
TEMPSENSOR_REXT	External 100 KΩ (1% precision) resistor connection pin

Table 4. JTAG controller interface summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	100 kΩ pull-up
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended connections for unused analog interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended connections for unused analog interfaces

Module	Package Net Name	Recommendation if Unused
ADC	VDDA_ADC2_1P8, VDDA_ADC2_1P8, VDDA_ADC1_1P8, VDDA_ADC1_1P8	1.8 V
	ADC2_IN3, ADC2_IN2, ADC2_IN1, ADC2_IN0, ADC1_IN0, ADC1_IN1, ADC1_IN2, ADC1_IN3	Tie to ground
LDO	VDD_1P2_CAP	Floating if USB_HSIC is not used
MIPI	VDD_MIPI_1P0, VDDA_MIPI_1P8	Floating or tie to ground
	MIPI_DSI_D0_N, MIPI_DSI_D0_P, MIPI_VREG_0P4V, MIPI_DSI_CLK_N, MIPI_DSI_CLK_P, MIPI_DSI_D1_N, MIPI_DSI_D1_P, MIPI_CSI_D0_N, MIPI_CSI_D0_P, MIPI_CSI_CLK_N, MIPI_CSI_CLK_P, MIPI_CSI_D1_N, MIPI_CSI_D1_P	No connect

Table 5. Recommended connections for unused analog interfaces(continued)

Module	Package Net Name	Recommendation if Unused
PCIe	PCIE_REFCLKIN_N, PCIE_REFCLKIN_P, PCIE_REFCLKOUT_N, PCIE_REFCLKOUT_P, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, PCIE_TX_P	Floating
	PCIE_VP,PCIE_VP_RX,PCIE_VP_TX, PCIE_VPH,PCIE_VPH_RX,PCIE_VPH_TX, PCIE_REXT	Tie to ground
SNVS	SNVS_TAMPER00, SNVS_TAMPER01, SNVS_TAMPER02, SNVS_TAMPER03, SNVS_TAMPER04, SNVS_TAMPER05, SNVS_TAMPER06, SNVS_TAMPER07, SNVS_TAMPER08, SNVS_TAMPER09	Float—configure with software
Temperature sensor	TEMPSENSOR_REXT	Tie to ground or pulldown with 100 KΩ resistor
	TEMPSENSOR_RESERVE	Floating
	VDD_TEMPSENSOR_1P8	1.8 V
USB HSIC	VDD_USB_H_1P2	Tie to ground
	USB_H_DATA, USB_H_STROBE	Floating
USB OTG1	VDD_USB_OTG1_3P3_IN, VDD_USB_OTG1_1P0_CAP	Tie to ground
	USB_OTG1_VBUS, USB_OTG1_DP, USB_OTG1_DN, USB_OTG1_ID, USB_OTG1_REXT, USB_OTG1_CHD_B	Floating
USB OTG2	VDD_USB_OTG2_3P3_IN, VDD_USB_OTG2_1P0_CAP	Tie to ground
	USB_OTG2_VBUS, USB_OTG2_DP, USB_OTG2_DN, USB_OTG2_ID, USB_OTG2_REXT	Floating

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 7Dual family of processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 7Dual Chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	on page 21
FPBGA case “X” and case “Y” package thermal resistance	on page 22
Operating ranges	on page 23
External clock sources	on page 25

Table 6. i.MX 7Dual Chip-level conditions(continued)

For these characteristics, …	Topic appears …
Maximum supply currents	on page 26
Power modes	on page 29
USB PHY Suspend current consumption	on page 32

4.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed under Table 7 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operating ranges or parameters tables is not implied.

Table 7. Absolute maximum ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDD_ARM VDD_SOC	–0.5	1.5	V
GPIO supply voltage	NVCC_ENET1 NVCC_EPDC1 NVCC_EPDC2 NVCC_I2C NVCC_LCD NVCC_SAI NVCC_SD1 NVCC_SD2 NVCC_SD3 NVCC_SPI NVCC_UART	–0.3	3.6	V
DDR I/O supply voltage	NVCC_DRAM	–0.3	1.975	V
Clock I/O supply voltage	NVCC_DRAM_CKE	–0.3	1.98	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	–0.3	3.6	V
USB OTG PHY supply voltage	VDD_USB_OTG1_3P3_IN VDD_USB_OTG2_3P3_IN	–0.3	3.6	V
USB_VBUS input detected	USB_OTG1_VBUS USB_OTG2_VBUS	–0.3	5.25	V
Input voltage on USB_OTG*_DP, USB_OTG*_DN pins	USB_OTG1_DP/USB_OTG1_DN USB_OTG2_DP/USB_OTG2_DN	–0.3	3.63	V
USB_OTG1_CHD_B open-drain pullup voltage when external pullup resistor is connected to VDD_USB_OTG1_3P3_IN supply only	USB_OTG1_CHD_B	—	3.6	V

Table 7. Absolute maximum ratings(continued)

Parameter Description	Symbol	Min	Max	Unit
USB_OTG1_CHD_B open-drain pullup voltage when external pullup resistor is connected to any supply other than VDD_USB_OTG1_3P3_IN	USB_OTG2_CHD_B	—	1.975	V
Input/output voltage range	V_{in}/V_{out}	–0.3	OVDD[1]+0.3	V
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage temperature range	$T_{STORAGE}$	–40	150	°C

1 OVDD is the I/O supply voltage.

4.1.2 Thermal resistance

4.1.2.1 FPBGA case “X” and case “Y” package thermal resistance

Table 8 displays the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Test conditions	Symbol	12x12 pkg value	19x19 pkg value	Unit
Junction to Ambient[1]	Single-layer board (1s); natural convection[2] Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$ $R_{\theta JA}$	55.4 32.6	44.4 30.2	°C/W °C/W
Junction to Ambient[1]	Single-layer board (1s); airflow 200 ft/min[2,3] Four-layer board (2s2p); airflow 200 ft/min[2,3]	$R_{\theta JA}$ $R_{\theta JA}$	41.8 28.0	34.3 25.8	°C/W °C/W
Junction to Board[1,4]	—	$R_{\theta JB}$	16.0	17.4	°C/W
Junction to Case[1,5]	—	$R_{\theta JC}$	10.5	10.4	°C/W
Junction to Package Top[1,6]	Natural Convection	Ψ_{JT}	0.2	0.2	°C/W
Junction to Package Bottom	Natural Convection	$R_{\theta B\_CSB}$	15.3	17.3	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating ranges

Table 9 provides the operating ranges of the i.MX 7Dual family of processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 7Dual Application Processor Reference Manual* (IMX7DRM).

Table 9. Operating ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run Mode	VDD_ARM	0.95	1.0	1.25	V	Operation at 800 MHz and below
		1.045	1.1	1.25	V	Operation between 800 MHz and 1 GHz
		1.2	1.225	1.25	V	Operation between 1.0 GHz and 1.2 GHz. See Table 1 for maximum frequencies.
	VDD_SOC	0.95	1.0	1.25	V	—
Standby/ Deep Sleep mode	VDD_ARM	0	1.0	1.25	V	See Table 14, "Power modes," on page 29.
	VDD_SOC	0.95	1.0	1.155	V	
Power Supply Analog Domain and LDOs	VDDA_1P8	1.71	1.8	1.89	V	Power for analog LDO and internal analog blocks. Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN	2.4	3.0	3.6	V	—
LDO for Low-Power State Retention mode	VDD_LPSR	1.71	1.8	1.89	V	Power rail for Low Power State Retention mode
Supply for 24 MHz crystal	VDD_XTAL_1P8	1.650	1.8	1.950	V	—
Temperature sensor	VDD_TEMPSENSOR	1.710	1.8	1.890	V	—
USB supply voltages	VDD_USB_OTG1_3P3_IN	3.0	3.3	3.6	V	This rail is for USB
	VDD_USB_OTG2_3P3_IN	3.0	3.3	3.6	V	This rail is for USB

Table 9. Operating ranges(continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
DDR I/O supply voltage	NVCC_DRAM, NVCC_DRAM_CKE	1.14	1.2	1.3	V	LPDDR2, LPDDR3
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3L
	DRAM_VREF	0.49 × NVCC_DRAM)	0.5 × NVCC_DRAM	0.51 × NVCC_DRAM	V	Set to one-half NVCC_DRAM
GPIO supply voltages	NVCC_ENET1 NVCC_EPDC1 NVCC_EPDC2 NVCC_I2C NVCC_LCD NVCC_SAI NVCC_SD1 NVCC_SD2 NVCC_SD3 NVCC_SPI NVCC_UART	1.65, 3.0	1.8, 3.3	1.95, 3.6	V	—
	NVCC_GPIO1	1.65 3.0	1.8, 3.3	1.95, 3.6	V	Power for GPIO1_DATA00 ~ GPIO1_DATA07
	NVCC_GPIO2	1.65 3.0	1.8, 3.3	1.95, 3.6	V	Power for GPIO1_DATA08 ~ GPIO1_DATA15 and JTAG port
Voltage rails supplied from internal LDO	PCIE_VPH PCIE_VPH_RX PCIE_VPH_TX VDDA_MIPI_1P8	1.71	1.8	1.89	V	Supplied from VDDA_PHY_1P8
	PCIE_VP PCIE_VP_RX PCIE_VP_TX VDD_MIPI_1P0	0.95	1.0	1.050	V	Supplied from VDDD_CAP_1P0
	VDD_USB_H_1P2	1.150	1.2	1.250	V	Supplied from VDD_1P2_CAP
Temperature sensor accuracy	T_{delta}	—	±3	—	°C	Typical accuracy over the range –40°C to 125°C
A/D converter	VDDA_ADC1_1P8	1.71	1.8	1.89	V	—
	VDDA_ADC2_1P8	1.71	1.8	1.89	V	—
Fuse power	FUSE_FSOURCE	1.710	1.8	1.890	V	Power supply for internal use
Junction temperature, industrial	T_J	-20	—	105	°C	See Table 1 for complete list of junction temperature capabilities.

[1] Applying the maximum voltage results in maximum power consumption and heat generation. A voltage set point = (Vmin + the supply tolerance) is recommended. This results in an optimized power/speed ratio. Operating a voltage of 1.2V and above will reduce the overall lifetime of the part. For details, see *i.MX 7Dual/Solo Product Lifetime Usage* (AN5334).

Table 10 shows on-chip LDO regulators that can supply on-chip loads.

Table 10. On-chip LDOs[1] and their on-chip loads

Voltage Source	Load	Comment
VDDD_1P0_CAP	VDD_MIPI_1P0	Connect directly (short) via board level
	PCIE_VP	
	PCIE_VP_RX	
	PCIE_VP_TX	
VDD_1P2_CAP	VDD_USB_H_1P2	Connect directly (short) via board level
VDDA_PHY_1P8	VDDA_MIPI_1P8	Connect directly (short) via board level
	PCIE_VPH	
	PCIE_VPH_RX	
	PCIE_VPH_TX	

1 On-chip LDOs are designed to supply i.MX 7Dual loads and must not be used to supply external loads.

4.1.4 External clock sources

Each i.MX 7Dual processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal resistor-capacitor (RC) oscillator, which can be used instead of the RTC_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

Table 11. External input clock frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]	—	kHz
XTALI Oscillator[2,4]	f_{xtal}		24		MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. See *Hardware Development Guide for i.MX7Dual and 7Solo Applications Processors.*

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal appropriately coupled to the internal oscillator amplifier.