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i.MX53 Quick Start Board

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1. Introduction

This document is the Hardware Reference Manual for the i.MX53 Quick Start board based on the Freescale Semiconductor i.MX53 Applications Processor. This board is fully supported by Freescale Semiconductor. This Manual includes system setup and debugging, and provides detailed information on the overall design and usage of the i.MX53 Quick Start board from a Hardware Systems perspective.

1.1. i.MX53-QUICK START Board Overview

The Quick Start Board is an i.MX535 platform designed to showcase many of the most commonly used features of the i.MX535 Applications Processor in a small, low cost package. The MCIMX53-START is an entry level development board and a near perfect subset of its larger sister board, the MCIMX53SMD, which is available as a full, near-form factor tablet. Developers can start working with code on the Quick Start board, and then port it over to the SMD Tablet if additional features are desired. This gives the developer the option of becoming familiar with the i.MX535 Applications Processor before investing a large amount of resources in more specific designs. Features of the i.MX53 Quick Start board are:

Processor:	Freescale Applications Processor	MCIMX535DVV1B
DRAM Memory:	Micron 8Gb DDR3 SDRAM	MT41J128M16HA-187E:D
PMIC:	Dialog Semiconductor	DA9053
Mass Storage:	5 in 1 SD/MMC/SDIO Card Connector microSD Card Connector 7-pin SATA Data Connector	
Video Output:	15-Pin D-Sub VGA Connector 30-Pin LVDS Connector	
Ethernet:	RJ-45 Connector for 10/100 Base-T	
USB:	Dedicated HS USB 2.0 Standard-A Host Connector Shared HS USB 2.0 Standard - Host and Micro-B Device Connectors	
Audio Connectors:	3.5mm Stereo Head Phone output 3.5mm Mono-Microphone input and Mono Head Phone (right channel) output	
Power Connectors:	5V mm Barrel Connector	
Debug Connectors:	9-Pin D-Sub Debug UART Connector 20-Pin Standard ARM JTAG Connector	
Expansion Header:	120-Pin Header (Populated) to Support 1 of the following: Optional HDMI Output Daughter Card (orderable) Optional WVGA and WQVGA LCD Display Daughter Cards (orderable) Camera Daughter Card (custom) SDIO Based WiFi Daughter card (custom)	

User Interface Buttons:	Power, Reset, 2 User-Defined Buttons
Indicators:	8 Status LEDs – External Power, PMIC ON, Fault Condition, and more
Li-ION Battery Connector:	3-Pin Header (unpopulated) for Li-ION Battery for Low Power Operation
Coin Cell:	Connection point for 2-Pin Coin Cell (unpopulated) for RTC Operation
PCB:	3.0 inch x 3.0 inch (76.2 mm x 76.2 mm), 10 - layer board

1.2. i.MX53-QUICK START Board Kit Contents

The i.MX53-Quick Start Board comes with the following items:

- i.MX53-QUICK START Board
- microSD Card preloaded with Ubuntu Demonstration Software
- USB Cable (Standard-A to Micro-B connectors)
- 5V/2.0A Power Supply
- Quick Start Guide
- Documentation DVD

1.3. i.MX53 Quick Start Board Revision History

- Rev A – Proof of Concept
- Rev B – Prototype (Internal Freescale Development)
- Rev C – Production (Silicon: i.MX53 Rev 2.0, DA9053 Rev AA)

The board version will be printed on a label, usually attached to the top of the SD Card Connector (J5). The board version will be the letter designation following the schematic revision:

SCH-26565 REV C

2. List of Acronyms

The following acronyms will be used throughout this document.

AC97	- Audio Codec '97
CMC	- Common Mode Choke
CODEC	- Compression/Decompression
DDR	- Double Data Rate
DNP	- Do Not Populate
HDMI	- High Definition Multimedia Interface
I2C	- Inter-Integrated Circuit
I2S	- Integrated Interchip Sound
IC	- Integrated Circuit
IDE	- Integrated Debug Environment
LAN	- Local Area Network
LCB	- i.MX53 Smart-Start
LCD	-Liquid Crystal Display
LPDDR2	- Low Power DDR2
MMC	- Multi Media Card
PMIC	- Power Management Companion IC
RMII	- Reduced Media Independent Interface
RTC	- Real-Time Clock
SDRAM	- Synchronous Dynamic Random Access Memory
SD	- Secure Digital
SPI	- Serial Peripheral Interface
SSI	- Synchronous Serial Interface
ULPI	- UTMI Low Pin Interface
USB	- Universal Serial Bus
UTMI	- Universal Transceiver Macrocell Interface
WDOG	- Watch Dog
WLAN	- Wireless LAN

3. Specifications

3.1. i.MX535 Processor

The i.MX535 Applications Processor (AP) is based on ARM Cortex-A8™ Platform, which has the following features:

- MMU, L1 Instruction and L1 Data Cache
- Unified L2 cache
- Target frequency of the core (including Neon, VFPv3 and L1 Cache): 1.0 GHz
- Neon coprocessor (SIMD Media Processing Architecture) and Vector Floating Point (VFP-Lite) coprocessor supporting VFPv3
- TrustZone

The memory system consists of the following components:

- Level 1 Cache:
 - Instruction (32 Kbyte)
 - Data (32 Kbyte)
- Level 2 Cache:
 - Unified instruction and data (256 Kbyte)
- Level2 (internal) memory:
 - Boot ROM, including HAB (64 Kbyte)
 - Internal multimedia/shared, fast access RAM (128 Kbyte)
 - Secure/non-secure RAM (16 Kbyte)
- External memory interfaces:
 - 16/32-bit DDR2-800, LV-DDR2-800 or DDR3-800 up to 2 Gbyte
 - 32 bit LPDDR2
 - 8/16-bit NAND SLC/MLC Flash, up to 66 MHz, 4/8/14/16-bit ECC
 - 16-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces (data with NFC pins). I/O muxing logic selects WEIMv2 port, as primary muxing at system boot.
 - 16-bit SRAM, cellular RAM
 - Samsung One NAND™ and managed NAND including eMMC up to rev 4.4 (in muxed I/O mode)

The i.MX53 system is built around the following system on chip interfaces:

- 64-bit AMBA AXI v1.0 bus – used by ARM platform, multimedia accelerators (such as VPU, IPU, GPU3D, GPU2D) and the external memory controller (EXTMC) operating at 200 MHz.
- 32-bit AMBA AHB 2.0 bus – used by the rest of the bus master peripherals operating at 133 MHz.
- 32-bit IP bus – peripheral bus used for control (and slow data traffic) of the most system peripheral devices operating at 66 MHz.

The i.MX53 makes use of dedicated hardware accelerators to achieve state-of-the-art multimedia performance. The use of hardware accelerators provides both high performance and low power consumption while freeing up the CPU core for other tasks.

The i.MX53 incorporates the following hardware accelerator:

- VPU, version 3 – video processing unit
- GPU3D – 3D graphics processing unit, OpenGL ES 2.0, version 3, 33 Htri/s, 200 Mpix/s, and 800 Mpix/s z-plane performance, 256 Kbyte RAM memory.
- GPU2D – 2D graphics accelerator, OpenVG 1.1, version 1, 200 Mpix/s performance.
- IPU, version 3M – image processing unit
- ASRC – asynchronous sample rate converter

The i.MX53 includes the following interfaces to external devices:

NOTE

Not all the interfaces are available simultaneously depending on I/O multiplexer configuration.

- Hard disk drives:
 - PATA, up to U-DMA mode 5, 100 MByte/s
 - SATA II, 1.5 Gbps
- Displays:
 - Five interfaces available. Total rate of all interfaces is up to 180 Mpixels/s, 24 bpp. Up to two interfaces may be active as once.
 - Two parallel 24-bit display ports. The primary port is up to 165 Mpix/s (for example, UXGA @ 60 Hz).
 - LVDS serial ports: one dual channel port up to 165 Mpix/s or two independent single channel ports up to 85 MP/s (for example, WXGA @ 60 Hz) each.
 - TV-out/VGA port up to 150 Mpix/s (for example, 1080p60).
- Camera sensors:
 - Two parallel 20-bit camera ports. Primary up to 180-MHz peak clock frequency, secondary up to 120-MHz peak clock frequency.
- Expansion cards:
 - Four SD/MMC card ports: three supporting 416 Mbps (8-bit i/f) and one enhanced port supporting 832 Mbps (8-bit, eMMC 4.4)
- USB
 - High-speed (HS) USB 2.0 OTG (up to 480 Mbps), with integrated HS USB PHY
 - Three USB 2.0 (480 Mbps) hosts:
 - High-speed host with integrated on-chip high speed PHY
 - Two high-speed hosts for external HS/FS transceivers through ULPI/serial, support IC-USB

- Miscellaneous interfaces:
 - One-wire (OWIRE) port
 - Three I2S/SSI/AC97 ports, supporting up to 1.4 Mbps, each connected to audio multiplexer (AUDMUX) providing four external ports.
 - Five UART RS232 ports, up to 4.0 Mbps each. One supports 8-wire, the other four support 4-wire.
 - Two high speed enhanced CSPI (ECSPI) ports plus one CSPI port
 - Three I2C ports, supporting 400 kbps.
 - Fast Ethernet controller, IEEE1588 V1 compliant, 10/100 Mbps
 - Two controller area network (FlexCAN) interfaces, 1 Mbps each
 - Sony Philips Digital Interface (SPDIF), Rx and Tx
 - Enhanced serial audio interface (ESAI), up to 1.4 Mbps each channel
 - Key pad port (KPP)
 - Two pulse-width modulators (PWM)
 - GPIO with interrupt capabilities
 - Secure JTAG controller (SJC)

The system supports efficient and smart power control and clocking:

- Supporting DVFS (Dynamic Voltage and Frequency Scaling) and DPTC (Dynamic Process and Temperature Compensation) techniques for low power modes.
- Power gating SRPG (State Retention Power Gating) for ARM core and Neon
- Support for various levels of system power modes.
- Flexible clock gating control scheme
- On-chip temperature monitor
- On-chip oscillator amplifier supporting 32.768 kHz external crystal
- On-chip LDO voltage regulators for PLLs

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on)
- Secure JTAG controller (SJC) – Protecting JTAC from debug port attacks by regulating or blocking the access to the system debug features.
- Secure real-time clock (SRTC) – Tamper resistant RTC with dedicated power domain and mechanism to detect voltage and clock glitches.
- Real-time integrity checker, version 3 (RTICv3) – RTIC type 1, enhanced with SHA-256 engine
- SAHARAv4 Lite – Cryptographic accelerator that includes true random number generator (TRNG)
- Security controller, version 2 (SCCv2) – Improved SCC with AES engine, secure/nonsecure RAM and support for multiple keys as well as TZ/non-TZ separation.
- Central Security Unit (CSU) – Enhancement for the IIM (IC Identification Module). CSU is configured during boot and by e-fuses and determines the security level operation mode as well as the TrustZone (TZ) policy.
- Advanced High Assurance BOOT (A-HAB) – HAB with the next embedded enhancements: SHA-256, 2046-bit RSA key, version control mechanism, warm boot, CSU and TZ initialization.

3.2. DDR3 DRAM Memory

The i.MX53-Quick Start board uses four 2-Gigabit DDR3 SDRAM ICs manufactured by Micron for a total onboard RAM memory of 1 GigaByte. The SDRAM data width for each IC is 16-bits. The chips are arranged in pairs that are controlled by each of the two chip select pins to form 32-bit words for the i.MX53 CPU. On Die Termination (ODT) functionality has been implemented on the board, as well as the ability to separate out the I/O Voltage Supply from the main SDRAM Voltage Supply if desired.

3.3. Dialog DA9053 PMIC

The DA9053 device is a small (7 x 7 mm, 0.5mm pitch) 169 ball VFBGA that provides nearly all power supply functions for the Quick Start board. The following is a feature list of the major functionality provided by the DA9053 PMIC for the Quick Start board:

- Power Supply resources:
 - 12 Low Drop Out (LDO) regulators
 - 1 for internal PMIC purposes only (LDOCORE)
 - 1 for charging optional back up coin cell
 - 10 for platform needs
 - 4 DC/DC Buck Converters (3 with DVS)
 - 1 for the ARM Core supply (VBUCKCORE)
 - 1 for the Peripheral Core supply (VBUCKPRO)
 - 1 for the external SDRAM memory (VBUCKMEM)
 - 1 for the internal cache memory (VBUCKPERI)
 - 1 White LED driver and boost converter
- Li-ION battery Charger
- Resistive touch screen interface
- Expansion Port Card ID detect
- Wall voltage supply over-voltage protection
- 1 HS-I2C interface
- External LDO regulator enable

3.4. MicroSD Card Slot (J4)

The microSD Card slot is used as the primary means to boot the Quick Start board. The power source for the microSD Card slot is VLDO3_3V3. The microSD Card slot is not normally configured with a card detect feature. The MicroSD Card slot can be configured to boot from a MMCmicro card with an alternate boot option setting (see section on Boot Options).

3.5. SD Card Slot (J5)

The SD Card slot is a 5-in-1 SD/MMC connector that acts as a secondary external memory media slot. The power source for the SD Card Slot is the auxiliary LDO regulator (DCDC_3V2). The SD Card slot can be configured as the boot source with an alternate boot option setting, as well as being configured for either SD or MMC card operation (see section on Boot Options). The SD Card Slot supports full 8-bit parallel data transfers and can support SDIO cards (WiFi, BT, etc) designed to fit in a standard SD card slot. The Quick Start board has specifically been tested with an Atheros SD-25 WiFi card.

3.6. SATA 7-pin Data Connector (J7)

The SATA connector provides the means to connect an external SATA memory device to the Quick Start board. Commonly, this would be an External hard drive or a DVD/CD reader. Power for the SATA device needs to be supplied externally by the user via a 12-pin power connector. It is possible to boot from a SATA drive by making OTP fuse changes. Once the fuse changes are made, they cannot be reversed.

3.7. VGA Video Output (J8)

A standard VGA signal is output directly from the i.MX53 Processor with minimum external components required. Power for the TVE module of the i.MX535 Processor is supplied by VLDO7 of the PMIC and is set to 2.75V. If VGA output is not desired, it is possible to program the PMIC to turn off VLDO7 to conserve power. The VGA output supports a variety of video formats up to 150 Mega-Pixels per second. Level shifters are required on the Horizontal and Vertical Synchronization signals as well as the VGA I2C communications signals in order to meet VGA specifications.

3.8. LVDS Video Output (J9)

The LVDS module of the i.MX53 Processor is connected to a 30-pin LVDS connector. While the i.MX53 Processor is capable of outputting to two separate LVDS displays, only one connector is pinned out on the Quick Start board. The pin outs on the LVDS connector match the optional cable and 10" HannStar LVDS display that can be purchased optionally from Freescale. The single LVDS connector will support video formats up to 165 Mega-Pixels per second. The power source for the LVDS module is a switchable output of the VBUCKPERI DCDC converter. This rail is shared with the SATA module and the USB module. If these modules are not being used, the PMIC can be programmed to turn off power to these three modules without affecting other 2.5V supplies to the remainder of the i.MX53 Applications Processor.

3.9. Ethernet (J2B)

The i.MX53 Processor Fast Ethernet Module outputs RMII formatted signals to an external Ethernet PHY. The processor is capable of 10/100 Base-T speeds. The Quick Start board uses the SMSC LAN8720A Ethernet Transceiver in a QFN-24 package. 3.2V power is supplied to the Ethernet IC from the external LDO regulator. The output of the Ethernet PHY is connected to an RJ45 jack with integrated magnetic.

3.10. Dual USB Host Connector (J2A)

The USB module of the i.MX53 Processor provides two high speed USB PHYs that are connected to each of the USB-A Host Jacks on connector J2. One PHY provides Host-only functionality and is connected to the upper USB jack on the connector tower. The second PHY is USB 2.0 OTG capable and is connected to the lower USB jack on the connector tower. Both jacks receive 5V power directly from the 5V Wall Power Supply, via a FET that can be controlled by software, and a 1.1A Poly-fuse. The PMIC provides an over-voltage functionality to limit voltage applied to the USB jack in the event that a DC Power Supply other than the original supply provided is used. Also, there is no current regulating device to limit current supplied to each jack, other than the Poly-fuse.

NOTE

The lower USB Host Jack is cross connected with the Micro-B USB Device connector. This was done as a convenience to the user as cables with micro-A plugs are still uncommon at the time the board was designed. The USB OTG PHY will switch to 'device' mode if a USB Host is attached to the micro-B connector with a cable. This design is not recommended for release to the general electronics consumer population. This board has not been tested for USB compliance.

3.11. Micro-B USB Device Connector (J3)

The micro-B USB connector is connected to the USB OTG PHY on the i.MX53 Processor, and is also connected to the Lower USB Host Jack on the connector tower. The connector's external USB 5V power pin is connected to the USB_OTG_ID pin, which is normally pulled to ground via a 3.3K Ohm resistor. When a powered USB Host device is attached to the micro-B USB connector, the USB_OTG_ID pin is pulled high and sends a signal to the USB OTG PHY to operate in device mode. The connector's external USB 5V power pin is not connected to the PMIC, or any other power rails on the Quick Start board. Therefore, it is not possible to supply power to the Quick Start board via the USB connections.

3.12. Audio Input/Output (J6/J18)

Analog audio input and output are provided by Freescale's Low Power Stereo Codec, SGTL5000. The audio codec is connected to the i.MX53 Applications Processor via 4-wire I2S communications, utilizing the AUDMUX5 port of the processor. The audio codec's Headphone Amp provides up to 58 mW output to 16-Ohm headphones at a typical SNR of 98 dB and THD+N of -86 dB. Typical power consumption is 11.6 mW. In addition, the audio codec can perform several enhancements to the output including virtual surround, added bass and three different types of equalization. The Microphone Input module of the Stereo Codec is also used, with the microphone input connected to the tip pin of the Microphone Jack (J6). Microphone Bias voltage is applied on the Quick Start board and not as a separate connection to the Microphone Jack. If the user desires to use a combined microphone, mono headphone device, the ferrite bead on L25 can be moved to the L22 pads, redirecting the right channel output to the Microphone Jack. A 2.5mm to 3.5mm adapter may be necessary to convert the microphone, mono headphone device to fit the Microphone Jack. On both the Headphone Jack and Microphone jack, a fourth pin is used to detect the insertion of a plug into either jack. When a standard 3-pin device is inserted into the 4-pin jack, the detect line is grounded, indicating to the i.MX53 Processor that the plug has been inserted.

3.13. 5V Power Connector (J1)

A 2.0mm x 6.5mm barrel connector is used which should fit standard DC Plugs with an inner dimension of 2.1mm and an outer dimension of 5.5mm. If an alternate power supply is used (not the original, supplied power supply), it should supply no more than 5.25V / 3A output. If the PMIC senses too high voltage at the connector input, it will turn off isolation FET Q1 to protect the Quick Start board. In between the Power Connector and the isolation FET is a single blow, fast acting fuse to protect the Quick Start board from an over current situation fault. If a Wall Power Supply is properly connected to the Quick Start board, and the green 5V power LED indicator is not lit, it could mean that either the fuse has been blown, or that the voltage output of the power supply is too high.

3.14. Debug UART Connector (J16)

UART1 of the i.MX53 Processor is connected to an RS-232 output to be used as a debug output for the developer. The Transmit (TX) and Receive (RX) signals are sent through two 1.8V to 3.2V level shifters to convert the logic signal voltages to the correct values for the Sipex SP3232 RS-232 transceiver. The CTS and RTS signals are not used on the Quick Start board. The RS-232 transceiver receives its power from the external 3.2V LDO Regulator. If the output of the regulator is turned off for power savings measures, debug output will be lost.

If the designer wishes to use the port as an Applications UART Port, changes can be made in software to reconfigure the port. A male-to-male gender changer can be used to properly convert the port.

To access the debug data output during development, connect the Debug UART Connector to a suitable host computer and open a terminal emulation program (ie, Teraterm or HyperTerminal). Proper settings for the terminal program are:

- BAUD RATE: 115,200
- DATA: 8 bit
- PARITY: None
- STOP BIT: 1-bit
- FLOW CONTROL: None

3.15. JTAG Connector (J15)

A standard 20-pin ARM JTAG connector is provided on the Quick Start board. Logic signals to the JTAG connector are 1.8V signals. A 1.8V reference signal is provided to pin 1 of the connector so that the attached JTAG tool can automatically configure the logic signals for the right voltage. If the JTAG tool does not have an automatic logic voltage sense, make sure that the tool is configured for 1.8V logic.

JTAG tools that have been specifically tested with the Quick Start board are:

- JTAG Commander (Macraigor)
- DS-5 and RealView (ARM Ltd.)
- Trace32 (Lauterbach)
- J-Link (Segger/Codesourcery)
- J-Link (IAR)

3.16. Expansion Header (J13)

A 120-pin Expansion Port Header is provided on the Quick Start board for use with many optionally expansion boards available from Freescale, or for custom designed boards made by the developer. At the time of initial production, the following expansion boards are available from Freescale:

- MCIMXHDMICARD HDMI signal output daughter card
- MCIMX28LCD 4.3" WVGA Touch Panel LCD Display

The Expansion Port makes the following features of the i.MX53 Processor available to be used on a custom built expansion card:

- Two Serial Peripheral Interfaces (SPI) CSPI, eCSDPI2
- Two I2S/SSI/AC97 Ports AUDMUX4, AUDMUX5
- Two Inter-Integrated Circuits (I2C) I2C1, I2C2
- 2 UARTs UART4, UART5
- SPDIF Audio
- USB ULPI Port USBH2
- 24-bit Data and display control signals
- Resistive Touch Screen Interface
- Various Voltage rails

3.17. User Interface Buttons

There are four user interface buttons on the Quick Start board. Their functionality is as follows:

POWER: In the 'Power Off' state, momentarily pressing the POWER button will begin the PMIC power on cycle. The PMIC supplied voltage rails will come up in the proper sequence to power the i.MX53 Processor. When the processor is fully powered, the boot cycle will be initiated.

In the 'Power On' state, momentarily pressing the POWER button will send a signal to a GPIO port for user defined action, but will not initiate a hardware shutdown.

In the 'Power On' state, holding the power button down for greater than 5 seconds will result in the PMIC initiating a shutdown to the 'Standby' power condition. This will also be the result from the 'Power Off' state as the PMIC will transition into the 'Power On' state and will still see the POWER button as held down.

RESET: Pressing the RESET button in the 'Power On' state will force the i.MX53 Applications Processor to immediately turn off, and reinitiate a boot cycle from the Processor Power Off state. The RESET button has no effect on the PMIC or the voltage rails.

Pressing the RESET button when the Quick Start board is powered off will have no effect.

USERDEF1: These two buttons are user defined buttons attached to PATA_DATA14 (P6) for
USERDEF2: USERDEF1 and PATA_DATA15 (P5) for USERDEF2. The two GPIO pins are normally pulled high by an internal resistor. The two buttons function by connecting the pins to ground, thus inserting a low signal. The developer is left to determine the actions of these two pins in code. Sample codes do not assign functionality to either pin.

3.18. User Interface LED Indicators

There are eight LED status indicators located next to the microSD card connector. These LEDs have the following functions:

- 5V:** The 5V status LED (D1) is a Green LED connected directly to the 5V_MAIN power rail. This LED indicates that 5V wall power is being properly supplied to the Quick Start board. If this light is not lit, it would indicate one of three problems:
- 1) Fuse F1 has been blown and needs to be replaced.
 - 2) Voltage from the wall supply is greater than 5.5V and the over voltage protection feature is disabling power to the board.
 - 3) The DC Power supply is not plugged in or malfunctioning.
- PMIC:** The PMIC status LED (D9) is a Green LED gated by the PMIC SYS_UP signal from the PMIC. This LED indicates that the PMIC is in the fully on condition and supplying power to the processor and other voltage rails as directed by software.
- USER:** The User status LED (D16) is a Green LED gated by the PATA_DATA1 (L3) GPIO pin. The developer is left to determine the action of this pin in code. Sample codes do not assign functionality to the pin. The LED comes on by default when the processor starts up.
- FLT:** The FLT status LED (D14) is a Red LED gated by the NVDD_FAULT signal from the PMIC. The LED will turn on anytime the PMIC is not outputting the requested voltages or when the PMIC senses a fault condition and will begin to power down the voltage rails. This may aid in trouble shooting power problems if both the PMIC and FLT LEDs are on at the same time, it indicates that the PMIC is causing a shutdown based on a fault it has sensed.
- 3.3V:** The 3.3V status LED (D10) is a Blue LED gated by the External Regulator 3.2V power rail. This power rail can be turned off by software for power savings measures. This LED provides an easy visual recognition as to the status of this bus.

- SATA:** The SATA status LED (D11) is a Blue LED gated by the SATA_1V3 (VLDO5) power rail. This power rail can be turned off by software for power savings measures. This LED provides an easy visual recognition as to the status of this bus.
- VGA:** The VGA status LED (D12) is a Blue LED gated by the TVDAC_2V75 (VLDO7) power rail. This power rail can be turned off by software for power savings measures. This LED provides an easy visual recognition as to the status of this bus.
- LCD:** The LCD status LED (D13) is a Blue LED gated by the LCD_3V2 power rail. Normally the LCD_3V2 power rail receives power directly from the DCDC_3V2 power rail, but the LCD can also be configured to receive power from VIOHI_2V772 (VLDO4). In the alternate voltage supply configuration, this LED will provide visual recognition as to the status of the LCD bus.

3.19. Optional Li-ION Battery Connector (J14)

On the Quick Start board, there is a footprint (J14) available to solder a three pin wafer connector (Molex 0530470310 or equivalent). This connector will mate to Li-ION batteries commercially available as replacement batteries to commonly available MP3 players. The developer should make sure that the polarity of the battery matches the polarity of the connector as replacement batteries may vary from different manufacturers. When installed, a battery can be charged from the external 5V wall power source. A battery will not be charged when only a USB cable is connected to the Quick Start board. When powering a board from only a battery, the 5V power rail and the DCDC_3V2 power rail will not be powered. Therefore, the Ethernet subsystem and Audio subsystem will not be operational under normal board configurations. Depending on the battery capacity, it may be necessary to power down additional subsystem voltage rails to extend battery life to a usable amount.

The battery charging feature is an autonomous operation of the Dialog DA9053 PMIC that does not require software support. Battery charging may be prevented by software by making registry changes to the PMIC. The developer may need to verify in software that PMIC registry settings are proper for battery charging operations. The footprints for testing with a battery were included for skilled developers looking to experiment.

3.20. Optional Back-Up Coin Cell posts (JP1, JP2)

On the Quick Start board, there are two through-holes (JP1 and JP2) next to the power connector. These through-holes are positioned to hold a Lithium coin cell battery (Sanyo ML1220-VM1 or equivalent). For proper operation, the coin cell posts should be soldered direction to the Quick Start board, with the positive terminal connected to JP1 and the negative terminal connected to JP2. The DA9053 PMIC will charge the coin cell when 5V Wall Power is available. When 5V Wall Power is removed, the coin cell will provide power only to the RTC power rail (VLDO1) supplying power to the i.MX53 processor. The length of time a coin cell can power the RTC subsystem may vary.

3.21. PCB Shorting Traces

On the Quick Start PCB, there are 29 sets of standard footprints with a copper trace between them to short the two pads together. The PCB is produced with these pads unpopulated. These shorting traces are placed throughout the PCB at locations in line with major power rails and critical components. The purpose of these shorting traces is to allow the skilled developer to manually cut the trace between the pads to either:

- 1) Isolate power to major subsystems or components.
- 2) Install small value precision resistors to measure current consumption of major subsystems.
- 3) Or reconfigure power sources to subsystems or components using wires soldered to the pads.

To restore a shorting trace back to normal after the trace is cut, it is only necessary to solder a Zero Ohm resistor to the pads.

4. Quick Start Board Connectors and Expansion Port

The Quick Start board provides a number of connectors for a variety of inputs and outputs to and from the board. The following subsections describe these connections in detail.

4.1.Wall 5V Power Jack (J1)

The 5V/2A AC-to-DC power supply that comes with the Quick Start board is plugged into the Power Jack (J1) on the board as show in **Figure 1**. If the original power supply is lost, it is possible to use a substitute power supply for the Quick Start board. Voltage above 5.5V, and below 12V, will trigger the Over-Voltage protection circuitry on the board. It is not recommended to use a higher voltage since, in the event of a failure to the protection circuitry, damage to the board will result. A voltage supply above 12V will damage the PMIC part.

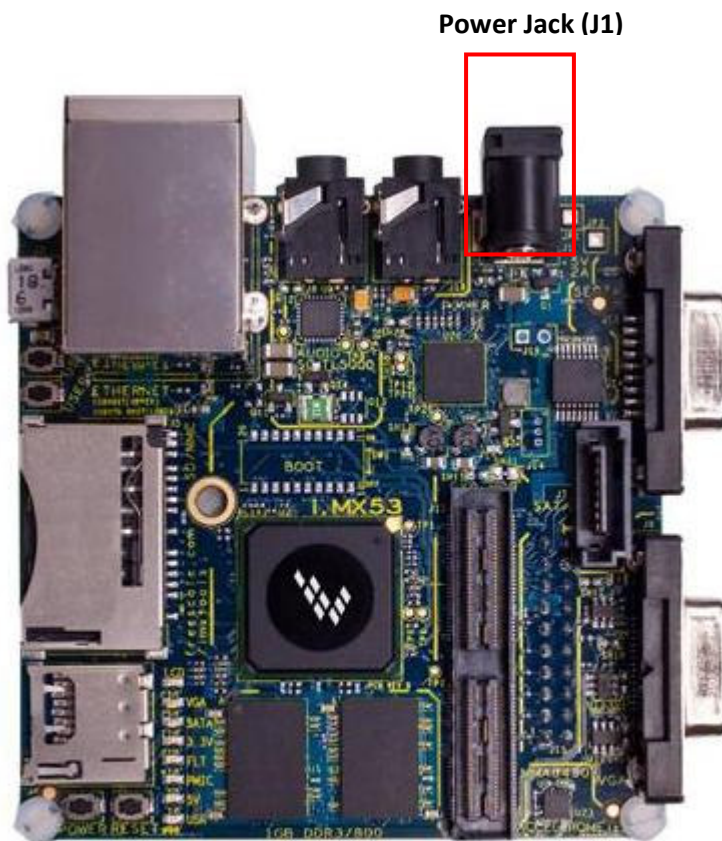


Figure 1. DC Power Jack

4.2. RJ45 Ethernet Connector (J2B)

A standard Cat-V Ethernet cable is attached to the Quick Start board at the Ethernet/Dual USB connector J2. The connector contains integrated magnetic which allows the Ethernet IC to auto configure the port for the correct connection to either a switch or directly to a host PC on a peer-to-peer network. It is not necessary to use a crossover cable when connecting directly to another computer. The Ethernet/Dual USB connector is shown in **Figure 2**.



Figure 2a. Ethernet Port

Ethernet/Dual USB
Connector (J2)

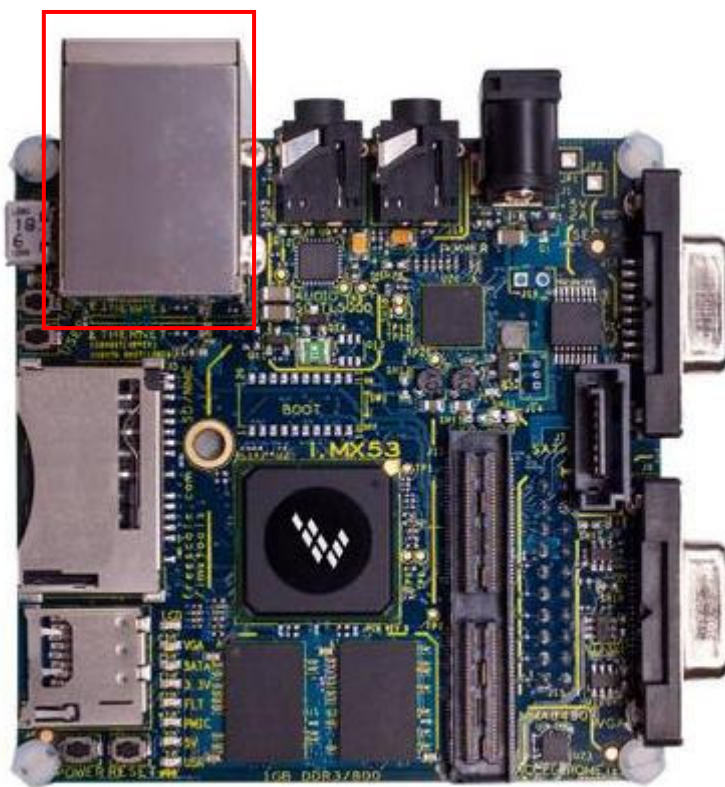


Figure 2. RJ45 Ethernet Connector