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Addendum to MC68HC908QB8, rev. 3

This addendum introduces a change to this data sheet.

Chapter 17 Development Support, Section 17.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE

Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors.

Changes to:

Chapter 17 Development Support, Section 17.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE

Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors. An improved security function denies monitor mode entry if five or more of the eight security bytes are $00 (zero bytes).

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MC68HC908QB8
MC68HC908QB4
MC68HC908QY8

Data Sheet

M68HC08
Microcontrollers

MC68HC908QB8
Rev. 3
04/2010

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MC68HC908QB8
MC68HC908QB4
MC68HC908QY8

Data Sheet

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http://freescale.com/

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
September, 2005	1	Initial full release	N/A
April, 2007	2	Chapter 3 Analog-to-Digital Converter (ADC10) Module — Renamed ADCSC register to ADSCR to be consistent with development tools.	37
		Figure 4-1. Auto Wakeup Interrupt Request Generation Logic — Changed BUSCLK4 to BUSCLK2 and removed reference to CGMXCLK	51
		4.3 Functional Description — Reworked for clarity	52
		4.6.4 Configuration Register 2 — Changed BUSCLK4 to BUSCLK2	55
		4.6.5 Configuration Register 1 — Changed BUSCLK4 to BUSCLK2, added bit description for SSREC, and removed SSREC from the note	56
		Chapter 5 Configuration Register (CONFIG) — Changed CGMXCLK to BUSCLKX4	57
		Chapter 13 Enhanced Serial Communications Interface (ESCI) Module — Changed SCIBDSRC to ESCIBDSRC, CGMXCLK to BUSCLKX4, and BUS_CLK to BUS CLOCK	109
		Table 13-5. ESCI LIN Control Bits — Corrected Functionality column	130
		13.9.3 Bit Time Measurement — Corrected first sentence of listing number 1	136
		Figure 17-18. Monitor Mode Entry Timing — Changed CGMXCLK to BUSCLKX4	206
April, 2010	3	Clarify internal oscillator trim register information.	29, 36, 96, 101

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Chapter 1
General Description

1.1 Introduction

The MC68HC908QB8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Device Variations

Device	FLASH/RAM Memory Size	ADC	16-Bit Timer Channels	ESCI	SPI	Pin Count
MC68HC908QB8	8K/256 bytes	10 channel, 10 bit	4	Yes	Yes	16 pins
MC68HC908QB4	4K/128 bytes	10 channel, 10 bit	4	Yes	Yes	16 pins
MC68HC908QY8	8K/256 bytes	4 channel, 10 bit	2	No	No	16 pins

1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- 5-V and 3-V operating voltages (V_{DD})
- 8-MHz internal bus operation at 5 V, 4-MHz at 3 V
- Trimmable internal oscillator
  - Software selectable 1 MHz, 2 MHz, or 3.2 MHz internal bus operation
  - 8-bit trim capability
  - ± 25% untrimmed
  - Trimmable to approximately 0.4%(1)
- Software selectable crystal oscillator range, 32–100 kHz, 1–8 MHz, and 8–32 MHz
- Software configurable input clock from either internal or external source
- Auto wakeup from STOP capability using dedicated internal 32-kHz RC or bus clock source
- On-chip in-application programmable FLASH memory
  - Internal program/erase voltage generation
  - Monitor ROM containing user callable program/erase routines
  - FLASH security(2)

1. See 18.11 Oscillator Characteristics for internal oscillator specifications
2. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

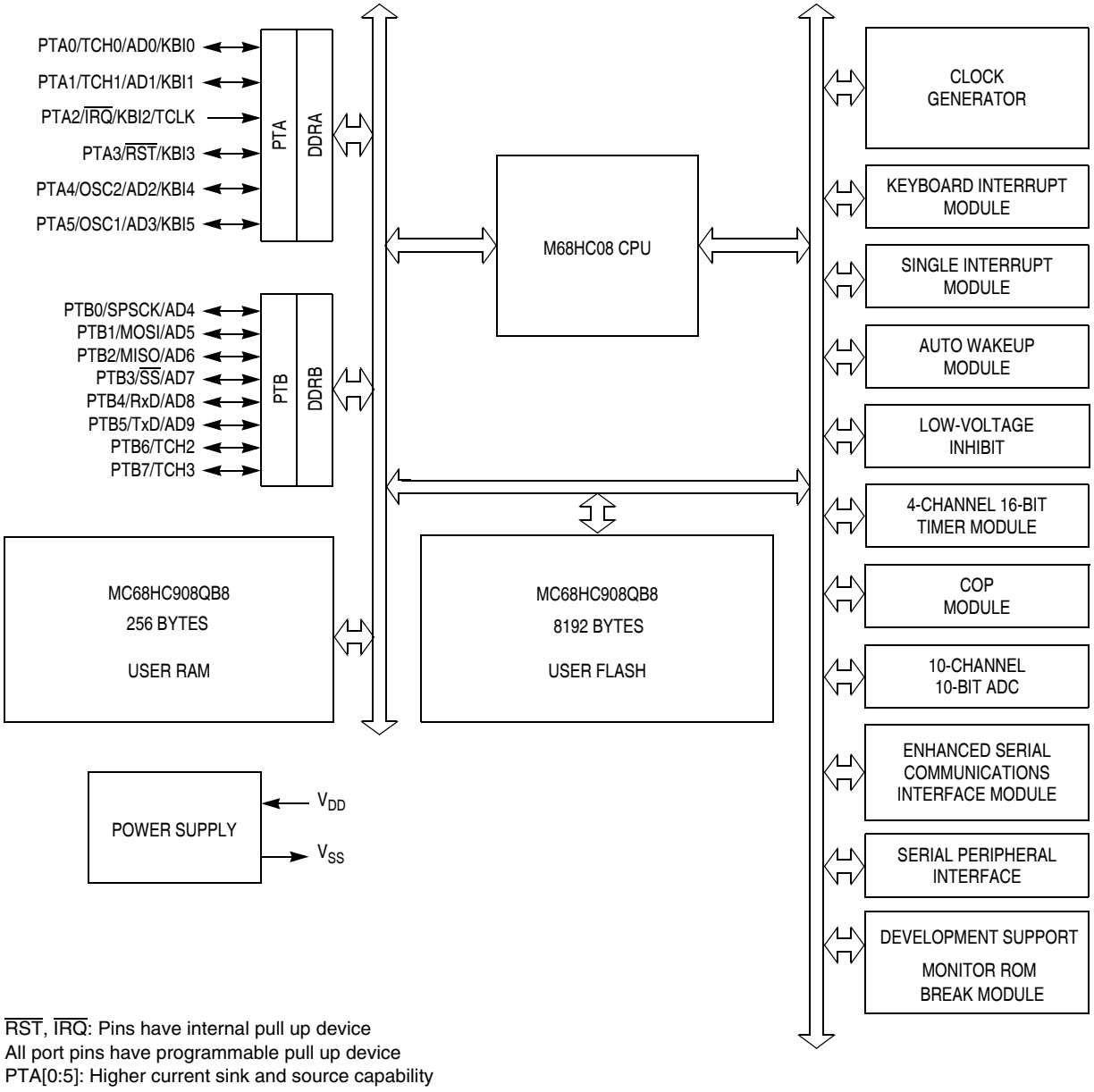
- On-chip random-access memory (RAM)
- Enhanced serial communications interface (ESCI) module
- Serial peripheral interface (SPI) module
- 4-channel, 16-bit timer interface (TIM) module
- 10-channel, 10-bit analog-to-digital converter (ADC) with internal bandgap reference channel (ADC10)
- Up to 13 bidirectional input/output (I/O) lines and one input only:
  - Six shared with KBI
  - Ten shared with ADC
  - Four shared with TIM
  - Two shared with ESCI
  - Four shared with SPI
  - One input only shared with IRQ
  - High current sink/source capability on all port pins
  - Selectable pullups on all ports, selectable on an individual bit basis
  - Three-state ability on all port pins
- 6-bit keyboard interrupt with wakeup feature (KBI)
  - Programmable for rising/falling or high/low level detect
- Low-voltage inhibit (LVI) module features:
  - Software selectable trip point
- System protection features:
  - Computer operating properly (COP) watchdog
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ}}$) shared with general-purpose input pin
- Master asynchronous reset pin with internal pullup ($\overline{\text{RST}}$) shared with general-purpose input/output (I/O) pin
- Memory mapped I/O registers
- Power saving stop and wait modes
- MC68HC908QB8, MC68HC908QB4 and MC68HC908QY8 are available in these packages:
  - 16-pin plastic dual in-line package (PDIP)
  - 16-pin small outline integrated circuit (SOIC) package
  - 16-pin thin shrink small outline packages (TSSOP)

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908QB8.



RST, IRQ: Pins have internal pull up device
All port pins have programmable pull up device
PTA[0:5]: Higher current sink and source capability

Figure 1-1. Block Diagram

1.4 Pin Assignments

The MC68HC908QB8, MC68HC908QB4, and MC68HC908QY8 are available in 16-pin packages. Figure 1-2 shows the pin assignment for these packages.

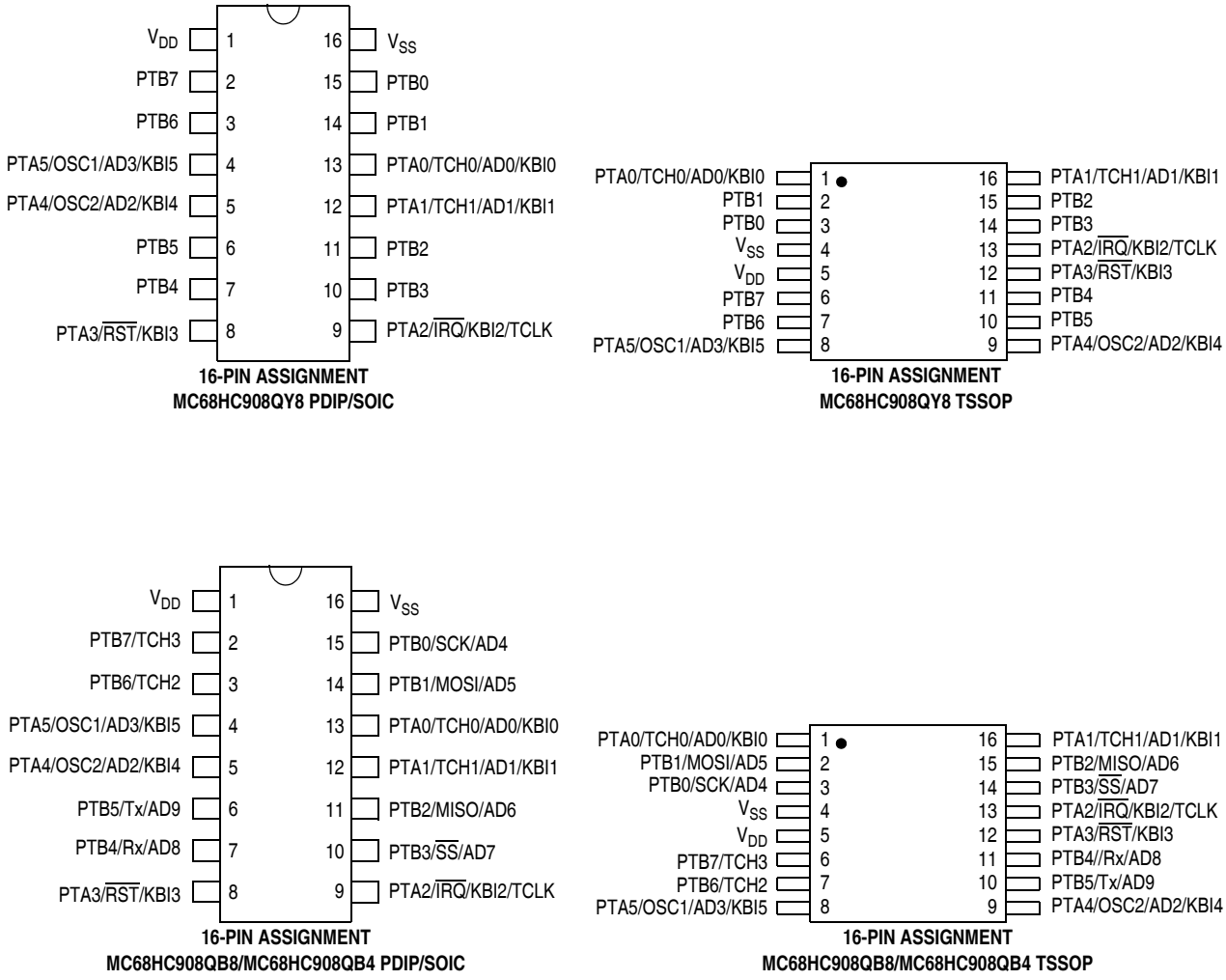


Figure 1-2. MCU Pin Assignments

1.5 Pin Functions

Table 1-2 provides a description of the pin functions.

Table 1-2. Pin Functions

Pin Name	Description	Input/Output
V_{DD}	Power supply	Power
V_{SS}	Power supply ground	Power
PTA0	PTA0 — General purpose I/O port	Input/Output
	TCH0 — Timer Channel 0 I/O	Input/Output
	AD0 — A/D channel 0 input	Input
	KBI0 — Keyboard interrupt input 0	Input
PTA1	PTA1 — General purpose I/O port	Input/Output
	TCH1 — Timer Channel 1 I/O	Input/Output
	AD1 — A/D channel 1 input	Input
	KBI1 — Keyboard interrupt input 1	Input
PTA2	PTA2 — General purpose input-only port	Input
	$\overline{IRQ}$ — External interrupt with programmable pullup and Schmitt trigger input	Input
	KBI2 — Keyboard interrupt input 2	Input
	TCLK — Timer clock input	Input
PTA3	PTA3 — General purpose I/O port	Input/Output
	$\overline{RST}$ — Reset input, active low with internal pullup and Schmitt trigger	Input
	KBI3 — Keyboard interrupt input 3	Input
PTA4	PTA4 — General purpose I/O port	Input/Output
	OSC2 —XTAL oscillator output (XTAL option only) RC or internal oscillator output (OSC2EN = 1 in PTAPUE register)	Output Output
	AD2 — A/D channel 2 input	Input
	KBI4 — Keyboard interrupt input 4	Input
PTA5	PTA5 — General purpose I/O port	Input/Output
	OSC1 — XTAL, RC, or external oscillator input	Input
	AD3 — A/D channel 3 input	Input
	KBI5 — Keyboard interrupt input 5	Input
PTB0	PTB0 — General-purpose I/O port	Input/Output
	SPSCK — SPI serial clock	Input/Output
	AD4 — A/D channel 4 input	Input
PTB1	PTB1 — General-purpose I/O port	Input/Output
	MOSI — SPI Master out Slave in	Input/Output
	AD5 — A/D channel 5 input	Input
PTB2	PTB2 — General-purpose I/O port	Input/Output
	MISO — SPI Master in Slave out	Input/Output
	AD6 — A/D channel 6 input	Input
PTB3	PTB3 — General-purpose I/O port	Input/Output
	$\overline{SS}$ — SPI slave select	Input
	AD7 — A/D channel 7 input	Input

— Continued on next page

Table 1-2. Pin Functions (Continued)

Pin Name	Description	Input/Output
PTB4	PTB4 — General-purpose I/O port	Input/Output
	RxD — ESCI receive data I/O	Input/Output
	AD8 — A/D channel 8 input	Input
PTB5	PTB5 — General-purpose I/O port	Input/Output
	TxD — ESCI transmit data I/O	Output
	AD9 — A/D channel 9 input	Input
PTB6	PTB6 — General-purpose I/O port	Input/Output
	TCH2 — Timer channel 2 I/O	Input/Output
PTB7	PTB7 — General-purpose I/O port	Input/Output
	TCH3 — Timer channel 3 I/O	Input/Output

1.6 Pin Function Priority

Table 1-3 is meant to resolve the priority if multiple functions are enabled on a single pin.

NOTE

Upon reset all pins come up as input ports regardless of the priority table.

Table 1-3. Function Priority in Shared Pins

Pin Name	Highest-to-Lowest Priority Sequence
PTA0[1]	AD0 → TCH0 → KBI0 → PTA0
PTA1[1]	AD1 → TCH1 → KBI1 → PTA1
PTA2	$\overline{\text{IRQ}}$ → TCLK → KBI2 → PTA2
PTA3	$\overline{\text{RST}}$ → KBI3 → PTA3
PTA4[1]	OSC2 → AD2 → KBI4 → PTA4
PTA5[1]	OSC1 → AD3 → KBI5 → PTA5
PTB0[1]	AD4 → SPSCK → PTB0
PTB1[1]	AD5 → MOSI → PTB1
PTB2[1]	AD6 → MISO → PTB2
PTB3[1]	AD7 → $\overline{\text{SS}}$ → PTB3
PTB4[1]	AD8 → RxD → PTB4
PTB5[1]	AD9 → TxD → PTB5
PTB6	TCH2 → PTB6
PTB7	TCH3 → PTB7

1. When a pin is to be used as an ADC pin, the I/O port function should be left as an input and all other shared modules should be disabled. The ADC does not override additional modules using the pin.

Chapter 2
Memory

2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in Figure 2-1.

2.2 Unimplemented Memory Locations

Executing code from an unimplemented location will cause an illegal address reset. In Figure 2-1, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In Figure 2-1, register locations are marked with the word Reserved or with the letter R.

2.4 Direct Page Registers

Figure 2-2 shows the memory mapped registers of the MC68HC908QB8. Registers with addresses between $0000 and $00FF are considered direct page registers and all instructions including those with direct page addressing modes can access them. Registers between $0100 and $FFFF require non-direct page addressing modes. See Chapter 7 Central Processor Unit (CPU) for more information on addressing modes.