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MC68HLC908QY4
MC68HLC908QT4
MC68HLC908QY2
MC68HLC908QT2
MC68HLC908QY1
MC68HLC908QT1

Data Sheet

M68HC08
Microcontrollers

MC68HLC908QY4/D
Rev. 3
07/2005

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MC68HLC908QY4
MC68HLC908QT4
MC68HLC908QY2
MC68HLC908QT2
MC68HLC908QY1
MC68HLC908QT1

Data Sheet

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
August, 2003	N/A	Initial release	N/A
October, 2003	1.0	Figure 2-2. Control, Status, and Data Registers Deleted unimplemented areas from $FFB0–$FFBD and $FFC2–$FFCF as they are actually available. Also corrected $FFBF designation from unimplemented to reserved.	26
		Figure 6-1. COP Block Diagram — Reworked for clarity	57
		6.3.2 STOP Instruction — Added subsection for STOP instruction	58
		13.4.2 Active Resets from Internal Sources — Reworked notes for clarity.	115
		15.3 Monitor Module (MON) — Clarified seventh bullet.	154
		16.5 DC Electrical Characteristics — Corrected notes 4 and 5.	169
		16.6 Control Timing — Updated values for $\overline{\text{RST}}$ input pulse width low and $\overline{\text{IRQ}}$ interrupt pulse width low	170
January, 2004	2.0	Figure 2-2. Control, Status, and Data Registers — Corrected reset state for the FLASH Block Protect Register at address location $FFBE and the Internal Oscillator Trim Value at $FFC0.	30
		Figure 2-5. FLASH Block Protect Register (FLBPR) — Restated reset state for clarity.	37
July, 2005	3.0	Reformatted to meet current documentation standards	Throughout
		Chapter 7 Central Processor Unit (CPU) — In 7.7 Instruction Set Summary: Reworked definitions for STOP instruction Added WAIT instruction	 70 71
		13.8.1 SIM Reset Status Register — Clarified SRSR flag setting.	117
		14.9.1 TIM Status and Control Register — Added information to TSTOP note.	127
		17.3 Package Dimensions — Updated package information.	163

List of Chapters

Table of Contents

Chapter 1
General Description

Chapter 2
Memory

Chapter 3
Analog-to-Digital Converter (ADC)

Chapter 4
Auto Wakeup Module (AWU)

Chapter 5
Configuration Register (CONFIG)

Chapter 6
Computer Operating Properly (COP)

Chapter 7
Central Processor Unit (CPU)

Chapter 8
External Interrupt (IRQ)

Chapter 9
Keyboard Interrupt Module (KBI)

Chapter 10
Low-Voltage Inhibit (LVI)

Chapter 11
Oscillator Module (OSC)

Chapter 12
Input/Output Ports (PORTS)

Chapter 13
System Integration Module (SIM)

Chapter 14
Timer Interface Module (TIM)

Chapter 15
Development Support

Chapter 16
Electrical Specifications

Chapter 17
Ordering Information and Mechanical Specifications

Chapter 1
General Description

1.1 Introduction

The MC68HLC908QY4 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is a Complex Instruction Set Computer (CISC) with a Von Neumann architecture. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

Table 1-1. Summary of Device Variations

Device	FLASH Memory Size	Analog-to-Digital Converter	Pin Count
MC68HLC908QT1	1536 bytes	—	8 pins
MC68HLC908QT2	1536 bytes	4 ch, 8 bit	8 pins
MC68HLC908QT4	4096 bytes	4 ch, 8 bit	8 pins
MC68HLC908QY1	1536 bytes	—	16 pins
MC68HLC908QY2	1536 bytes	4 ch, 8 bit	16 pins
MC68HLC908QY4	4096 bytes	4 ch, 8 bit	16 pins

1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- Operating voltage range of 2.2 V to 3.6 V
- 2-MHz internal bus operation
- Trimmable internal oscillator
  - 1.0 MHz internal bus operation
  - 8-bit trim capability allows 0.4% accuracy(1)
  - ± 25% untrimmed
- Auto wakeup from STOP capability
- Configuration (CONFIG) register for MCU configuration options, including:
  - Low-voltage inhibit (LVI) trip point
- In-system FLASH programming
- FLASH security(2)

1. The oscillator frequency is guaranteed to ±5% over temperature and voltage range after trimming.
2. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.

- On-chip in-application programmable FLASH memory (with internal program/erase voltage generation)
  - MC68HLC908QY4 and MC68HLC908QT4 — 4096 bytes
  - MC68HLC908QY2, MC68HLC908QY1, MC68HLC908QT2, and MC68HLC908QT1— 1536 bytes
- 128 bytes of on-chip random-access memory (RAM)
- 2-channel, 16-bit timer interface module (TIM)
- 4-channel, 8-bit analog-to-digital converter (ADC) on MC68HLC908QY2, MC68HLC908QY4, MC68HLC908QT2, and MC68HLC908QT4
- 5 or 13 bidirectional input/output (I/O) lines and one input only:
  - Six shared with keyboard interrupt function and ADC
  - Two shared with timer channels
  - One shared with external interrupt (IRQ)
  - Eight extra I/O lines on 16-pin package only
  - High current sink/source capability on all port pins
  - Selectable pullups on all ports, selectable on an individual bit basis
  - Three-state ability on all port pins
- 6-bit keyboard interrupt with wakeup feature (KBI)
- Low-voltage inhibit (LVI) module features:
  - Software selectable trip point in CONFIG register
- System protection features:
  - Computer operating properly (COP) watchdog
  - Low-voltage detection with optional reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ}}$) shared with general-purpose input pin
- Master asynchronous reset pin ($\overline{\text{RST}}$) shared with general-purpose input/output (I/O) pin
- Power-on reset
- Internal pullups on $\overline{\text{IRQ}}$ and $\overline{\text{RST}}$ to reduce external components
- Memory mapped I/O registers
- Power saving stop and wait modes
- MC68HLC908QY4, MC68HLC908QY2, and MC68HLC908QY1 are available in these packages:
  - 16-pin plastic dual in-line package (PDIP)
  - 16-pin small outline integrated circuit (SOIC) package
  - 16-pin thin shrink small outline package (TSSOP)
- MC68HLC908QT4, MC68HLC908QT2, and MC68HLC908QT1 are available in these packages:
  - 8-pin PDIP
  - 8-pin SOIC
  - 8-pin dual flat no lead (DFN) package

Features of the CPU08 include the following:

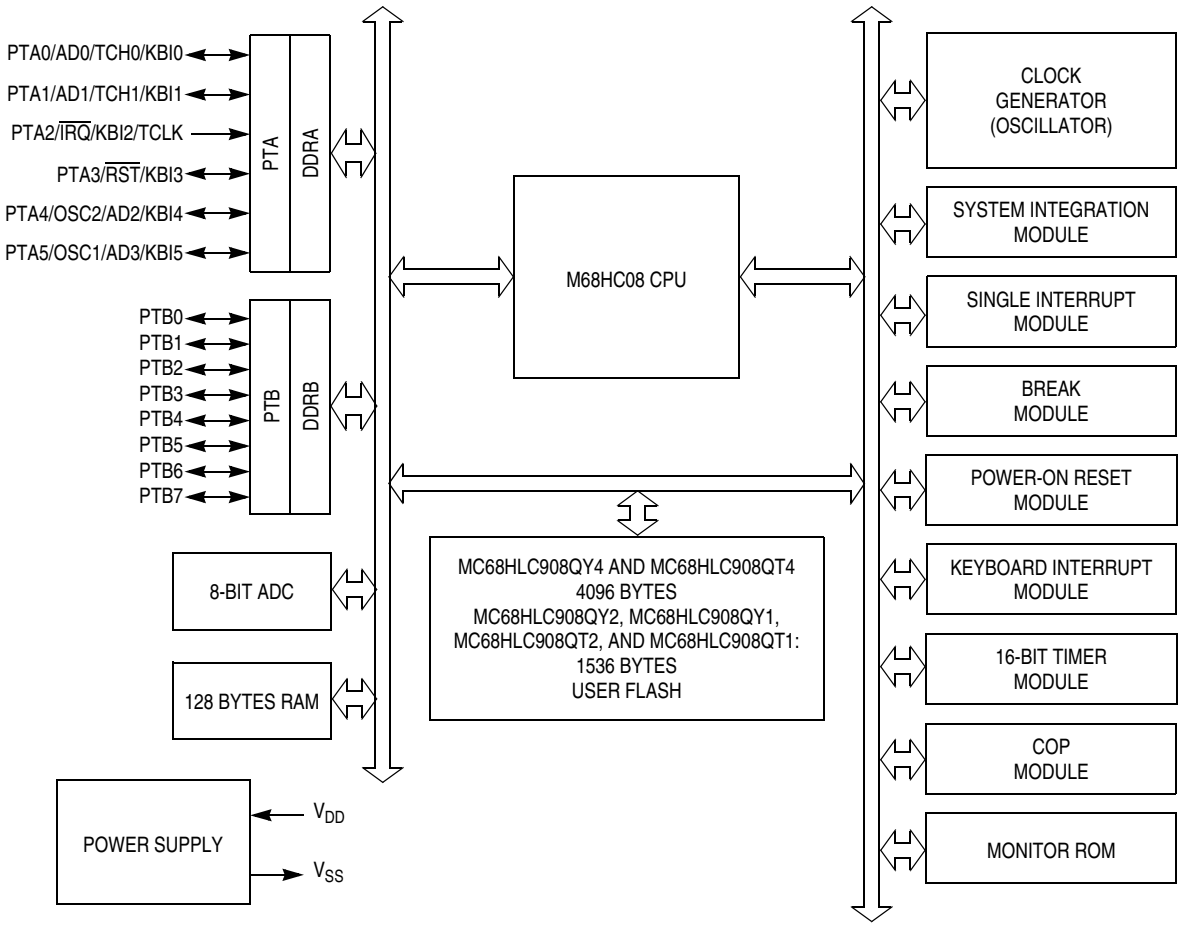
- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HLC908QY4.

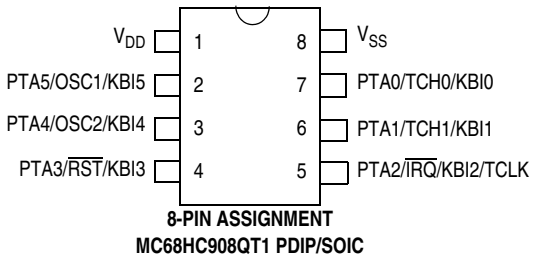
1.4 Pin Assignments

The MC68HLC908QT4, MC68HLC908QT2, and MC68HLC908QT1 are available in 8-pin packages and the MC68HLC908QY4, MC68HLC908QY2, and MC68HLC908QY1 in 16-pin packages. Figure 1-2 shows the pin assignment for these packages.

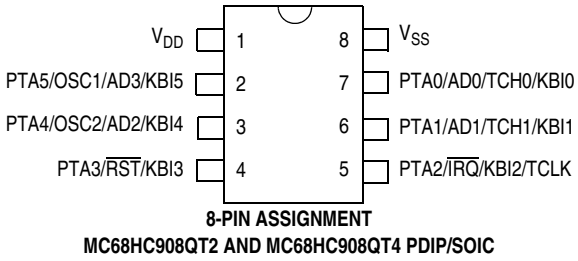


RST, IRQ: Pins have internal (about 30K Ohms) pull up
PTA[0:5]: High current sink and source capability
PTA[0:5]: Pins have programmable keyboard interrupt and pull up
PTB[0:7]: Not available on 8-pin devices – MC68HLC908QT1, MC68HLC908QT2, and MC68HLC908QT4 (see note in 12.1 Introduction)
ADC: Not available on the MC68HLC908QY1 and MC68HC9L08QT1

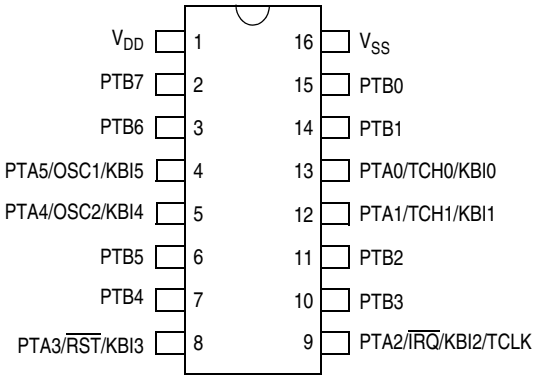
Figure 1-1. Block Diagram



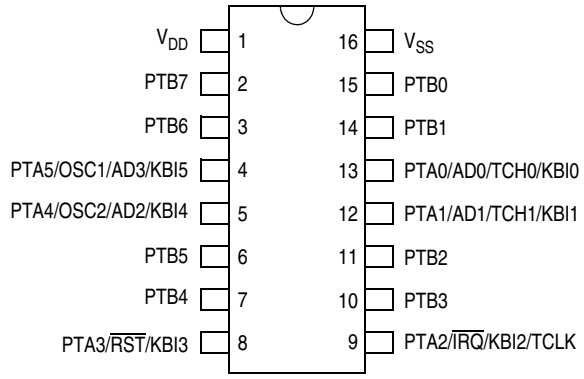
8-PIN ASSIGNMENT
MC68HC908QT1 PDIP/SOIC



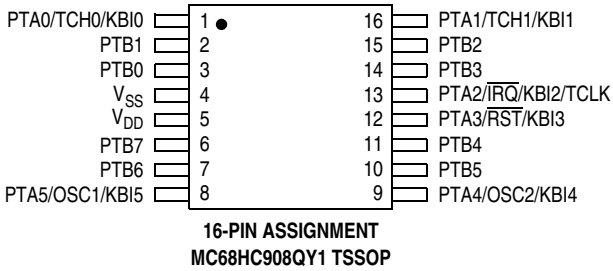
8-PIN ASSIGNMENT
MC68HC908QT2 AND MC68HC908QT4 PDIP/SOIC



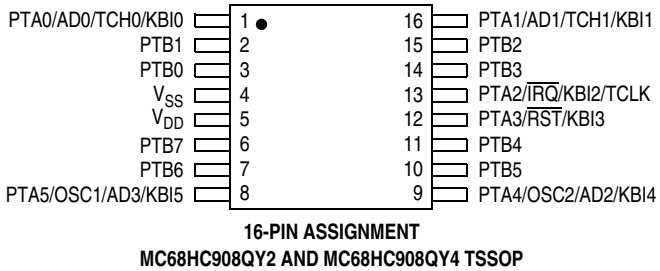
16-PIN ASSIGNMENT
MC68HC908QY1 PDIP/SOIC



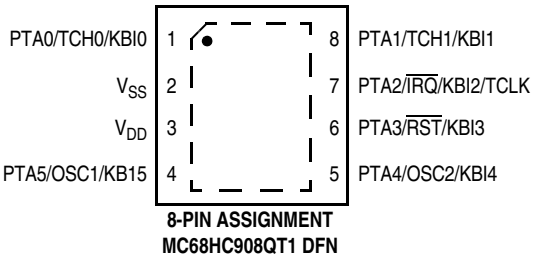
16-PIN ASSIGNMENT
MC68HC908QY2 AND MC68HC908QY4 PDIP/SOIC



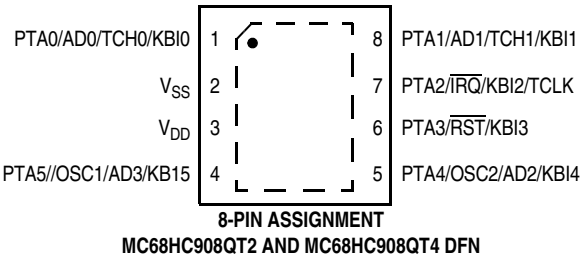
16-PIN ASSIGNMENT
MC68HC908QY1 TSSOP



16-PIN ASSIGNMENT
MC68HC908QY2 AND MC68HC908QY4 TSSOP



8-PIN ASSIGNMENT
MC68HC908QT1 DFN



8-PIN ASSIGNMENT
MC68HC908QT2 AND MC68HC908QT4 DFN

Figure 1-2. MCU Pin Assignments

1.5 Pin Functions

Table 1-2 provides a description of the pin functions.

Table 1-2. Pin Functions

Pin Name	Description	Input/Output
V_{DD}	Power supply	Power
V_{SS}	Power supply ground	Power
PTA0	PTA0 — General purpose I/O port	Input/Output
	AD0 — A/D channel 0 input	Input
	TCH0 — Timer Channel 0 I/O	Input/Output
	KBI0 — Keyboard interrupt input 0	Input
PTA1	PTA1 — General purpose I/O port	Input/Output
	AD1 — A/D channel 1 input	Input
	TCH1 — Timer Channel 1 I/O	Input/Output
	KBI1 — Keyboard interrupt input 1	Input
PTA2	PTA2 — General purpose input-only port	Input
	$\overline{IRQ}$ — External interrupt with programmable pullup and Schmitt trigger input	Input
	KBI2 — Keyboard interrupt input 2	Input
	TCLK — Timer clock input	Input
PTA3	PTA3 — General purpose I/O port	Input/Output
	$\overline{RST}$ — Reset input, active low with internal pullup and Schmitt trigger	Input
	KBI3 — Keyboard interrupt input 3	Input
PTA4	PTA4 — General purpose I/O port	Input/Output
	OSC2 —XTAL oscillator output (XTAL option only) RC or internal oscillator output (OSC2EN = 1 in PTAPUE register)	Output Output
	AD2 — A/D channel 2 input	Input
	KBI4 — Keyboard interrupt input 4	Input
PTA5	PTA5 — General purpose I/O port	Input/Output
	$\overline{OSC1}$ —XTAL, RC, or external oscillator input	Input
	$\overline{AD3}$ — A/D channel 3 input	Input
	KBI5 — Keyboard interrupt input 5	Input
PTB[0:7](1)	8 general-purpose I/O ports	Input/Output

1. The PTB pins are not available on the 8-pin packages (see note in 12.1 Introduction).

1.6 Pin Function Priority

Table 1-3 is meant to resolve the priority if multiple functions are enabled on a single pin.

NOTE

Upon reset all pins come up as input ports regardless of the priority table.

Table 1-3. Function Priority in Shared Pins

Pin Name	Highest-to-Lowest Priority Sequence
PTA0	AD0 → TCH0 → KBI0 → PTA0
PTA1	AD1 →TCH1 → KBI1 → PTA1
PTA2	$\overline{\text{IRQ}}$ → KBI2 → TCLK → PTA2
PTA3	$\overline{\text{RST}}$ → KBI3 → PTA3
PTA4	OSC2 → AD2 → KBI4 → PTA4
PTA5	OSC1 → AD3 → KBI5 → PTA5

Chapter 2
Memory

2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in Figure 2-1, includes:

- 4096 bytes of user FLASH for MC68HLC908QT4 and MC68HLC908QY4
- 1536 bytes of user FLASH for MC68HLC908QT2, MC68HLC908QT1, MC68HLC908QY2, and MC68HLC908QY1
- 128 bytes of random access memory (RAM)
- 48 bytes of user-defined vectors, located in FLASH
- 416 bytes of monitor read-only memory (ROM)
- 1536 bytes of FLASH program and erase routines, located in ROM

2.2 Unimplemented Memory Locations

Accessing an unimplemented location can have unpredictable effects on MCU operation. In Figure 2-1 and in register figures in this document, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In Figure 2-1 and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.

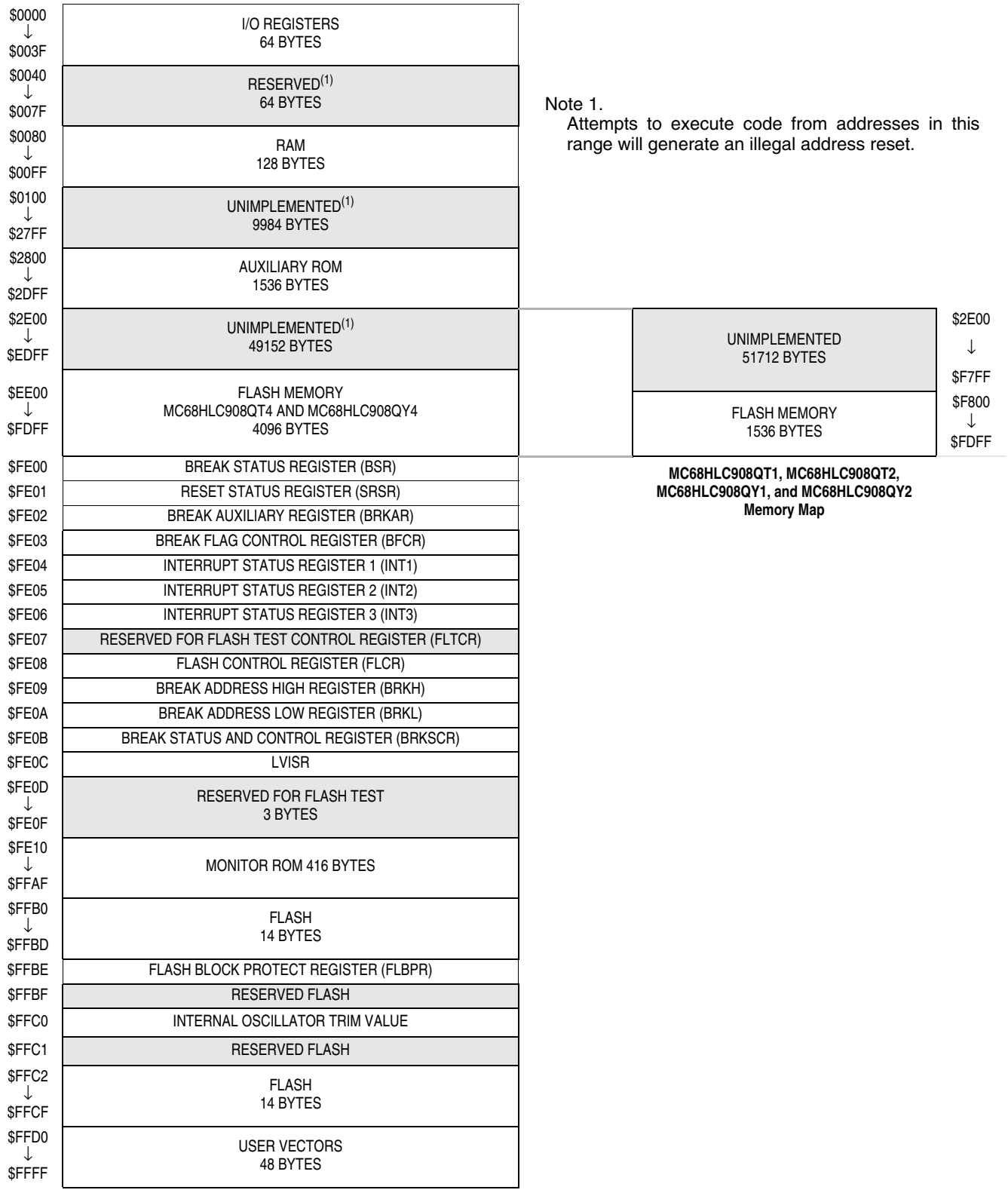


Figure 2-1. Memory Map

2.4 Input/Output (I/O) Section

Addresses $0000–$003F, shown in Figure 2-2, contain most of the control, status, and data registers. Additional I/O registers have these addresses:

- $FE00 — Break status register, BSR
- $FE01 — Reset status register, SRSR
- $FE02 — Break auxiliary register, BRKAR
- $FE03 — Break flag control register, BFCR
- $FE04 — Interrupt status register 1, INT1
- $FE05 — Interrupt status register 2, INT2
- $FE06 — Interrupt status register 3, INT3
- $FE07 — Reserved
- $FE08 — FLASH control register, FLCR
- $FE09 — Break address register high, BRKH
- $FE0A — Break address register low, BRKL
- $FE0B — Break status and control register, BRKSCR
- $FE0C — LVI status register, LVISR
- $FE0D — Reserved
- $FFBE — FLASH block protect register, FLBPR
- $FFC0 — Internal OSC trim value — Optional
- $FFFF — COP control register, COPCTL

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 98.	Read:	R	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PTB) See page 100.	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
$0002	Unimplemented									
$0003	Unimplemented									
$0004	Data Direction Register A (DDRA) See page 98.	Read:	R	R	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 6)