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**MC68HLC908QY4**  
**MC68HLC908QT4**  
**MC68HLC908QY2**  
**MC68HLC908QT2**  
**MC68HLC908QY1**  
**MC68HLC908QT1**

Data Sheet

**M68HC08**  
**Microcontrollers**

MC68HLC908QY4/D  
Rev. 3  
07/2005

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**MC68HLC908QY4**  
**MC68HLC908QT4**  
**MC68HLC908QY2**  
**MC68HLC908QT2**  
**MC68HLC908QY1**  
**MC68HLC908QT1**  
**Data Sheet**

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## Revision History

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

## Revision History

Date	Revision Level	Description	Page Number(s)
August, 2003	N/A	Initial release	N/A
October, 2003	1.0	Figure 2-2. Control, Status, and Data Registers Deleted unimplemented areas from \$FFB0–\$FFBD and \$FFC2–\$FFCF as they are actually available. Also corrected \$FFBF designation from unimplemented to reserved.	26
		Figure 6-1. COP Block Diagram — Reworked for clarity	57
		6.3.2 STOP Instruction — Added subsection for STOP instruction	58
		13.4.2 Active Resets from Internal Sources — Reworked notes for clarity.	115
		15.3 Monitor Module (MON) — Clarified seventh bullet.	154
		16.5 DC Electrical Characteristics — Corrected notes 4 and 5.	169
January, 2004	2.0	Figure 2-2. Control, Status, and Data Registers — Corrected reset state for the FLASH Block Protect Register at address location \$FFBE and the Internal Oscillator Trim Value at \$FFC0.	30
		Figure 2-5. FLASH Block Protect Register (FLBPR) — Restated reset state for clarity.	37
July, 2005	3.0	Reformatted to meet current documentation standards	Throughout
		<a href="#">Chapter 7 Central Processor Unit (CPU)</a> — In <a href="#">7.7 Instruction Set Summary</a> : Reworked definitions for STOP instruction Added WAIT instruction	70 71
		<a href="#">13.8.1 SIM Reset Status Register</a> — Clarified SRSR flag setting.	117
		<a href="#">14.9.1 TIM Status and Control Register</a> — Added information to TSTOP note.	127
		<a href="#">17.3 Package Dimensions</a> — Updated package information.	163

# List of Chapters

<b>Chapter 1 General Description</b> .....	<b>15</b>
<b>Chapter 2 Memory</b> .....	<b>23</b>
<b>Chapter 3 Analog-to-Digital Converter (ADC)</b> .....	<b>39</b>
<b>Chapter 4 Auto Wakeup Module (AWU)</b> .....	<b>47</b>
<b>Chapter 5 Configuration Register (CONFIG)</b> .....	<b>53</b>
<b>Chapter 6 Computer Operating Properly (COP)</b> .....	<b>57</b>
<b>Chapter 7 Central Processor Unit (CPU)</b> .....	<b>61</b>
<b>Chapter 8 External Interrupt (IRQ)</b> .....	<b>73</b>
<b>Chapter 9 Keyboard Interrupt Module (KBI)</b> .....	<b>79</b>
<b>Chapter 10 Low-Voltage Inhibit (LVI)</b> .....	<b>85</b>
<b>Chapter 11 Oscillator Module (OSC)</b> .....	<b>89</b>
<b>Chapter 12 Input/Output Ports (PORTS)</b> .....	<b>97</b>
<b>Chapter 13 System Integration Module (SIM)</b> .....	<b>103</b>
<b>Chapter 14 Timer Interface Module (TIM)</b> .....	<b>119</b>
<b>Chapter 15 Development Support</b> .....	<b>135</b>
<b>Chapter 16 Electrical Specifications</b> .....	<b>151</b>
<b>Chapter 17 Ordering Information and Mechanical Specifications</b> .....	<b>163</b>



**List of Chapters**

# Table of Contents

## Chapter 1 General Description

1.1	Introduction	15
1.2	Features	15
1.3	MCU Block Diagram	17
1.4	Pin Assignments	17
1.5	Pin Functions	20
1.6	Pin Function Priority	21

## Chapter 2 Memory

2.1	Introduction	23
2.2	Unimplemented Memory Locations	23
2.3	Reserved Memory Locations	23
2.4	Input/Output (I/O) Section	25
2.5	Random-Access Memory (RAM)	31
2.6	FLASH Memory (FLASH)	32
2.6.1	FLASH Control Register	32
2.6.2	FLASH Page Erase Operation	33
2.6.3	FLASH Mass Erase Operation	34
2.6.4	FLASH Program Operation	34
2.6.5	FLASH Protection	35
2.6.6	FLASH Block Protect Register	37
2.6.7	Wait Mode	38
2.6.8	Stop Mode	38

## Chapter 3 Analog-to-Digital Converter (ADC)

3.1	Introduction	39
3.2	Features	39
3.3	Functional Description	39
3.3.1	ADC Port I/O Pins	39
3.3.2	Voltage Conversion	41
3.3.3	Conversion Time	42
3.3.4	Continuous Conversion	42
3.3.5	Accuracy and Precision	42
3.4	Interrupts	42
3.5	Low-Power Modes	42
3.5.1	Wait Mode	42
3.5.2	Stop Mode	42



## Table of Contents

3.6	Input/Output Signals . . . . .	43
3.7	Input/Output Registers . . . . .	43
3.7.1	ADC Status and Control Register . . . . .	43
3.7.2	ADC Data Register . . . . .	44
3.7.3	ADC Input Clock Register . . . . .	45

### Chapter 4 Auto Wakeup Module (AWU)

4.1	Introduction . . . . .	47
4.2	Features . . . . .	47
4.3	Functional Description . . . . .	47
4.4	Wait Mode . . . . .	49
4.5	Stop Mode . . . . .	49
4.6	Input/Output Registers . . . . .	49
4.6.1	Port A I/O Register . . . . .	49
4.6.2	Keyboard Status and Control Register . . . . .	50
4.6.3	Keyboard Interrupt Enable Register . . . . .	51

### Chapter 5 Configuration Register (CONFIG)

5.1	Introduction . . . . .	53
5.2	Functional Description . . . . .	53

### Chapter 6 Computer Operating Properly (COP)

6.1	Introduction . . . . .	57
6.2	Functional Description . . . . .	57
6.3	I/O Signals . . . . .	58
6.3.1	BUSCLKX4 . . . . .	58
6.3.2	STOP Instruction . . . . .	58
6.3.3	COPCTL Write . . . . .	58
6.3.4	Power-On Reset . . . . .	58
6.3.5	Internal Reset . . . . .	58
6.3.6	COPD (COP Disable) . . . . .	58
6.3.7	COPRS (COP Rate Select) . . . . .	59
6.4	COP Control Register . . . . .	59
6.5	Interrupts . . . . .	59
6.6	Monitor Mode . . . . .	59
6.7	Low-Power Modes . . . . .	59
6.7.1	Wait Mode . . . . .	59
6.7.2	Stop Mode . . . . .	59
6.8	COP Module During Break Mode . . . . .	59

## Chapter 7 Central Processor Unit (CPU)

7.1	Introduction . . . . .	61
7.2	Features . . . . .	61
7.3	CPU Registers . . . . .	61
7.3.1	Accumulator . . . . .	62
7.3.2	Index Register . . . . .	62
7.3.3	Stack Pointer . . . . .	63
7.3.4	Program Counter . . . . .	63
7.3.5	Condition Code Register . . . . .	64
7.4	Arithmetic/Logic Unit (ALU) . . . . .	65
7.5	Low-Power Modes . . . . .	65
7.5.1	Wait Mode . . . . .	65
7.5.2	Stop Mode . . . . .	65
7.6	CPU During Break Interrupts . . . . .	65
7.7	Instruction Set Summary . . . . .	66
7.8	Opcode Map . . . . .	71

## Chapter 8 External Interrupt (IRQ)

8.1	Introduction . . . . .	73
8.2	Features . . . . .	73
8.3	Functional Description . . . . .	73
8.3.1	MODE = 1 . . . . .	75
8.3.2	MODE = 0 . . . . .	75
8.4	Interrupts . . . . .	76
8.5	Low-Power Modes . . . . .	76
8.5.1	Wait Mode . . . . .	76
8.5.2	Stop Mode . . . . .	76
8.6	IRQ Module During Break Interrupts . . . . .	76
8.7	I/O Signals . . . . .	76
8.7.1	IRQ Input Pins ( $\overline{\text{IRQ}}$ ) . . . . .	77
8.8	Registers . . . . .	77

## Chapter 9 Keyboard Interrupt Module (KBI)

9.1	Introduction . . . . .	79
9.2	Features . . . . .	79
9.3	Functional Description . . . . .	79
9.3.1	Keyboard Operation . . . . .	79
9.3.2	Keyboard Initialization . . . . .	82
9.4	Wait Mode . . . . .	82
9.5	Stop Mode . . . . .	82
9.6	Keyboard Module During Break Interrupts . . . . .	82

## Table of Contents

9.7	Input/Output Registers . . . . .	83
9.7.1	Keyboard Status and Control Register . . . . .	83
9.7.2	Keyboard Interrupt Enable Register . . . . .	84

## Chapter 10 Low-Voltage Inhibit (LVI)

10.1	Introduction . . . . .	85
10.2	Features . . . . .	85
10.3	Functional Description . . . . .	85
10.3.1	Polled LVI Operation . . . . .	86
10.3.2	Forced Reset Operation . . . . .	86
10.3.3	Voltage Hysteresis Protection . . . . .	86
10.3.4	LVI Trip Selection . . . . .	86
10.4	LVI Status Register . . . . .	87
10.5	LVI Interrupts . . . . .	87
10.6	Low-Power Modes . . . . .	88
10.6.1	Wait Mode . . . . .	88
10.6.2	Stop Mode . . . . .	88

## Chapter 11 Oscillator Module (OSC)

11.1	Introduction . . . . .	89
11.2	Features . . . . .	89
11.3	Functional Description . . . . .	89
11.3.1	Internal Oscillator . . . . .	89
11.3.1.1	Internal Oscillator Trimming . . . . .	91
11.3.1.2	Internal to External Clock Switching . . . . .	91
11.3.2	External Oscillator . . . . .	91
11.3.3	XTAL Oscillator . . . . .	92
11.3.4	RC Oscillator . . . . .	92
11.4	Oscillator Module Signals . . . . .	93
11.4.1	Crystal Amplifier Input Pin (OSC1) . . . . .	93
11.4.2	Crystal Amplifier Output Pin (OSC2/PTA4/BUSCLKX4) . . . . .	93
11.4.3	Oscillator Enable Signal (SIMOSCEN) . . . . .	94
11.4.4	XTAL Oscillator Clock (XTALCLK) . . . . .	94
11.4.5	RC Oscillator Clock (RCCLK) . . . . .	94
11.4.6	Internal Oscillator Clock (INTCLK) . . . . .	94
11.4.7	Oscillator Out 2 (BUSCLKX4) . . . . .	94
11.4.8	Oscillator Out (BUSCLKX2) . . . . .	94
11.5	Low Power Modes . . . . .	94
11.5.1	Wait Mode . . . . .	94
11.5.2	Stop Mode . . . . .	94
11.6	Oscillator During Break Mode . . . . .	95
11.7	CONFIG2 Options . . . . .	95
11.8	Input/Output (I/O) Registers . . . . .	95
11.8.1	Oscillator Status Register . . . . .	95
11.8.2	Oscillator Trim Register (OSCTRIM) . . . . .	96

## Chapter 12 Input/Output Ports (PORTS)

12.1	Introduction .....	97
12.2	Port A .....	97
12.2.1	Port A Data Register .....	98
12.2.2	Data Direction Register A .....	98
12.2.3	Port A Input Pullup Enable Register .....	99
12.3	Port B .....	100
12.3.1	Port B Data Register .....	100
12.3.2	Data Direction Register B .....	101
12.3.3	Port B Input Pullup Enable Register .....	102

## Chapter 13 System Integration Module (SIM)

13.1	Introduction .....	103
13.2	$\overline{RST}$ and $\overline{IRQ}$ Pins Initialization .....	103
13.3	SIM Bus Clock Control and Generation .....	104
13.3.1	Bus Timing .....	105
13.3.2	Clock Start-Up from POR .....	105
13.3.3	Clocks in Stop Mode and Wait Mode .....	105
13.4	Reset and System Initialization .....	105
13.4.1	External Pin Reset .....	105
13.4.2	Active Resets from Internal Sources .....	106
13.4.2.1	Power-On Reset .....	107
13.4.2.2	Computer Operating Properly (COP) Reset .....	107
13.4.2.3	Illegal Opcode Reset .....	108
13.4.2.4	Illegal Address Reset .....	108
13.4.2.5	Low-Voltage Inhibit (LVI) Reset .....	108
13.5	SIM Counter .....	108
13.5.1	SIM Counter During Power-On Reset .....	108
13.5.2	SIM Counter During Stop Mode Recovery .....	108
13.5.3	SIM Counter and Reset States .....	109
13.6	Exception Control .....	109
13.6.1	Interrupts .....	109
13.6.1.1	Hardware Interrupts .....	109
13.6.1.2	SWI Instruction .....	112
13.6.2	Interrupt Status Registers .....	112
13.6.2.1	Interrupt Status Register 1 .....	112
13.6.2.2	Interrupt Status Register 2 .....	113
13.6.2.3	Interrupt Status Register 3 .....	113
13.6.3	Reset .....	113
13.6.4	Break Interrupts .....	113
13.6.5	Status Flag Protection in Break Mode .....	114
13.7	Low-Power Modes .....	114
13.7.1	Wait Mode .....	114
13.7.2	Stop Mode .....	115

## Table of Contents

13.8	SIM Registers .....	116
13.8.1	SIM Reset Status Register .....	117
13.8.2	Break Flag Control Register .....	118

## Chapter 14 Timer Interface Module (TIM)

14.1	Introduction .....	119
14.2	Features .....	119
14.3	Pin Name Conventions .....	119
14.4	Functional Description .....	121
14.4.1	TIM Counter Prescaler .....	122
14.4.2	Input Capture .....	122
14.4.3	Output Compare .....	122
14.4.3.1	Unbuffered Output Compare .....	122
14.4.3.2	Buffered Output Compare .....	122
14.4.4	Pulse Width Modulation (PWM) .....	123
14.4.4.1	Unbuffered PWM Signal Generation .....	124
14.4.4.2	Buffered PWM Signal Generation .....	124
14.4.4.3	PWM Initialization .....	125
14.5	Interrupts .....	125
14.6	Wait Mode .....	126
14.7	TIM During Break Interrupts .....	126
14.8	Input/Output Signals .....	126
14.8.1	TIM Clock Pin (PTA2/TCLK) .....	126
14.8.2	TIM Channel I/O Pins (PTA0/TCH0 and PTA1/TCH1) .....	126
14.9	Input/Output Registers .....	126
14.9.1	TIM Status and Control Register .....	127
14.9.2	TIM Counter Registers .....	128
14.9.3	TIM Counter Modulo Registers .....	129
14.9.4	TIM Channel Status and Control Registers .....	130
14.9.5	TIM Channel Registers .....	132

## Chapter 15 Development Support

15.1	Introduction .....	135
15.2	Break Module (BRK) .....	135
15.2.1	Functional Description .....	135
15.2.1.1	Flag Protection During Break Interrupts .....	137
15.2.1.2	TIM During Break Interrupts .....	137
15.2.1.3	COP During Break Interrupts .....	137
15.2.2	Break Module Registers .....	137
15.2.2.1	Break Status and Control Register .....	138
15.2.2.2	Break Address Registers .....	138
15.2.2.3	Break Auxiliary Register .....	139
15.2.2.4	Break Status Register .....	139
15.2.2.5	Break Flag Control Register .....	139
15.2.3	Low-Power Modes .....	140

15.3	Monitor Module (MON)	140
15.3.1	Functional Description	140
15.3.1.1	Normal Monitor Mode	144
15.3.1.2	Forced Monitor Mode	145
15.3.1.3	Monitor Vectors	145
15.3.1.4	Data Format	146
15.3.1.5	Break Signal	146
15.3.1.6	Baud Rate	146
15.3.1.7	Commands	146
15.3.2	Security	150

## Chapter 16 Electrical Specifications

16.1	Introduction	151
16.2	Absolute Maximum Ratings	151
16.3	Functional Operating Range	152
16.4	Thermal Characteristics	152
16.5	DC Electrical Characteristics	153
16.6	Control Timing	154
16.7	Typical 3.0-V Output Drive Characteristics	155
16.8	Oscillator Characteristics	156
16.9	Supply Current Characteristics	157
16.10	Analog-to-Digital (ADC) Converter Characteristics	159
16.10.1	ADC Electrical Operating Conditions	159
16.10.2	ADC Performance Characteristics	159
16.11	Timer Interface Module Characteristics	160
16.12	Memory Characteristics	161

## Chapter 17 Ordering Information and Mechanical Specifications

17.1	Introduction	163
17.2	MC Order Numbers	163
17.3	Package Dimensions	163



**Table of Contents**

# Chapter 1

## General Description

### 1.1 Introduction

The MC68HLC908QY4 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is a Complex Instruction Set Computer (CISC) with a Von Neumann architecture. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

**Table 1-1. Summary of Device Variations**

Device	FLASH Memory Size	Analog-to-Digital Converter	Pin Count
MC68HLC908QT1	1536 bytes	—	8 pins
MC68HLC908QT2	1536 bytes	4 ch, 8 bit	8 pins
MC68HLC908QT4	4096 bytes	4 ch, 8 bit	8 pins
MC68HLC908QY1	1536 bytes	—	16 pins
MC68HLC908QY2	1536 bytes	4 ch, 8 bit	16 pins
MC68HLC908QY4	4096 bytes	4 ch, 8 bit	16 pins

### 1.2 Features

Features include:

- High-performance M68HC08 CPU core
- Fully upward-compatible object code with M68HC05 Family
- Operating voltage range of 2.2 V to 3.6 V
- 2-MHz internal bus operation
- Trimmable internal oscillator
  - 1.0 MHz internal bus operation
  - 8-bit trim capability allows 0.4% accuracy<sup>(1)</sup>
  - $\pm 25\%$  untrimmed
- Auto wakeup from STOP capability
- Configuration (CONFIG) register for MCU configuration options, including:
  - Low-voltage inhibit (LVI) trip point
- In-system FLASH programming
- FLASH security<sup>(2)</sup>

1. The oscillator frequency is guaranteed to  $\pm 5\%$  over temperature and voltage range after trimming.

2. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the FLASH difficult for unauthorized users.



## General Description

- On-chip in-application programmable FLASH memory (with internal program/erase voltage generation)
  - MC68HLC908QY4 and MC68HLC908QT4 — 4096 bytes
  - MC68HLC908QY2, MC68HLC908QY1, MC68HLC908QT2, and MC68HLC908QT1— 1536 bytes
- 128 bytes of on-chip random-access memory (RAM)
- 2-channel, 16-bit timer interface module (TIM)
- 4-channel, 8-bit analog-to-digital converter (ADC) on MC68HLC908QY2, MC68HLC908QY4, MC68HLC908QT2, and MC68HLC908QT4
- 5 or 13 bidirectional input/output (I/O) lines and one input only:
  - Six shared with keyboard interrupt function and ADC
  - Two shared with timer channels
  - One shared with external interrupt (IRQ)
  - Eight extra I/O lines on 16-pin package only
  - High current sink/source capability on all port pins
  - Selectable pullups on all ports, selectable on an individual bit basis
  - Three-state ability on all port pins
- 6-bit keyboard interrupt with wakeup feature (KBI)
- Low-voltage inhibit (LVI) module features:
  - Software selectable trip point in CONFIG register
- System protection features:
  - Computer operating properly (COP) watchdog
  - Low-voltage detection with optional reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- External asynchronous interrupt pin with internal pullup ( $\overline{IRQ}$ ) shared with general-purpose input pin
- Master asynchronous reset pin ( $\overline{RST}$ ) shared with general-purpose input/output (I/O) pin
- Power-on reset
- Internal pullups on  $\overline{IRQ}$  and  $\overline{RST}$  to reduce external components
- Memory mapped I/O registers
- Power saving stop and wait modes
- MC68HLC908QY4, MC68HLC908QY2, and MC68HLC908QY1 are available in these packages:
  - 16-pin plastic dual in-line package (PDIP)
  - 16-pin small outline integrated circuit (SOIC) package
  - 16-pin thin shrink small outline package (TSSOP)
- MC68HLC908QT4, MC68HLC908QT2, and MC68HLC908QT1 are available in these packages:
  - 8-pin PDIP
  - 8-pin SOIC
  - 8-pin dual flat no lead (DFN) package

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast  $8 \times 8$  multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

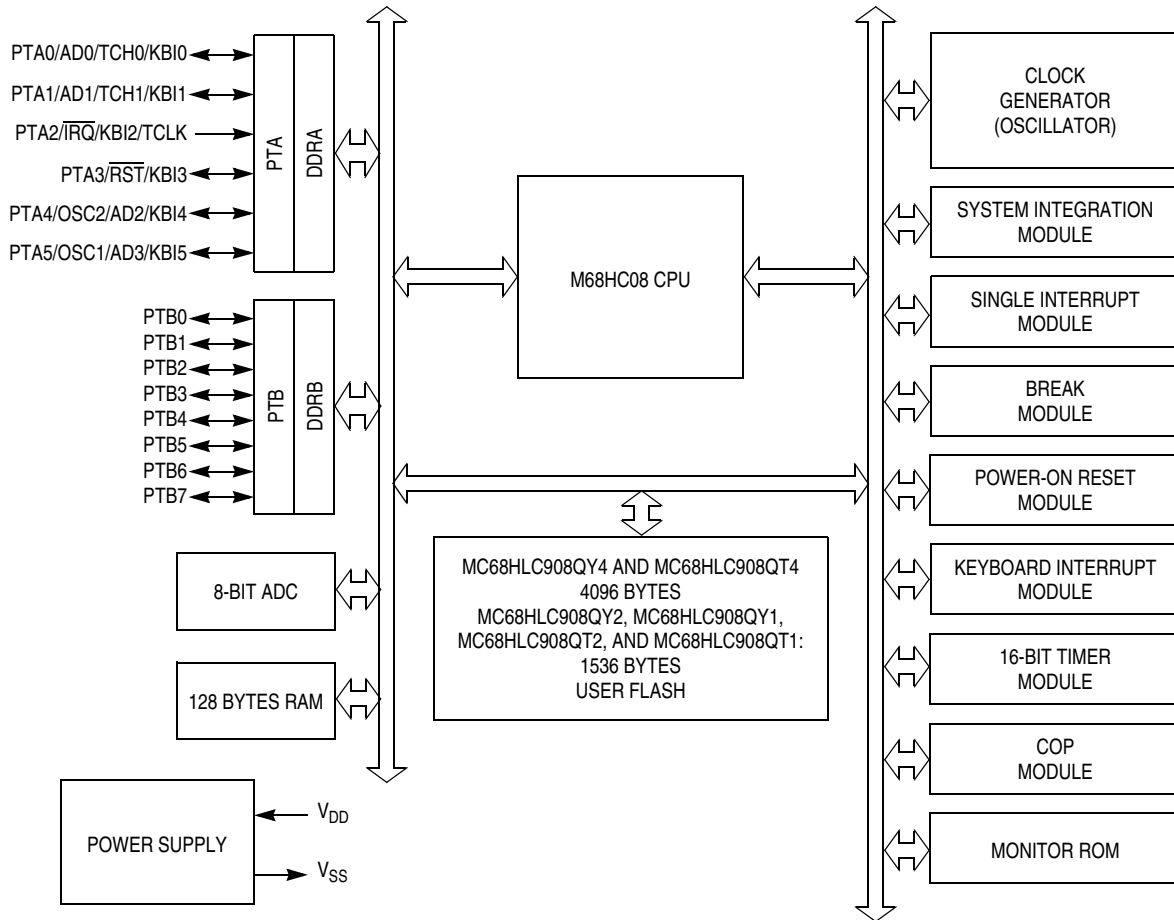
### 1.3 MCU Block Diagram

[Figure 1-1](#) shows the structure of the MC68HLC908QY4.

### 1.4 Pin Assignments

The MC68HLC908QT4, MC68HLC908QT2, and MC68HLC908QT1 are available in 8-pin packages and the MC68HLC908QY4, MC68HLC908QY2, and MC68HLC908QY1 in 16-pin packages. [Figure 1-2](#) shows the pin assignment for these packages.

## General Description



$\overline{RST}$ ,  $\overline{IRQ}$ : Pins have internal (about 30K Ohms) pull up

PTA[0:5]: High current sink and source capability

PTA[0:5]: Pins have programmable keyboard interrupt and pull up

PTB[0:7]: Not available on 8-pin devices – MC68HLC908QT1, MC68HLC908QT2, and MC68HLC908QT4 (see note in [12.1 Introduction](#))

ADC: Not available on the MC68HLC908QY1 and MC68HLC908QT1

**Figure 1-1. Block Diagram**

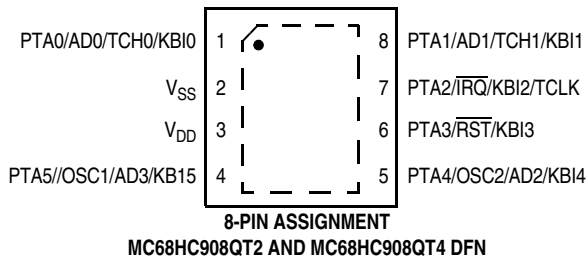
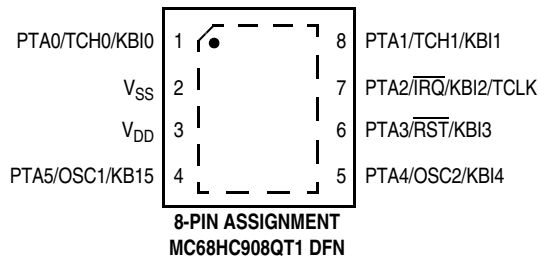
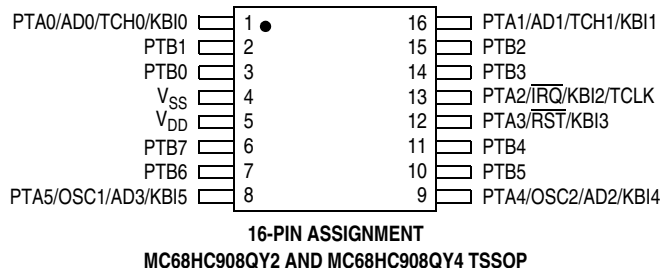
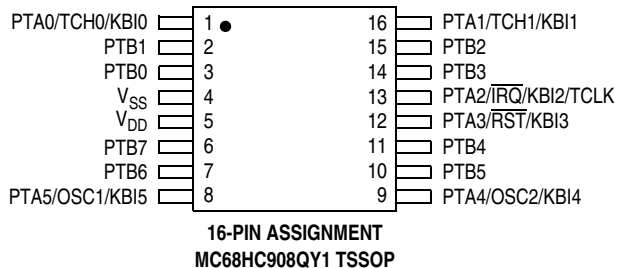
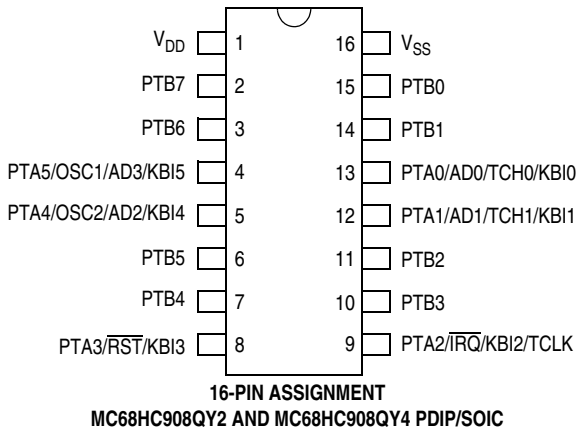
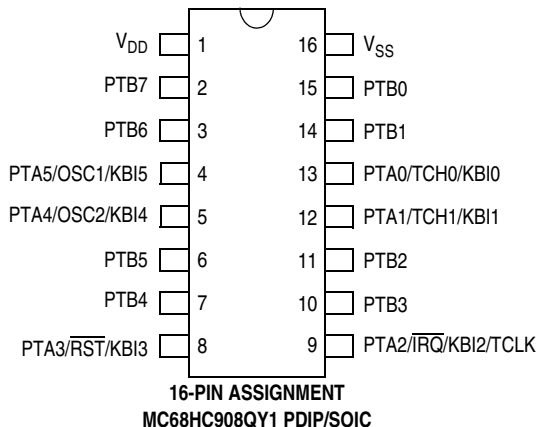
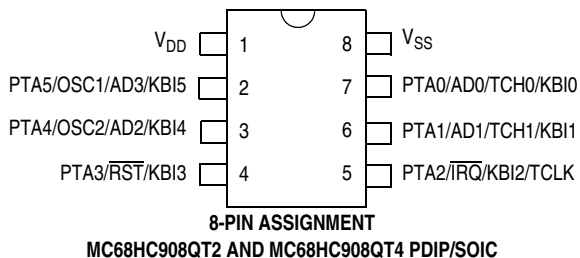
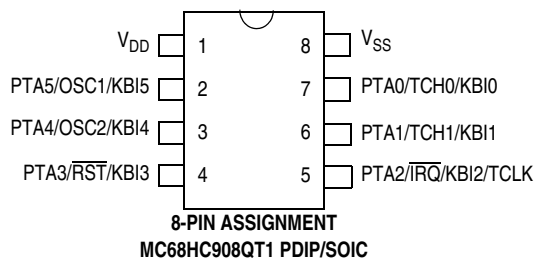


Figure 1-2. MCU Pin Assignments

## 1.5 Pin Functions

Table 1-2 provides a description of the pin functions.

**Table 1-2. Pin Functions**

Pin Name	Description	Input/Output
V <sub>DD</sub>	Power supply	Power
V <sub>SS</sub>	Power supply ground	Power
PTA0	PTA0 — General purpose I/O port	Input/Output
	AD0 — A/D channel 0 input	Input
	TCH0 — Timer Channel 0 I/O	Input/Output
	KBI0 — Keyboard interrupt input 0	Input
PTA1	PTA1 — General purpose I/O port	Input/Output
	AD1 — A/D channel 1 input	Input
	TCH1 — Timer Channel 1 I/O	Input/Output
	KBI1 — Keyboard interrupt input 1	Input
PTA2	PTA2 — General purpose input-only port	Input
	$\overline{IRQ}$ — External interrupt with programmable pullup and Schmitt trigger input	Input
	KBI2 — Keyboard interrupt input 2	Input
	TCLK — Timer clock input	Input
PTA3	PTA3 — General purpose I/O port	Input/Output
	$\overline{RST}$ — Reset input, active low with internal pullup and Schmitt trigger	Input
	KBI3 — Keyboard interrupt input 3	Input
PTA4	PTA4 — General purpose I/O port	Input/Output
	OSC2 — XTAL oscillator output (XTAL option only) RC or internal oscillator output (OSC2EN = 1 in PTAPUE register)	Output Output
	AD2 — A/D channel 2 input	Input
	KBI4 — Keyboard interrupt input 4	Input
PTA5	PTA5 — General purpose I/O port	Input/Output
	$\overline{OSC1}$ — XTAL, RC, or external oscillator input	Input
	AD3 — A/D channel 3 input	Input
	KBI5 — Keyboard interrupt input 5	Input
PTB[0:7] <sup>(1)</sup>	8 general-purpose I/O ports	Input/Output

1. The PTB pins are not available on the 8-pin packages (see note in [12.1 Introduction](#)).

## 1.6 Pin Function Priority

Table 1-3 is meant to resolve the priority if multiple functions are enabled on a single pin.

**NOTE**

*Upon reset all pins come up as input ports regardless of the priority table.*

**Table 1-3. Function Priority in Shared Pins**

Pin Name	Highest-to-Lowest Priority Sequence
PTA0	AD0 → TCH0 → KBI0 → PTA0
PTA1	AD1 → TCH1 → KBI1 → PTA1
PTA2	$\overline{\text{IRQ}}$ → KBI2 → TCLK → PTA2
PTA3	$\overline{\text{RST}}$ → KBI3 → PTA3
PTA4	OSC2 → AD2 → KBI4 → PTA4
PTA5	OSC1 → AD3 → KBI5 → PTA5



# Chapter 2

## Memory

### 2.1 Introduction

The central processor unit (CPU08) can address 64 Kbytes of memory space. The memory map, shown in [Figure 2-1](#), includes:

- 4096 bytes of user FLASH for MC68HLC908QT4 and MC68HLC908QY4
- 1536 bytes of user FLASH for MC68HLC908QT2, MC68HLC908QT1, MC68HLC908QY2, and MC68HLC908QY1
- 128 bytes of random access memory (RAM)
- 48 bytes of user-defined vectors, located in FLASH
- 416 bytes of monitor read-only memory (ROM)
- 1536 bytes of FLASH program and erase routines, located in ROM

### 2.2 Unimplemented Memory Locations

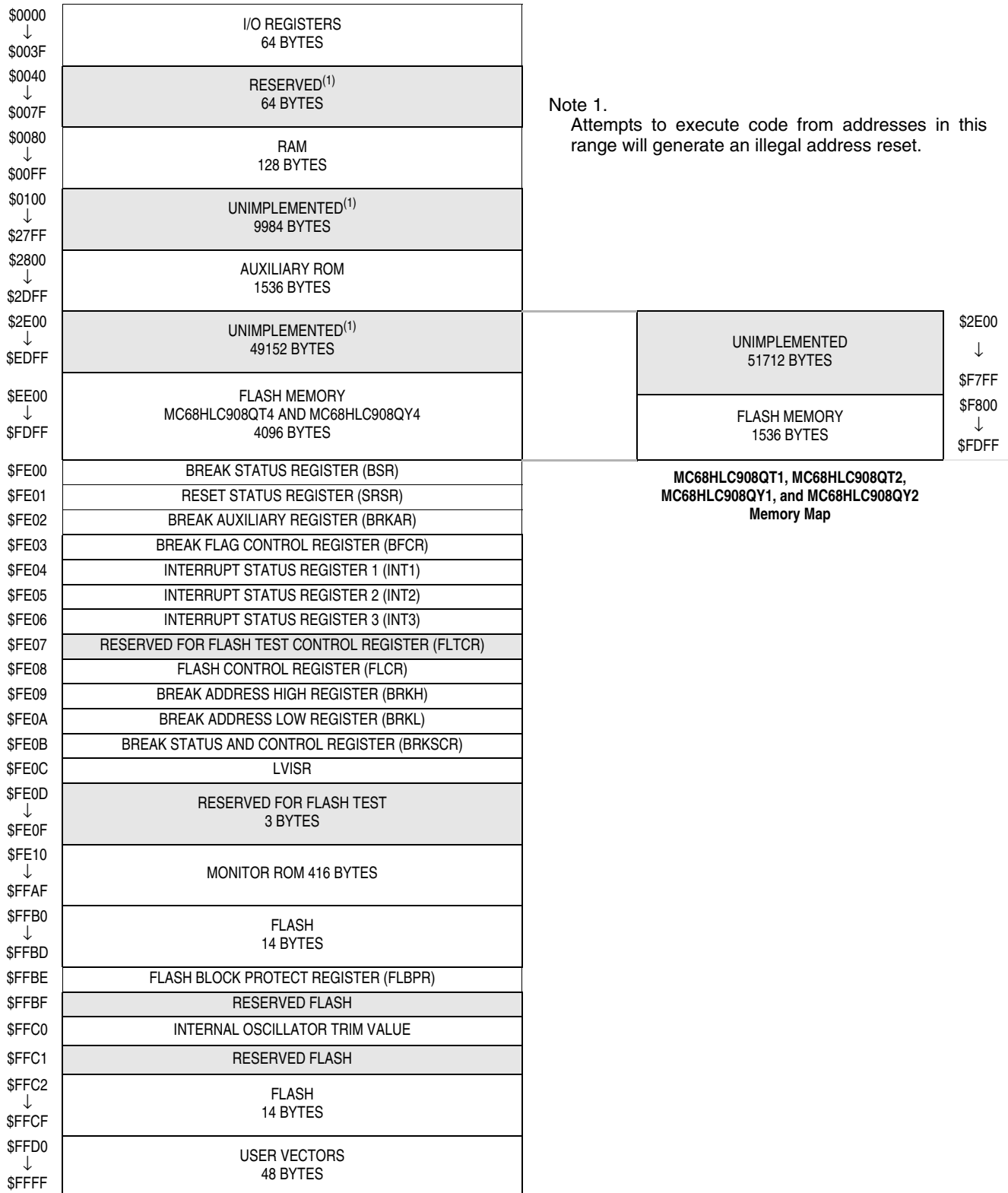
Accessing an unimplemented location can have unpredictable effects on MCU operation. In [Figure 2-1](#) and in register figures in this document, unimplemented locations are shaded.

### 2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In [Figure 2-1](#) and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.



## Memory



Note 1.  
Attempts to execute code from addresses in this range will generate an illegal address reset.

**Figure 2-1. Memory Map**

## 2.4 Input/Output (I/O) Section

Addresses \$0000–\$003F, shown in [Figure 2-2](#), contain most of the control, status, and data registers. Additional I/O registers have these addresses:

- \$FE00 — Break status register, BSR
- \$FE01 — Reset status register, SRSR
- \$FE02 — Break auxiliary register, BRKAR
- \$FE03 — Break flag control register, BFCR
- \$FE04 — Interrupt status register 1, INT1
- \$FE05 — Interrupt status register 2, INT2
- \$FE06 — Interrupt status register 3, INT3
- \$FE07 — Reserved
- \$FE08 — FLASH control register, FLCR
- \$FE09 — Break address register high, BRKH
- \$FE0A — Break address register low, BRKL
- \$FE0B — Break status and control register, BRKSCR
- \$FE0C — LVI status register, LVISR
- \$FE0D — Reserved
- \$FFBE — FLASH block protect register, FLBPR
- \$FFC0 — Internal OSC trim value — Optional
- \$FFFF — COP control register, COPCTL

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0	
\$0000	Port A Data Register (PTA) <a href="#">See page 98.</a>	Read:	R	AWUL	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
\$0001	Port B Data Register (PTB) <a href="#">See page 100.</a>	Read:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
\$0002	Unimplemented									
\$0003	Unimplemented									
\$0004	Data Direction Register A (DDRA) <a href="#">See page 98.</a>	Read:	R	R	DDRA5	DDRA4	DDRA3	0	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented     
 R = Reserved     
 U = Unaffected

**Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 6)**