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MCP14A0051/2

0.5A MOSFET Driver With Low Threshold Input And Enable

Features

- High Peak Output Current: 0.5A (typical)
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- Low Shoot-Through/Cross-Conduction Current in Output Stage
- High Capacitive Load Drive Capability:
  - 1000 pF in 40 ns (typical)
- Short Delay Times: 33 ns (t_{D1}), 24 ns (t_{D2}) (typical)
- Low Supply Current: 375 µA (typical)
- Low Voltage Threshold Input and Enable with Hysteresis
- Latch-Up Protected: Withstands 500 mA Reverse Current
- Space-Saving Packages:
  - 6L SOT-23
  - 6L 2 x 2 DFN

Applications

- Switch Mode Power Supplies
- Pulse Transformer Drive
- Line Drivers
- Level Translator
- Motor and Solenoid Drive

General Description

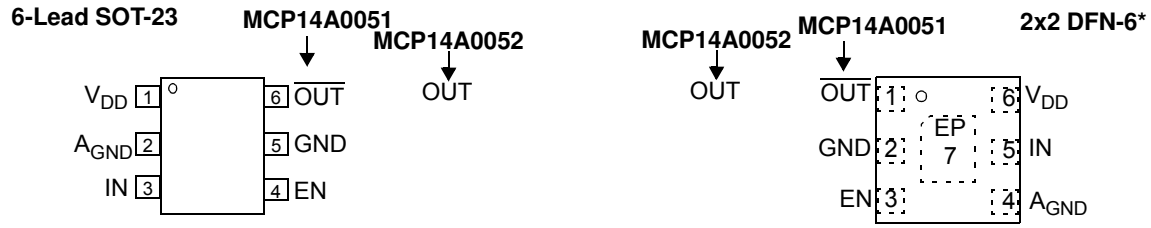
The MCP14A0051/2 devices are high-speed MOSFET drivers that are capable of providing up to 0.5A of peak current while operating from a single 4.5V to 18V supply. The inverting (MCP14A0051) or non-inverting (MCP14A0052) single-channel output is directly controlled from either TTL or CMOS (2V to 18V) logic. These devices also feature low shoot-through current, matched rise and fall times, and short propagation delays which make them ideal for high switching frequency applications.

The MCP14A0051/2 family of devices offer enhanced control with Enable functionality. The active-high Enable pin can be driven low to drive the output of the MCP14A0051/2 low regardless of the status of the Input pin. An integrated pull-up resistor allows the user to leave the Enable pin floating for standard operation.

Additionally, the MCP14A0051/2 devices feature separate ground pins (A_{GND} and GND), allowing greater noise isolation between the level-sensitive Input/Enable pins and the fast, high-current transitions of the push-pull output stage.

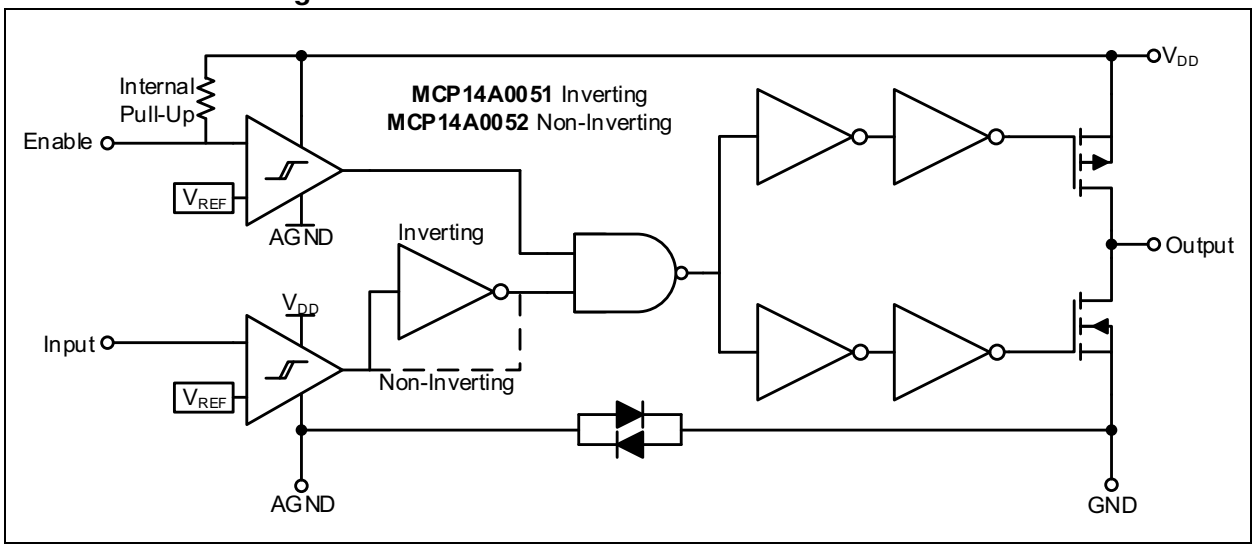
These devices are highly latch-up resistant under any condition within their power and voltage ratings. They can accept up to 500 mA of reverse current being forced back into their outputs without damage or logic upset. All terminals are fully protected against electrostatic discharge (ESD) up to 1.75 kV (HBM) and 100V (MM).

Package Types



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD}, Supply Voltage.....+20V
V_{IN}, Input Voltage.....(V_{DD} + 0.3V) to (GND - 0.3V)
V_{EN}, Enable Voltage.....(V_{DD} + 0.3V) to (GND - 0.3V)
Package Power Dissipation (T_A = +50°C)
6L SOT-23.....0.52 W
6L 2 x 2 DFN.....1.09 W
ESD Protection on all Pins.....1.75 kV (HBM)
.....100V (MM)

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V_{IN}	GND - 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.2	0.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.4	—	V	
Input Current	I_{IN}	-1	—	+1	µA	0V ≤ V_{IN} ≤ V_{DD}
Enable						
Enable Voltage Range	V_{EN}	GND - 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Enable Voltage	V_{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.2	0.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.4	—	V	
Enable Pin Pull-Up Resistance	R_{ENBL}	—	1.8	—	MΩ	V_{DD} = 18V, ENB = A_{GND}
Enable Input Current	I_{EN}	—	10	—	µA	V_{DD} = 18V, ENB = A_{GND}
Propagation Delay	t_{D3}	—	35	43	ns	V_{DD} = 18V, V_{EN} = 5V, see Figure 4-3, (**Note 1**)
Propagation Delay	t_{D4}	—	23	31	ns	V_{DD} = 18V, V_{EN} = 5V, see Figure 4-3, (**Note 1**)
Output						
High Output Voltage	V_{OH}	V_{DD} - 0.025	—	—	V	I_{OUT} = 0A
Low Output Voltage	V_{OL}	—	—	0.025	V	I_{OUT} = 0A
Output Resistance, High	R_{OH}	—	12.5	17	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	7.5	10	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	0.5	—	A	V_{DD} = 18V (**Note 1**)
Latch-Up Protection Withstand Reverse Current	I_{REV}	0.5	—	—	A	Duty cycle ≤ 2%, t ≤ 300 µs (**Note 1**)
Switching Time (**Note 1**)						
Rise Time	t_R	—	40	51	ns	V_{DD} = 18V, C_L = 1000 pF, see Figure 4-1, Figure 4-2 (**Note 1**)
Fall Time	t_F	—	28	39	ns	V_{DD} = 18V, C_L = 1000 pF, see Figure 4-1, Figure 4-2 (**Note 1**)

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_A = +25°C, with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Delay Time	t_{D1}	—	33	41	ns	V_{DD} = 18V, V_{IN} = 5V, see Figure 4-1, Figure 4-2, (**Note 1**)
Delay Time	t_{D2}	—	24	32	ns	V_{DD} = 18V, V_{IN} = 5V, see Figure 4-1, Figure 4-2, (**Note 1**)
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	330	560	µA	V_{IN} = 3V, V_{EN} = 3V
	I_{DD}	—	360	580	µA	V_{IN} = 0V, V_{EN} = 3V
	I_{DD}	—	360	580	µA	V_{IN} = 3V, V_{EN} = 0V
	I_{DD}	—	375	600	µA	V_{IN} = 0V, V_{EN} = 0V

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE) (Note 1)

Electrical Specifications: Unless otherwise indicated, over the operating range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V_{IN}	GND - 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.2	0.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.4	—	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Enable						
Enable Voltage Range	V_{EN}	GND - 0.3V	—	V_{DD} + 0.3	V	
Logic '1' High Enable Voltage	V_{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.2	0.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.4	—	V	
Enable Input Current	I_{EN}	—	12	—	µA	V_{DD} = 18V, ENB = A_{GND}
Propagation Delay	t_{D3}	—	33	41	ns	V_{DD} = 18V, V_{EN} = 5V, T_A = +125°C, see Figure 4-3
Propagation Delay	t_{D4}	—	25	33	ns	V_{DD} = 18V, V_{EN} = 5V, T_A = +125°C, see Figure 4-3
Output						
High Output Voltage	V_{OH}	V_{DD} - 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	—	24	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	—	15	Ω	I_{OUT} = 10 mA, V_{DD} = 18V

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMP. RANGE) (Note 1) (CONTINUED)

Electrical Specifications: Unless otherwise indicated, over the operating range with 4.5V ≤ V_{DD} ≤ 18V.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switching Time (Note 1)						
Rise Time	t_R	—	45	56	ns	V_{DD} = 18V, C_L = 1000 pF, T_A = +125°C, see Figure 4-1, Figure 4-2
Fall Time	t_F	—	34	45	ns	V_{DD} = 18V, C_L = 1000 pF, T_A = +125°C, see Figure 4-1, Figure 4-2
Delay Time	t_{D1}	—	32	40	ns	V_{DD} = 18V, V_{IN} = 5V, T_A = +125°C, see Figure 4-1, Figure 4-2
Delay Time	t_{D2}	—	27	35		V_{DD} = 18V, V_{IN} = 5V, T_A = +125°C, see Figure 4-1, Figure 4-2
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	—	760	uA	V_{IN} = 3V, V_{EN} = 3V
	I_{DD}	—	—	780	uA	V_{IN} = 0V, V_{EN} = 3V
	I_{DD}	—	—	780	uA	V_{IN} = 3V, V_{EN} = 0V
	I_{DD}	—	—	800	uA	V_{IN} = 0V, V_{EN} = 0V

Note 1: Tested during characterization, not production tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V

Parameter	Sym.	Min.	Typ.	Max.	Units	Comments
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 6LD 2x2 DFN	θ_{JA}	—	91	—	°C/W	
Thermal Resistance, 6LD SOT-23	θ_{JA}	—	192	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

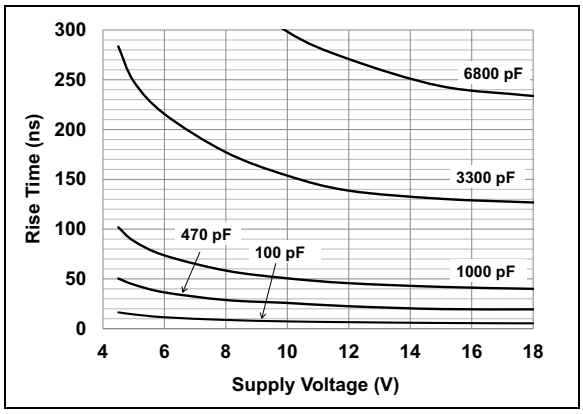


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

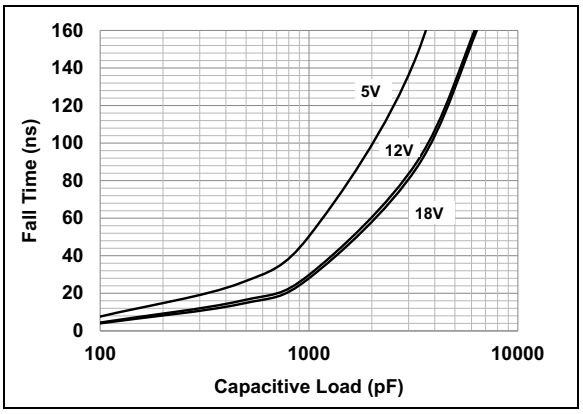


FIGURE 2-4: *Fall Time vs. Capacitive Load.*

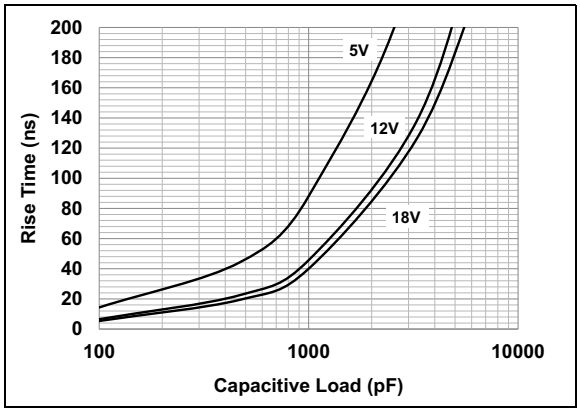


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

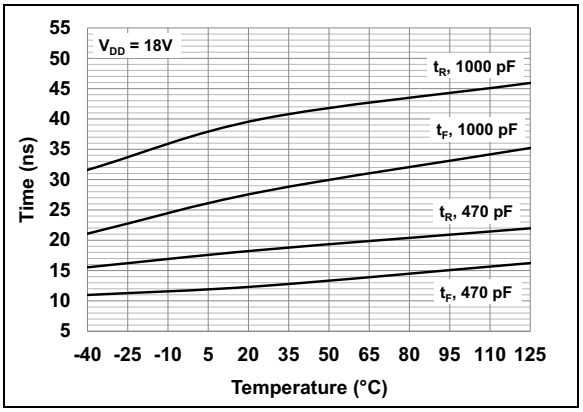


FIGURE 2-5: *Rise and Fall Time vs. Temperature.*

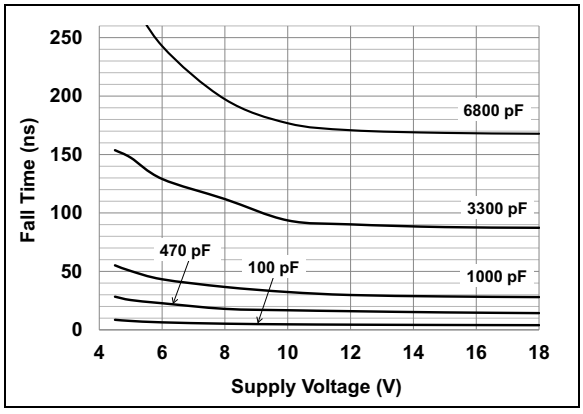


FIGURE 2-3: *Fall Time vs. Supply Voltage.*

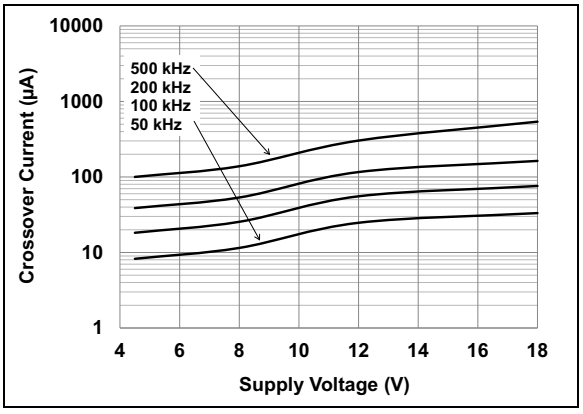


FIGURE 2-6: *Crossover Current vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

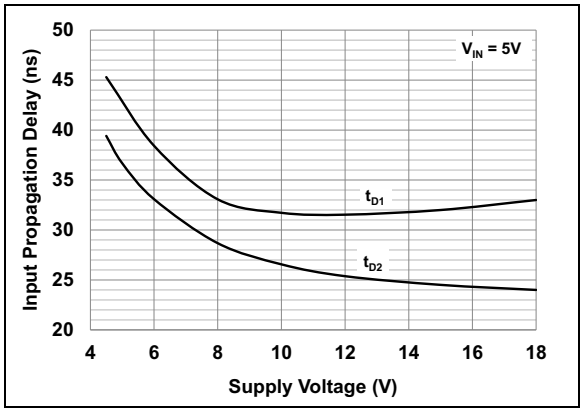


FIGURE 2-7: *Input Propagation Delay vs. Supply Voltage.*

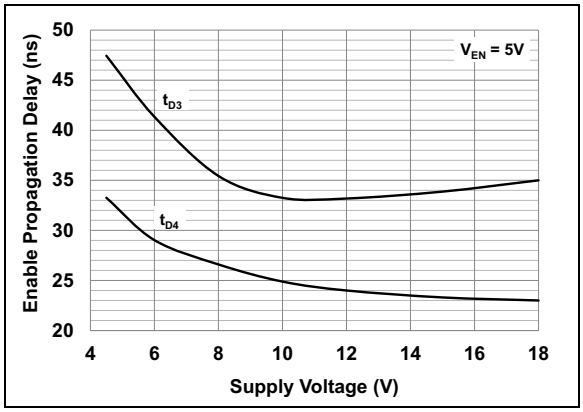


FIGURE 2-10: *Enable Propagation Delay vs. Supply Voltage.*

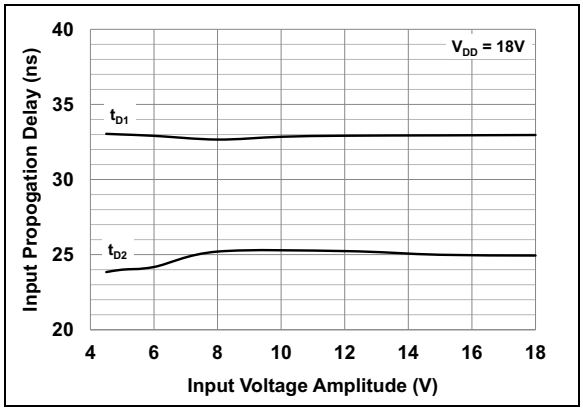


FIGURE 2-8: *Input Propagation Delay Time vs. Input Amplitude.*

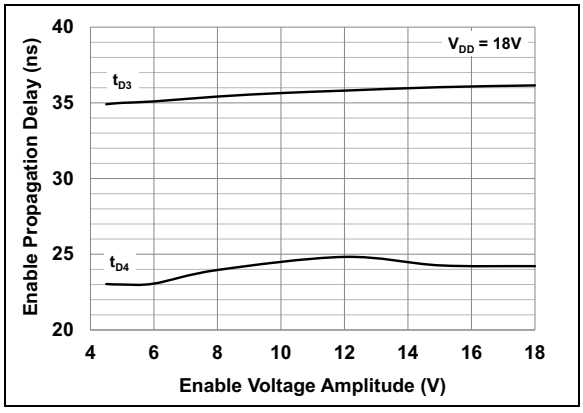


FIGURE 2-11: *Enable Propagation Delay Time vs. Enable Voltage Amplitude.*

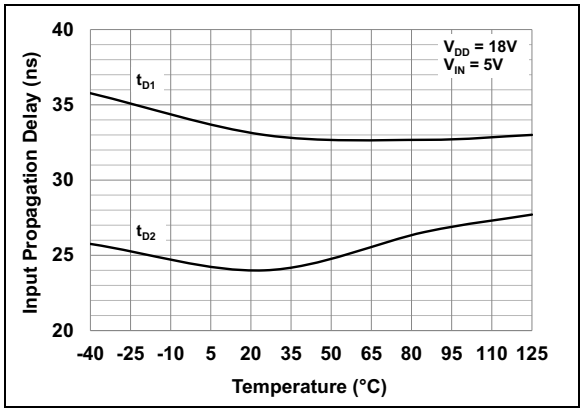


FIGURE 2-9: *Input Propagation Delay vs. Temperature.*

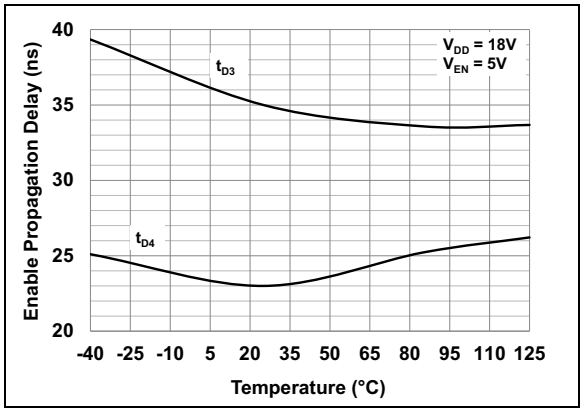


FIGURE 2-12: *Enable Propagation Delay vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

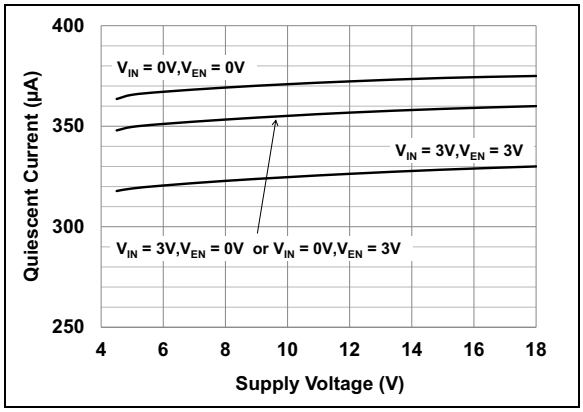


FIGURE 2-13: *Quiescent Supply Current vs. Supply Voltage.*

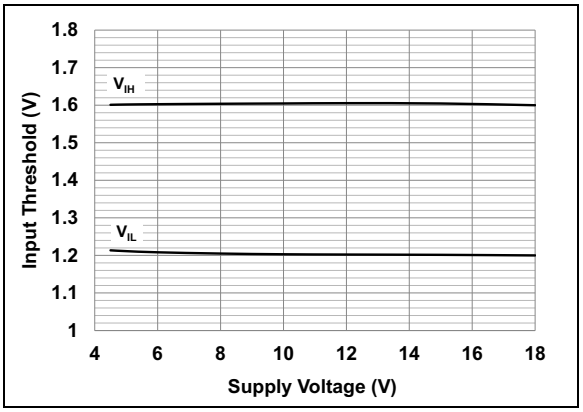


FIGURE 2-16: *Input Threshold vs Supply Voltage.*

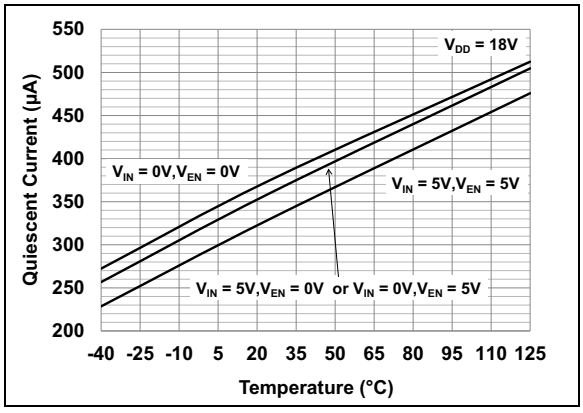


FIGURE 2-14: *Quiescent Supply Current vs. Temperature.*

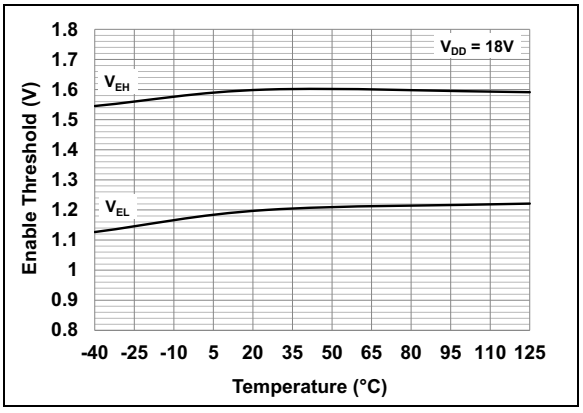


FIGURE 2-17: *Enable Threshold vs. Temperature.*

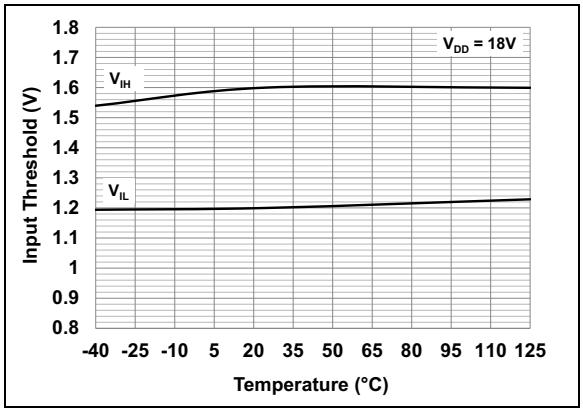


FIGURE 2-15: *Input Threshold vs. Temperature.*

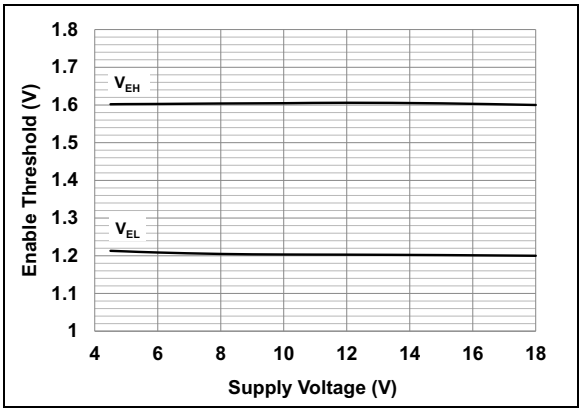


FIGURE 2-18: *Enable Threshold vs Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

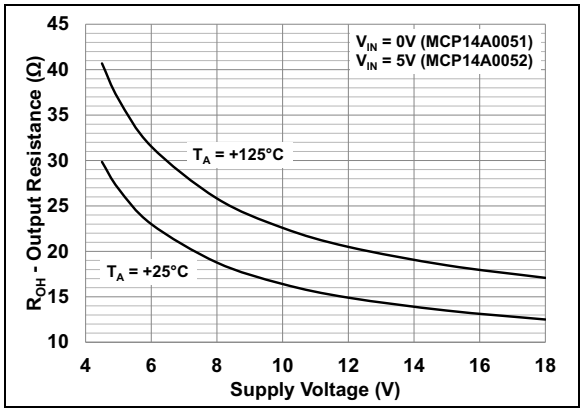


FIGURE 2-19: *Output Resistance (Output High) vs. Supply Voltage.*

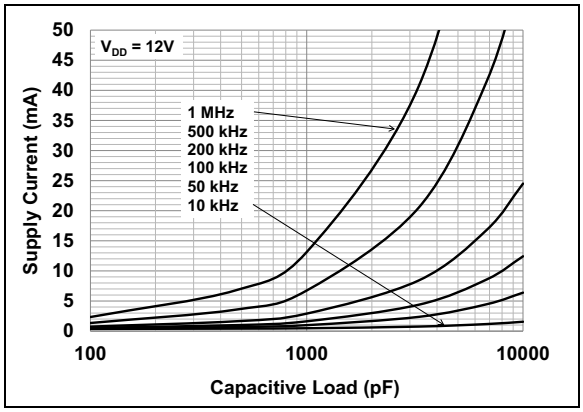


FIGURE 2-22: *Supply Current vs. Capacitive Load (V_{DD} = 12V).*

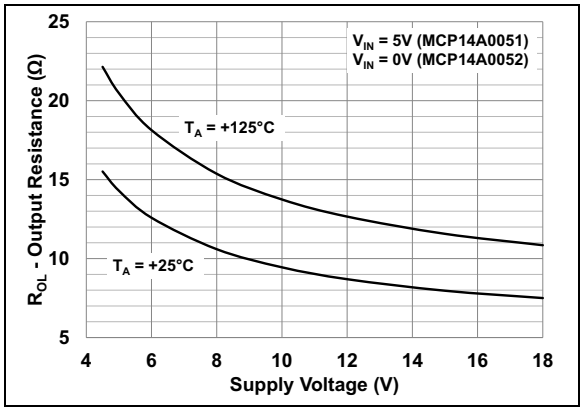


FIGURE 2-20: *Output Resistance (Output Low) vs. Supply Voltage.*

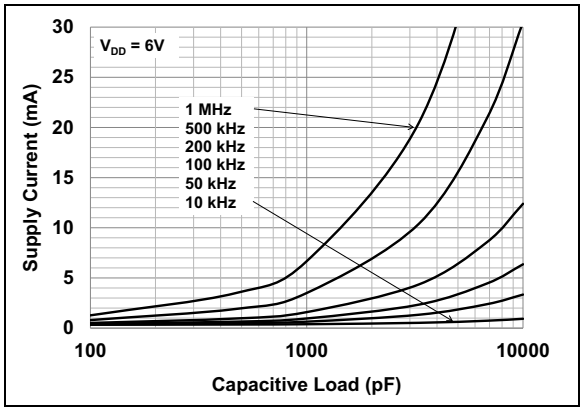


FIGURE 2-23: *Supply Current vs. Capacitive Load (V_{DD} = 6V).*

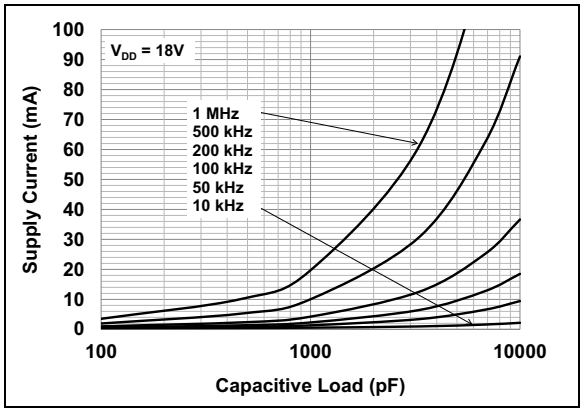


FIGURE 2-21: *Supply Current vs. Capacitive Load (V_{DD} = 18V).*

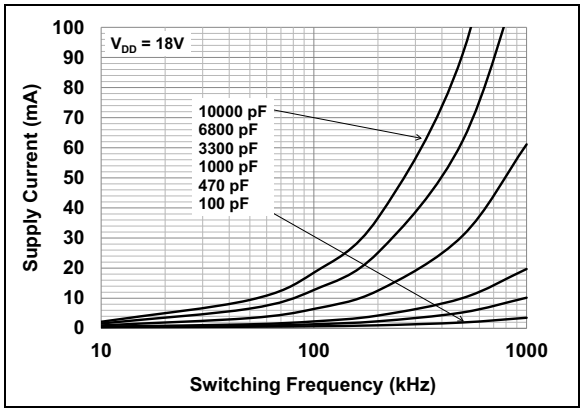


FIGURE 2-24: *Supply Current vs. Frequency (V_{DD} = 18V).*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V.

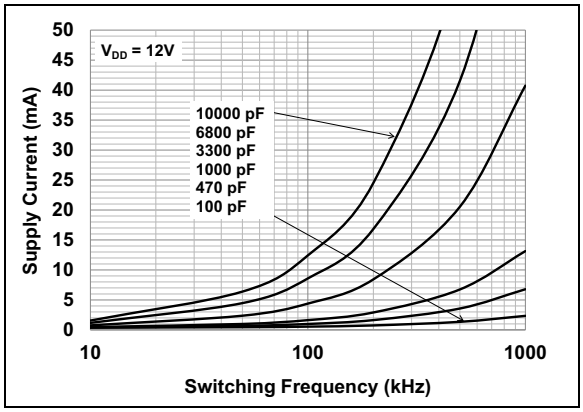


FIGURE 2-25: *Supply Current vs. Frequency (V_{DD} = 12V).*

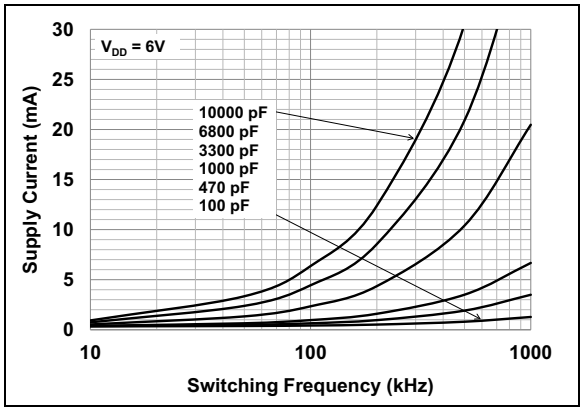


FIGURE 2-26: *Supply Current vs. Frequency (V_{DD} = 6V).*

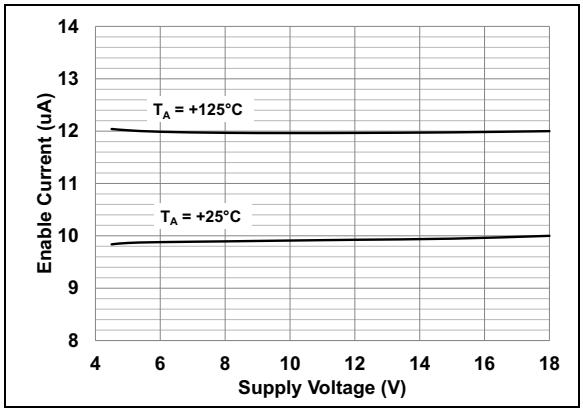


FIGURE 2-27: *Enable Current vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.		Symbol	Description
6L 2x2 DFN	6L SOT-23		
1	6	$\overline{OUT}$/OUT	Push-Pull Output
2	5	GND	Power Ground
3	4	EN	Device Enable
4	2	A_{GND}	Analog Ground
5	3	IN	Control Input
6	1	V_{DD}	Supply Input
EP	—	EP	Exposed Thermal Pad (GND)

3.1 Output Pin (OUT, $\overline{OUT}$)

The Output is a CMOS push-pull output that is capable of sourcing and sinking 0.5A of peak current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET stays in the intended state even during large transients. This output also has a reverse current latch-up rating of 500 mA.

3.2 Power Ground Pin (GND)

GND is the device return pin for the output stage. The GND pin should have a low-impedance connection to the bias supply source return. When the capacitive load is being discharged, high peak currents will flow out of the ground pin.

3.3 Device Enable Pin (EN)

The MOSFET driver Device Enable is a high-impedance, TTL/CMOS compatible input. The Enable input also has hysteresis between the high and low-input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity. Driving the Enable pin below the threshold will disable the output of the device, pulling $\overline{OUT}$/OUT low, regardless of the status of the Input pin. Driving the Enable pin above the threshold allows normal operation of the $\overline{OUT}$/OUT pin based on the status of the Input pin. The Enable pin utilizes an internal pull up resistor, allowing the pin to be left floating for standard driver operation.

3.4 Analog Ground Pin (A_{GND})

AGND is the device return pin for the input and enable stages of the MOSFET driver. The AGND pin should be connected to an electrically “quiet” ground node to provide a low noise reference for the input and enable pins.

3.5 Control Input Pin (IN)

The MOSFET driver Control Input is a high-impedance, TTL/CMOS compatible input. The Input also has hysteresis between the high and low-input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity.

3.6 Supply Input Pin (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

3.7 Exposed Metal Pad Pin (EP)

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane, or other copper plane on a printed circuit board, to aid in heat removal from the package.

4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high peak currents to charge/discharge the gate capacitance of external MOSFETs or Insulated-Gate Bipolar Transistors (IGBTs). In high-frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver such as the MCP14A0051/2 family can be used to provide additional source/sink current capability.

4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully-off state to a fully-on state is characterized by the driver's rise time (t_R), fall time (t_F) and propagation delays (t_{D1} and t_{D2}). Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP14A0051/2 timing.

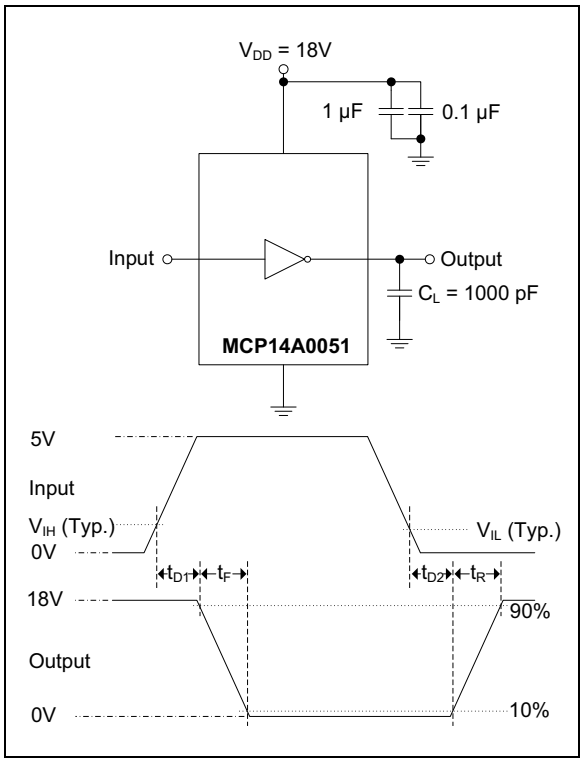


FIGURE 4-1: *Inverting Driver Timing Waveform.*

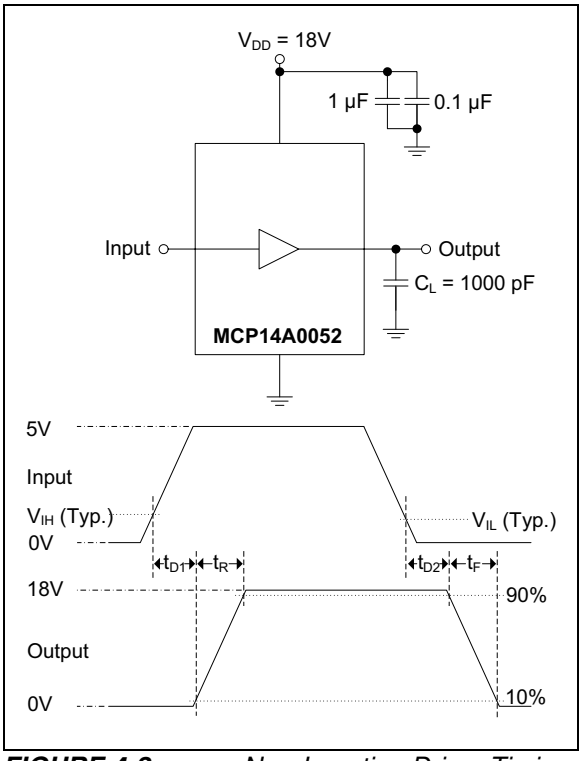


FIGURE 4-2: *Non-Inverting Driver Timing Waveform.*

4.3 Enable Function

The enable pin (EN) provides additional control of the output pin (OUT).This pin is active high and is internally pulled up to V_{DD} so that the pin can be left floating to provide standard MOSFET driver operation.

When the enable pin's voltage is above the Enable pin high-voltage threshold, (V_{EN_H}), the output is enabled and allowed to react to the status of the Input pin. However, when the voltage applied to the Enable pin falls below the low threshold voltage (V_{EN_L}), the driver output is disabled and doesn't respond to changes in the status of the Input pin. When the driver is disabled, the output is pulled down to a low state. Refer to Table 4-1 for enable pin logic. The threshold voltage levels for the Enable pin are similar to the threshold voltage levels of the Input pin, and are TTL and CMOS compatible. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays, t_{D3} and t_{D4}, are graphically represented in Figure 4-3.

TABLE 4-1: ENABLE PIN LOGIC

ENB	IN	MCP14A0051 OUT	MCP14A0052 OUT
H	H	L	H
H	L	H	L
L	X	L	L

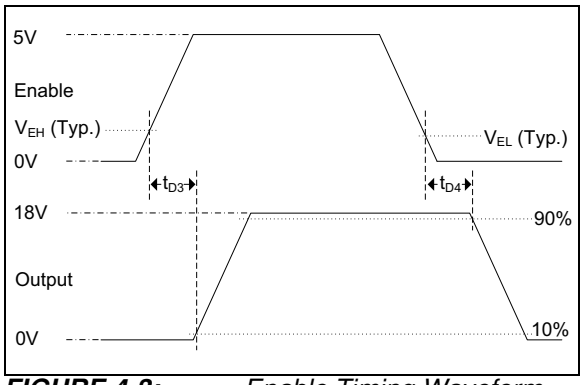


FIGURE 4-3: *Enable Timing Waveform.*

4.4 Decoupling Capacitors

Careful PCB layout and decoupling capacitors are required when using power MOSFET drivers. Large current is required to charge and discharge capacitive loads quickly. For example, approximately 720 mA are needed to charge a 1000 pF load with 18V in 25 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, it is recommended to place 1.0 µF and 0.1 µF low ESR ceramic capacitors in parallel between the driver V_{DD} and GND. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

4.5 PCB Layout Considerations

Proper Printed Circuit Board (PCB) layout is important in high-current, fast switching circuits to provide proper device operation and robustness of design. Improper component placement may cause errant switching, excessive voltage ringing or circuit latch-up. The PCB trace loop length and inductance should be minimized by the use of ground planes or traces under the MOSFET gate drive signal, separate analog and power grounds, and local driver decoupling.

Placing a ground plane beneath the MCP14A0051/2 devices will help as a radiated noise shield, as well as providing some heat sinking for power dissipated within the device.

4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements, as shown in Equation 4-1.

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

P_T	=	Total power dissipation
P_L	=	Load power dissipation
P_Q	=	Quiescent power dissipation
P_{CC}	=	Operating power dissipation

4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of the frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is shown in Equation 4-2.

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

f	=	Switching frequency
C_T	=	Total load capacitance
V_{DD}	=	MOSFET driver supply voltage

4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends on the state of the Input and Enable pins. Refer to **Section 1.0 "Electrical Characteristics"** for typical quiescent current draw values in different operating states. The quiescent power dissipation is shown in Equation 4-3.

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

I_{QH}	=	Quiescent current in the High state
D	=	Duty cycle
I_{QL}	=	Quiescent current in the Low state
V_{DD}	=	MOSFET driver supply voltage

4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions because, for a very short period of time, both MOSFETs in the output stage are on simultaneously. This cross-conduction current leads to a power dissipation described in Equation 4-4.

EQUATION 4-4:

$$P_{CC} = CC \times f \times V_{DD}$$

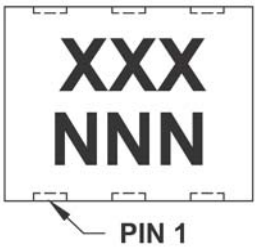
Where:

CC	=	Cross-Conduction constant (Ampere x second)
f	=	Switching frequency
V_{DD}	=	MOSFET driver supply voltage

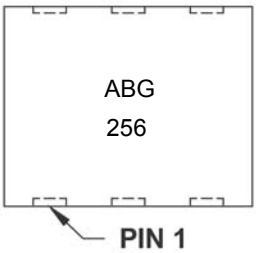
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

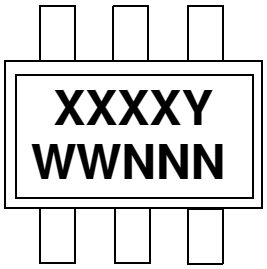
6-Lead DFN (2x2x0.9 mm)



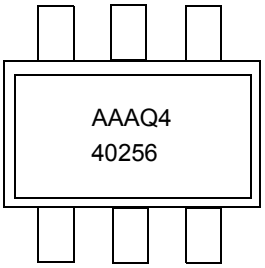
Example



6-Lead SOT-23



Example



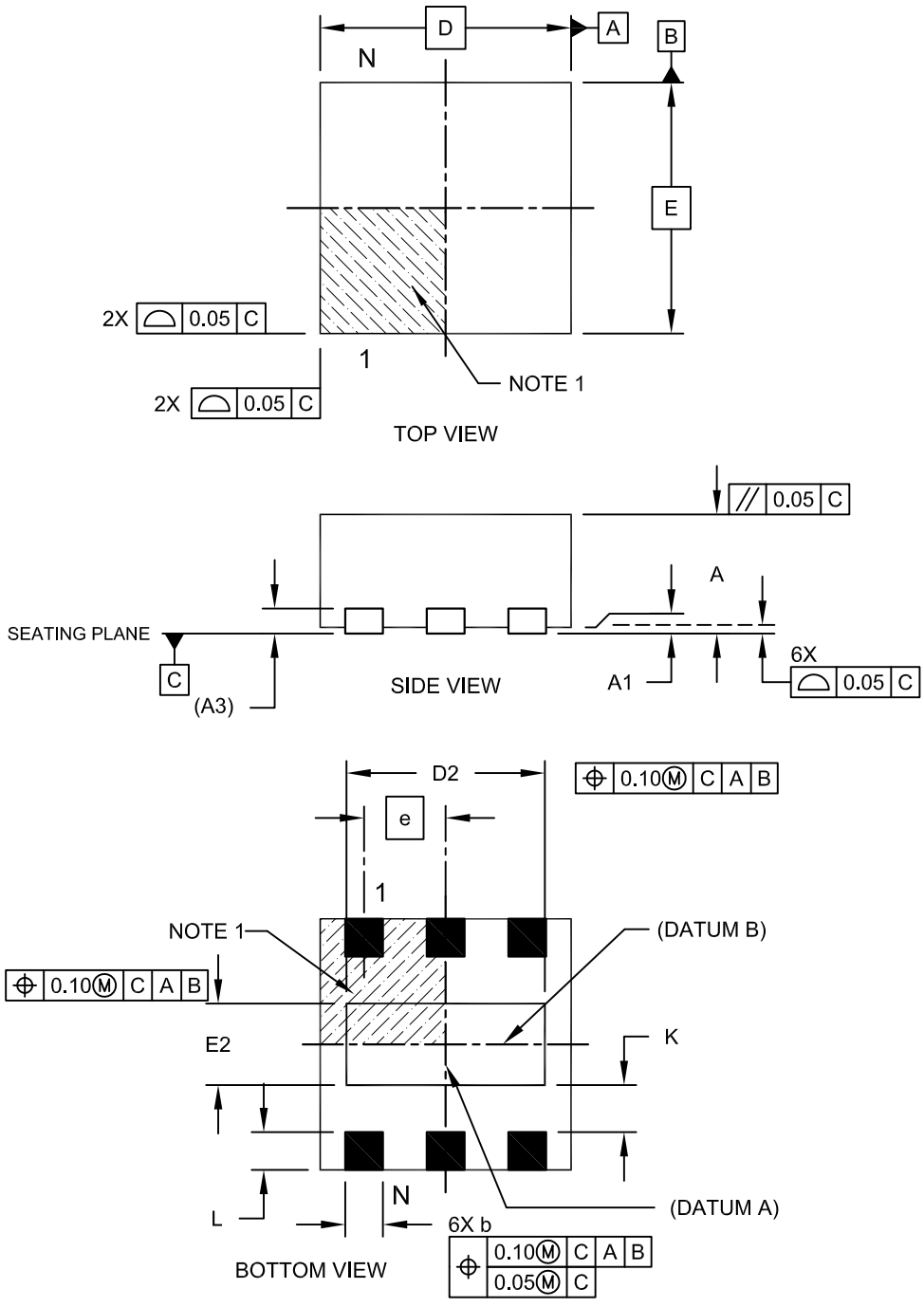
Standard Markings for SOT-23	
Part Number	**Code**
MCP14A0051T-E/MAY	ABG
MCP14A0052T-E/MAY	ABH
MCP14A0051T-E/CH	AAAQY
MCP14A0052T-E/CH	AAARY

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

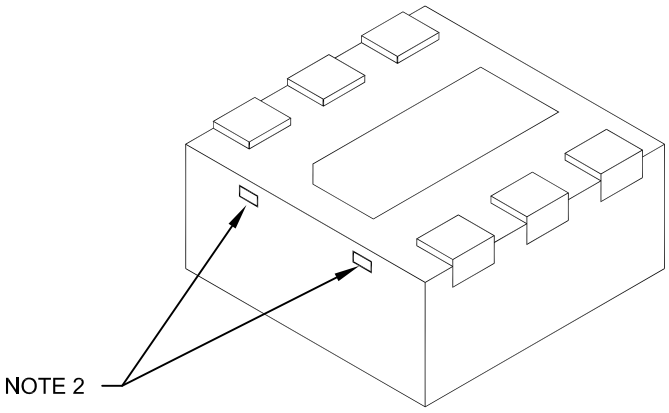
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-120C Sheet 1 of 2

6-Lead Plastic Dual Flat, No Lead Package (MA[Y]) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		2.00 BSC	
Exposed Pad Length	D2	1.50	1.60	1.70
Exposed Pad Width	E2	0.90	1.00	1.10
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

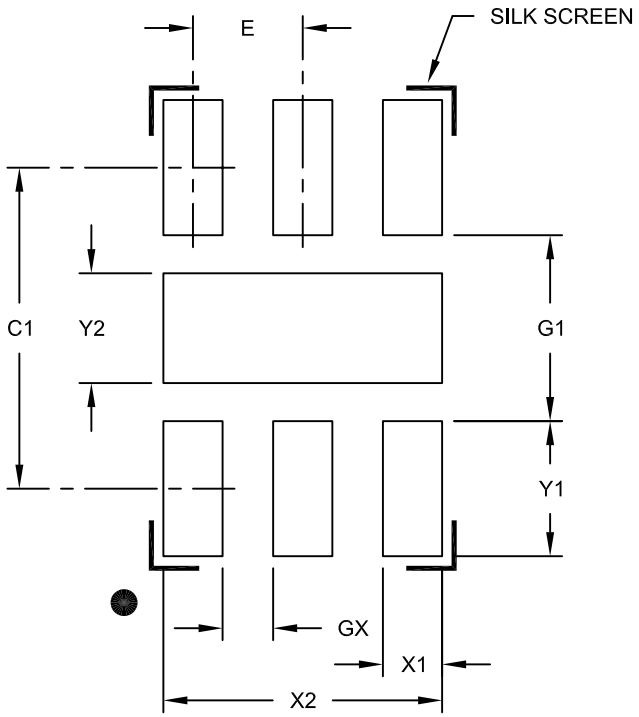
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-120C Sheet 2 of 2

6-Lead Plastic Dual Flat, No Lead Package (MA) - 2x2x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	Y2			1.00
Optional Center Pad Length	X2			1.70
Contact Pad Spacing	C1		2.10	
Contact Pad Width (X6)	X1			0.35
Contact Pad Length (X6)	Y1			0.65
Distance Between Pads	GX	0.20		
Distance Between Pads	G1	1.10		

Notes:

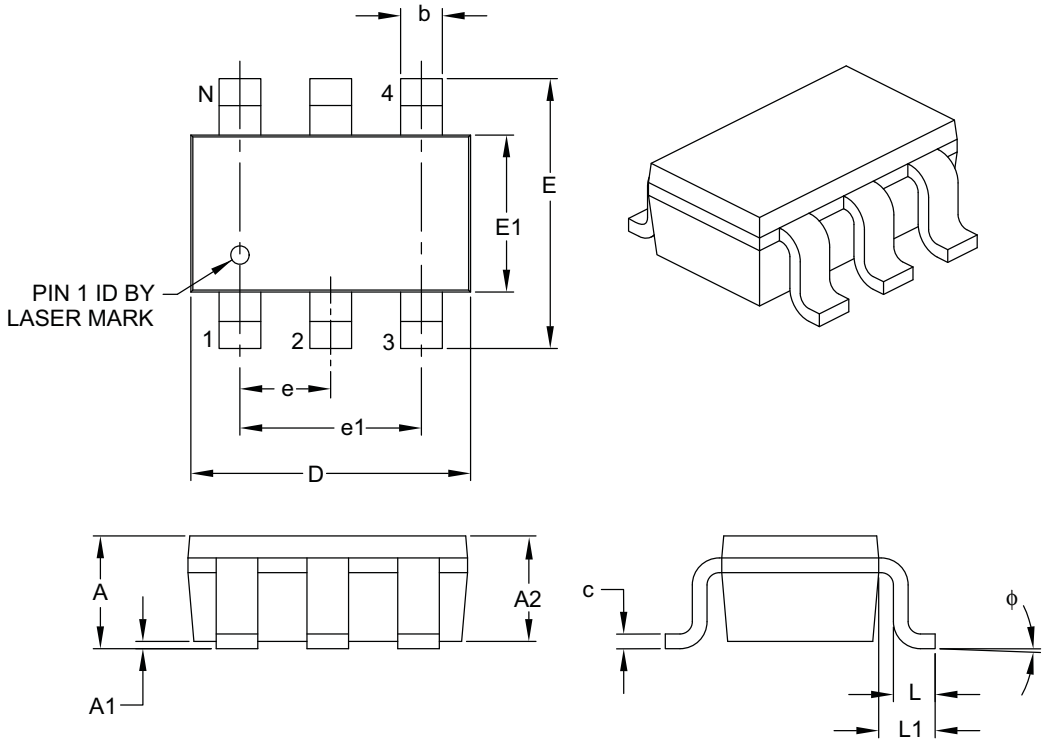
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2120A

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		6	
Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

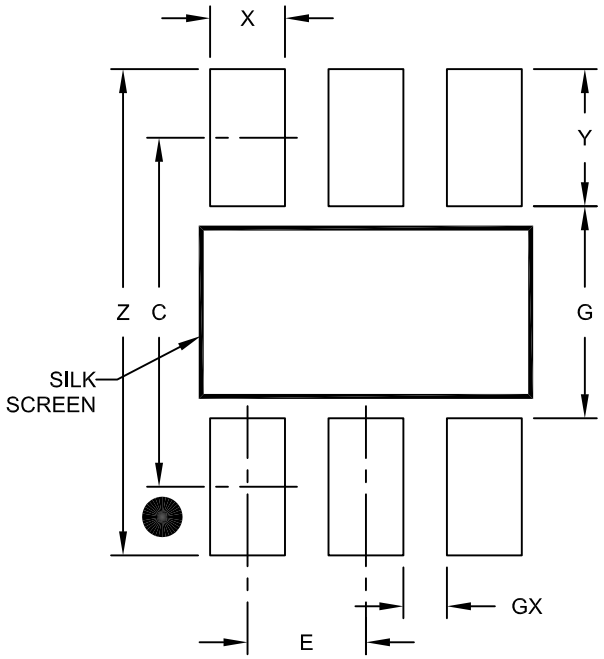
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (CH) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

APPENDIX A: REVISION HISTORY

Revision A (December 2014)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	–X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP14A0051T: High-Speed MOSFET Driver (Tape and Reel) MCP14A0052T: High-Speed MOSFET Driver (Tape and Reel)
Temperature Range:	E = -40°C to +125°C (Extended)
Package:	CH = Plastic Small Outline Transistor (SOT-23), 6-lead MAY = Plastic Dual Flat, No Lead Package - 2 x 2 x 0.9 mm Body (DFN) 6-lead

Examples:

a) MCP14A0051T-E/CH: Tape and Reel, Extended temperature, 6LD SOT-23 package

a) MCP14A0052T-E/MAY: Tape and Reel Extended temperature, 6LD DFN package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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