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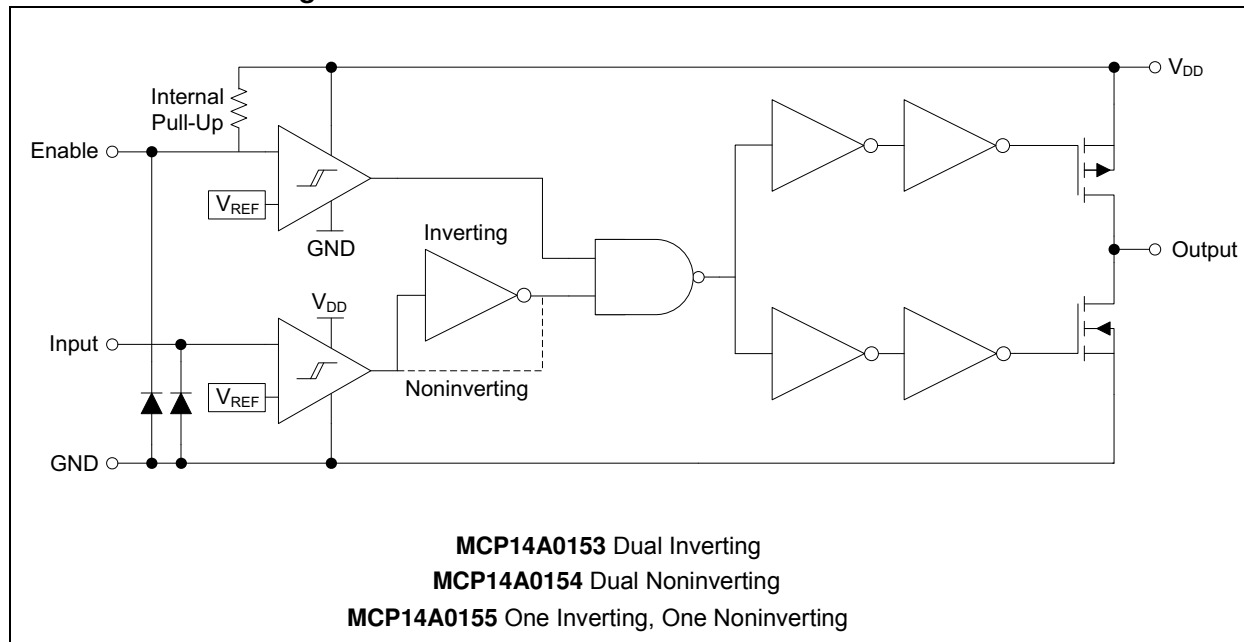
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MCP14A0153/4/5

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V _{DD} , Supply Voltage.....	+20V
V _{IN} , Input Voltage.....	(V _{DD} + 0.3V) to (GND - 0.3V)
V _{EN} , Enable Voltage.....	(V _{DD} + 0.3V) to (GND - 0.3V)
Package Power Dissipation (T _A = +50°C)	
8L MSOP	0.63W
8L SOIC	1.00W
8L 2 x 3 TDFN.....	1.86W
ESD Protection on all Pins	2 kV (HBM)
.....	200V (MM)

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T _A = +25°C, with 4.5V ≤ V _{DD} ≤ 18V.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V _{IN}	GND - 0.3	—	V _{DD} + 0.3	V	
Logic '1' High Input Voltage	V _{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V _{IL}	—	1.2	0.8	V	
Input Voltage Hysteresis	V _{HYST(IN)}	—	0.4	—	V	
Input Current	I _{IN}	-1	—	+1	μA	0V ≤ V _{IN} ≤ V _{DD}
Enable						
Enable Voltage Range	V _{EN}	GND - 0.3V	—	V _{DD} + 0.3	V	
Logic '1' High Enable Voltage	V _{EH}	2	1.6	—	V	
Logic '0' Low Enable Voltage	V _{EL}	—	1.2	0.8	V	
Enable Voltage Hysteresis	V _{HYST(EN)}	—	0.4	—	V	
Enable Pin Pull-Up Resistance	R _{ENBL}	—	1.8	—	MΩ	V _{DD} = 18V, EN = GND
Enable Input Current	I _{EN}	—	10	—	μA	V _{DD} = 18V, EN = GND
Propagation Delay	t _{D3}	—	25	32	ns	V _{DD} = 18V, V _{EN} = 5V, see Figure 4-3, (Note 1)
Propagation Delay	t _{D4}	—	24	31	ns	V _{DD} = 18V, V _{EN} = 5V, see Figure 4-3, (Note 1)
Output						
High Output Voltage	V _{OH}	V _{DD} - 0.025	—	—	V	I _{OUT} = 0A
Low Output Voltage	V _{OL}	—	—	0.025	V	I _{OUT} = 0A
Output Resistance, High	R _{OH}	—	4.5	6.5	Ω	I _{OUT} = 10 mA, V _{DD} = 18V
Output Resistance, Low	R _{OL}	—	3.0	4.5	Ω	I _{OUT} = 10 mA, V _{DD} = 18V
Peak Output Current	I _{PK}	—	1.5	—	A	V _{DD} = 18V (Note 1)
Latch-Up Protection Withstand Reverse Current	I _{REV}	0.5	—	—	A	Duty cycle ≤ 2%, t ≤ 300 μs (Note 1)
Switching Time (Note 1)						
Rise Time	t _R	—	11.5	18.5	ns	V _{DD} = 18V, C _L = 1000 pF, see Figure 4-1, Figure 4-2 (Note 1)

Note 1: Tested during characterization, not production tested.

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DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $T_A = +25^\circ\text{C}$, with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Fall Time	t_F	—	10	17	ns	$V_{DD} = 18\text{V}$, $C_L = 1000\text{ pF}$, see Figure 4-1, Figure 4-2 (Note 1)
Delay Time	t_{D1}	—	25	32	ns	$V_{DD} = 18\text{V}$, $V_{IN} = 5\text{V}$, see Figure 4-1, Figure 4-2 (Note 1)
	t_{D2}	—	24	31	ns	$V_{DD} = 18\text{V}$, $V_{IN} = 5\text{V}$, see Figure 4-1, Figure 4-2 (Note 1)
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	675	1120	μA	$V_{INA/B} = 3\text{V}$, $V_{ENA/B} = 3\text{V}$
	I_{DD}	—	715	1160	μA	$V_{INA/B} = 0\text{V}$, $V_{ENA/B} = 3\text{V}$
	I_{DD}	—	715	1160	μA	$V_{INA/B} = 3\text{V}$, $V_{ENA/B} = 0\text{V}$
	I_{DD}	—	750	1200	μA	$V_{INA/B} = 0\text{V}$, $V_{ENA/B} = 0\text{V}$

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE) (Note 1)

Electrical Specifications: Unless otherwise indicated, over the operating range with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage Range	V_{IN}	GND - 0.3V	—	$V_{DD} + 0.3$	V	
Logic '1' High Input Voltage	V_{IH}	2.0	1.6	—	V	
Logic '0' Low Input Voltage	V_{IL}	—	1.2	1.8	V	
Input Voltage Hysteresis	$V_{HYST(IN)}$	—	0.4	—	V	
Input Current	I_{IN}	-10	—	+10	μA	$0\text{V} \leq V_{IN} \leq V_{DD}$
Enable						
Enable Voltage Range	V_{EN}	GND - 0.3V	—	$V_{DD} + 0.3$	V	
Logic '1' High Enable Voltage	V_{EH}	2.0	1.6	—	V	
Logic '0' Low Enable Voltage	V_{EL}	—	1.2	1.8	V	
Enable Voltage Hysteresis	$V_{HYST(EN)}$	—	0.4	—	V	
Enable Input Current	I_{EN}	—	12	—	μA	$V_{DD} = 18\text{V}$, $EN = \text{GND}$
Propagation Delay	t_{D3}	—	28	35	ns	$V_{DD} = 18\text{V}$, $V_{EN} = 5\text{V}$, $T_A = +125^\circ\text{C}$, see Figure 4-3
Propagation Delay	t_{D4}	—	27	34	ns	$V_{DD} = 18\text{V}$, $V_{EN} = 5\text{V}$, $T_A = +125^\circ\text{C}$, see Figure 4-3
Output						
High Output Voltage	V_{OH}	$V_{DD} - 0.025$	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance, High	R_{OH}	—	—	9	Ω	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18\text{V}$
Output Resistance, Low	R_{OL}	—	—	6.5	Ω	$I_{OUT} = 10\text{ mA}$, $V_{DD} = 18\text{V}$

Note 1: Tested during characterization, not production tested.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE) (Note 1)

Electrical Specifications: Unless otherwise indicated, over the operating range with $4.5V \leq V_{DD} \leq 18V$.						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Switching Time (Note 1)						
Rise Time	t_R	—	14	21	ns	$V_{DD} = 18V$, $C_L = 1000$ pF, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
Fall Time	t_F	—	13	20	ns	$V_{DD} = 18V$, $C_L = 1000$ pF, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
Delay Time	t_{D1}	—	28	35	ns	$V_{DD} = 18V$, $V_{IN} = 5V$, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
	t_{D2}	—	27	34		$V_{DD} = 18V$, $V_{IN} = 5V$, $T_A = +125^\circ C$, see Figure 4-1, Figure 4-2
Power Supply						
Supply Voltage	V_{DD}	4.5	—	18	V	
Power Supply Current	I_{DD}	—	—	1520	μA	$V_{IN} = 3V$, $V_{EN} = 3V$
	I_{DD}	—	—	1560	μA	$V_{IN} = 0V$, $V_{EN} = 3V$
	I_{DD}	—	—	1560	μA	$V_{IN} = 3V$, $V_{EN} = 0V$
	I_{DD}	—	—	1600	μA	$V_{IN} = 0V$, $V_{EN} = 0V$

Note 1: Tested during characterization, not production tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$.							
Parameter	Sym.	Min.	Typ.	Max.	Units	Comments	
Temperature Ranges							
Specified Temperature Range	T_A	-40	—	+125	$^\circ C$		
Maximum Junction Temperature	T_J	—	—	+150	$^\circ C$		
Storage Temperature Range	T_A	-65	—	+150	$^\circ C$		
Package Thermal Information							
Junction-to-Ambient Thermal Resistance, 8LD MSOP	θ_{JA}	—	158	—	$^\circ C/W$	Note 1	
Junction-to-Ambient Thermal Resistance, 8LD SOIC	θ_{JA}	—	99.8	—	$^\circ C/W$	Note 1	
Junction-to-Ambient Thermal Resistance, 8LD TDFN	θ_{JA}	—	53.7	—	$^\circ C/W$	Note 1	
Junction-to-Top Characterization Parameter, 8LD MSOP	Ψ_{JT}	—	2.4	—	$^\circ C/W$	Note 1	
Junction-to-Top Characterization Parameter, 8LD SOIC	Ψ_{JT}	—	5.9	—	$^\circ C/W$	Note 1	
Junction-to-Top Characterization Parameter, 8LD TDFN	Ψ_{JT}	—	0.5	—	$^\circ C/W$	Note 1	
Junction-to-Board Characterization Parameter, 8LD MSOP	Ψ_{JB}	—	115.2	—	$^\circ C/W$	Note 1	
Junction-to-Board Characterization Parameter, 8LD SOIC	Ψ_{JB}	—	64.8	—	$^\circ C/W$	Note 1	
Junction-to-Board Characterization Parameter, 8LD TDFN	Ψ_{JB}	—	24.4	—	$^\circ C/W$	Note 1	

Note 1: Parameter is determined using a High K 2S2P 4-Layer board as described in JESD 51-7, as well as JESD 51-5 for packages with exposed pads.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

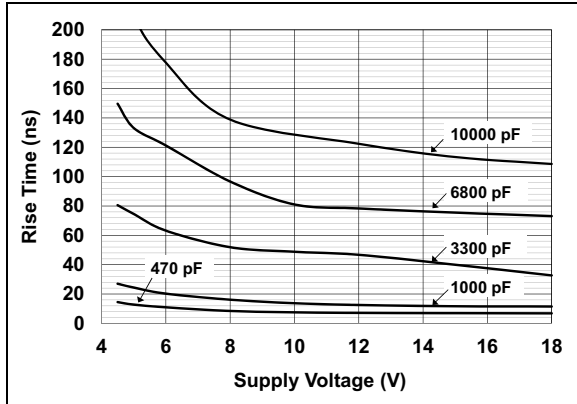


FIGURE 2-1: Rise Time vs. Supply Voltage.

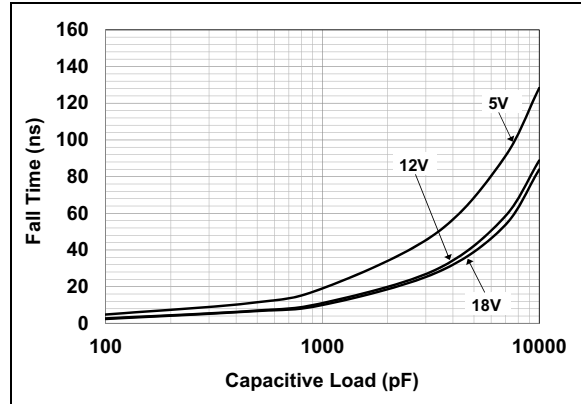


FIGURE 2-4: Fall Time vs. Capacitive Load.

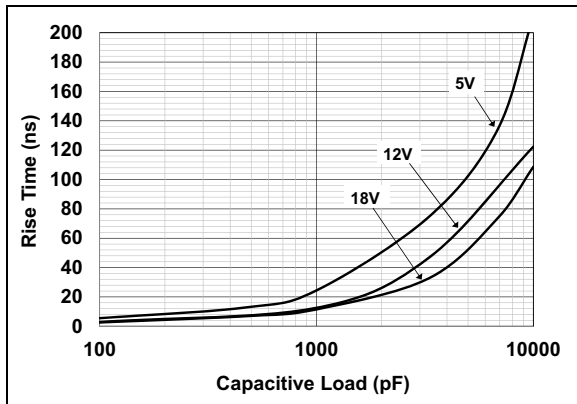


FIGURE 2-2: Rise Time vs. Capacitive Load.

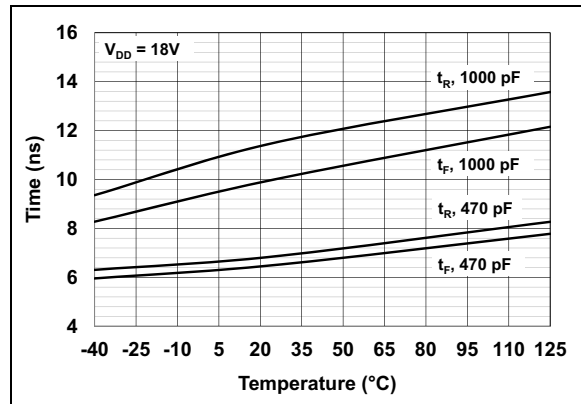


FIGURE 2-5: Rise and Fall Time vs. Temperature.

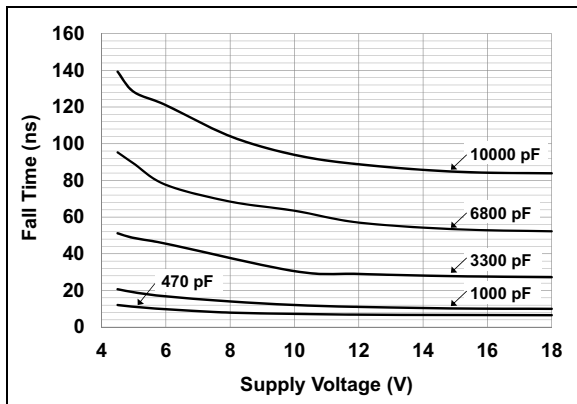


FIGURE 2-3: Fall Time vs. Supply Voltage.

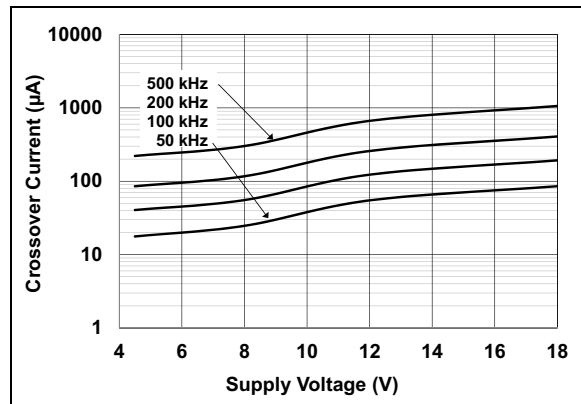


FIGURE 2-6: Crossover Current vs. Supply Voltage.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

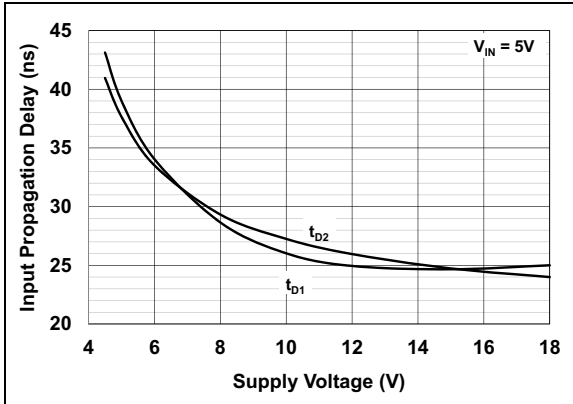


FIGURE 2-7: Input Propagation Delay vs. Supply Voltage.

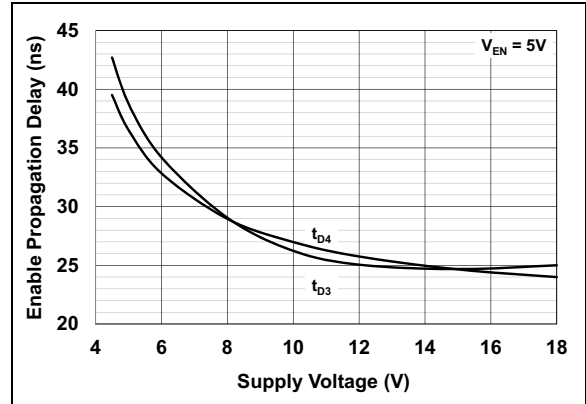


FIGURE 2-10: Enable Propagation Delay vs. Supply Voltage.

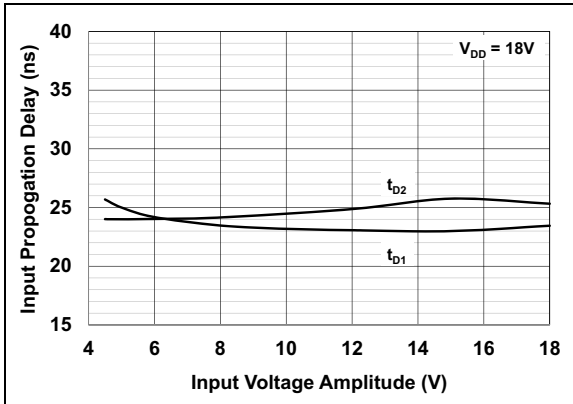


FIGURE 2-8: Input Propagation Delay Time vs. Input Amplitude.

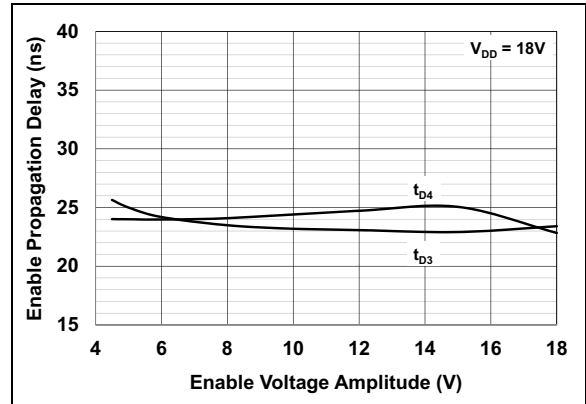


FIGURE 2-11: Enable Propagation Delay Time vs. Enable Voltage Amplitude.

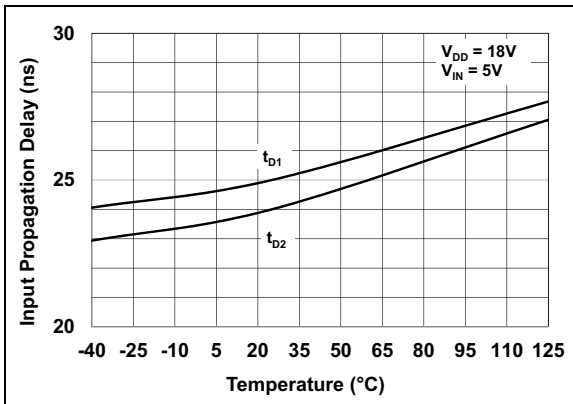


FIGURE 2-9: Input Propagation Delay vs. Temperature.

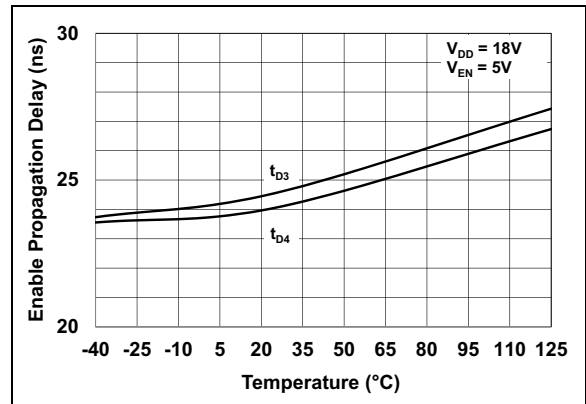


FIGURE 2-12: Enable Propagation Delay vs. Temperature.

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

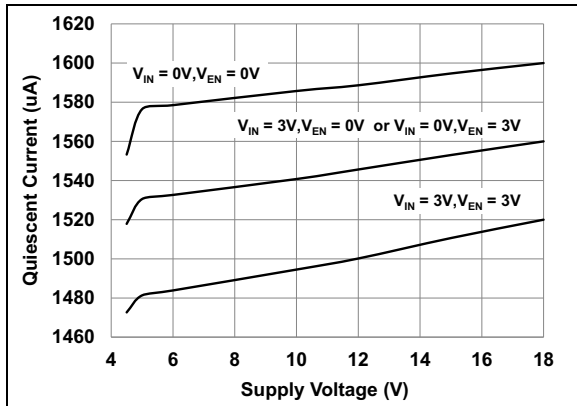


FIGURE 2-13: Quiescent Supply Current vs. Supply Voltage.

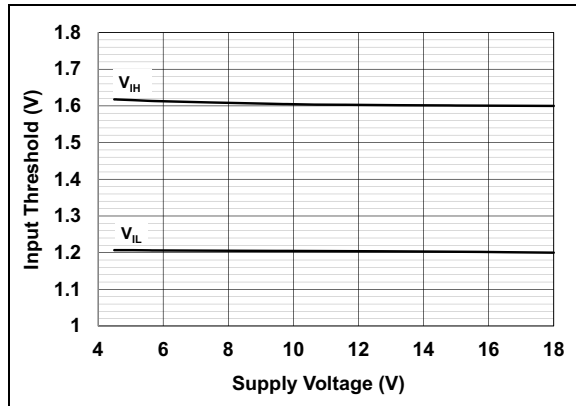


FIGURE 2-16: Input Threshold vs Supply Voltage.

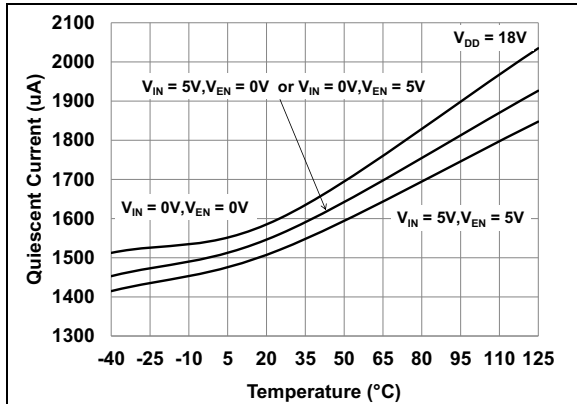


FIGURE 2-14: Quiescent Supply Current vs. Temperature.

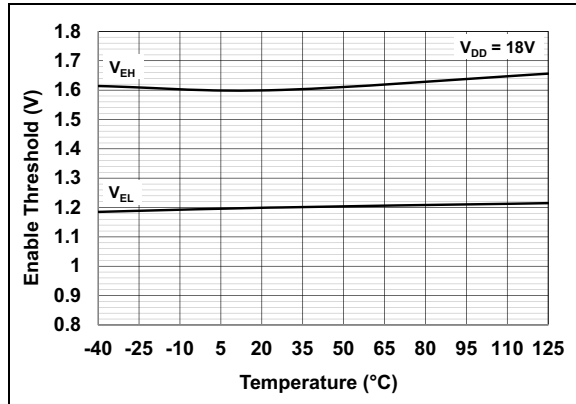


FIGURE 2-17: Enable Threshold vs. Temperature.

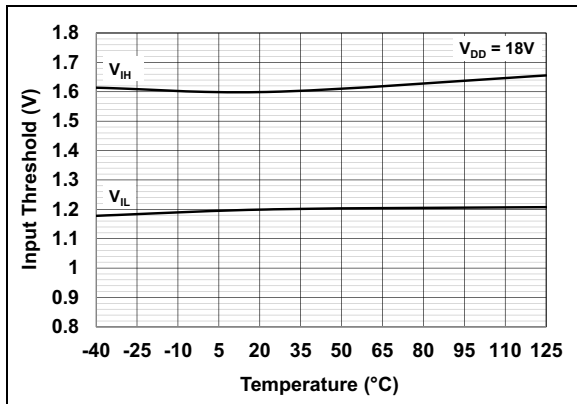


FIGURE 2-15: Input Threshold vs. Temperature.

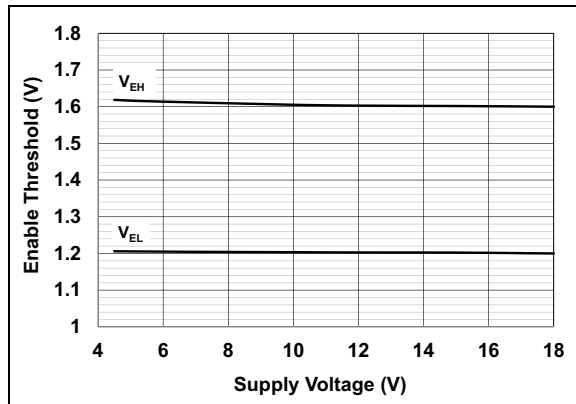


FIGURE 2-18: Enable Threshold vs Supply Voltage.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

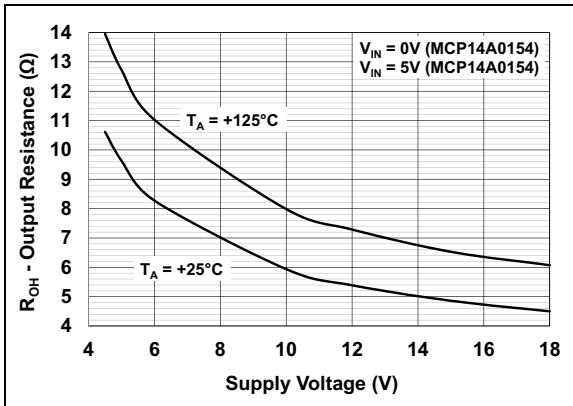


FIGURE 2-19: Output Resistance (Output High) vs. Supply Voltage.

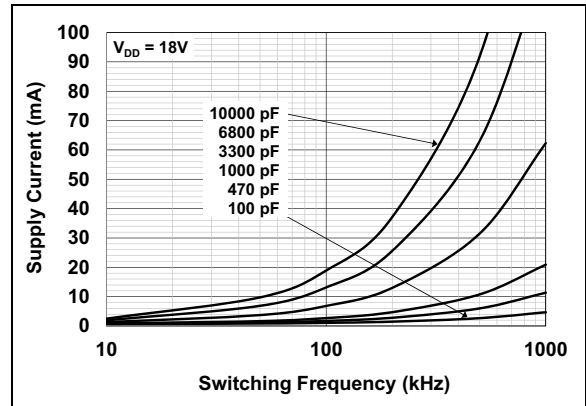


FIGURE 2-22: Supply Current vs. Capacitive Load ($V_{DD} = 12\text{V}$).

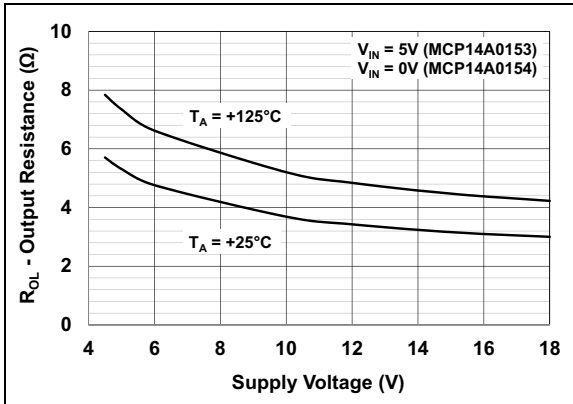


FIGURE 2-20: Output Resistance (Output Low) vs. Supply Voltage.

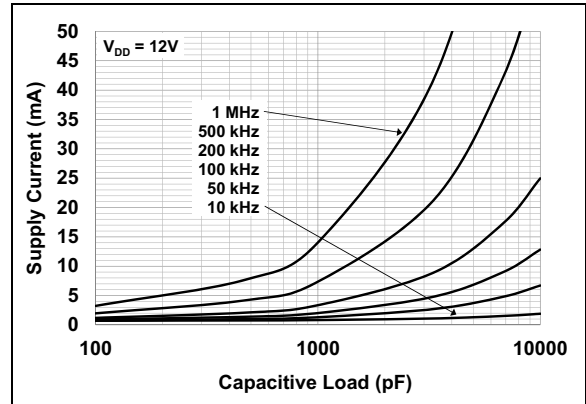


FIGURE 2-23: Supply Current vs. Capacitive Load ($V_{DD} = 6\text{V}$).

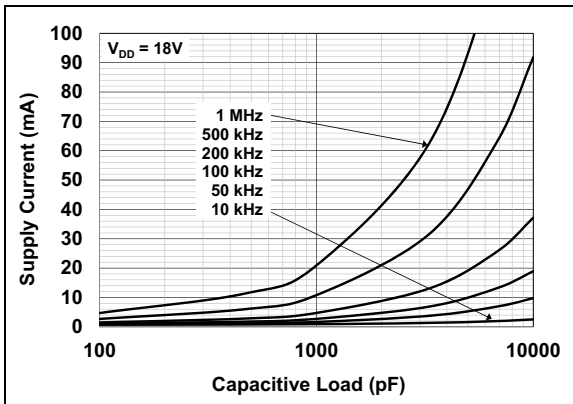


FIGURE 2-21: Supply Current vs. Capacitive Load ($V_{DD} = 18\text{V}$).

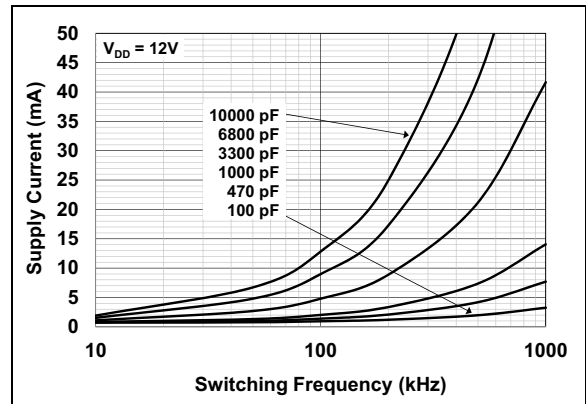


FIGURE 2-24: Supply Current vs. Frequency ($V_{DD} = 18\text{V}$).

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Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$ with $4.5\text{V} \leq V_{DD} \leq 18\text{V}$.

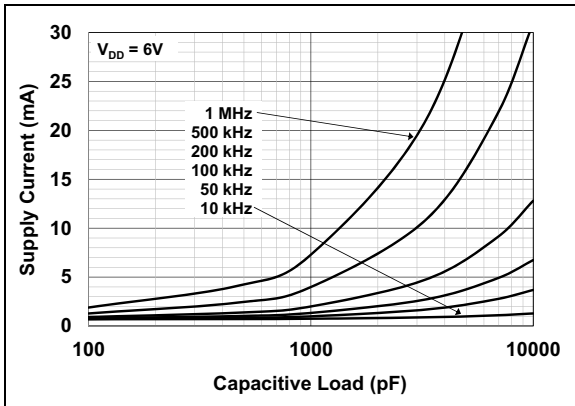


FIGURE 2-25: Supply Current vs. Frequency ($V_{DD} = 12\text{V}$).

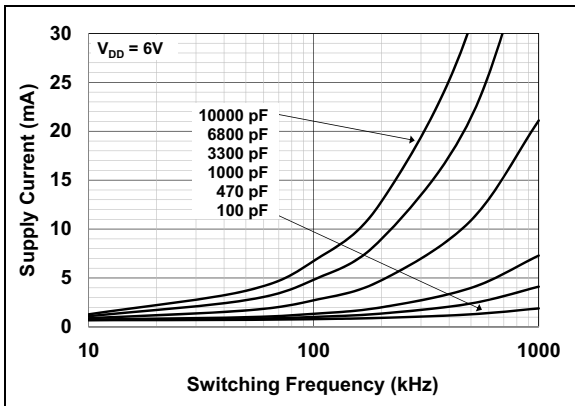


FIGURE 2-26: Supply Current vs. Frequency ($V_{DD} = 6\text{V}$).

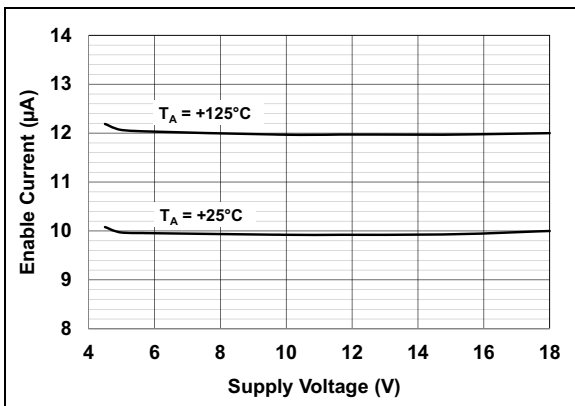


FIGURE 2-27: Enable Current vs. Supply Voltage.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

MCP14A0153, MCP14A0153, MCP14A0153		Symbol	Description
2x3 TDFN	MSOP/SOIC		
1	1	EN A	Enable - Channel A
2	2	IN A	Input - Channel A
3	3	GND	Device Ground
4	4	IN B	Input - Channel B
5	5	$\overline{\text{OUT B}}/\text{OUT B}$	Output - Channel B
6	6	V_{DD}	Supply Input
7	7	$\overline{\text{OUT A}}/\text{OUT A}$	Output - Channel A
8	8	EN B	Enable - Channel B
EP	—	EP	Exposed Thermal Pad (GND)

3.1 Output Pins ($\overline{\text{OUT A}}/\text{OUT A}$, $\overline{\text{OUT B}}/\text{OUT B}$)

The outputs are CMOS push-pull circuits that are capable of sourcing and sinking 1.5A of peak current ($V_{DD} = 18V$). The low output impedance ensures the gate of the external MOSFET stays in the intended state even during large transients. This output also has a reverse current latch-up rating of 500 mA.

3.2 Device Ground Pin (GND)

GND is the device return pin for the input and output stages. The GND pin should have a low-impedance connection to the bias supply source return. When the capacitive load is being discharged, high peak currents will flow through the ground pin.

3.3 Device Enable Pins (EN A, EN B)

The MOSFET driver device enable pins are high-impedance inputs featuring low threshold levels. The enable inputs also have hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity. Driving the enable pins below the threshold will disable the corresponding output of the device, pulling $\overline{\text{OUT}}/\text{OUT}$ low, regardless of the status of the Input pin. Driving the enable pins above the threshold allows normal operation of the $\overline{\text{OUT}}/\text{OUT}$ pin based on the status of the Input pin. The enable pins utilize internal pull up resistors, allowing the pins to be left floating for standard driver operation.

3.4 Control Input Pins (IN A, IN B)

The MOSFET driver control inputs are high-impedance inputs featuring low threshold levels. The Inputs also have hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity.

3.5 Supply Input Pin (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are provided to the load.

3.6 Exposed Metal Pad Pin (EP)

The exposed metal pad of the TDFN package is internally connected to GND. Therefore, this pad should be connected to a Ground plane to aid in heat removal from the package.

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4.0 APPLICATION INFORMATION

4.1 General Information

MOSFET drivers are high-speed, high-current devices which are intended to source/sink high-peak currents that are intended to charge/discharge the gate capacitance of external MOSFETs or Insulated-Gate Bipolar Transistors (IGBTs). In high frequency switching power supplies, the Pulse-Width Modulation (PWM) controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver such as the MCP14A0153/4/5 family can be used to provide additional source/sink current capability.

4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully-off state to a fully-on state is characterized by the driver's rise time (t_R), fall time (t_F) and propagation delays (t_{D1} and t_{D2}). Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP14A0153/4/5 timing.

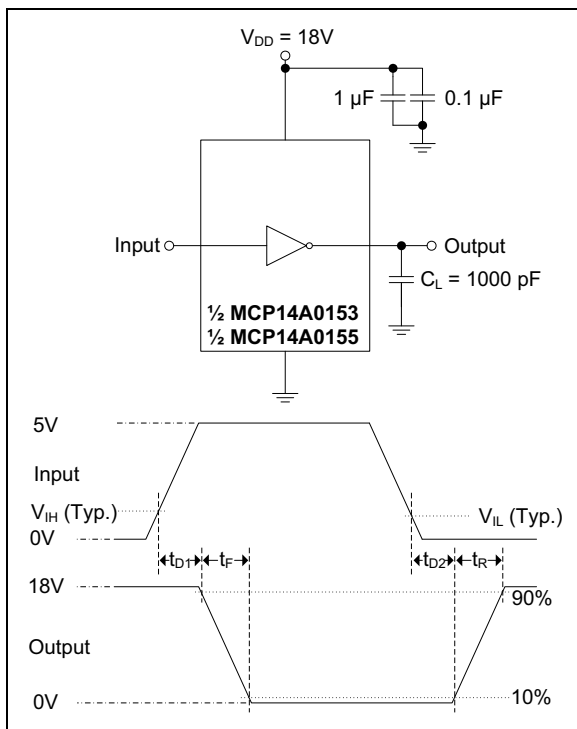


FIGURE 4-1: Inverting Driver Timing Waveform.

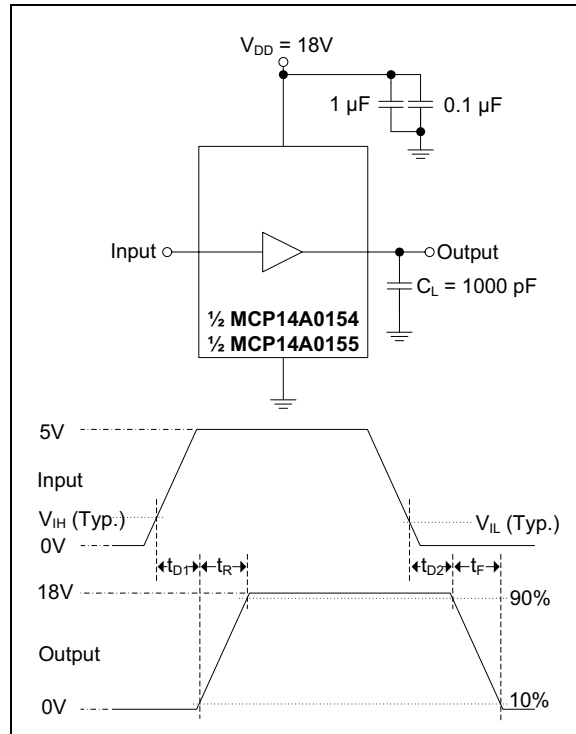


FIGURE 4-2: Noninverting Driver Timing Waveform.

4.3 Enable Function

The enable pins (EN A, EN B) provide additional control of the output pins (OUT). These pins are active high and are internally pulled up to V_{DD} so that the pins can be left floating to provide standard MOSFET driver operation.

When the enable pin input voltage's are above the enable pin high voltage threshold, (V_{EN_H}), the corresponding output is enabled and allowed to react to the status of the Input pin. However, when the voltage applied to the Enable pins falls below the low threshold voltage (V_{EN_L}), the driver's corresponding output is disabled and doesn't respond to changes in the status of the Input pins. When the driver is disabled, the output is pulled down to a low state. Refer to Table 4-1 for the Enable pin logic. The threshold voltage levels for the Enable pin are similar to the threshold voltage levels of the Input pin, and are TTL compatible. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays, t_{D3} and t_{D4} , are graphically represented in Figure 4-3.

TABLE 4-1: ENABLE PIN LOGIC

EN	IN	$\overline{\text{OUT}}$	OUT
H	H	L	H
H	L	H	L
L	X	L	L

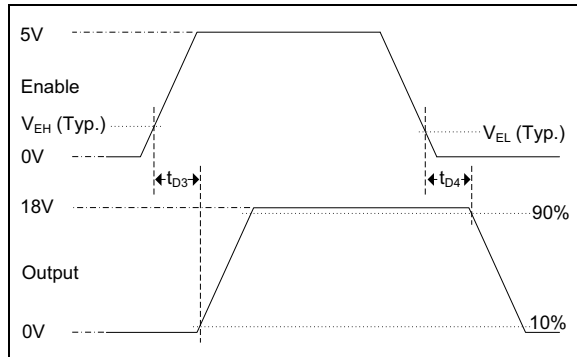


FIGURE 4-3: Enable Timing Waveform.

4.4 Decoupling Capacitors

Careful PCB layout and decoupling capacitors are required when using power MOSFET drivers. Large current is required to charge and discharge capacitive loads quickly. For example, approximately 720 mA are needed to charge a 1000 pF load with 18V in 25 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, it is recommended to place 1.0 μF and 0.1 μF low ESR ceramic capacitors in parallel between the driver V_{DD} and GND. These capacitors should be placed close to the driver to minimize circuit board parasitics and provide a local source for the required current.

4.5 PCB Layout Considerations

Proper Printed Circuit Board (PCB) layout is important in high-current, fast switching circuits to provide proper device operation and robustness of design. Improper component placement may cause errant switching, excessive voltage ringing or circuit latch-up. The PCB trace loop length and inductance should be minimized by the use of ground planes or traces under the MOSFET gate drive signal. Separate analog and power grounds and local driver decoupling should also be used.

Placing a ground plane beneath the MCP14A0153/4/5 devices will help as a radiated noise shield, as well as providing some heat sinking for power dissipated within the device.

4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements, as shown in Equation 4-1.

EQUATION 4-1:

$$P_T = P_L + P_Q + P_{CC}$$

Where:

- P_T = Total power dissipation
- P_L = Load power dissipation
- P_Q = Quiescent power dissipation
- P_{CC} = Operating power dissipation

4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of the frequency, total capacitive load and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is shown in Equation 4-2.

EQUATION 4-2:

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

- f = Switching frequency
- C_T = Total load capacitance
- V_{DD} = MOSFET driver supply voltage

4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw depends on the state of the Input and Enable pins. See Section 1.0 “Electrical Characteristics” for typical quiescent current draw values in different operating states. The quiescent power dissipation is shown in Equation 4-3.

EQUATION 4-3:

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

- I_{QH} = Quiescent current in the High state
- D = Duty cycle
- I_{QL} = Quiescent current in the Low state
- V_{DD} = MOSFET driver supply voltage

MCP14A0153/4/5

4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions because, for a very short period of time, both MOSFETs in the output stage are on simultaneously. This crossover current leads to a power dissipation described in [Equation 4-4](#).

EQUATION 4-4:

$$P_{CC} = V_{DD} \times I_{CO}$$

Where:

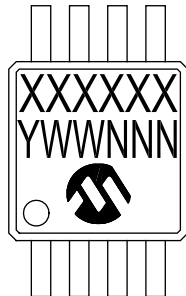
I_{CO} = Crossover current

V_{DD} = MOSFET driver supply voltage

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

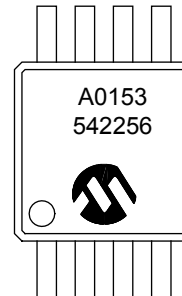
8-Lead MSOP (3x3 mm)



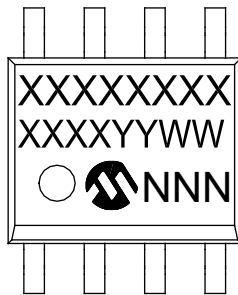
Device	Code
MCP14A0153T-E/MS	A0153
MCP14A0154T-E/MS	A0154
MCP14A0155T-E/MS	A0155

Note: Applies to 8-Lead MSOP

Example



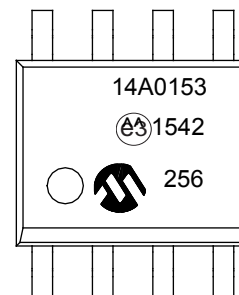
8-Lead SOIC (3.90 mm)



Device	Code
MCP14A0153T-E/SN	14A0153
MCP14A0154T-E/SN	14A0154
MCP14A0155T-E/SN	14A0155

Note: Applies to 8-Lead SOIC

Example



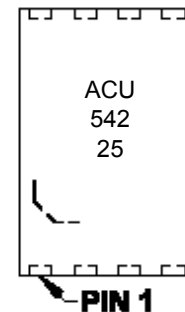
8-Lead TDFN (2x3x0.75 mm)



Device	Code
MCP14A0153T-E/MNY	ACU
MCP14A0154T-E/MNY	ACM
MCP14A0155T-E/MNY	ACV

Note: Applies to 8-Lead 2x3 TDFN

Example



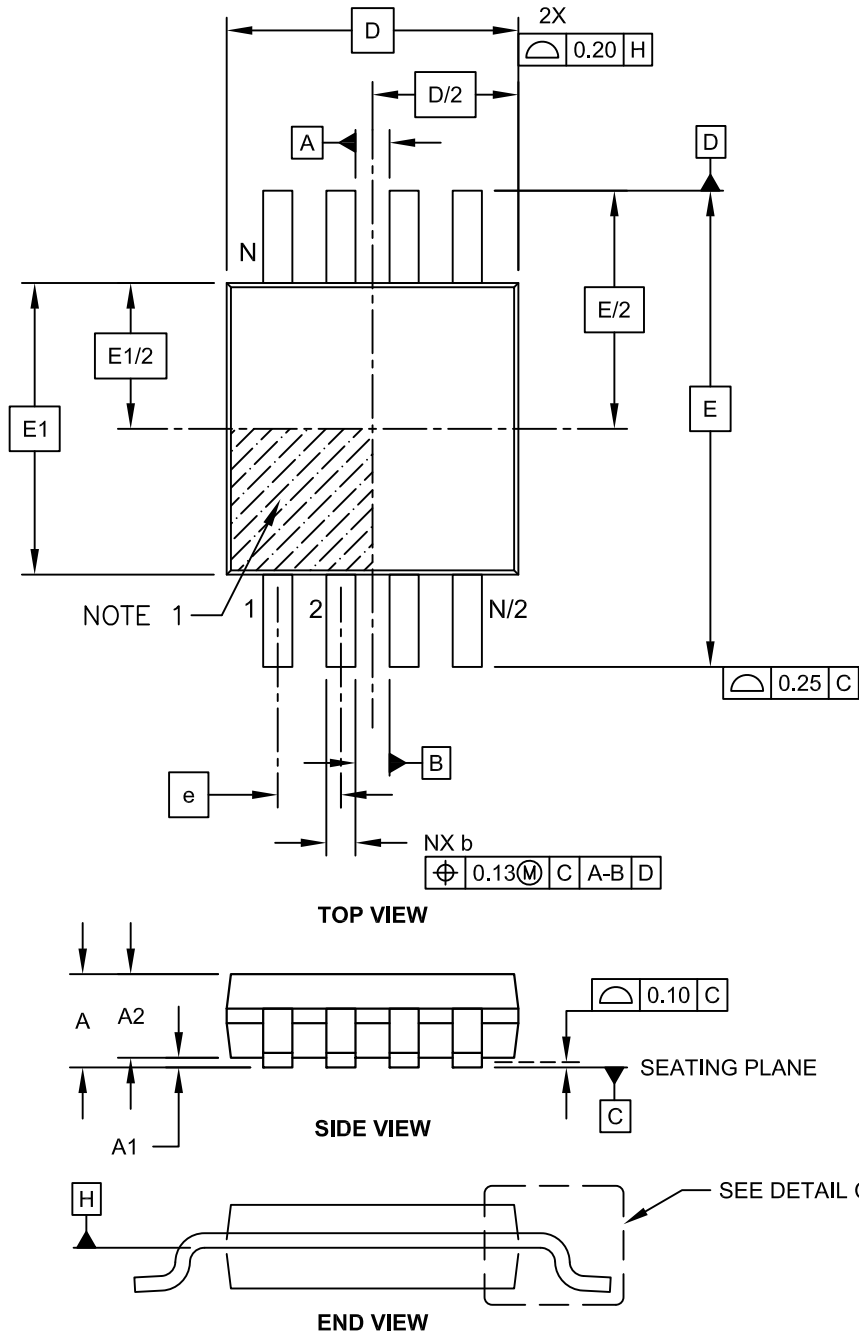
Legend:	Description
XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP14A0153/4/5

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

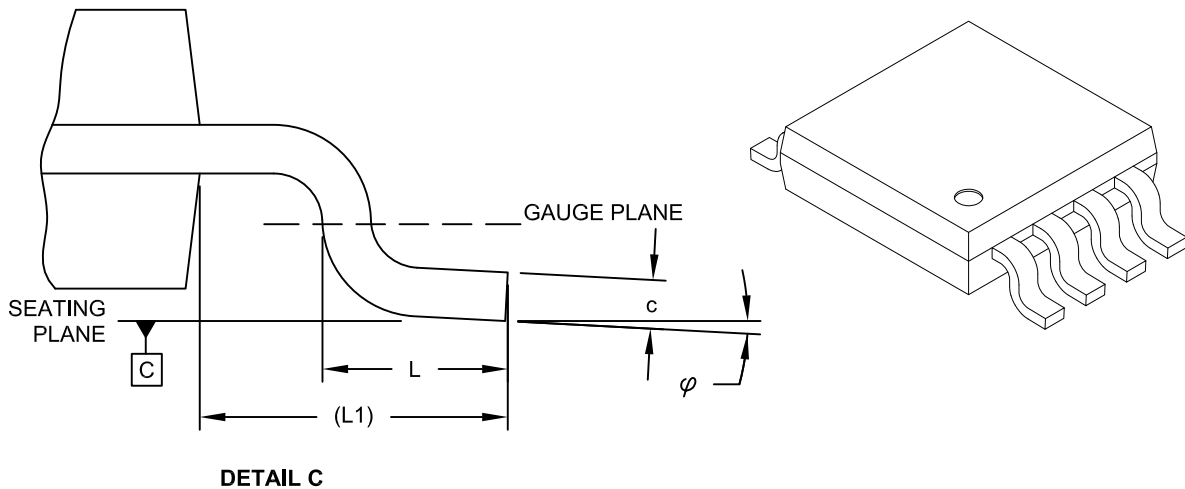
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

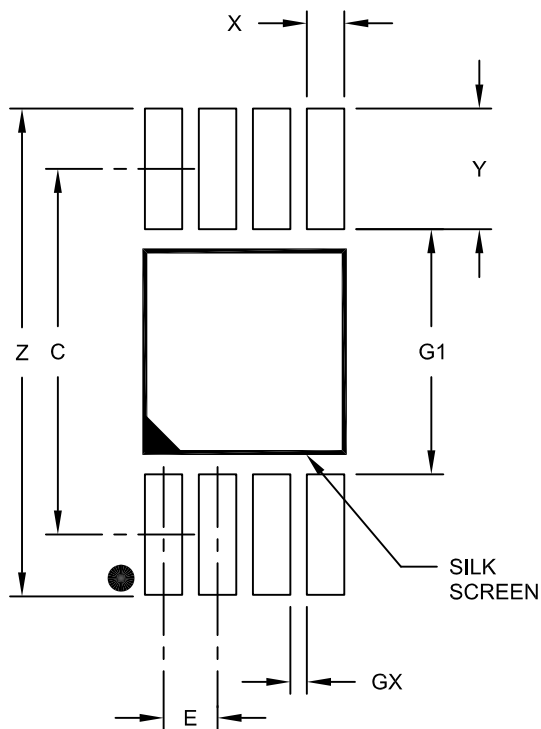
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

MCP14A0153/4/5

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

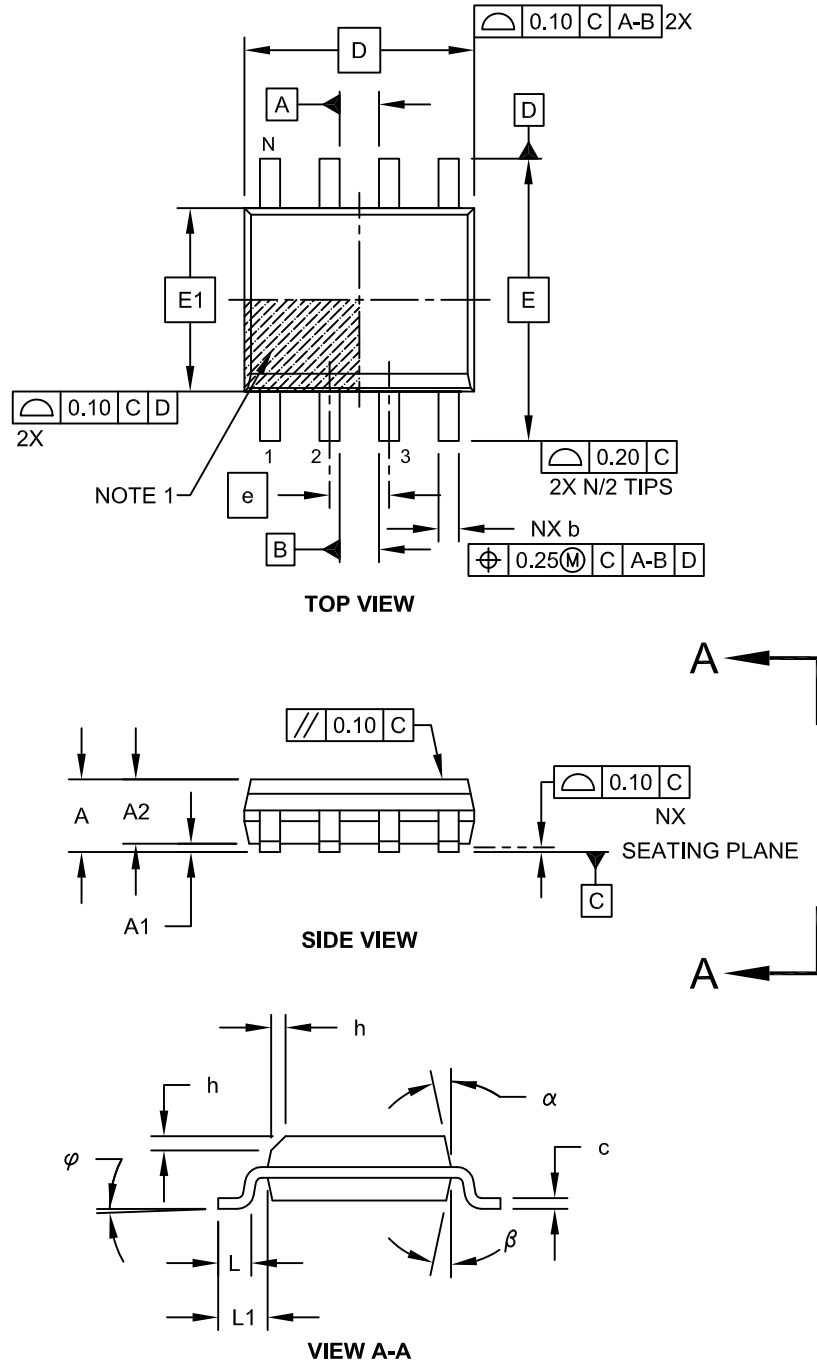
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

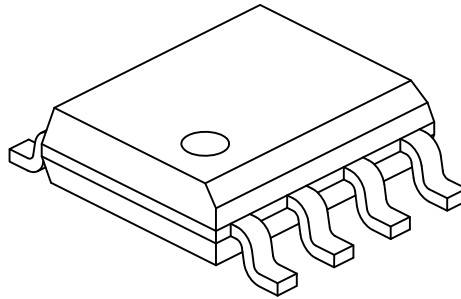


Microchip Technology Drawing No. C04-057C Sheet 1 of 2

MCP14A0153/4/5

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

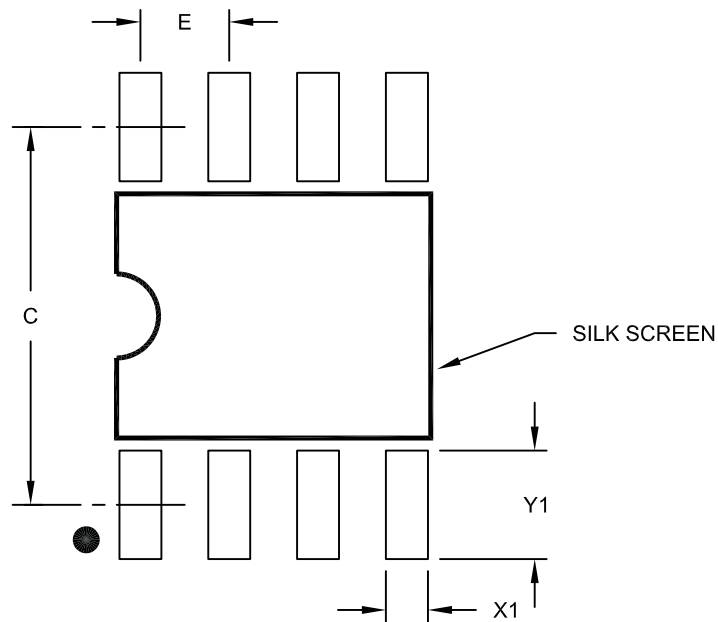
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

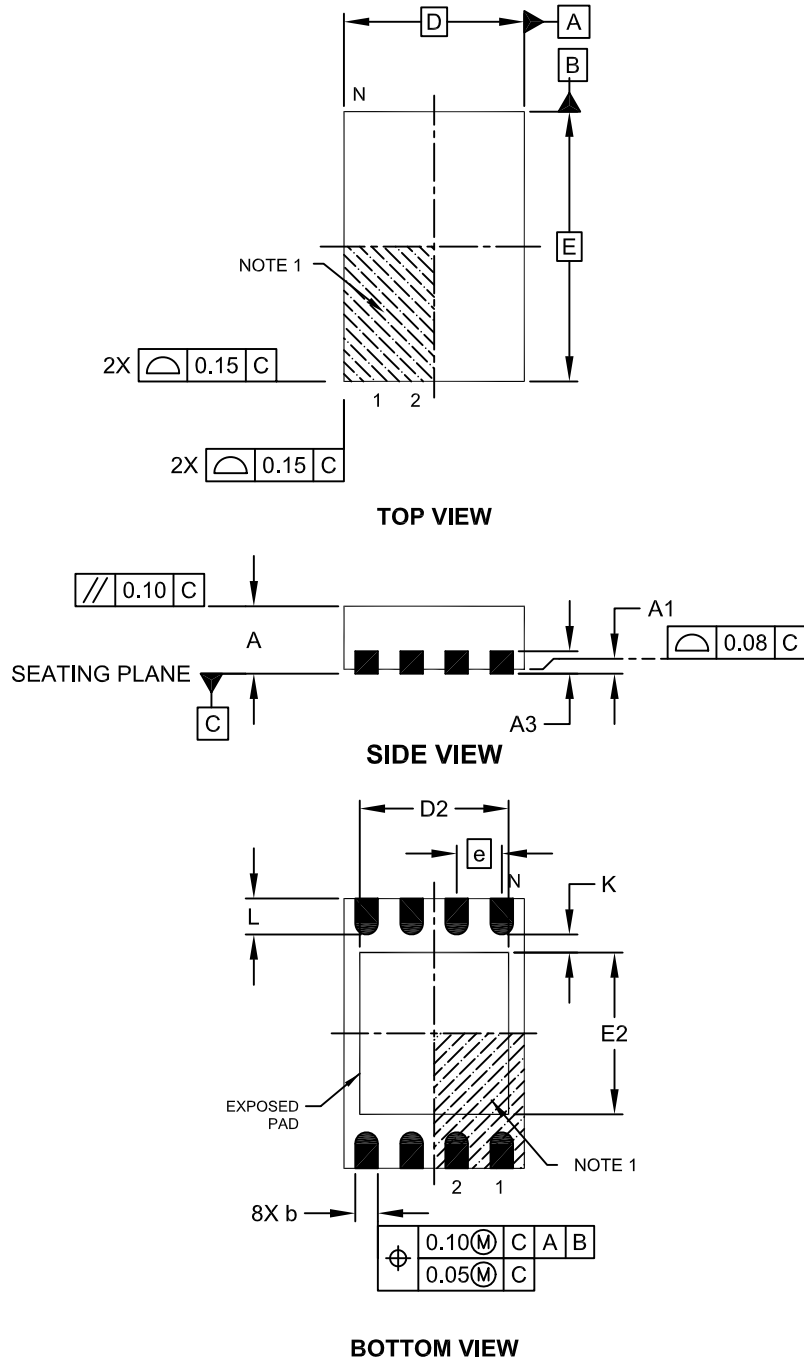
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

MCP14A0153/4/5

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

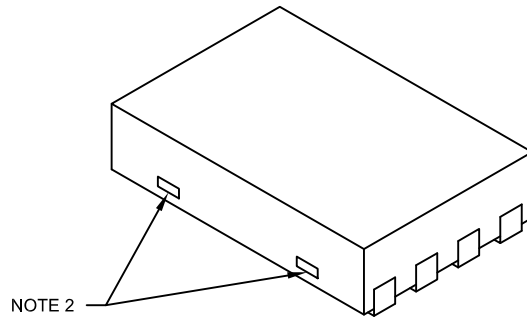
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-129C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated
- Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

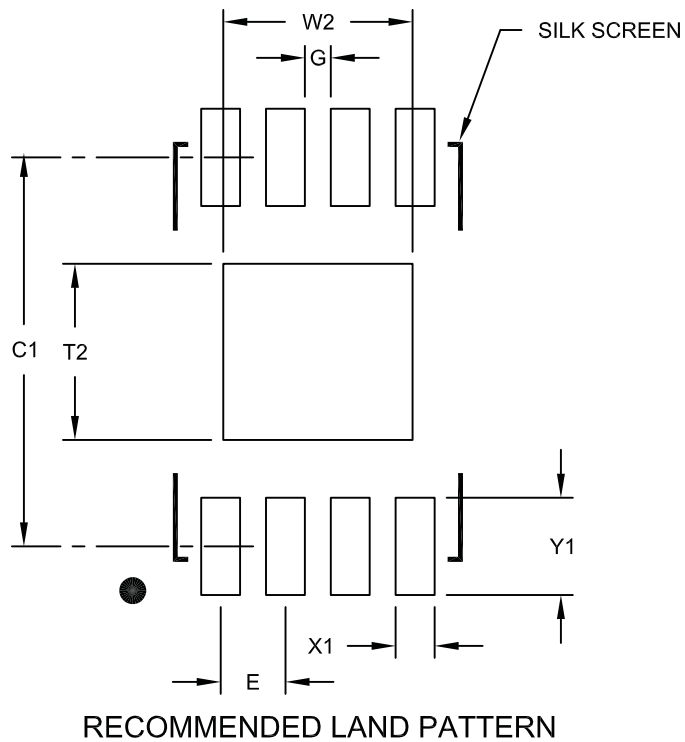
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

MCP14A0153/4/5

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1	3.00		
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision A (December 2015)

- Original release of this document