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Obsolete Device

For further designs, please refer to the MIC24046 Data Sheet

MCP16323

18V Input, 3A Output, High Efficiency Synchronous Buck Regulator with Power Good Indication

Features

- Up to 95% Typical Efficiency
- Input Voltage Range: 6.0V to 18V
- 3A Output Current
- Fixed Output Voltages: 0.9V, 1.5V, 1.8V, 2.5V, 3.3V, 5V with 2% Output Voltage Accuracy
- Adjustable Version Output Voltage Range: 0.9V to 5V with 1.5% Reference Voltage Accuracy
- Integrated N-Channel High-Side Switch: 180 mΩ
- Integrated N-Channel Low-Side Switch: 120 mΩ
- 1 MHz Fixed Frequency
- Low Device Shutdown Current
- Peak Current Mode Control
- Internal Compensation
- Stable with Ceramic Capacitors
- Internal Soft-Start
- Cycle-by-Cycle Peak Current Limit
- Undervoltage Lockout (UVLO): 5.75V
- Overtemperature Protection
- V_{OUT} Overvoltage Protection
- V_{OUT} Voltage Supervisor Reported at the PG Pin
- Available Package: QFN-16 (3x3 mm)

Applications

- PIC®/dsPIC® Microcontroller Bias Supply
- 12V Industrial Input DC-DC Conversion
- Set-Top Boxes
- DSL Cable Modems
- Automotive
- Wall Cube Regulation
- SLA Battery Powered Devices
- AC-DC Digital Control Power Source
- Power Meters
- Consumer
- Medical and Health Care
- Distributed Power Supplies

Description

The MCP16323 is a highly integrated, high-efficiency, fixed frequency, synchronous step-down DC-DC converter in a 16-pin QFN package that operates from input voltages up to 18V. Integrated features include a high-side and low-side N-Channel switch, fixed frequency Peak Current Mode Control, internal compensation, peak current limit, V_{OUT} overvoltage protection and overtemperature protection. Minimal external components are necessary to develop a complete synchronous step-down DC-DC converter power supply.

High converter efficiency is achieved by integrating a high-speed, current limited, low resistance, high-side N-Channel MOSFET, as well as a high-speed, low-resistance, low-side N-Channel MOSFET and associated drive circuitry. High switching frequency minimizes the size of the inductor and output capacitor, resulting in a small solution size.

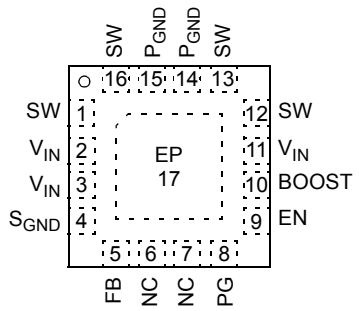
The MCP16323 device can supply 3A of continuous current while regulating the output voltage from 0.9V to 5V. A high-performance peak current mode architecture keeps the output voltage tightly regulated, even during input voltage steps and output current transient conditions that are common in power supplies.

The regulator can be turned on and off with a logic level signal applied to the EN input. The EN pin is internally pulled up to a 4.2V reference and is rated for a maximum of 6V. With EN low, typically 5 µA of current is consumed from the input, making the part ideal for power shedding and load distribution applications. The PG output is an open-drain output pin used to interface with other components of the system, and can be pulled up to a maximum of 6V.

The output voltage can either be fixed at output voltages of 0.9V, 1.5V, 1.8V, 2.5V, 3.3V, 5V or adjustable using an external resistor divider. The MCP16323 is offered in a 3x3 QFN-16 surface mount package.

Package Type

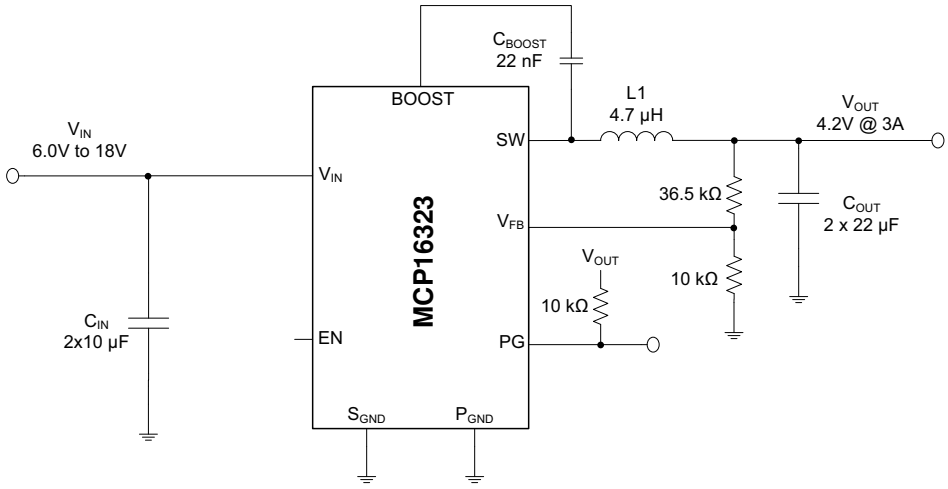
MCP16323
3x3 QFN*



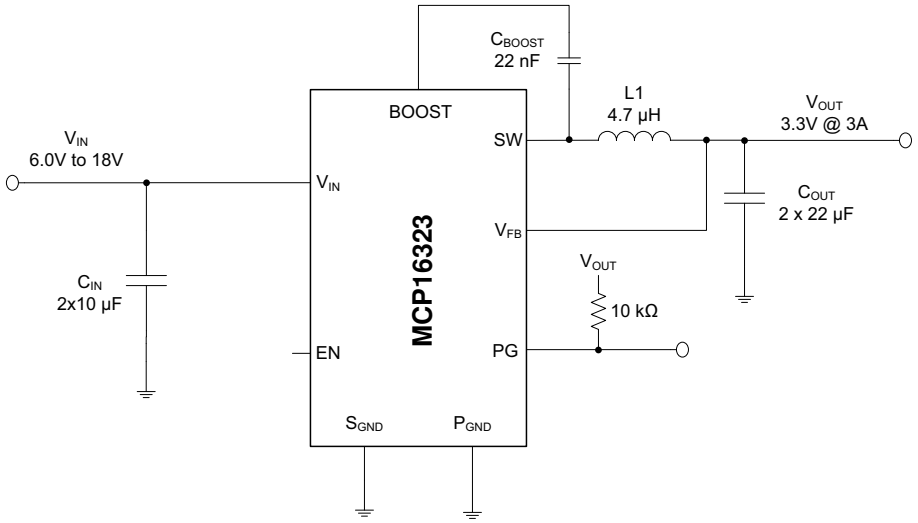
* Includes Exposed Thermal Pad (EP); see Table 3-1.

Typical Applications

Typical Application with Adjustable Output Voltage



Typical Application with Fixed Output Voltage



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} ..... -0.3V to 20V
SW ..... -1V to 20V
BOOST – GND ..... -0.3V to (V_{IN}+6V)
EN,V_{FB}, PG Voltage ..... -0.3V to 6V
Continuous Total Power Dissipation .....
..... See Thermal Characteristics
Storage Temperature ..... -65°C to +150°C
Operating Junction Temperature ..... -40°C to +125°C
ESD Protection On All Pins:
HBM ..... 3 kV
MM 200V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 300 mA, L = 4.7 µH, C_{OUT} = 2x22 µF, C_{IN} = 2x10 µF. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{IN} Supply Voltage						
Input Voltage	V_{IN}	**6.0**	—	**18**	V	
Quiescent Current (Switching)	I_Q	—	5.2	—	mA	I_{OUT} = 0 mA
Quiescent Current (Non-Switching)	I_Q	—	2.3	—	mA	Closed Loop in Overvoltage I_{OUT} = 0 mA
Quiescent Current - Shutdown	I_Q	—	5	**10**	µA	EN = 0
V_{IN} Undervoltage Lockout						
Undervoltage Lockout Start	$UVLO_{STRT}$	**5.5**	5.75	**6.0**	V	V_{IN} Rising
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	—	0.65	—	V	Non-Switching
Output Characteristics						
Maximum Output Current **MCP16323**	I_{OUT}	**3**	—	—	A	**Note 2**
Output Voltage Adjust Range	V_{OUT}	**0.9**	—	**5.0**	V	
Output Voltage Tolerance in PWM Mode	$V_{OUT-PWM}$	**V_{OUT} - 2%**	V_{OUT}	**V_{OUT} + 2%**	V	I_{OUT} = 1A
Output Voltage Tolerance in PFM Mode	$V_{OUT-PFM}$	**V_{OUT} - 1%**	V_{OUT} + 1%	**V_{OUT} + 3.5%**	V	I_{OUT} = 0A
Feedback Voltage	V_{FB}	**0.886**	0.9	**0.914**	V	
Feedback Reference Tolerance	V_{FB-TOL}	**-1.5**	—	**1.5**	%	

Note 1: Regulator SW pin is forced off for 240 ns every eight cycles to ensure the BOOST cap is replenished.

2: As a result of the maximum duty cycle limitations, 3A of output current for 5V output conditions may not regulate the voltage. External component selection may have an impact on this. A minimum input voltage of 6.5V is recommended.

DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 300 mA, L = 4.7 µH, C_{OUT} = 2x22 µF, C_{IN} = 2x10 µF. **Boldface** specifications apply over the T_J range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PFM Mode Feedback Comparator Threshold	V_{FB-PFM}	—	V_{OUT} + 1%	—	V	
Feedback Input Bias Current	I_{FB}	—	100	—	nA	
EN Input Characteristics						
EN Input Logic High	V_{IH}	**2.2**	—	—	V	
EN Input Logic Low	V_{IL}	—	—	**0.8**	V	
EN Input Hysteresis	$V_{EN-HYST}$	—	480	—	mV	
EN Input Leakage Current	I_{ENLK}	—	3.5	—	µA	V_{EN} = 5V
		—	-1.5	—	µA	V_{EN} = 0V
Soft-Start Time	t_{SS}	—	4	—	ms	
Switching Characteristics						
Switching Frequency	f_{SW}	**0.9**	1	**1.1**	MHz	Open Loop V_{FB} Low
Maximum Duty Cycle	DC_{MAX}	**95**	97	**99**	%	Open Loop V_{FB} Low **Note 1**
Minimum Duty Cycle		—	7	—	%	
NMOS Low-Side Switch On Resistance	Low-Side $R_{DS(ON)}$	—	120	—	mΩ	
NMOS High-Side Switch On Resistance	High-Side $R_{DS(ON)}$	—	180	—	mΩ	
NMOS High-Side Switch Current Limit	$I_{N(MAX)}$	**3.4**	3.8	**4.4**	A	**MCP16323**
PG Output Characteristics						
PG Low-level Output Voltage	PG_{IL}	—	—	**0.01**	V	I_{PG} = -0.3 mA
PG High-Level Output Leakage Current	I_{PGLK}	—	0.5	—	µA	V_{PG} = 5V
PG Release Timer	t_{PG}	—	10	—	ms	
V_{OUT} Undervoltage Threshold	V_{OUT-UV}	**91% V_{OUT}**	93% V_{OUT}	**95% V_{OUT}**		
V_{OUT} Undervoltage Hysteresis	V_{OUT-UV_HYST}	—	1.5% V_{OUT}	—		
V_{OUT} Overvoltage Threshold	V_{OUT-OV}	—	103% V_{OUT}	—		
V_{OUT} Overvoltage Hysteresis	V_{OUT-OV_HYST}	—	1% V_{OUT}	—		
Thermal Characteristics						
Thermal Shutdown Die Temperature	T_{SD}	—	170	—	°C	
Die Temperature Hysteresis	T_{SDHYS}	—	10	—	°C	

Note 1: Regulator SW pin is forced off for 240 ns every eight cycles to ensure the BOOST cap is replenished.

2: As a result of the maximum duty cycle limitations, 3A of output current for 5V output conditions may not regulate the voltage. External component selection may have an impact on this. A minimum input voltage of 6.5V is recommended.

TABLE 1-1: TEMPERATURE CHARACTERISTICS

Electrical Characteristics						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	125	°C	Steady State
Storage Temperature Range	T_A	-65	—	150	°C	
Maximum Junction Temperature	T_J	—	—	150	°C	Transient
Package Thermal Resistances						
Thermal Resistance, 16L 3x3-QFN	θ_{JA}	—	38.5	—	°C/W	

Note 1: Measured using a 4-layer FR4 Printed Circuit Board with a 13.5 in^2, 1 oz internal copper ground plane.

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V, EN = Floating (internally pulled up), C_{IN} = 20 µF, C_{OUT} = 2x22 µF, L = 4.7 µH (XAL6060-472MEB), I_{LOAD} = 200 mA, T_A = +25°C.

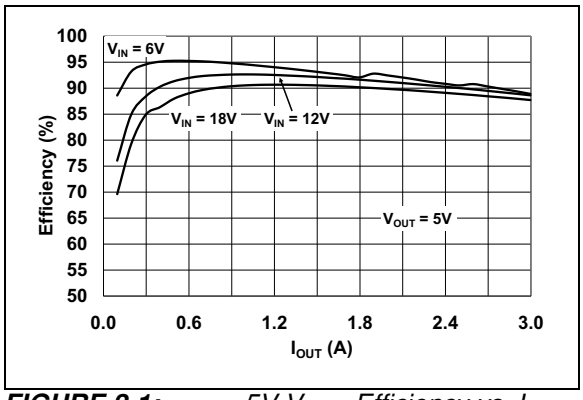


FIGURE 2-1: *5V V_{OUT} Efficiency vs. I_{OUT}.*

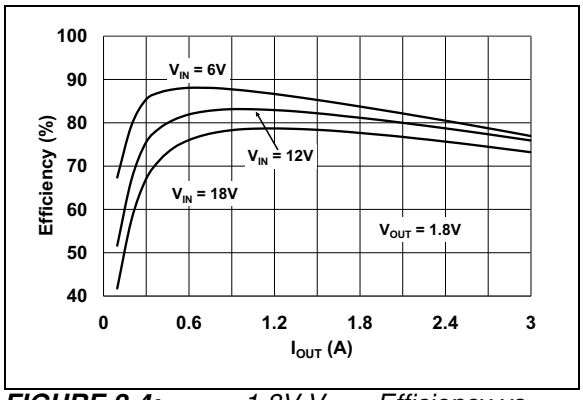


FIGURE 2-4: *1.8V V_{OUT} Efficiency vs. I_{OUT}.*

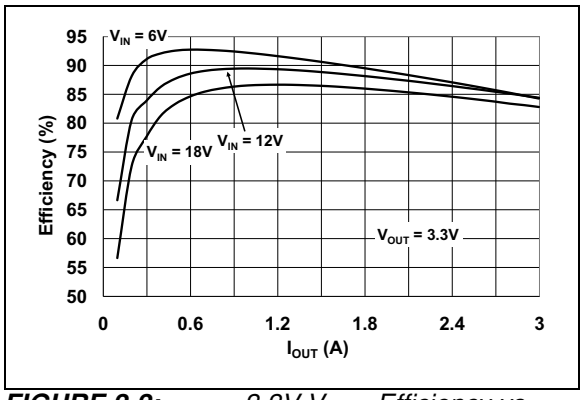


FIGURE 2-2: *3.3V V_{OUT} Efficiency vs. I_{OUT}.*

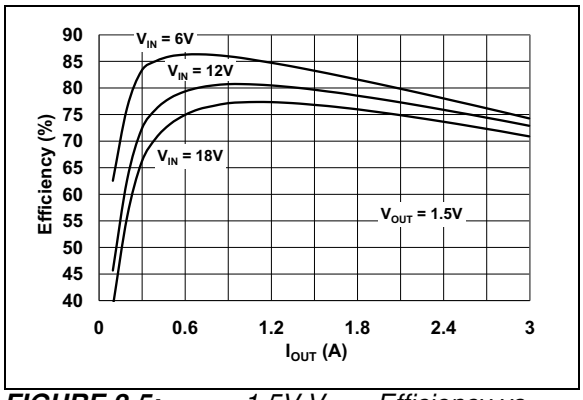


FIGURE 2-5: *1.5V V_{OUT} Efficiency vs. I_{OUT}.*

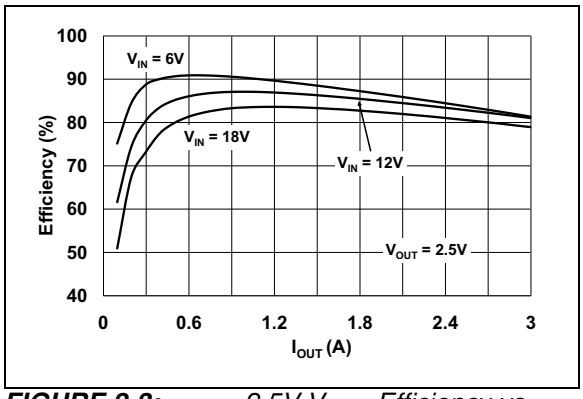


FIGURE 2-3: *2.5V V_{OUT} Efficiency vs. I_{OUT}.*

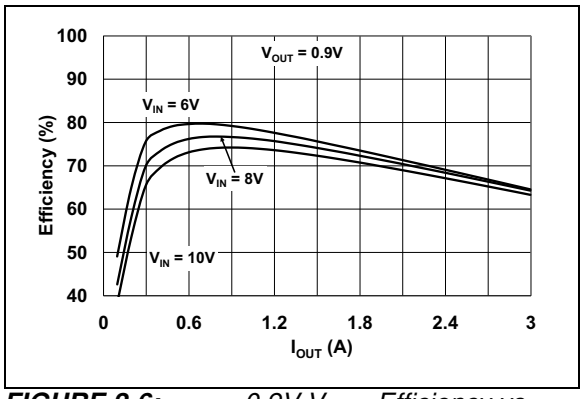


FIGURE 2-6: *0.9V V_{OUT} Efficiency vs. I_{OUT}.*

Note: Unless otherwise indicated, V_{IN} = 12V, EN = Floating (internally pulled up), C_{IN} = 20 µF, C_{OUT} = 2x22 µF, L = 4.7 µH, I_{LOAD} = 200 mA, T_A = +25°C.

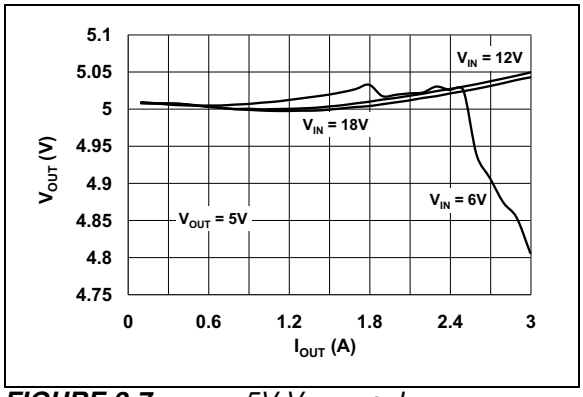


FIGURE 2-7: *5V V_{OUT} vs. I_{OUT}.*

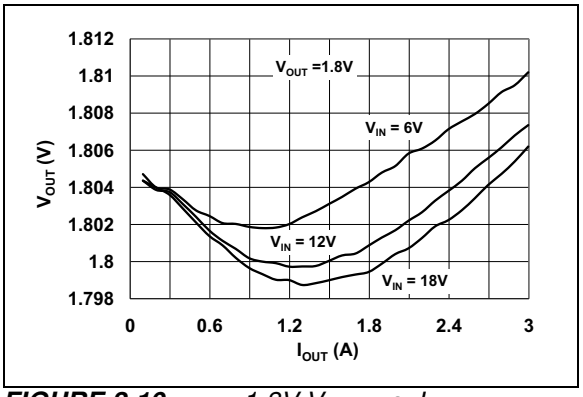


FIGURE 2-10: *1.8V V_{OUT} vs. I_{OUT}.*

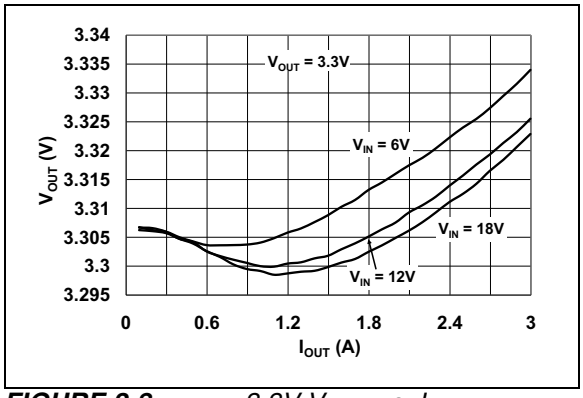


FIGURE 2-8: *3.3V V_{OUT} vs. I_{OUT}.*

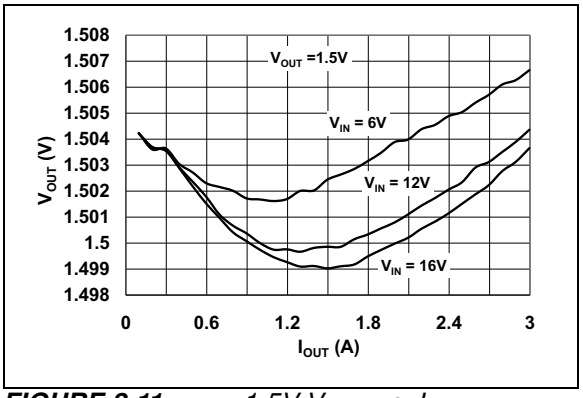


FIGURE 2-11: *1.5V V_{OUT} vs. I_{OUT}.*

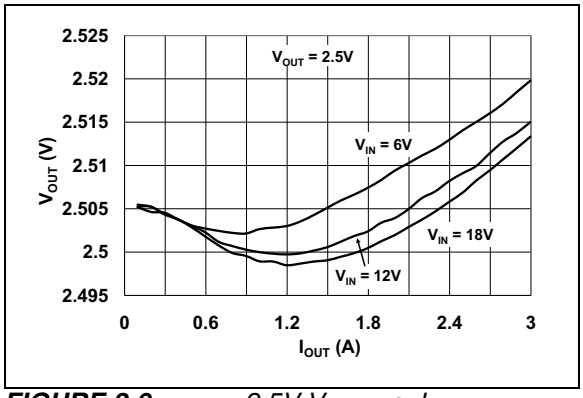


FIGURE 2-9: *2.5V V_{OUT} vs. I_{OUT}.*

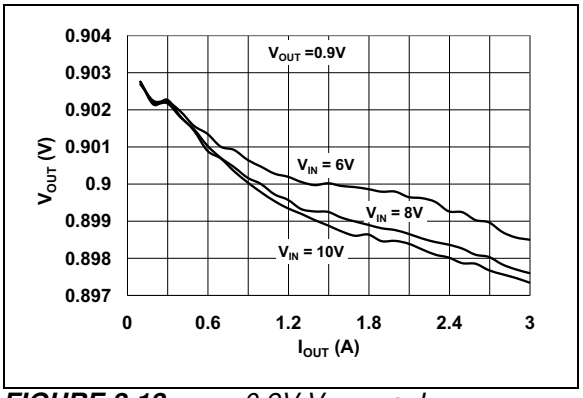


FIGURE 2-12: *0.9V V_{OUT} vs. I_{OUT}.*

Note: Unless otherwise indicated, V_{IN} = 12V, EN = Floating (internally pulled up), C_{IN} = 20 µF, C_{OUT} = 2x22 µF, L = 4.7 µH, I_{LOAD} = 200 mA, T_A = +25°C.

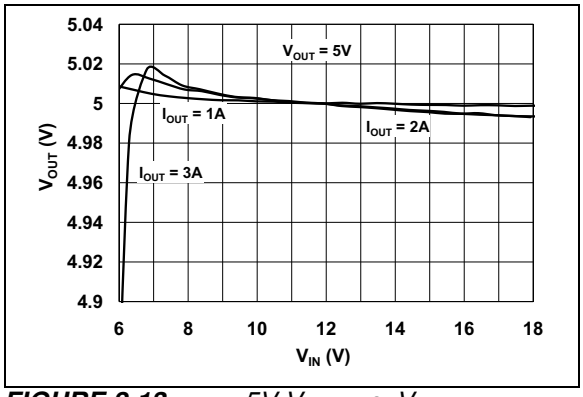


FIGURE 2-13: *5V V_{OUT} vs. V_{IN}.*

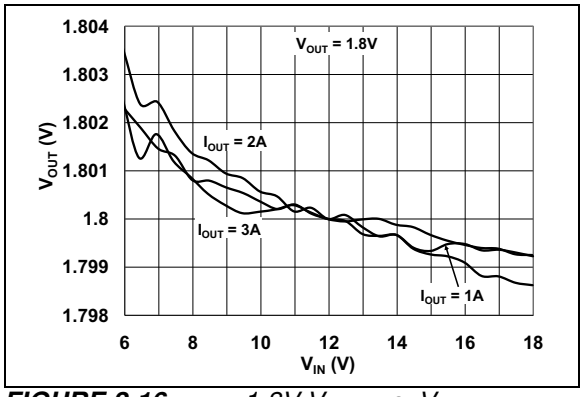


FIGURE 2-16: *1.8V V_{OUT} vs. V_{IN}.*

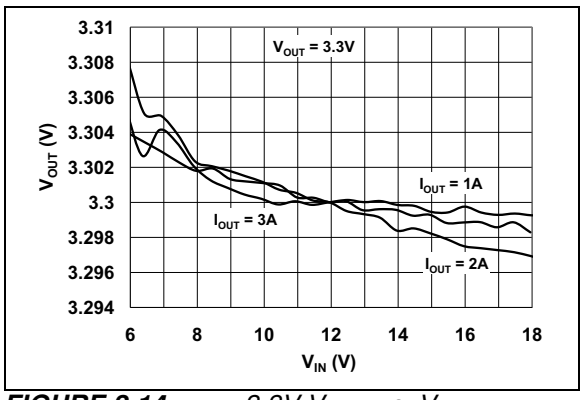


FIGURE 2-14: *3.3V V_{OUT} vs. V_{IN}.*

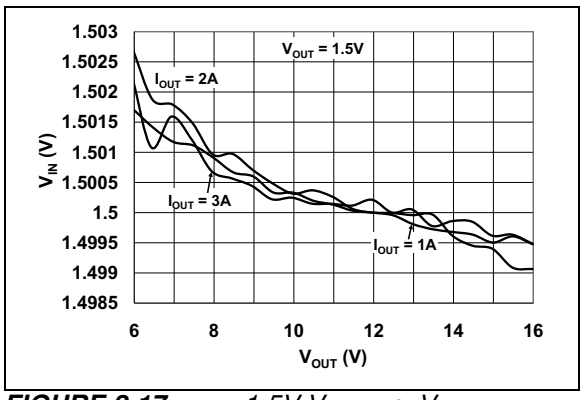


FIGURE 2-17: *1.5V V_{OUT} vs. V_{IN}.*

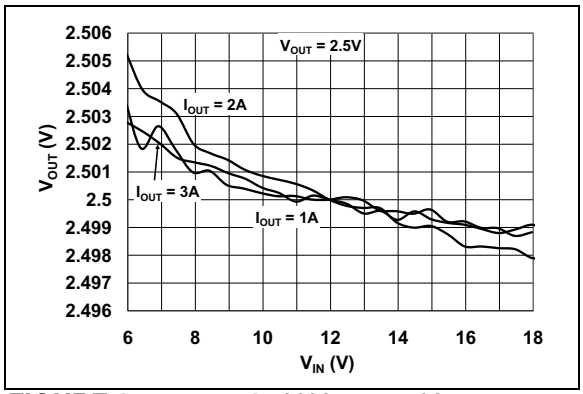


FIGURE 2-15: *2.5V V_{OUT} vs. V_{IN}.*

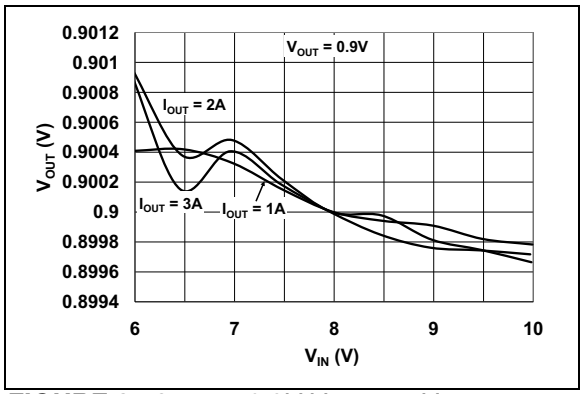


FIGURE 2-18: *0.9V V_{OUT} vs. V_{IN}.*

Note: Unless otherwise indicated, V_{IN} = 12V, EN = Floating (internally pulled up), C_{IN} = 20 µF, C_{OUT} = 2x22 µF, L = 4.7 µH, I_{LOAD} = 200 mA, T_A = +25°C.

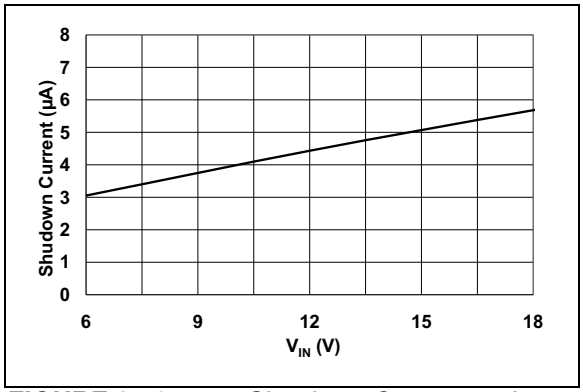


FIGURE 2-19: *Shutdown Current vs. Input Voltage.*

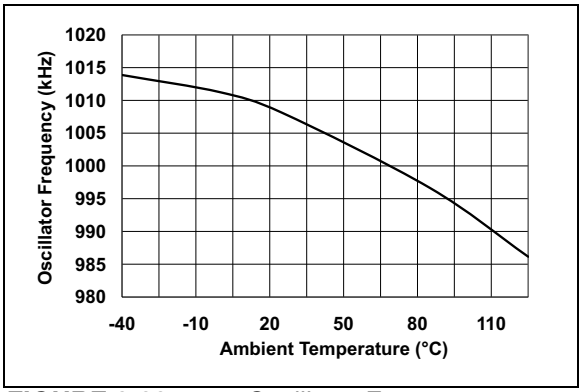


FIGURE 2-22: *Oscillator Frequency vs. Temperature (I_{OUT} = 300 mA).*

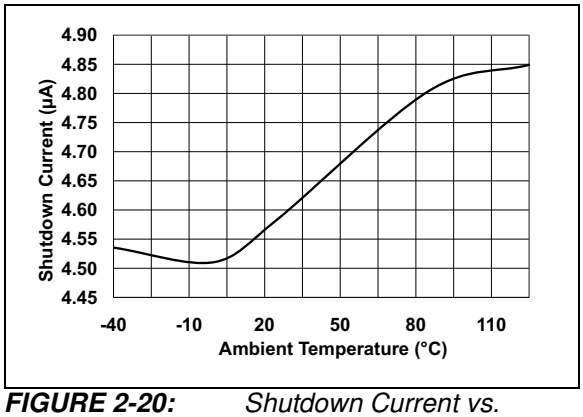


FIGURE 2-20: *Shutdown Current vs. Temperature.*

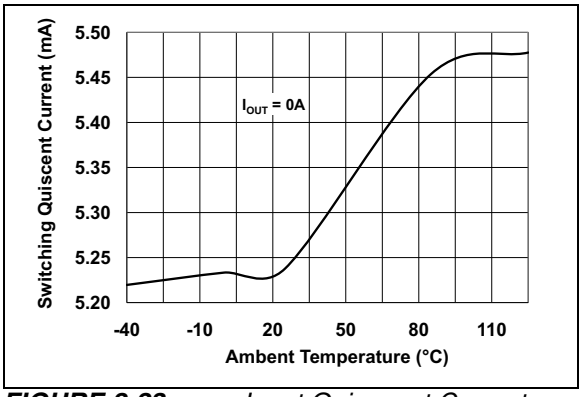


FIGURE 2-23: *Input Quiescent Current vs. Temperature (No Load, Switching).*

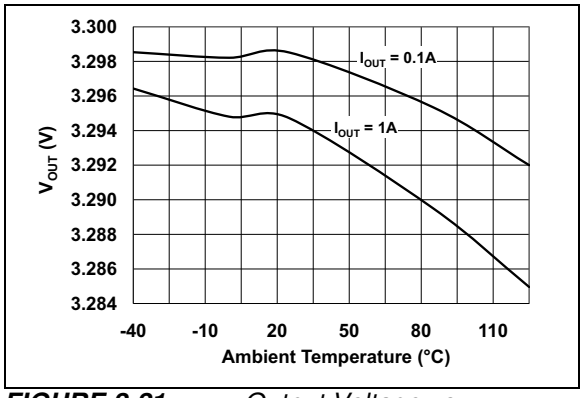


FIGURE 2-21: *Output Voltage vs. Temperature.*

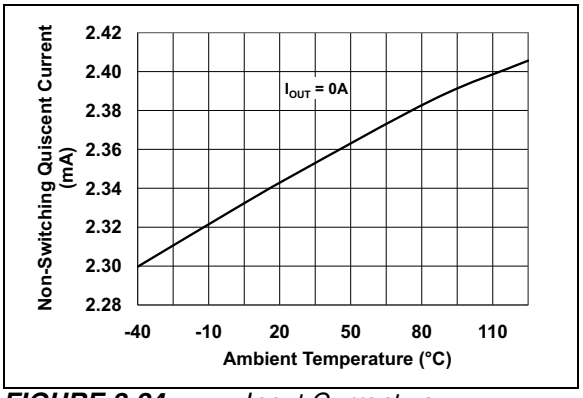


FIGURE 2-24: *Input Current vs. Temperature (No Load, No Switching).*

Note: Unless otherwise indicated, V_{IN} = 12V, EN = Floating (internally pulled up), C_{IN} = 20 µF, C_{OUT} = 2x22 µF, L = 4.7 µH, I_{LOAD} = 200 mA, T_A = +25°C.

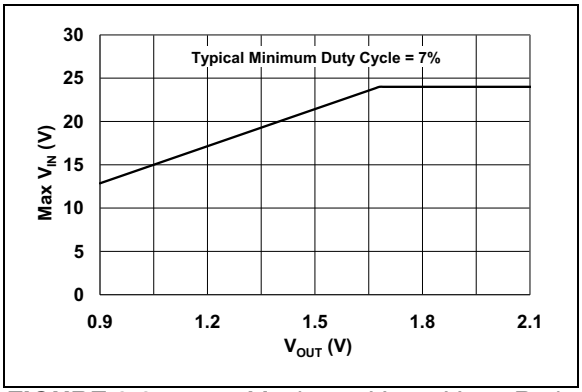


FIGURE 2-25: *Maximum V_{IN} to V_{OUT} Ratio for Continuous Switching.*

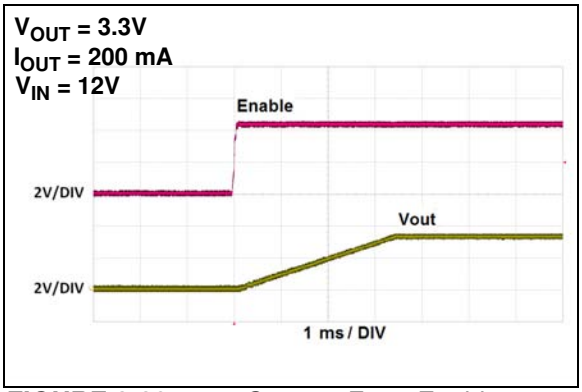


FIGURE 2-28: *Start-up From Enable.*

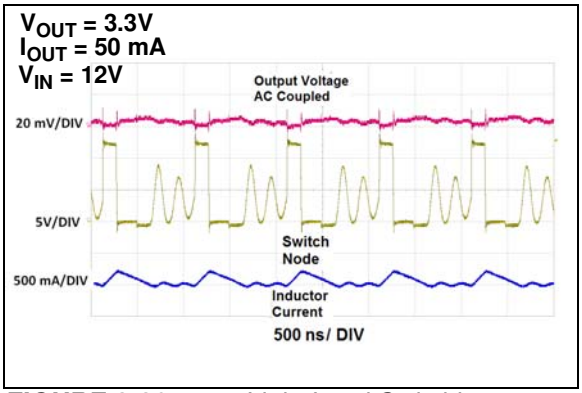


FIGURE 2-26: *Light Load Switching Waveforms.*

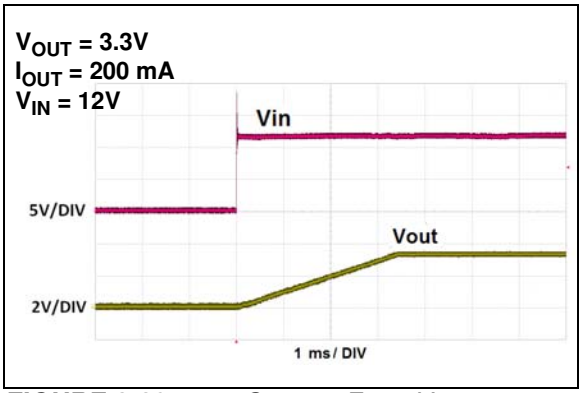


FIGURE 2-29: *Start-up From V_{IN}.*

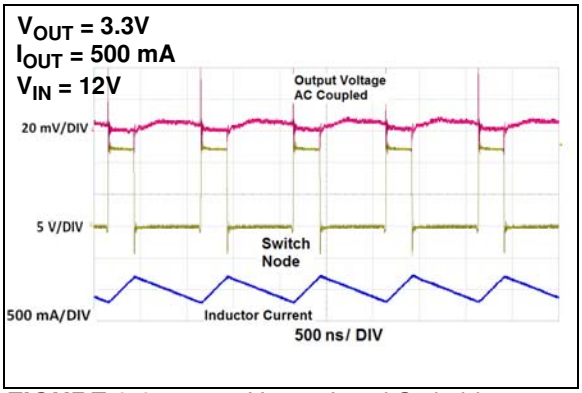


FIGURE 2-27: *Heavy Load Switching Waveforms.*

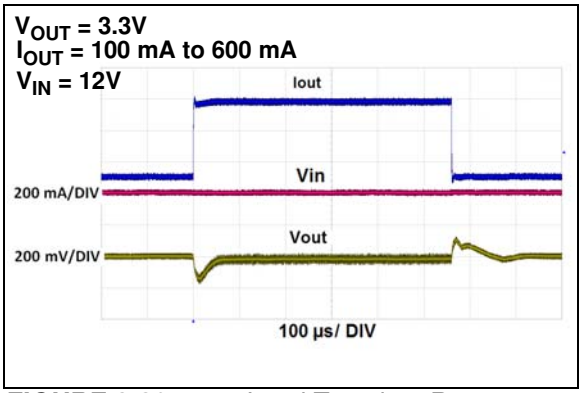


FIGURE 2-30: *Load Transient Response.*

Note: Unless otherwise indicated, V_{IN} = 12V, EN = Floating (internally pulled up), C_{IN} = 20 µF, C_{OUT} = 2x22 µF, L = 4.7 µH, I_{LOAD} = 200 mA, T_A = +25°C.

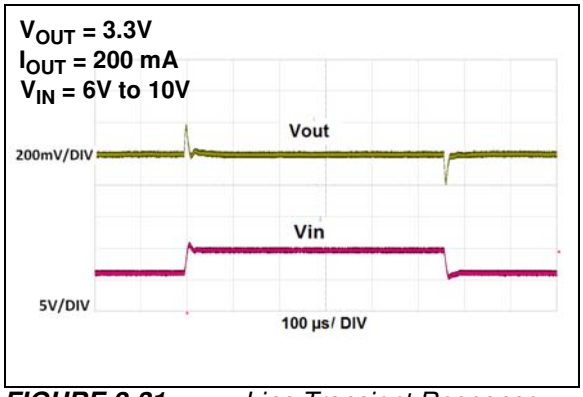


FIGURE 2-31: *Line Transient Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP16323 3x3 QFN	Symbol	Description
1	SW	Output switch node, connects to the inductor and the bootstrap capacitor
2	V_{IN}	Input supply voltage pin for power and internal biasing
3	V_{IN}	Input supply voltage pin for power and internal biasing
4	SGND	Primary signal ground
5	V_{FB}	Output voltage feedback pin. Connect V_{FB} to V_{OUT} for fixed version and output resistor divider for adjustable version.
6	NC	No Connection
7	NC	No Connection
8	PG	Power Good open-drain output, pulled up to a maximum of 6V
9	EN	Enable input pin. Logic high enables the operation. Internally pulled up, pull EN pin low to disable regulator's output. Maximum voltage on EN input is 6V.
10	BOOST	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
11	V_{IN}	Input supply voltage pin for power and internal biasing
12	SW	Output switch node, connects to the inductor and the bootstrap capacitor
13	SW	Output switch node, connects to the inductor and the bootstrap capacitor
14	PGND	GND supply for the internal low-side NMOS/integrated diode
15	PGND	GND supply for the internal low-side NMOS/integrated diode
16	SW	Output switch node, connects to the inductor and the bootstrap capacitor
17	EP	Exposed Thermal Pad (EP); must be connected to GND

3.1 Switch Pin (SW)

The drain of the low-side N-Channel switch is connected internally to the source of the high-side N-Channel switch, and externally to the SW node consisting of the inductor and bootstrap capacitor. The SW node can rise very fast as a result of the internal high-side switch turning on. It should be connected directly to the 4.7 µH inductor with a wide, short trace.

3.2 Power Supply Input Voltage Pin (V_{IN})

Connect the input voltage source to V_{IN}. The input source should be decoupled to GND using 2 x 10 µF capacitors. The amount of the capacitance depends on the impedance of the source and output current. The input capacitors provide AC current for the high-side power switch and a stable voltage source for the internal device power. This capacitor should be connected as close as possible to the V_{IN} and GND pins.

3.3 Signal Ground Pin (S_{GND})

This ground is used for the majority of the device, including the analog reference, control loop, and other circuits.

3.4 Feedback Voltage Pin (V_{FB})

The V_{FB} input pin is used to provide output voltage regulation by either using a resistor divider or V_{OUT} directly. For the adjustable version, the V_{FB} will be 0.9V typical with the output voltage in regulation. For the fixed version, the V_{FB} will be equal to the corresponding V_{OUT} value.

3.5 Power Good Pin (PG)

PG is an open-drain, active-low output. The regulator output voltage is monitored and the PG line will remain low until the output voltage reaches the V_{OUT-UV} threshold. Once the internal comparator detects that the output voltage is above the V_{OUT-UV} threshold, an internal delay timer is activated. After a 10 ms delay, the PG open-drain output pin can be pulled high, indicating that the output voltage is in regulation. The maximum voltage applied to the PG output pin should not exceed 6V.

3.6 Enable Pin (EN)

The EN input pin is a logic-level input used to enable or disable the device. A logic high (> 2.2V) will enable the regulator output, while a logic low (< 0.8V) will ensure that the regulator is disabled. This pin is internally pulled up to an internal reference and will be enabled when V_{IN} > UVLO, unless the EN pin is pulled low. The maximum input voltage applied to the EN pin should not exceed 6V.

3.7 BOOST Pin (BOOST)

This pin will provide the bootstrap voltage required for driving the upper internal NMOS switch of the buck regulator. An external ceramic capacitor placed between the BOOST input pin and the SW pin will provide the necessary drive voltage for the upper switch. During steady state operation, the capacitor is recharged on every low-side, synchronous switching cycle. If the Switch mode approaches 100% duty cycle for the high-side MOSFET, the device will automatically reduce the duty cycle switch to a minimum off time of 240 ns on every 8^{th} cycle to recharge the boost capacitor.

3.8 Power Ground Pin (P_{GND})

This is a separate ground connection used for the low-side synchronous switch to isolate switching noise from the rest of the device.

3.9 Exposed Thermal Pad (EP)

There is no internal electrical connection between the Exposed Thermal Pad (EP) and the P_{GND} and S_{GND} pins. The EP must be connected to GND on the Printed Circuit Board (PCB).

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP16323 is a high input voltage step-down regulator, capable of supplying 3A to a regulated output voltage from 0.9V to 5V. Internally, the 1 MHz oscillator provides a fixed frequency, while the Peak Current Mode Control architecture varies the duty cycle for output voltage regulation. An internal floating driver is used to turn the high-side integrated N-Channel MOSFET on and off. The power for this driver is derived from an external boost capacitor whose energy is replenished when the low-side N-Channel MOSFET is turned on. When the maximum duty cycle approaches 100%, the boost capacitor is replenished for 240 ns after every eight cycles.

4.1.1 INTERNAL REFERENCE VOLTAGE V_{REF}

For the adjustable version, an integrated precise 0.9V reference combined with an external resistor divider sets the desired converter output voltage. The resistor divider can vary without affecting the control system gain. High-value resistors consume less current, but are more susceptible to noise. For the fixed version, an integrated precise voltage reference is set to the desired V_{OUT} value and is directly connected to V_{OUT}.

4.1.2 INTERNAL COMPENSATION

All control system components necessary for stable operation over the entire device operating range are integrated, including the error amplifier and inductor current slope compensation.

4.1.3 EXTERNAL COMPONENTS

External components consist of:

- Input capacitor
- Output filter (inductor and capacitor)
- Boost capacitor
- Resistor divider (adjustable version only)

The selection of the external inductor, output capacitor, input capacitor and boost capacitor is dependent upon the output voltage and the maximum output current.

4.1.4 ENABLE INPUT

The enable input (EN) is used to disable the device. If disabled, the device consumes a minimal current from the input. Once enabled, the internal soft start controls the output voltage rate of rise, preventing high-inrush current and output voltage overshoot. The EN is internally pulled up or enabled, to disable the converter, it must be pulled low.

4.1.5 SOFT START

The internal reference voltage rate of rise is controlled during start-up, minimizing the output voltage overshoot and the inrush current.

4.1.6 OUTPUT OVERVOLTAGE PROTECTION

If the output of the regulator exceeds 103% of the regulation voltage, the SW outputs will tri-state to protect the device from damage. This check occurs at the start of each switching cycle.

4.1.7 INPUT UNDERVOLTAGE LOCKOUT

An integrated Undervoltage Lockout (UVLO) prevents the converter from starting until the input voltage is high enough for normal operation. The converter will typically start at 5.75V (typical) and operate down to 5.25V (typical). Hysteresis of 500 mV (typical) is added to prevent starting and stopping during start-up, as a result of loading the input voltage source.

4.1.8 MINIMUM DUTY CYCLE

A minimum duty cycle of 70 ns typical prevents the device from constant switching for high step-down voltage ratios. Duty cycles less than this minimum will initiate pulse skipping to maintain output voltage regulation, resulting in higher output voltage ripple. Duty cycle for continuous inductor current operation is approximated by V_{OUT}/V_{IN}. For a 1 MHz switching frequency or 1 µs period, this results in a 7% duty cycle minimum. Maximum V_{IN} for continuous switching can be approximated dividing V_{OUT} by the minimum duty cycle or 7%. For example, the maximum input voltage for continuous switching for a 1.5V output is equal to approximately 21V.

4.1.9 OVERTEMPERATURE PROTECTION

Overtemperature protection limits the silicon die temperature to +170°C by turning the converter off. The normal switching resumes at +160°C.

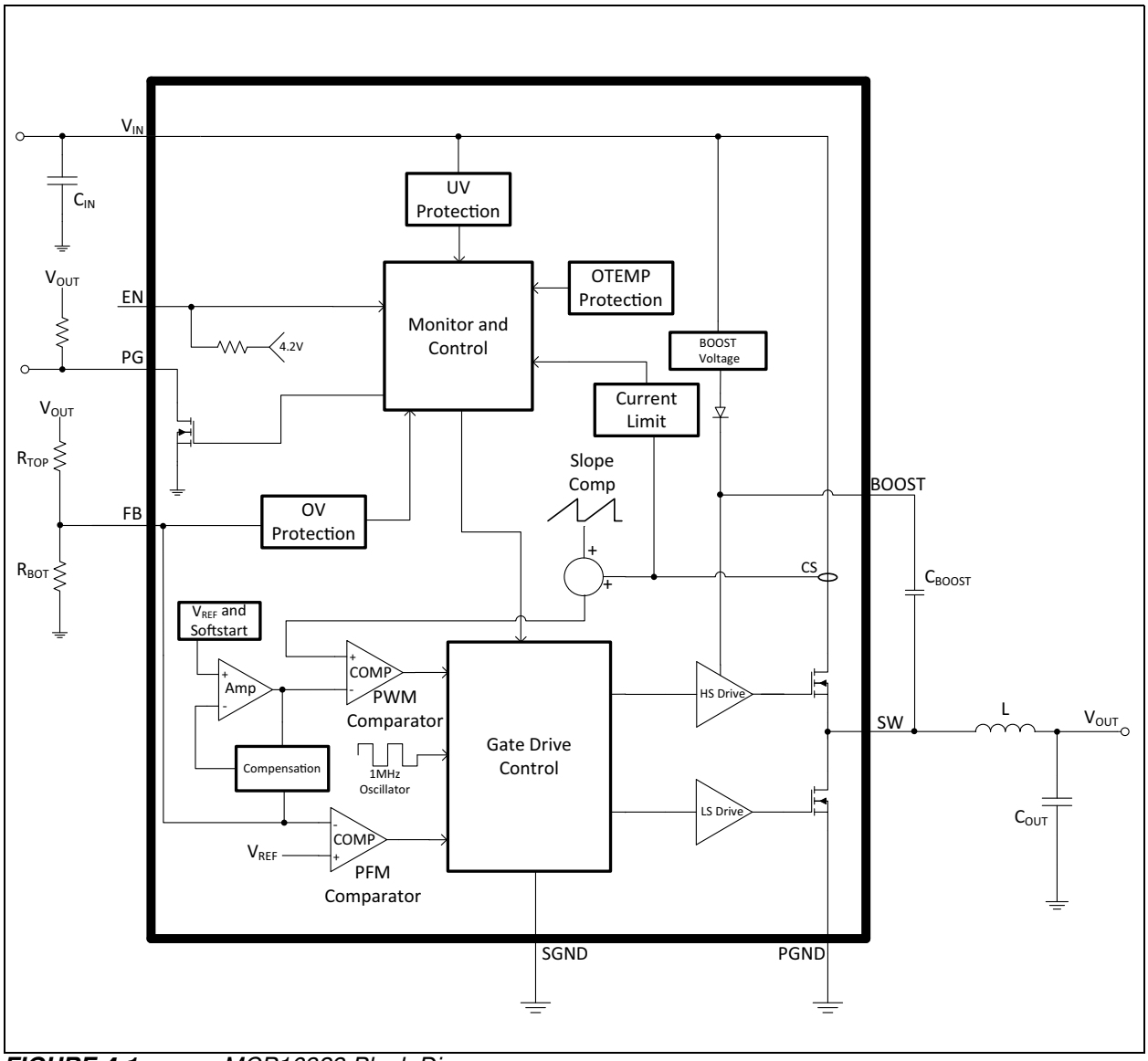


FIGURE 4-1: *MCP16323 Block Diagram.*

4.2 Functional Description

4.2.1 STEP-DOWN OR BUCK CONVERTER

The MCP16323 is a synchronous, step-down or buck converter capable of stepping input voltages ranging from 6V to 18V down to 0.9V to 5V.

The integrated high-side switch is used to chop or modulate the input voltage using a controlled duty cycle for output voltage regulation. The integrated low-side switch is used to freewheel current when the high-side switch is turned off. High efficiency is achieved by using low-resistance switches and low equivalent series resistance (ESR), inductor and capacitors. When the high-side switch is turned on, a DC voltage is applied to the inductor ($V_{IN} – V_{OUT}$), resulting in a positive linear ramp of inductor current. When the high-side switch turns off and the low-side switch turns on, the applied inductor voltage is equal to $–V_{OUT}$, resulting in a negative linear ramp of inductor current. In order to ensure there is no shoot through current, a dead time where both switches are off is implemented between the high-side switch turning off and the low-side switch turning on, and the low-side switch turning off and the high-side switch turning on.

For steady-state, continuous inductor current operation, the positive inductor current ramp must equal the negative current ramp in magnitude. While operating in steady state, the switch duty cycle must be equal to the relationship of V_{OUT}/V_{IN} for constant output voltage regulation, under the condition that the inductor current is continuous, or never reaches zero. For discontinuous inductor current operation, the steady-state duty cycle will be less than V_{OUT}/V_{IN} to maintain voltage regulation. When the inductor current reaches zero, the low-side switch is turned off so that current does not flow in the reverse direction, keeping the efficiency high. The average of the chopped input voltage or SW node voltage is equal to the output voltage, while the average inductor current is equal to the output current.

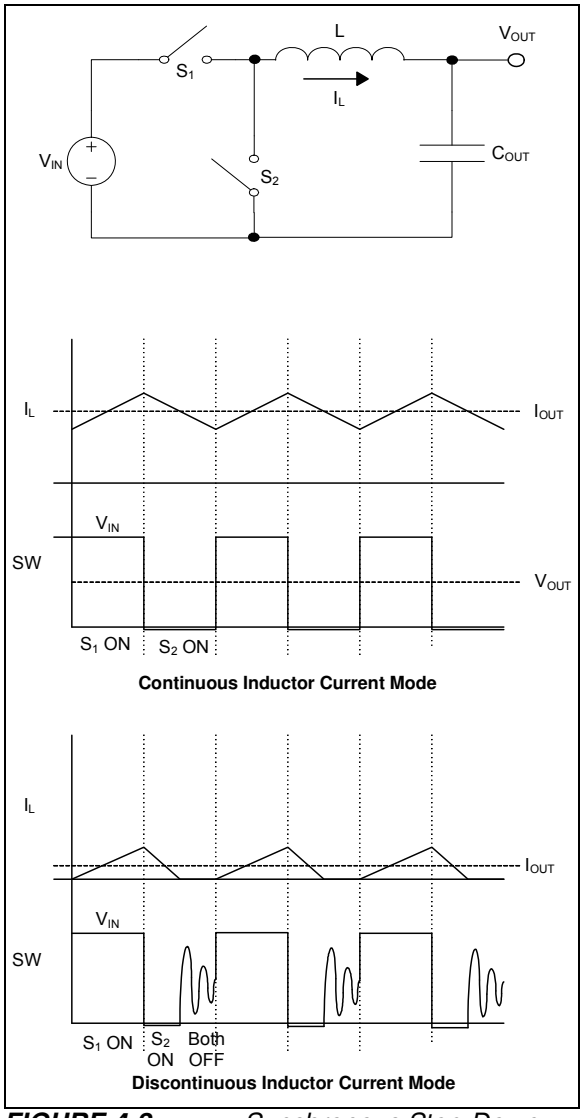


FIGURE 4-2: *Synchronous Step-Down Converter.*

4.2.2 PEAK CURRENT MODE CONTROL

The MCP16323 integrates a Peak Current Mode Control architecture, resulting in superior AC regulation while minimizing the number of voltage loop compensation components, and their size, for integration. Peak Current Mode Control takes a small portion of the inductor current, replicates it and compares this replicated current sense signal with the output of the integrated error voltage. In practice, the inductor current and the internal switch current are equal during the switch-on time. By adding this peak current sense to the system control, the step-down power train system can be approximated by a 1st order system rather than a 2nd order system. This reduces the system complexity and increases its dynamic performance.

For Pulse-Width Modulation (PWM) duty cycles that exceed 50%, the control system can become bimodal, where a wide pulse followed by a short pulse repeats instead of the desired fixed pulse width. To prevent this mode of operation, an internal compensating ramp is summed into the current sense signal.

4.2.3 PULSE WIDTH MODULATION (PWM)

The internal oscillator periodically starts the switching period, which in the MCP16323's case occurs every 1 µs or 1 MHz. With the high-side integrated N-Channel MOSFET turned on, the inductor current ramps up until the sum of the current sense and slope compensation ramp exceeds the integrated error amplifier output. Once this occurs, the high-side switch turns off and the low-side switch turns on. The error amplifier output slews up or down to increase or decrease the inductor peak current feeding into the output LC filter. If the regulated output voltage is lower than its target, the inverting error amplifier output rises. This results in an increase in the inductor current to correct for errors in the output voltage. The fixed frequency duty cycle is terminated when the sensed inductor peak current, summed with the internal slope compensation, exceeds the output voltage of the error amplifier. The PWM latch is set by turning off the high-side internal switch and preventing it from turning on until the beginning of the next cycle.

4.2.4 HIGH-SIDE DRIVE

The MCP16323 features an integrated high-side N-Channel MOSFET for high efficiency step-down power conversion. An N-Channel MOSFET is used for its low resistance and size (instead of a P-Channel MOSFET). The N-Channel MOSFET gate must be driven above its source to fully turn on the device, resulting in a gate-drive voltage above the input to turn on the high-side N-Channel. The high-side N-Channel source is connected to the inductor and boost cap or switch node. When the high-side switch is off and the low-side is on, the inductor current flows through the low-side switch, providing a path to recharge the boost cap from the boost voltage source. An internal boost-blocking diode is used to prevent current flow from the boost cap back into the output during the internal switch-on time. Prior to start-up, the boost cap has no stored charge to drive the switch. An internal regulator is used to "pre-charge" the boost cap. Once pre-charged, the switch is turned on and the inductor current flows. When the high-side switch turns off and the low-side turns on, current freewheels through the inductor and low-side switch, providing a path to recharge the boost cap. When the duty cycle approaches its maximum value, there is very little time for the boost cap to be recharged due to the short amount time that the low-side switch is on. Therefore, when the maximum duty cycle approaches, the switch node is forced off for 240 ns every eight cycles to ensure that the boost cap gets replenished.

5.0 APPLICATION INFORMATION

5.0.1 TYPICAL APPLICATIONS

The MCP16323 synchronous step-down converter operates over a wide input range, up to 18V maximum. Typical applications include generating a bias or V_{DD} voltage for PIC® microcontrollers, digital control system bias supply for AC-DC converters and 12V industrial input and similar applications.

5.0.2 ADJUSTABLE OUTPUT VOLTAGE CALCULATIONS

To calculate the resistor divider values for the MCP16323 adjustable version, use Equation 5-1. R_{TOP} is connected to V_{OUT}, R_{BOT} is connected to SGND, and both are connected to the V_{FB} input pin.

EQUATION 5-1: RESISTOR DIVIDER CALCULATION

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

EXAMPLE 5-1: 2.0V RESISTOR DIVIDER

V_{OUT} = 2.0V
V_{FB} = 0.9V
R_{BOT} = 10 kΩ
R_{TOP} = 12.2 kΩ (Standard Value = 12.3 kΩ)
V_{OUT} = 2.007V (using standard values)

EXAMPLE 5-2: 4.2V RESISTOR DIVIDER

V_{OUT} = 4.2V
V_{FB} = 0.9V
R_{BOT} = 10 kΩ
R_{TOP} = 36.7 kΩ (Standard Value = 36.5 kΩ)
V_{OUT} = 4.185V (using standard values)

The error amplifier is internally compensated to ensure loop stability. External resistor dividers, inductance and output capacitance, all have an impact on the control system and should be selected carefully and evaluated for stability. A 10 kΩ resistor is recommended as a good trade-off for quiescent current and noise immunity.

5.0.3 GENERAL DESIGN EQUATIONS

The step-down converter duty cycle can be estimated using Equation 5-2, while operating in Continuous Inductor Current Mode. This equation accounts for the forward drop of two internal N-Channel MOSFETS. As load current increases, the voltage drop in both internal switches will increase, requiring a larger PWM duty cycle to maintain the output voltage regulation. Switch voltage drop is estimated by multiplying the switch current times the switch resistance or R_{DSON}.

EQUATION 5-2: CONTINUOUS INDUCTOR CURRENT DUTY CYCLE

$$D = \frac{V_{OUT} + (I_{LSW} \times R_{DSONL})}{V_{IN} - (I_{HSW} \times R_{DSONH})}$$

5.0.4 INPUT CAPACITOR SELECTION

The step-down converter input capacitor must filter the high-input ripple current, as a result of pulsing or chopping the input voltage. The MCP16323 input voltage pin is used to supply voltage for the power train and as a source for internal bias. A low equivalent series resistance (ESR), preferably a ceramic capacitor, is recommended. The necessary capacitance is dependent upon the maximum load current and source impedance. Three capacitor parameters to keep in mind are the voltage rating, equivalent series resistance and the temperature rating. For wide temperature range applications, a multi-layer X7R dielectric is recommended, while for applications with limited temperature range, a multilayer X5R dielectric is acceptable. The input capacitor voltage rating must be V_{IN} plus margin.

5.0.5 OUTPUT CAPACITOR SELECTION

The output capacitor provides a stable output voltage during sudden load transients, and reduces the output voltage ripple. As with the input capacitor, X5R and X7R ceramic capacitors are well suited for this application.

The MCP16323 is internally compensated, so the output capacitance range is limited. See **TABLE 5-1: "Capacitor Value Range"** for the recommended output capacitor range.

The amount and type of output capacitance and equivalent series resistance will have a significant effect on the output ripple voltage and system stability. The range of the output capacitance is limited due to the integrated compensation of the MCP16323.

The output voltage capacitor rating should be a minimum of V_{OUT} plus margin.

TABLE 5-1: CAPACITOR VALUE RANGE

Parameter	Min	Max
C_{IN}	8 µF	None

TABLE 5-1: CAPACITOR VALUE RANGE

Parameter	Min	Max
C_{OUT}	33 µF	None

5.0.6 INDUCTOR SELECTION

The MCP16323 is designed to be used with small surface mount inductors. Several specifications should be considered prior to selecting an inductor. To optimize system performance, low ESR inductors should be used.

EQUATION 5-3: INDUCTOR CURRENT RIPPLE

$$\Delta I_L = \frac{V_L}{L} \times t_{ON}$$

EXAMPLE 5-3: MCP16323 PEAK INDUCTOR CURRENT – 3A

V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 3A
L = 4.7 µH

$$I_{LPK} = \frac{\Delta I_L}{2} + I_{OUT}$$

Inductor ripple current = 509 mA

Inductor peak current = 3.255A

An inductor saturation rating minimum of 3.255A is recommended. A trade-off between size, cost and efficiency is made to achieve the desired results.

TABLE 5-2: MCP16323 RECOMMENDED INDUCTORS

Part Number	Value (µH)	DCR (Ω)	I_{SAT} (A)	Size WxLxH (mm)
Coilcraft®				
MSS6132-472	4.7	0.056	2.84	6.1x6.1x3.2
LPS6225-472	4.7	0.065	3.2	6.2x6.2x2.5
MSS7341-502	4.7	0.024	3.16	7.3x7.3x4.1
DO1813H-472	4.7	0.054	2.6	8.89x6.1x5.0
Wurth Elektronik®				
7447785004	4.7	0.06	2.5	5.9x6.2x3.3
7447786004	4.7	0.057	2.8	5.9x6.2x5.1
7447789004	4.7	0.033	3.9	7.3x3.2x1.5
EPCOS®				
B82464G2	4.7	0.033	3.1	10.4x10.4x3.0
B82464A2	4.7	0.03	4.5	10.4x10.4x3.0

5.0.7 BOOST CAPACITOR

The boost capacitor is used to supply current for the internal high-side drive circuitry that is above the input voltage. The boost capacitor must store enough energy to completely drive the high-side switch on and off. A 22 nF X5R or X7R capacitor is recommended for all applications. The boost capacitor maximum voltage is 5.5V, so a 6.3V or 10V rated capacitor is recommended.

5.0.8 THERMAL CALCULATIONS

The MCP16323 is available in a 3x3 QFN-16 package. By calculating the power dissipation and applying the package thermal resistance (θ_{JA}), the junction temperature is estimated. The maximum continuous junction temperature rating for the MCP16323 is +125°C.

To quickly estimate the internal power dissipation for the switching step-down regulator, an empirical calculation using measured efficiency can be used. Given the measured efficiency, the internal power dissipation is estimated in Equation 5-4. This power dissipation includes all internal and external component losses. For a quick internal estimate, subtract the estimated inductor ESR loss from the P_{DIS} calculation in Equation 5-4.

EQUATION 5-4: TOTAL POWER DISSIPATION ESTIMATE

$$P_{DIS} = \frac{V_{OUT} \times I_{OUT}}{Efficency} - (V_{OUT} \times I_{OUT})$$

The difference between the first term, input power, and the second term, power delivered, is the total system power dissipation. The inductor losses are estimated by $P_L = I_{OUT}^2 \times L_{ESR}$.

EXAMPLE 5-4: POWER DISSIPATION

V_{IN} = 12V
V_{OUT} = 5.0V
I_{OUT} = 3 A
Efficiency = 88%
Total System Dissipation = 2.05 W
L_{ESR} = 0.02 Ω
P_L = 180 mW

MCP16323 internal power dissipation estimate:

$P_{DIS} - P_L$ = 1.87 W
θ_{JA} = 38.5°C/W
Estimated Junction = +71.995°C

Note 1: θ_{JA} = 38.5°C/W for a 4-layer FR4 Printed Circuit Board with a 13.5 in^2, 1 oz internal copper ground plane.

2: A smaller ground plane will result in a larger θ_{JA} temperature rise.

5.0.9 PCB LAYOUT INFORMATION

Good printed circuit board layout techniques are important to any switching circuitry, and switching power supplies are no different. When wiring the switching high-current paths, short and wide traces should be used. Therefore, it is important that the input and output capacitors be placed as close as possible to the MCP16323 to minimize the loop area.

The feedback resistors and feedback signal should be routed away from the switching node and the switching current loop. When possible, ground planes and traces should be used to help shield the feedback signal and minimize noise and magnetic interference.

A good MCP16323 layout starts with C_{IN} placement. C_{IN} supplies current to the input of the circuit when the switch is turned on. In addition to supplying high-frequency switch current, C_{IN} also provides a stable voltage source for the internal MCP16323 circuitry. Unstable PWM operation can result if there are excessive transients or ringing on the V_{IN} pin of the MCP16323 device. In Figure 5-1, C_{IN} is placed close to the V_{IN} pins. A ground plane on the bottom of the board provides a low resistive and low inductive path for the return current. The next priority in placement is the freewheeling current loop formed by C_{OUT} and L while strategically placing the C_{OUT} return close to C_{IN} return. Next, C_{BOOST} should be placed between the boost pin and the switch node pin. This leaves space close to the MCP16323 V_{FB} pin to place R_{TOP} and R_{BOT}. R_{TOP} and R_{BOT} are routed away from the switch node so noise is not coupled into the high-impedance V_{FB} input.

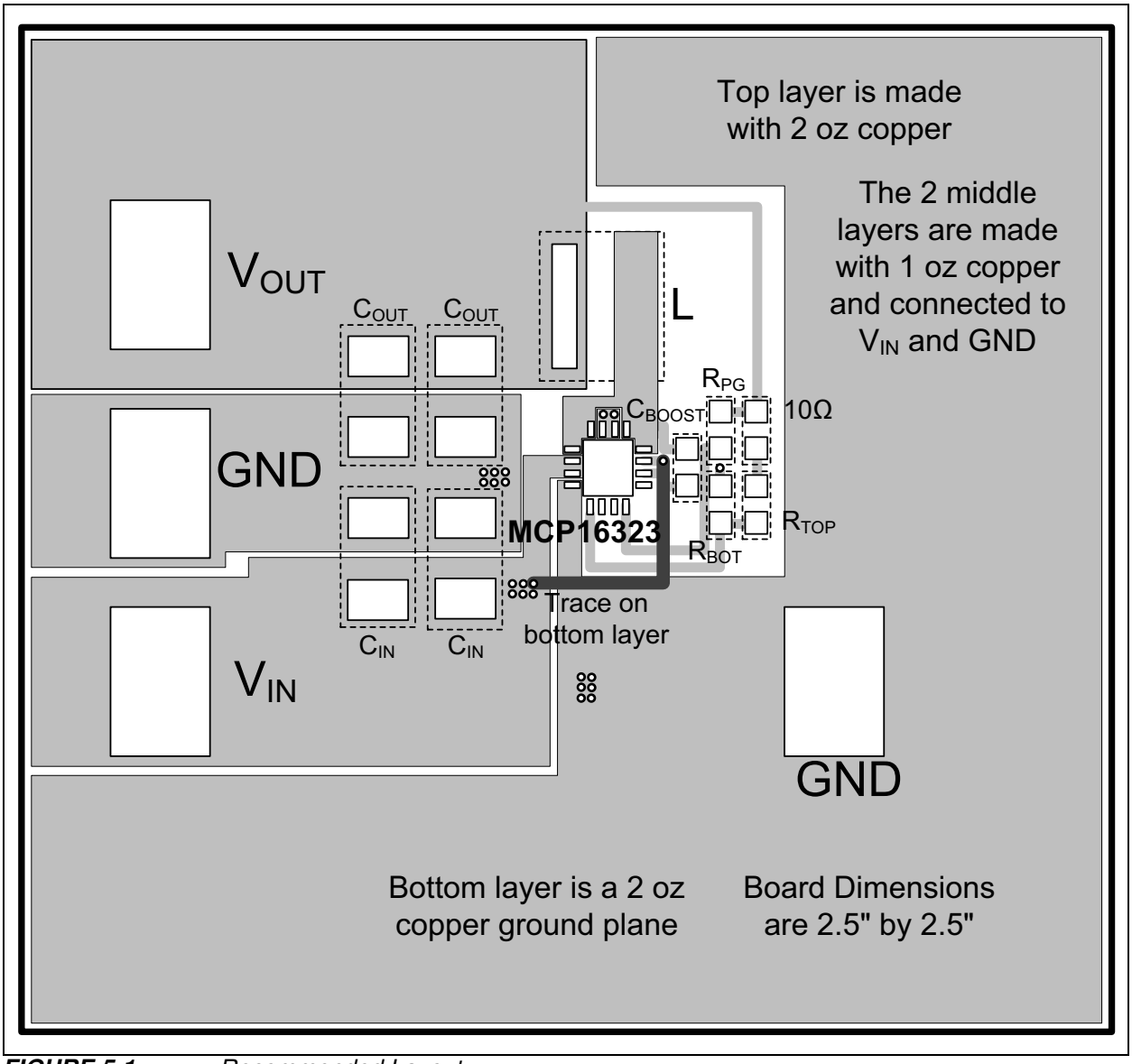


FIGURE 5-1: *Recommended Layout.*

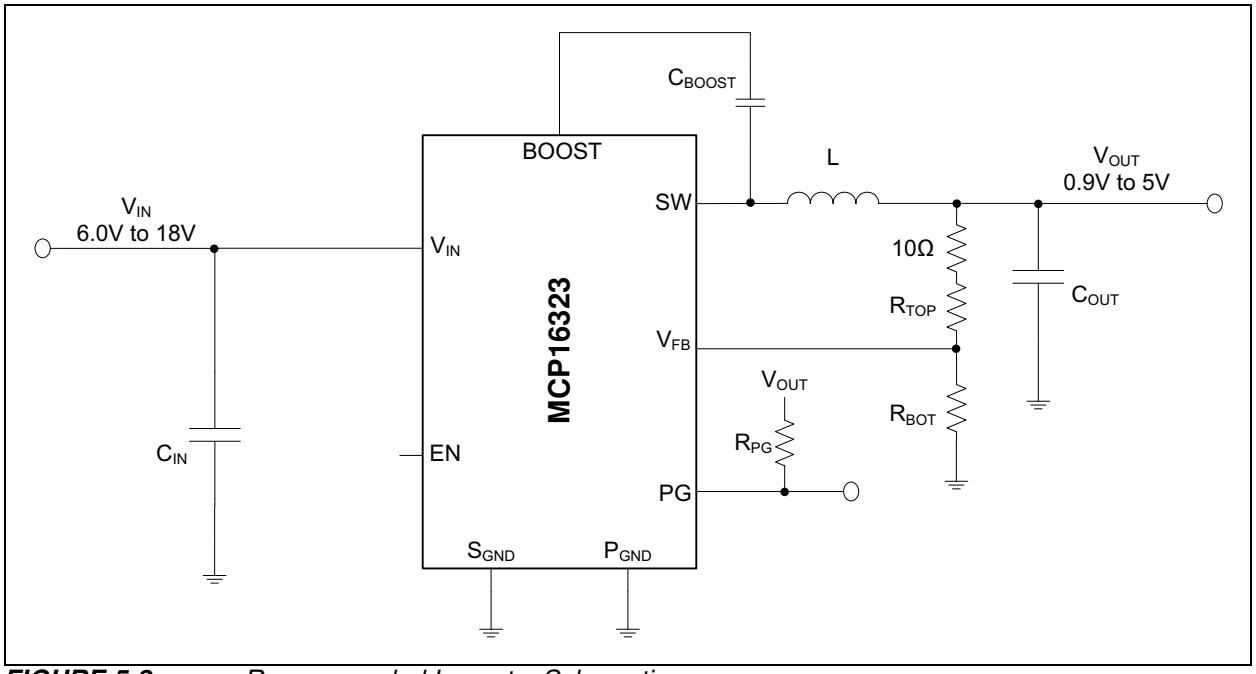


FIGURE 5-2: *Recommended Layout – Schematic.*

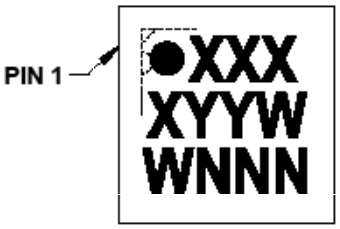
TABLE 5-3: RECOMMENDED LAYOUT COMPONENTS

Component	Value
C_{IN}	2 x 10 µF
C_{OUT}	2 x 22 µF
L	4.7 µH
R_{TOP}	36.5 kΩ
R_{BOT}	10 kΩ
R_{PG}	10 kΩ
C_{BOOST}	22 nF

6.0 PACKAGING INFORMATION

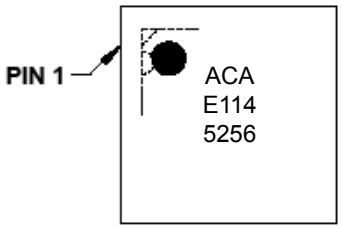
6.1 Package Marking Information

16-Lead QFN (3x3x0.9 mm)



Part Number	Code
MCP16323T-150E/NG	ACA
MCP16323T-180E/NG	ACB
MCP16323T-250E/NG	ACC
MCP16323T-330E/NG	ACD
MCP16323T-500E/NG	ACE
MCP16323T-ADJE/NG	ACF

Example

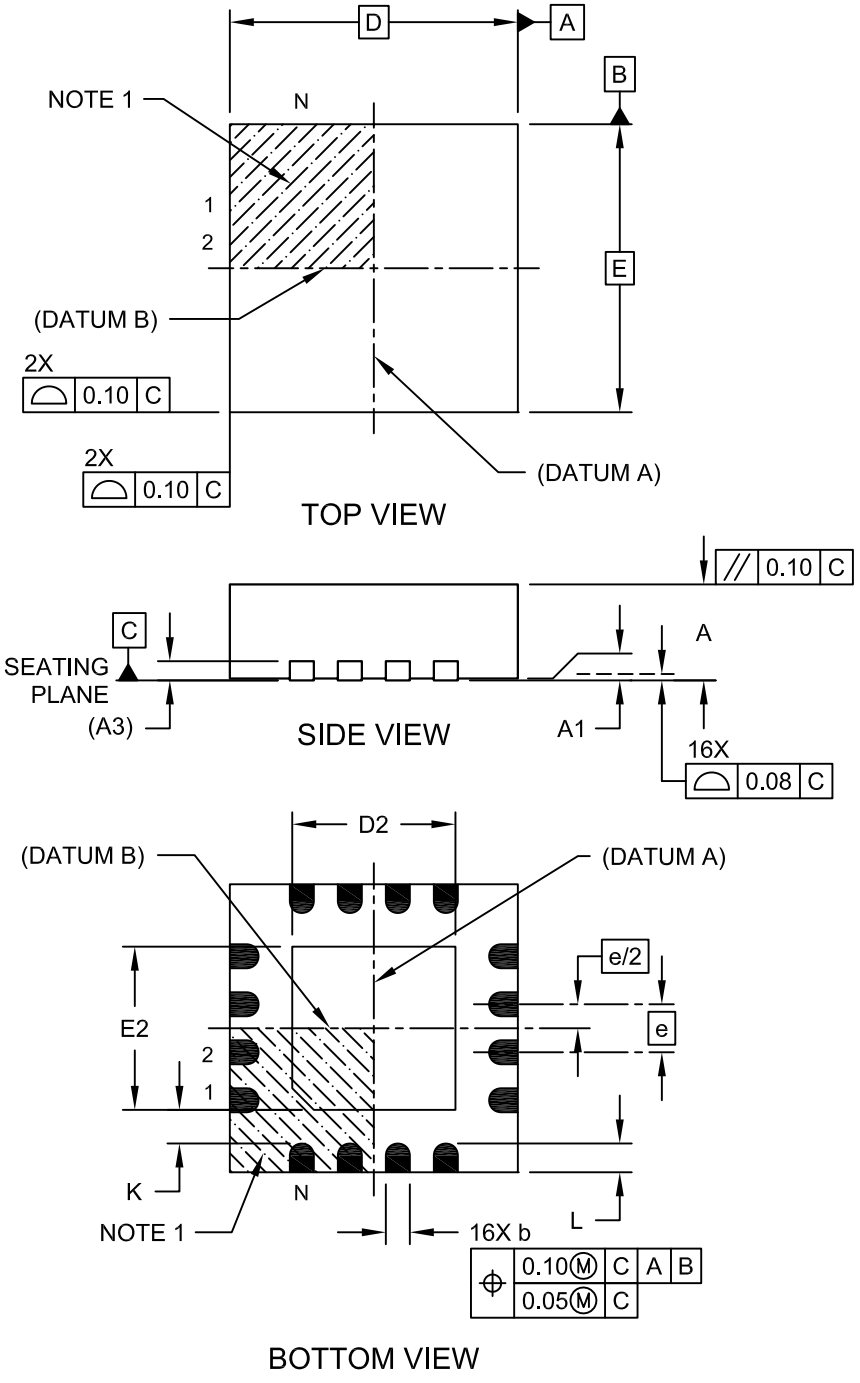


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Plastic Quad Flat, No Lead Package (NG) - 3x3x0.9 mm Body [QFN]

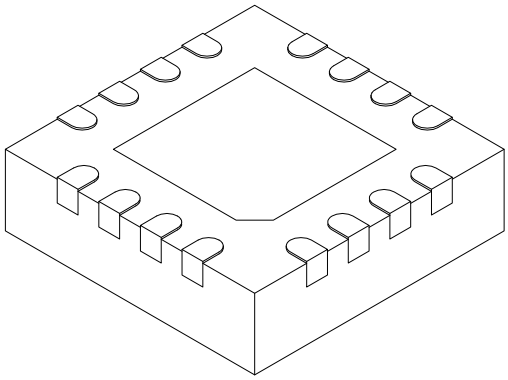
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-197A Sheet 1 of 2

16-Lead Plastic Quad Flat, No Lead Package (NG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.55	1.70	1.80
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.55	1.70	1.80
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.20	0.30	0.40
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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