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MCP1632

High-Speed, Low-Side PWM Controller

Features:

- High-Speed PWM Controller with Integrated Low-Side MOSFET Driver
- Multiple Switching Frequency Options (f_{SW}):
  - 300 kHz
  - 600 kHz
- Adjustable Reference Voltage Generator
- Adjustable Soft Start
- Internal Slope Compensation
- Shutdown Input Pin (EN)
- Low Operating Current: < 5 mA (typical)
- Undervoltage Lockout (UVLO) Protection
- Output Short Circuit Protection
- Overtemperature Protection
- Operating Temperature Range:
  - -40°C to +125°C

Applications:

- Switch Mode Power Supplies
- Brick DC-DC Converters
- Battery Charger Applications
- LED Drivers

Related Literature:

- “MCP1632 300 kHz Boost Converter Demo Board User’s Guide”, Microchip Technology Inc., DS20005252A, 2013

Description:

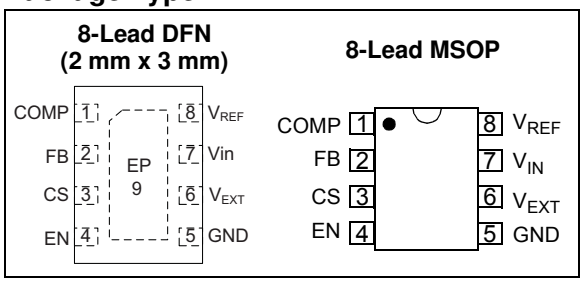
The MCP1632 high-speed PWM controller is a pulse-width modulator developed for stand-alone power supply applications. The MCP1632 includes a high-speed analog control loop, a logic-level MOSFET driver, an internal oscillator, a reference voltage generator, and internal slope compensation. This high level of integration makes it an ideal solution for standalone SMPS applications. MCP1632 is suitable for use in topologies requiring a low-side MOSFET control, such as Boost, Flyback, SEPIC, Ćuk, etc. Typical applications include battery chargers, intelligent power systems, brick DC-DC converters, LED drivers. Due to its low power consumption, the MCP1632 PWM controller is recommended for battery-operated applications.

The MCP1632 offers a Peak Current mode control in order to achieve consistent performance regardless of the topology of the power train or the operating conditions. In addition, the MCP1632 can implement the Voltage Mode Control for cost-sensitive solutions.

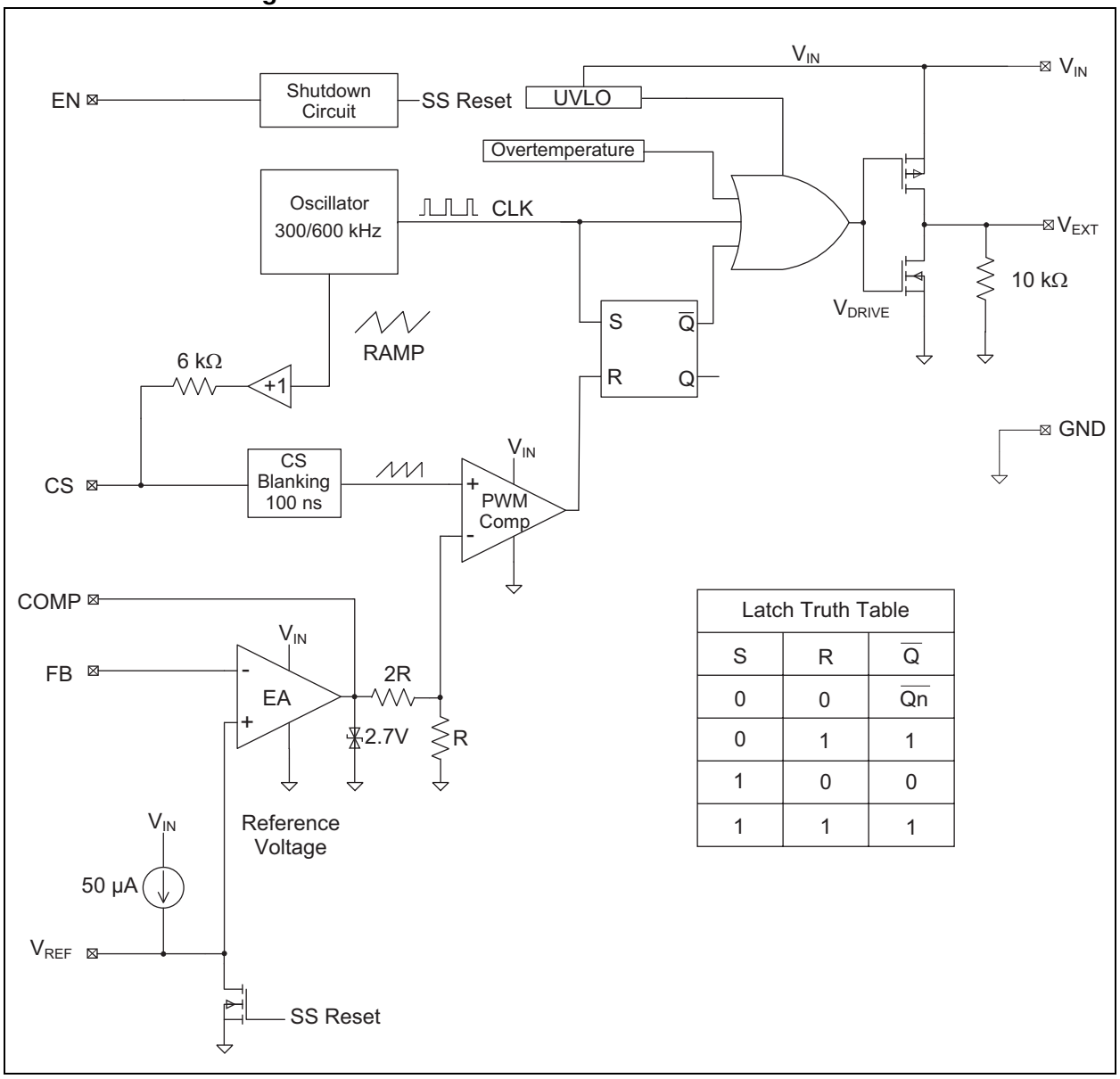
The MCP1632 PWM controller can be easily interfaced with PIC microcontrollers in order to develop an intelligent power solution.

Additional features include: UVLO, overtemperature and overcurrent protection, shutdown capability (EN pin) and an adjustable soft start option.

Package Type

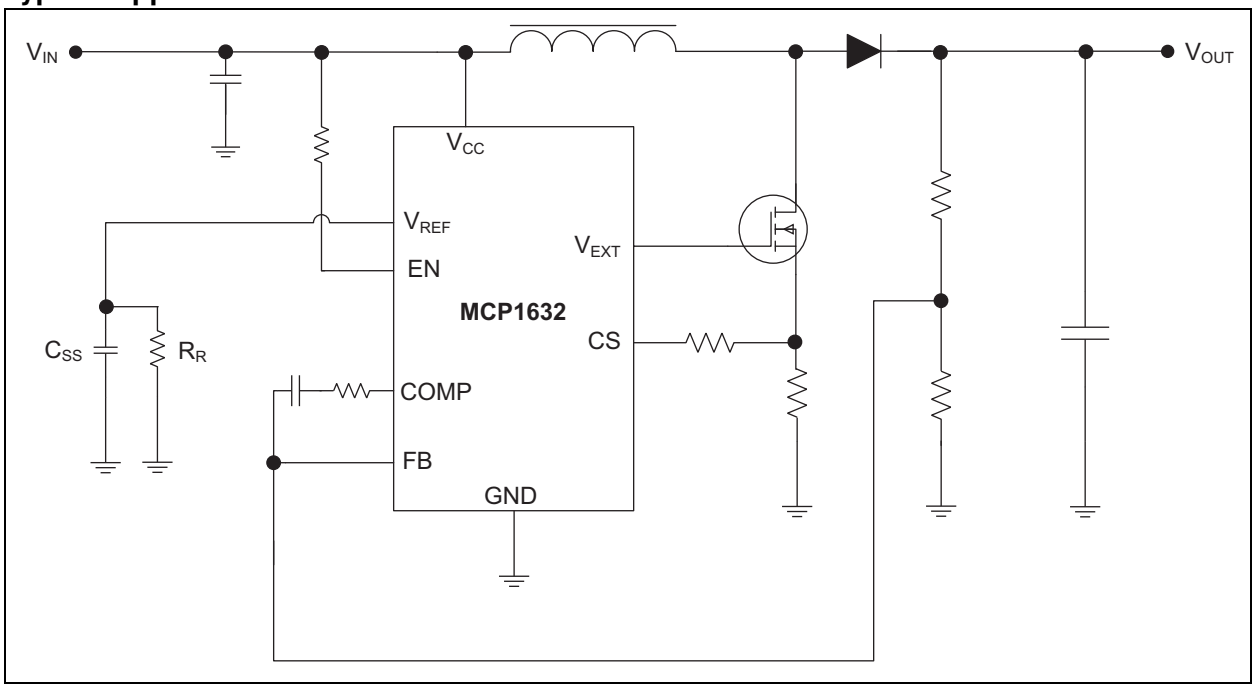


Functional Block Diagram

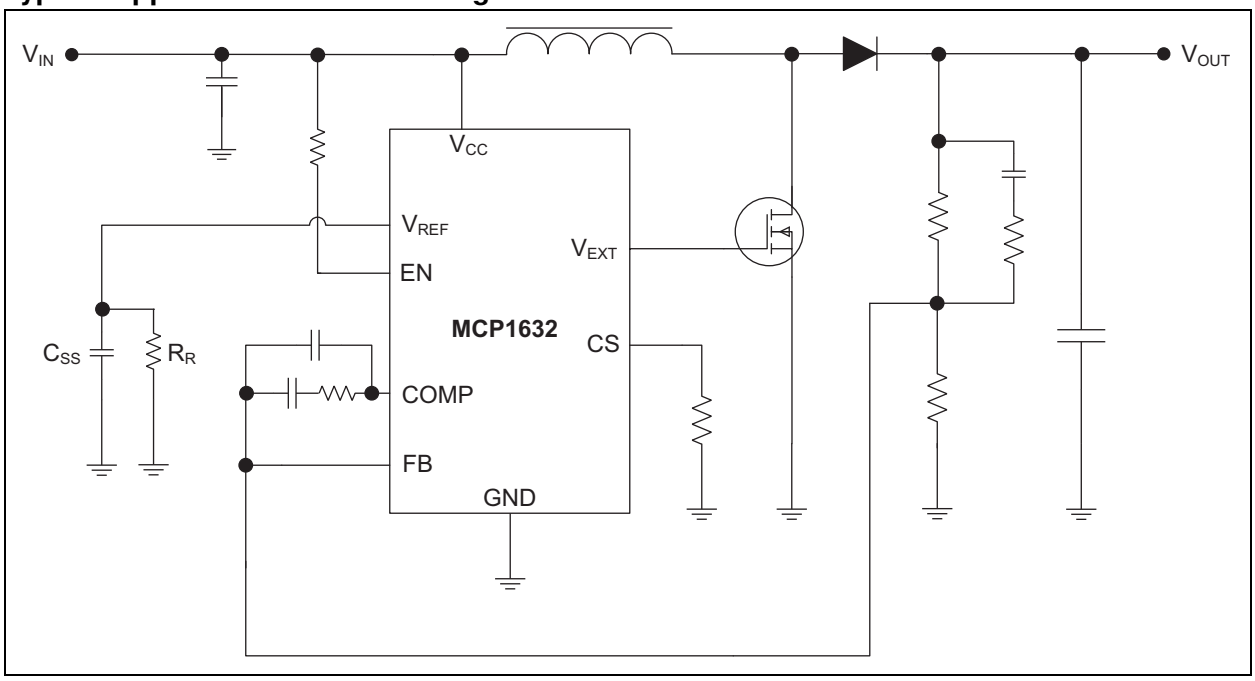


Latch Truth Table		
S	R	$\overline{Q}$
0	0	$\overline{Qn}$
0	1	1
1	0	0
1	1	1

Typical Application Circuit – Peak Current Mode Control



Typical Application Circuit – Voltage Mode Control



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD}.....6.0V
Maximum Voltage on Any Pin . (V_{GND} – 0.3)V to (V_{IN} + 0.3)V
V_{EXT} Short Circuit Current .....Internally Limited
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature, T_J .....+150°C
Continuous Operating Temperature Range ..-40°C to +125°C
ESD protection on all pins, HBM..... 2 kV

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, V_{IN} = 3.0V to 5.5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, V_{IN} for typical values = 5.0V, T_A = -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Voltage						
Input Operating Voltage	V_{IN}	3.0	—	5.5	V	
Input Quiescent Current	$I(V_{IN})$	—	5	7.5	mA	I_{EXT} = 0 mA
Input Shutdown Current	$I(V_{IN})_{SHDN}$	—	—	2	µA	EN = 0V
EN Input						
EN Input Voltage Low	EN_{LOW}	—	—	0.8	V	
EN Input Voltage High	EN_{HIGH}	75	—	—	% of V_{IN}	
Delay Time	—	—	190	210	µs	EN goes from low to high (**Note 1**)
			40	60	µs	EN goes from high to low (**Note 1**)
Internal Oscillator						
Internal Oscillator Range	F_{OSC}	250	300	350	kHz	Two options Refer to **Section 4.8 "Internal Oscillator"**.
		510	600	690		
Reference Voltage Section						
Reference Voltage Input Range	V_{REF}	0	—	V_{IN}	V	**Note 1** Refer to **Section 4.7 "Reference Voltage Generator"** for details.
Internal Constant Current Generator	I_{REF}	48	50	52	µA	Refer to **Section 4.7 "Reference Voltage Generator"** for details.
Error Amplifier						
Input Offset Voltage	V_{OS}	-4	0.1	+4	mV	
Error Amplifier	PSRR	65	80	—	dB	V_{IN} = 3.0V to 5.0V, V_{CM} = 1.2V (**Note 1**)
Common-Mode Input Range	V_{CM}	GND - 0.3	—	V_{IN}	V	**Note 1**
Common-Mode Rejection Ratio	CMRR	60	80	—	dB	V_{IN} = 5V, V_{CM} = 0V to 2.5V (**Note 1**)
Open-Loop Voltage Gain	A_{VOL}	80	95	—	dB	R_L = 5 kΩ to V_{IN}/2, 100 mV < V_{EAOUT} < V_{IN} - 100 mV, V_{CM} = 1.2V (**Note 1**)
Low-Level Output	V_{OL}	—	25	50	mV	R_L = 5 kΩ to V_{IN}/2
Gain Bandwidth Product	GBWP	3.5	5	—	MHz	V_{IN} = 5V (**Note 1**)
Error Amplifier Sink Current	I_{SINK}	4	8	—	mA	V_{IN} = 5V, V_{REF} = 1.2V, V_{FB} = 1.4V, V_{COMP} = 2.0V

Note 1: Ensured by design. Not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, V_{IN} = 3.0V to 5.5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, V_{IN} for typical values = 5.0V, T_A = -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Error Amplifier Source Current	I_{SOURCE}	4	6	—	mA	V_{IN} = 5V, V_{REF} = 1.2V, V_{FB} = 1.0V, V_{COMP} = 2.0V, Absolute Value
Current Sense Input						
Maximum Current Sense Signal	V_{CS_MAX}	0.8	0.9	0.97	V	Set by maximum error amplifier clamp voltage, divided by 3 (**Note 1**)
Blanking Time	T_{BLANK}	80	100	130	ns	**Note 1**
Delay from CS to V_{EXT}	T_{CS_VEXT}	—	—	35	ns	Excluding the blanking time (**Note 1**)
Current Sense Input Bias Current	I_{CS_B}	—	-0.1	—	µA	**Note 1**
PWM Section						
Minimum Duty Cycle	DC_{MIN}	—	—	0	%	V_{FB} = V_{REF} + 0.1V, V_{CS} = GND (**Note 1**)
Maximum Duty Cycle	DC_{MAX}	80	85	95	%	
Slope Compensation Ramp Generator						
Ramp Amplitude	V_{RAMP}	0.8	0.9	1	V_{PP}	Refer to **Section 4.6 "Slope Compensation"** for details.
DC Offset Low	—	0.15	0.32	0.45	V	Refer to **Section 4.6 "Slope Compensation"** for details.
DC Offset High	—	1.12	1.22	1.32	V	Refer to **Section 4.6 "Slope Compensation"** for details.
Ramp Generator Output Impedance	Z_{RG}	5.5	6	6.5	kΩ	Refer to **Section 4.6 "Slope Compensation"** for details.
Internal Driver						
R_{DSon} P-channel	R_{DSon_P}	—	10	30	Ω	
R_{DSon} N-channel	R_{DSon_N}	—	7	30	Ω	
V_{EXT} Rise Time	T_{RISE}	—	—	18	ns	C_L = 100 pF Typical for V_{IN} = 3V (**Note 1**)
V_{EXT} Fall Time	T_{FALL}	—	—	18	ns	C_L = 100 pF Typical for V_{IN} = 3V (**Note 1**)
Protection Features						
Undervoltage Lockout	UVLO	2.6	—	2.9	V	V_{IN} falling, V_{EXT} low state when in UVLO
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	50	110	180	mV	
Thermal Shutdown	T_{SHD}	—	150	—	°C	**Note 1**
Thermal Shutdown Hysteresis	T_{SHD_HYS}	—	20	—	°C	**Note 1**

Note 1: Ensured by design. Not production tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: V_{IN} = 3.0V to 5.5V, F_{OSC} = 600 kHz, C_{IN} = 0.1 µF. T_A = -40°C to +125°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_A	-40	—	+125	°C	Steady state
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Thermal Package Resistances						
Thermal Resistance, 8L-DFN (2 mm x 3 mm)	θ_{JA}	—	75	—	°C/W	Typical 4-layer board with two interconnecting vias.
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	Typical 4-layer board.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

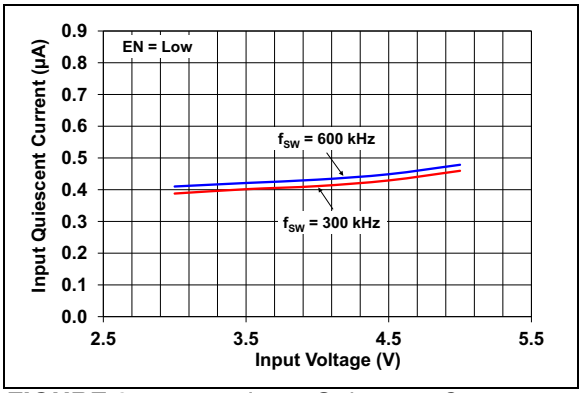


FIGURE 2-1: *Input Quiescent Current vs. Input Voltage (EN = Low).*

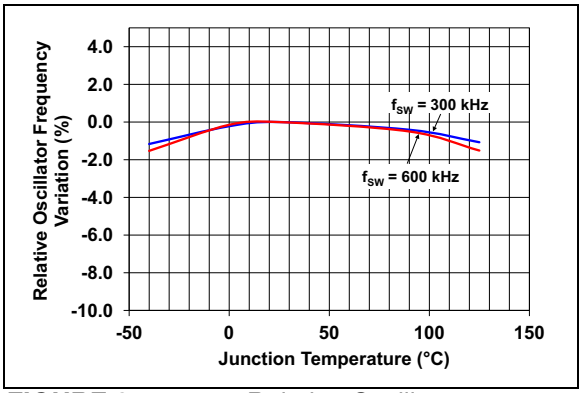


FIGURE 2-4: *Relative Oscillator Frequency Variation vs. Junction Temperature.*

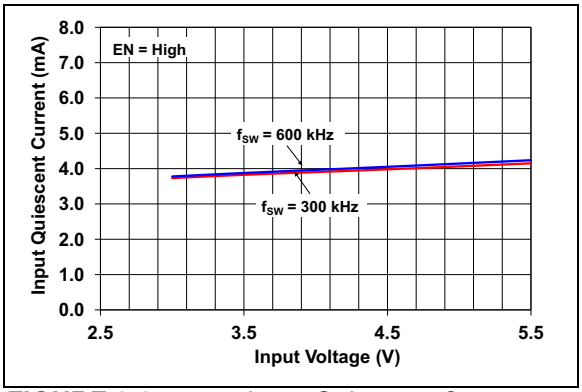


FIGURE 2-2: *Input Quiescent Current vs. Input Voltage (EN = High).*

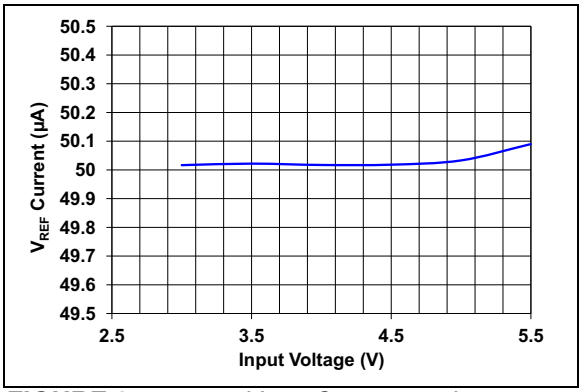


FIGURE 2-5: *V_{REF} Current vs. Input Voltage.*

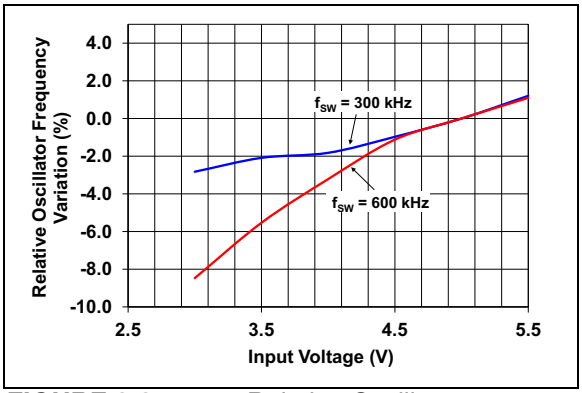


FIGURE 2-3: *Relative Oscillator Frequency Variation vs. Input Voltage.*

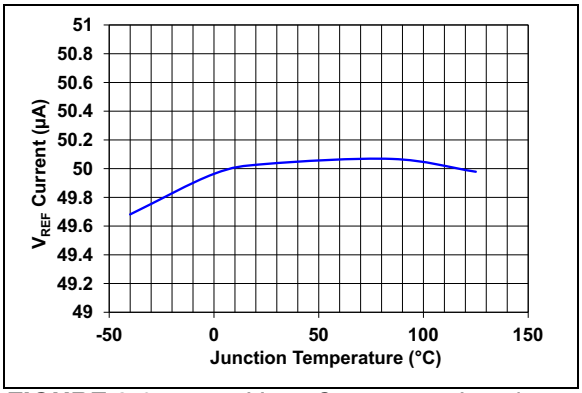


FIGURE 2-6: *V_{REF} Current vs. Junction Temperature.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

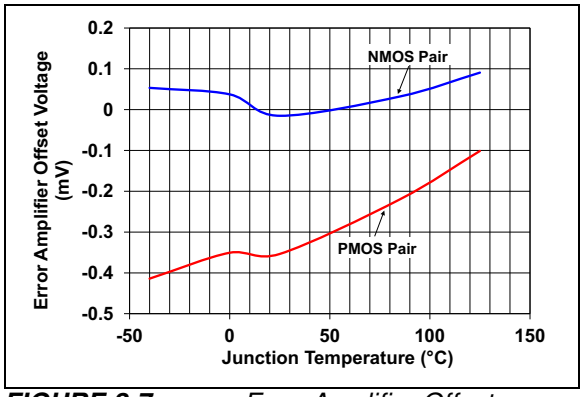


FIGURE 2-7: *Error Amplifier Offset Voltage vs. Temperature.*

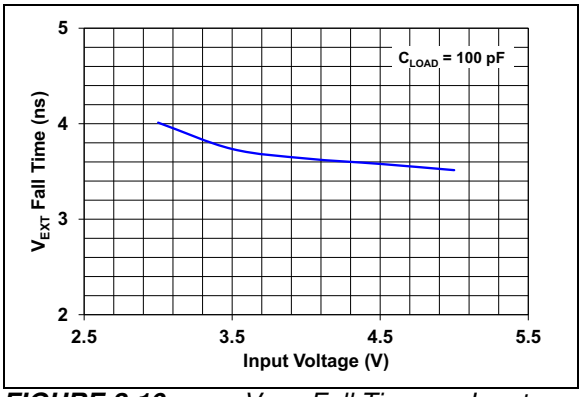


FIGURE 2-10: *V_{EXT} Fall Time vs. Input Voltage.*

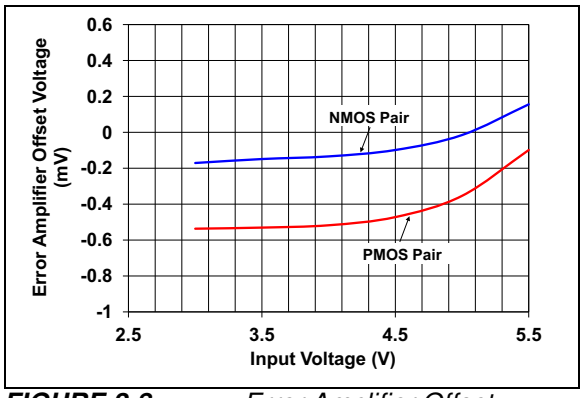


FIGURE 2-8: *Error Amplifier Offset Voltage vs. Input Voltage.*

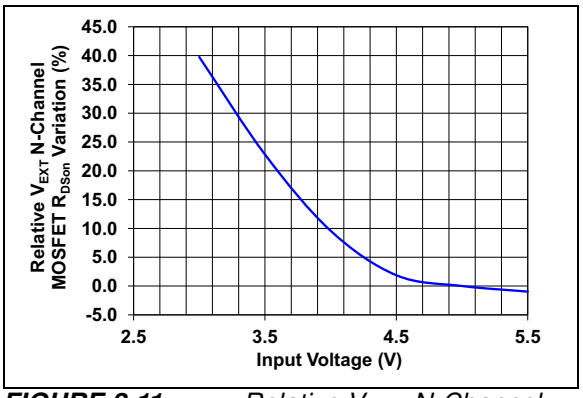


FIGURE 2-11: *Relative V_{EXT} N-Channel MOSFET R_{DSon} Variation vs. Input Voltage.*

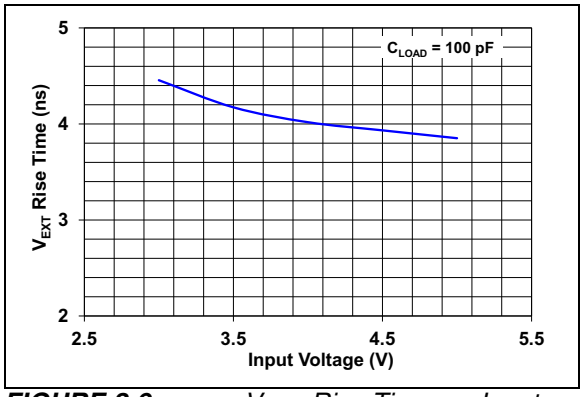


FIGURE 2-9: *V_{EXT} Rise Time vs. Input Voltage.*

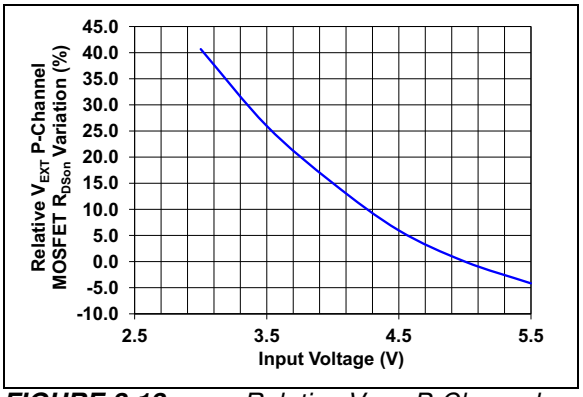


FIGURE 2-12: *Relative V_{EXT} P-Channel MOSFET R_{DSon} Variation vs. Input Voltage.*

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

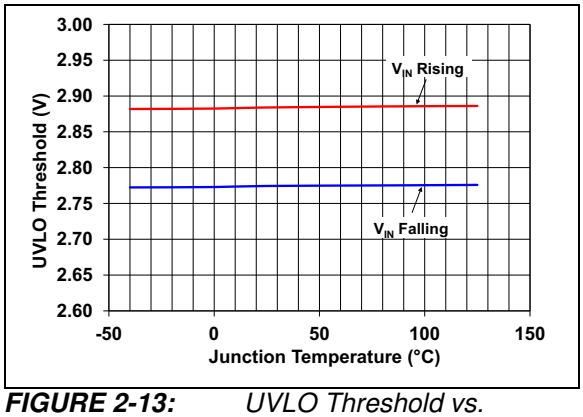


FIGURE 2-13: *UVLO Threshold vs. Temperature.*

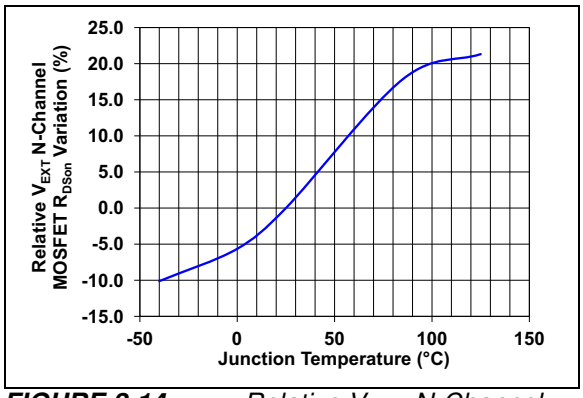


FIGURE 2-14: *Relative V_{EXT} N-Channel MOSFET R_{DSon} Variation vs. Junction Temperature.*

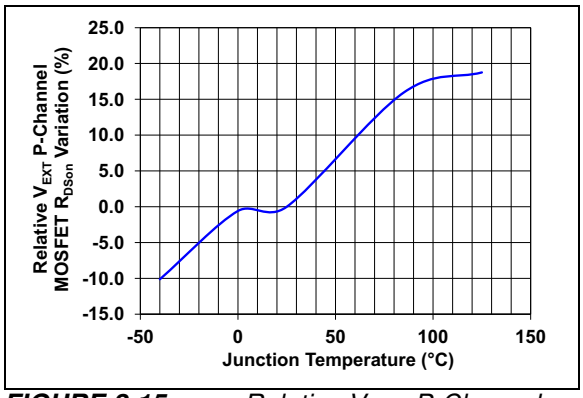


FIGURE 2-15: *Relative V_{EXT} P-Channel MOSFET R_{DSon} Variation vs. Junction Temperature.*

NOTES:

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

DFN/MSOP	Name	Function
1	COMP	Error Amplifier Output
2	FB	Error Amplifier Inverting Input
3	CS	Current Sense Input
4	EN	Enable Input
5	GND	Circuit Ground
6	V_{EXT}	External Driver Output
7	V_{IN}	Input Bias
8	V_{REF}	Reference Voltage Input/Internal Constant Current Generator Output
9	EP	Exposed Thermal Pad (EP); must be connected to GND

3.1 Error Amplifier Output (COMP)

COMP is the internal error amplifier output pin. External compensation is connected from the FB pin to the COMP pin for control-loop stabilization. Type II or III compensation networks must be used depending on the application. An internal voltage clamp is used to limit the maximum COMP pin voltage to 2.7V (typical). This clamp is used to set the maximum peak current in the power system switch by setting a maximum limit on the CS input for Peak Current Mode control systems.

3.2 Error Amplifier Inverting Input (FB)

FB is the internal error amplifier inverting input pin. The output (voltage or current) is sensed and fed back to the FB pin for regulation. Inverting or negative feedback is used.

3.3 Current Sense Input (CS)

This is the input for the switch current used for Peak Current Mode control. A blanking period of 100 ns (typical) for CS signal is provided to avoid leading edge spikes that can cause false PWM reset. The normal PWM duty cycle will be terminated when the voltage on the CS pin (including the slope compensation ramp) is equal to the output of the error amplifier divided by 3. For Current Mode operation, the CS pin will control the PWM output on a cycle-by-cycle basis. The internal error amplifier output is clamped to 2.7V (nominal) and divided by 3, so the maximum voltage of the CS pin is 0.9V. By limiting the inverting pin of the high-speed comparator to 0.9V, a current sense limit is established for all input bias voltage conditions (cycle-by-cycle overcurrent protection). To avoid the instability of the Peak Current Mode control when the duty cycle is higher than 50%, a slope compensation ramp generator is internally provided. This circuit will add to the CS signal an artificially generated ramp to avoid sub-harmonic oscillations. The amplitude of the slope compensation ramp is adjustable with one external resistor.

If this pin is left open, the PWM Controller will operate in Voltage Mode Control. In this mode, the external switching MOSFET transistor is not protected against overcurrent conditions. Certain limitations related to the stability of the closed-loop system must be taken into account by the designer when the part operates in Voltage Mode Control. Refer to **Section 5.2 "Operation in Voltage Mode Control"** for details about the operation in Voltage Mode Control.

3.4 Enable Input (EN)

When this pin is connected to GND (logic "Low") for more than 50 µs (typical), the chip will go into Shutdown state. A logic "High" enables the normal operation of the MCP1632 device. When the device is disabled, the V_{EXT} output is held low. Do not let the EN pin float. If not used, connect EN to V_{IN} through a 10 kΩ resistor.

3.5 Circuit Ground (GND)

Connect the circuit ground to the GND pin. For most applications, this should be connected to the analog (quiet) ground plane. Effort should be made to minimize the noise on this ground, as it can adversely affect the cycle-by-cycle comparison between the CS input and the error amplifier output.

3.6 External Driver Output (V_{EXT})

V_{EXT} is the internal MOSFET driver output pin, used to drive the external transistor. For high-power or high-side drives, this output should be connected to the logic-level input of an appropriate MOSFET driver. For low-power, low-side applications, the V_{EXT} pin can be used to directly drive the gate of an N-channel MOSFET.

3.7 Input Bias (V_{IN})

V_{IN} is the input voltage pin. Connect the input voltage source to the V_{IN} pin. For normal operation, the voltage on the V_{IN} pin should range from +3.0V to +5.5V. A bypass capacitor of at least 0.1 µF should be connected between the V_{IN} pin and the GND pin. This decoupling capacitor must be located as close as possible to the controller package.

3.8 Reference Voltage Input/Internal Constant Current Generator Output (V_{REF})

This pin is the output of the internal Constant Current Generator (50 µA typical). An external resistor must be connected between this pin and GND. The current flowing in this resistor will set the reference voltage. Optionally, a capacitor may also be connected between this pin and GND to set the soft start ramp behavior. This pin may be overdriven by an external voltage source, enabling the reference voltage to be controlled externally. Refer to **Section 4.7 "Reference Voltage Generator"** for details.

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP1632 device is comprised of an internal oscillator, an internal constant current generator, a high-speed comparator, a high-bandwidth amplifier, an internal ramp generator for slope compensation and logic gates, and is intended to be used to develop a stand-alone switch-mode power supply. There are two (orderable) switching frequency options for this device: 300 kHz or 600 kHz. Refer to Functional Block Diagram for details about the internal functional blocks.

4.2 PWM Circuitry

MCP1632 implements a typical Peak Current Mode control loop. The V_{EXT} output of the MCP1632 device is determined by the output level of the internal high-speed comparator and the level of the internal CLK signal. When the CLK signal level is high, the PWM output (V_{EXT}) is forced low, limiting the maximum duty cycle to approximately 85% (typical). When the CLK signal is low, the PWM output is determined by the output level of the internal high-speed comparator. During UVLO, the V_{EXT} pin is held in low state. During overtemperature operation, the V_{EXT} pin is high-impedance (10 kΩ to ground, typical).

4.3 Normal Cycle-by-Cycle Control

The beginning of a PWM cycle is defined by the internal CLK signal (a transition from high to low). Refer to Figure 4-1 for the detailed timing operation of the MCP1632 PWM controller.

For normal operation, the state of the high-speed comparator output (R) is low and the $\overline{Q}$ output of the latch is low. On the high-to-low transition of the CLK signal, the $\overline{SR}$ inputs to the high-speed latch are both low and the $\overline{Q}$ output will remain unchanged (low). The output of the OR gate (V_{DRIVE}) will transition from high to low, turning on the P-Channel drive transistor in the output stage of the PWM. This will change the PWM output (V_{EXT}) from low to high, turning on the power train MOSFET and ramping current in the power train magnetic device. The sensed current in the magnetic device is fed into the CS input, shown as a ramp, and increases linearly until it reaches the same level as the divided down output of the error amplifier at the non-inverting input of the high-speed comparator. The comparator output (R) changes state (low to high) and resets the PWM latch. The $\overline{Q}$ output transition from low to high turns off the V_{EXT} drive to the external MOSFET driver, thus terminating the current conduction cycle. The CLK signal will transition from low to high while the V_{EXT} pin remains unchanged. If the CS input pin never reaches the same level as the error amplifier output, the low-to-high transition on the CLK signal terminates the current switching cycle. This would be considered as the maximum duty cycle. In either case, while the CLK signal is high, the V_{EXT} drive pin is low, turning off the external power train switch. The next switching cycle will start on another transition of the CLK signal from high to low.

4.4 Error Amplifier/Comparator Current Limit Function

The internal amplifier is used to create an error output signal that is determined by the V_{REF} input pin and the power supply output voltage fed back into the FB pin. The error amplifier output is rail-to-rail and is clamped by a precision 2.7V internal voltage source. The output of the error amplifier is then divided down 3:1 and connected to the inverting input of the high-speed comparator. The maximum output of the error amplifier is 2.7V, so the maximum input to the inverting pin of the high-speed comparator is 0.9V. As the output load current demand increases, the error amplifier output increases too, causing the inverting input pin of the high-speed comparator to increase. Eventually, the output of the error amplifier will hit the 2.7V clamp, limiting the input of the high-speed comparator to 0.9V maximum. Even if the FB input continues to decrease, calling for more current, the inverting input is limited to 0.9V. By limiting the inverting input to 0.9V, the current sense (CS) input is limited to 0.9V, thus limiting the current that flows in the main switch. Limiting the maximum peak current in the switch prevents the destruction of the semiconductor device and the saturation of the inductor during overloads. The resistor divider placed at the output of the error amplifier decreases the gain of the control loop by 9.5 dB. The designer must take into account this gain reduction during the compensation loop process. The error amplifier is rail-to-rail at the input and the common-mode range includes the GND and V_{IN} potentials.

4.5 0% Duty Cycle Operation

The duty cycle of the V_{EXT} output is capable of reaching 0% when the FB pin (inverting error amplifier) is held higher than the voltage present on the V_{REF} (Reference Voltage) pin. This is accomplished by the rail-to-rail output capability of the error amplifier and the offset voltage of the high-speed comparator. The minimum error amplifier output voltage, divided by 3, is less than the offset voltage of the high-speed comparator. In case the output voltage of the converter is above the desired regulation point, the FB input will be above the V_{REF} input and the error amplifier will be pulled to the bottom rail (GND). This low voltage is divided down 3:1 by the 2R and 1R resistor, and is connected to the input of the high-speed comparator. This voltage will be low enough so that there is no triggering of the comparator, allowing narrow pulse widths at V_{EXT}.

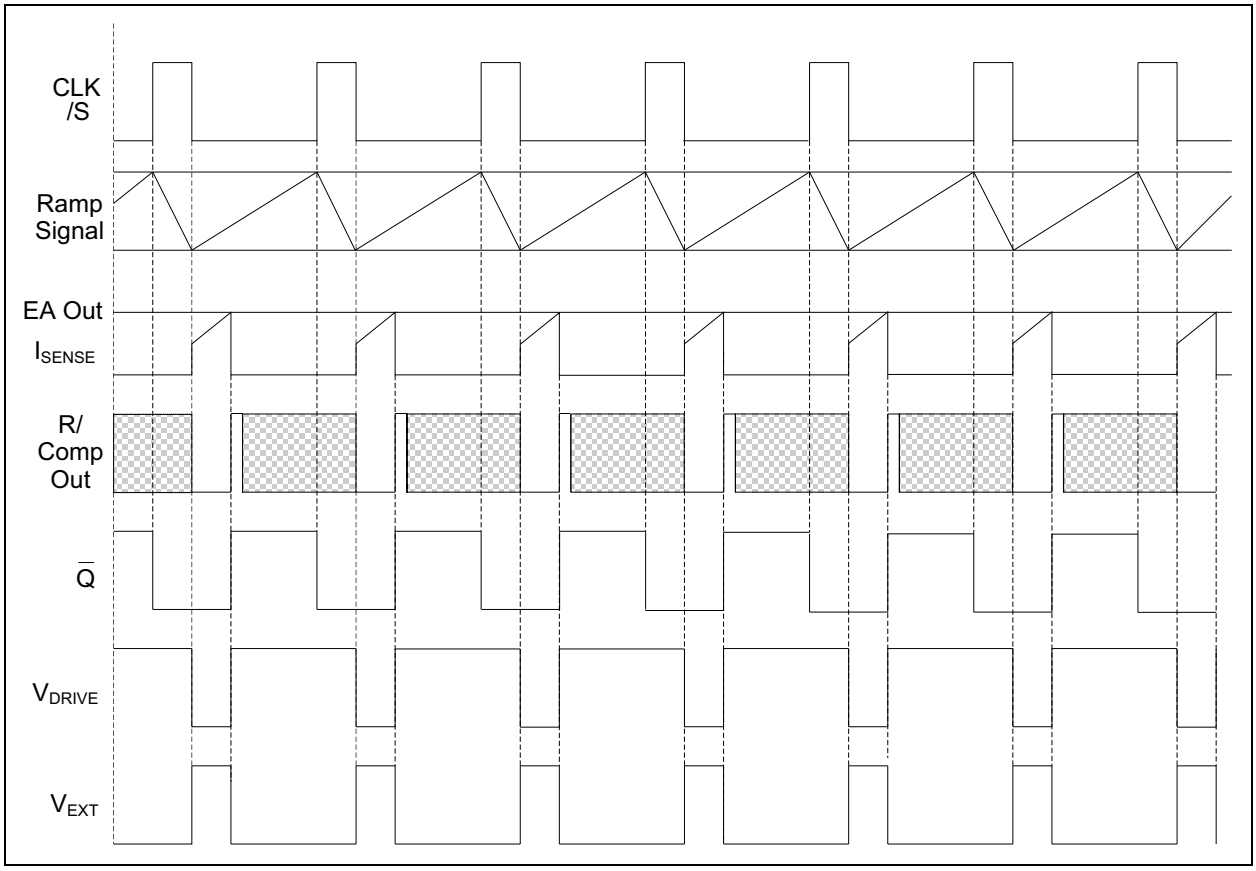


FIGURE 4-1: *PWM Timing Diagram.*

4.6 Slope Compensation

In order to prevent sub-harmonic oscillations that occur when a Peak Current Mode converter exceeds a 50% duty cycle, the MCP1632 provides an internal ramp generator that can be used for slope compensation. Refer to Figure 4-2 for details about the slope generator circuit. The amplitude of the generated ramp signal is 0.9 V_{PP} (typical) and the DC offset value is 770 mV (typical). The impedance of the internal ramp generator (R_G) is 6 kΩ (typical). The amplitude of the slope compensation ramp can be adjusted by modifying the value of the R_{SLOPE} resistor. Refer to Figure 4-3 for details about the slope compensation ramp signal applied to CS pin. The parameters of the slope compensation ramp signal can be calculated with the provided equations.

The MCP1632 device is equipped with a blanking circuit for the CS pin in order to prevent any false resets of the RS latch due to noise. However, for certain applications, it is recommended to place a small value capacitor (C_{FILTER}) between the CS pin and GND to provide additional filtering for the current sense signal. The recommended value ranges from 10 pF to 30 pF. Use caution, because a higher value may affect the slope compensation ramp.

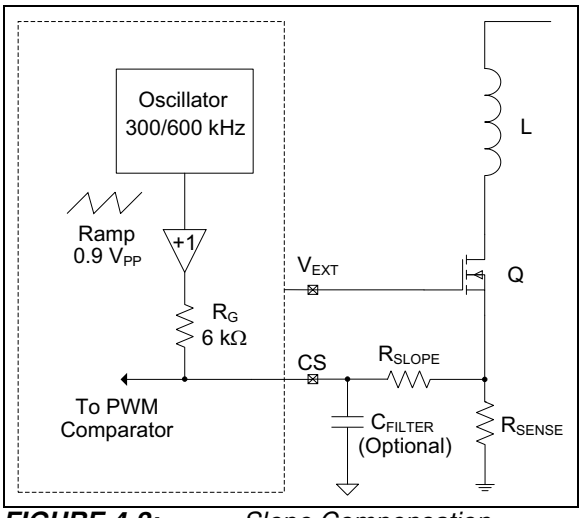


FIGURE 4-2: *Slope Compensation Circuit.*

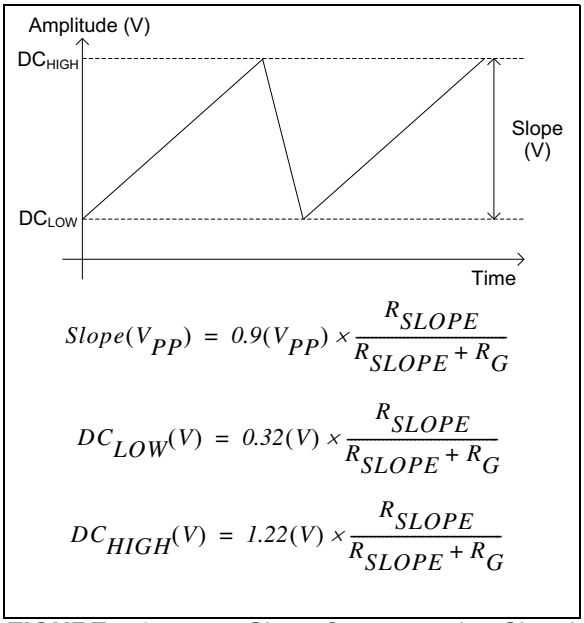


FIGURE 4-3: *Slope Compensation Signal (CS) Pin.*

4.7 Reference Voltage Generator

The internal precision constant current generator and an external resistor connected between the V_{REF} pin and GND form the reference voltage generator. Refer to Figure 4-4 for details. Optionally, a capacitor (C_{SS}) can be connected in parallel with R_{VREF} to activate the soft start function that will minimize overshoots of the output voltage during start-up. The equations in Figure 4-4 calculate the value of the resistor (R_{VREF}) for a given reference voltage and the value of the soft start capacitor (C_{SS}) based on the necessary time to reach 90% of the final value for V_{REF}. An internal circuit of the MCP1632 device will discharge the capacitor during the shutdown period. This capacitor must be of good quality, with low leakage currents, in order to avoid any errors that can affect the reference voltage. The reference voltage should not exceed 80% of the bias input voltage (V_{IN} pin) in order to avoid any errors that affect the internal constant current generator.

An external low-noise, low-impedance source can be used to overdrive the V_{REF} pin in order to control the reference voltage. In this case, the resistor/capacitor group connected to GND is not necessary, and the soft start profile must be controlled by the external reference voltage generator.

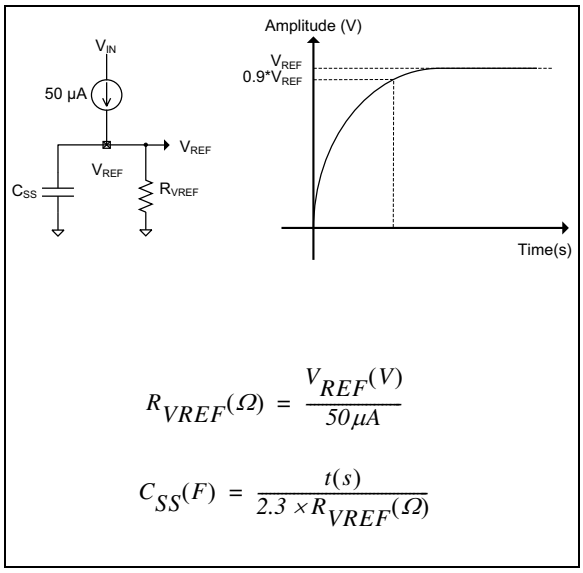


FIGURE 4-4: *Reference Voltage Generator.*

4.8 Internal Oscillator

The MCP1632 PWM controller provides two (orderable) switching frequency options: 300 kHz and 600 kHz.

4.9 Undervoltage Lockout (UVLO)

When the input voltage (V_{IN}) is less than the UVLO threshold, the V_{EXT} is held in low state. This will ensure that, if the voltage is not adequate to power the MCP1632 device, the main power supply switch will be held in off state. In order to prevent oscillations when the input voltage is near the UVLO threshold, the UVLO circuit offers 100 mV (typical) hysteresis. Typically, the MCP1632 device will not start until the input voltage at V_{IN} is between 2.8V and 2.9V (typical).

4.10 Overtemperature Protection

To protect the V_{EXT} output if shorted to V_{IN} or GND, the V_{EXT} output of the MCP1632 device will be high-impedance if the junction temperature is above the thermal shutdown threshold. An internal 10 kΩ pull-down resistor is connected from V_{EXT} to ground to provide some pull-down during overtemperature conditions. The protection is set to 150°C (typical), with a hysteresis of 20°C.

NOTES:

5.0 APPLICATION CIRCUITS

5.1 Typical Applications

The MCP1632 PWM controller can be used for applications that require low-side MOSFET control, such as Boost, Buck-Boost, Flyback, SEPIC or Ćuk converters. By using an external high-side MOSFET driver (e.g. MCP14628), the MCP1632 device is able to control the buck converter. The MCP1632 PWM controller can be easily interfaced with a microcontroller in order to develop intelligent solutions, such as battery chargers or LED drivers.

Figure 5-1 depicts the typical boost converter controlled by MCP1632. The input voltage applied on the V_{IN} pin of the MCP1632 device should be kept below 5.5V. If the converter must operate with input voltages higher than 5.5V, a linear voltage regulator can be used to bias the MCP1632 controller. The Peak Current Mode control used in this case will ensure consistent performance over a wide range of operating conditions.

The Q1 MOSFET is protected against overcurrent by internally limiting the maximum voltage at the output of the error amplifier of the controller. If the voltage applied on the CS pin exceeds 0.9V, the MCP1632 device will reduce the duty cycle in order to prevent overcurrent in Q1 MOSFET. The maximum drain peak current in Q1 can be calculated using Equation 5-1. The slope compensation ramp amplitude may limit the maximum peak current and must be considered when calculating this parameter. The DC offset of the slope compensation ramp (DC_{HIGH}) is calculated using the equations provided in Figure 4-3.

Note that the boost converter is not protected against the output short circuit.

EQUATION 5-1:

$$I_{Peak}Max(A) = \frac{0.9V - D \times DC_{HIGH}(V)}{R_{SENSE}(\Omega)}$$

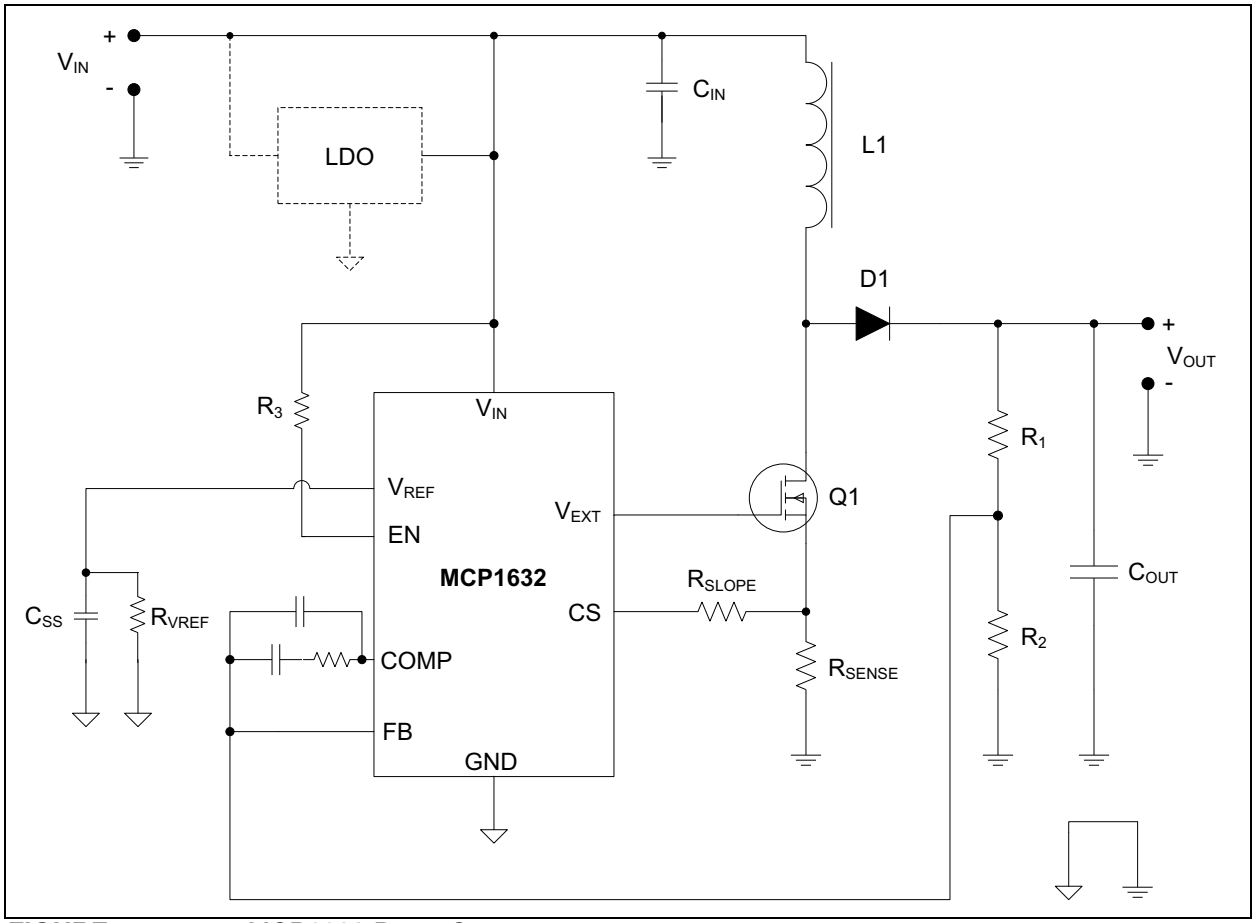


FIGURE 5-1: *MCP1632 Boost Converter.*

The single-ended primary inductor converter (SEPIC) used to drive an LED string is presented in Figure 5-2. This converter offers buck-boost functionality and is protected against the output short circuit. The inductors can share the same magnetic core (coupled inductors); in this case, the mutual inductance doubles the value of the inductor, reducing the ripple of the current. The LED string can be dimmed by driving the EN pin (PWM dimming) or by adjusting the value of the R_{VREF} resistor (current dimming). The maximum allowable peak current into Q1 MOSFET can be calculated using Equation 5-1. The SEPIC converter exhibits poor dynamic performance and is recommended only for applications with low step response demands, like LED drivers or battery chargers.

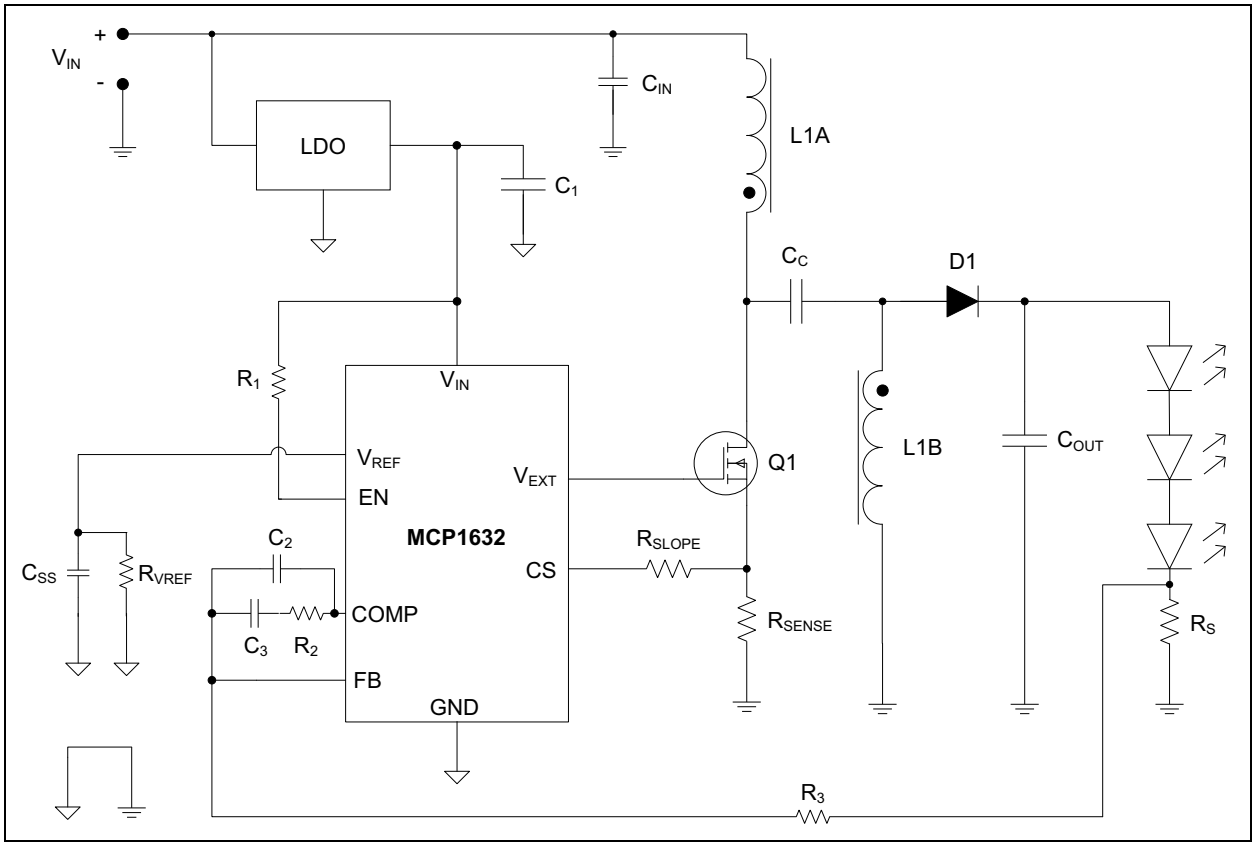


FIGURE 5-2: *MCP1632 SEPIC Converter.*

A typical charger application for one- or two-cell Li-Ion batteries is presented in Figure 5-3. The PIC microcontroller handles all the necessary functions of the charger and the MCP1632 device controls the power train. Using the SEPIC converter allows developing a universal charger where the input voltage can be higher or lower than the battery voltage. The microcontroller can control the reference voltage across certain limits using its internal high-frequency PWM generator and the external circuit consisting of D2 and R1.

This circuit can be replaced with a digital-to-analog converter (DAC) for a better range and accuracy of the reference voltage control. The charging current is monitored using a low-side shunt (R_S) and an inverting amplifier. The floating voltage of the charger is controlled by MCP1632 and can be adjusted by varying the value of the R_{VREF} resistor or the ratio of the feedback divider (R_5, R_6). Additional protection features can be implemented in the microcontroller's firmware.

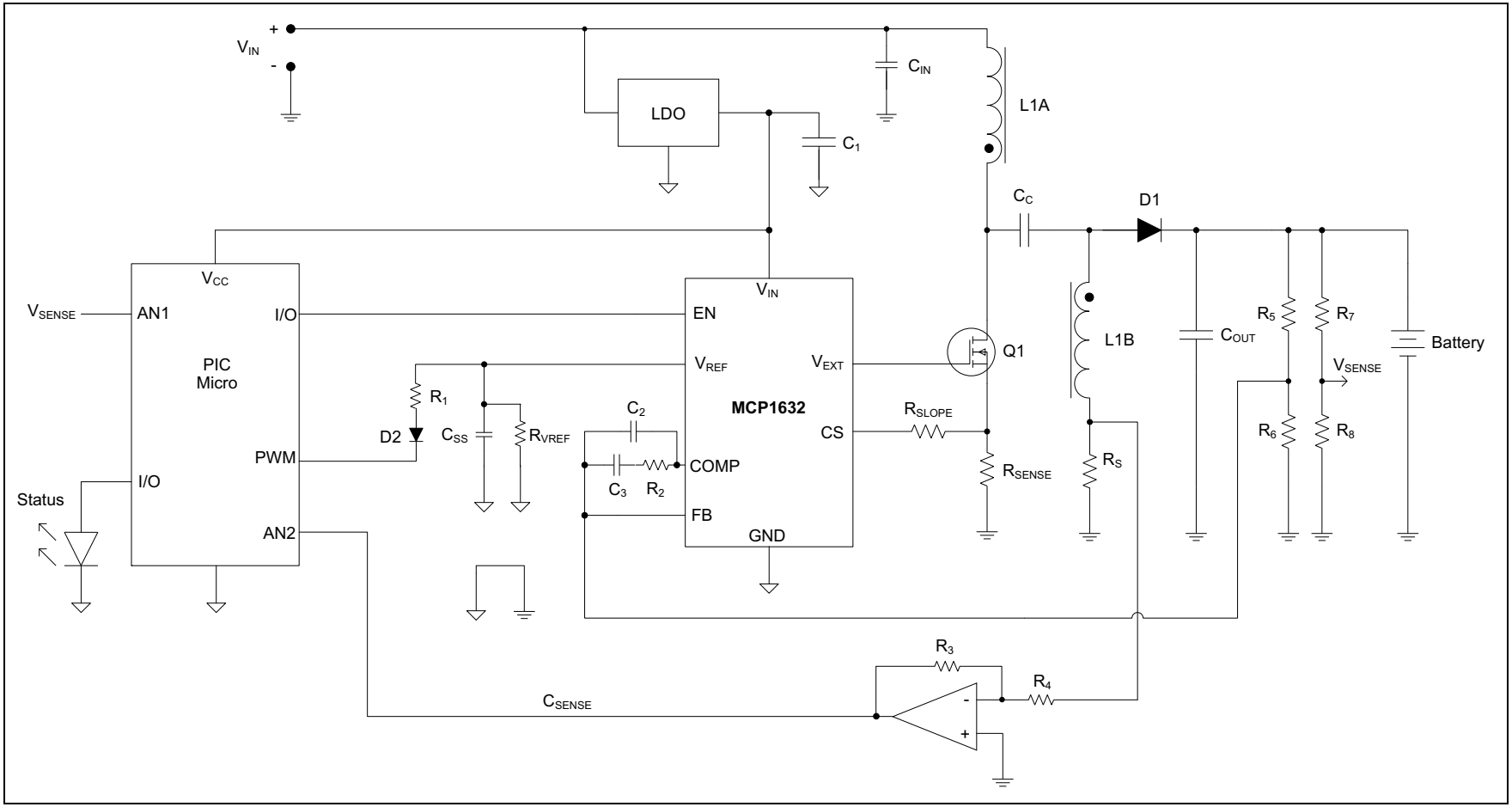


FIGURE 5-3: *Battery Charger Circuit.*

5.2 Operation in Voltage Mode Control

The MCP1632 PWM controller can operate in Voltage Mode Control using the internal slope compensation ramp to generate the PWM signal. The current sense resistor is not necessary for this application, thus the overall efficiency of the converter can be improved. Refer to Typical Application Circuit – Voltage Mode Control. Certain limitations occur in this operating mode. The compensation network for Voltage Mode Control must be of Type III, increasing the number of components.The closed-loop system is now a second order system and stability can be difficult to achieve over a wide range of operating conditions. The position of the dominant pole (double pole) in boost-derived converters varies with the operating conditions (input/output voltages); maintaining acceptable phase and gain margins across the entire operating range of the converter becomes a difficult task in this case.

Note that there is no inherent protection mechanism that can limit the inductor's current during transients or overloads. A resistor placed between the CS pin and GND allows adjusting the maximum duty cycle by controlling the amplitude of the ramp signal. Refer to Figure 5-4 for details. If the $R_{DC\ Adj}$ resistor is not placed, the maximum duty cycle is set to approximately 60% (typical). The duty cycle can be increased up to 85% (typical) by adjusting the value of the $R_{DC\ Adj}$ resistor. The designer must limit the maximum operating duty cycle of the converter to a safe value by adjusting the value of this resistor. The DC offset of the ramp enables operation with 0% duty cycle if the output of the error amplifier divided by 3 is lower than DC_{LOW}.

The Voltage Mode Control should be used only for systems with low input voltages, low DC conversion ratios and limited dynamics of the load (e.g., LED drivers or battery chargers).

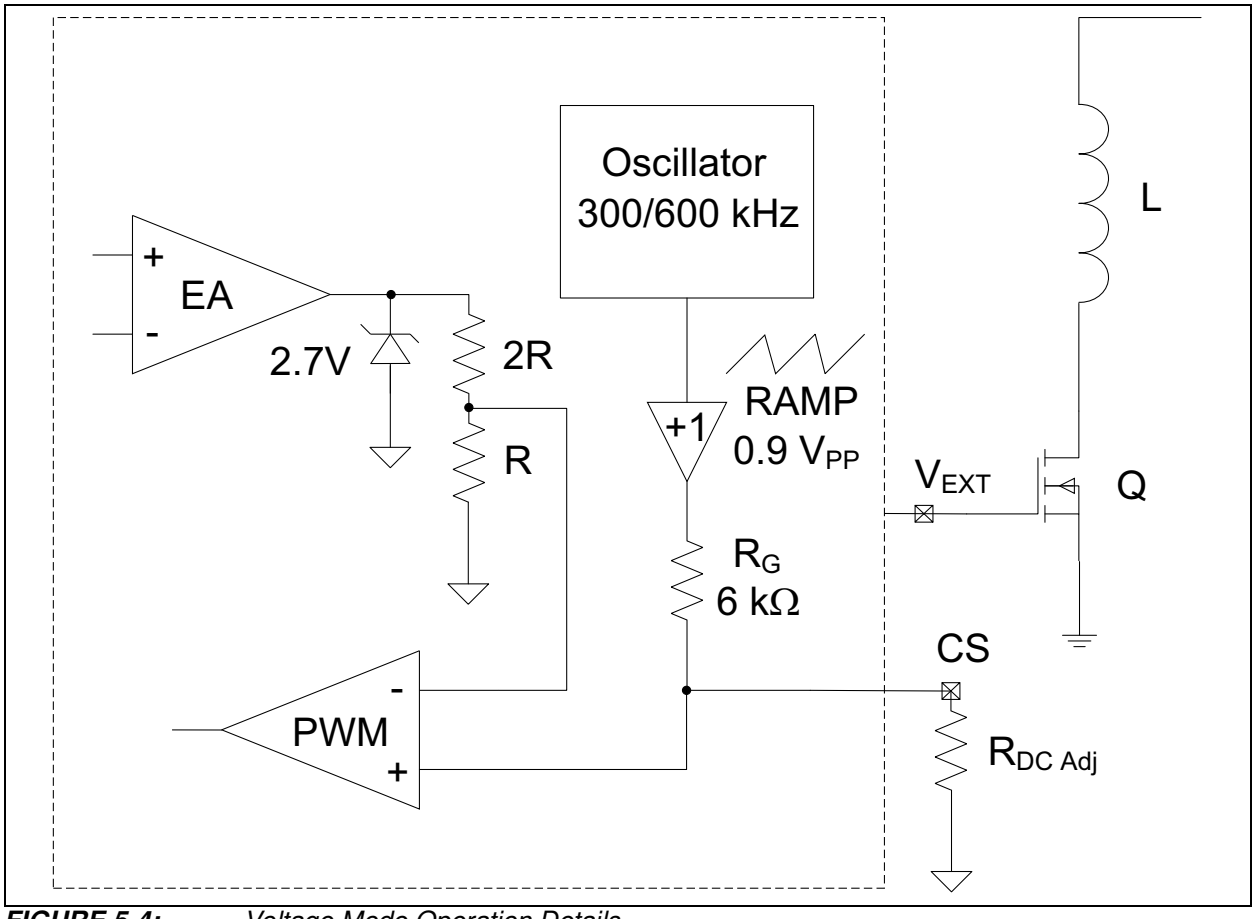


FIGURE 5-4: *Voltage Mode Operation Details.*

5.3 PCB Layout Recommendations

The PCB layout is critical for switch-mode power supplies. When developing the PCB, the designer must follow the general rules for switching converters in order to achieve consistent performance. The guidelines include:

- Identify the high-current, high-frequency loops before starting the PCB design. Figure 5-5 depicts these loops for boost converters. I_1 and I_2 are the main currents of the boost converter. The I_{RR} is the current produced by the reverse recovery of the output rectifier D1. The I_{RR} current is an important source of noise/EMI.
- Minimize the area of the high-current loops. Use copper planes or large traces for high-current connections in order to minimize the parasitic inductances.
- Four-layer PCBs with internal ground plane offer the best performance for switch-mode power supplies. For cost-sensitive applications, two-layer PCBs can be used. In this case, the bottom layer must be used like a ground plane.
- Use separate grounds for small-signal and power signals. These grounds must be connected (when possible) in a single point located near the GND pin of the MCP1632 controller.
- Keep the current sense (CS) and feedback (FB) signals away from noisy nodes, such as the drain of the main switch (Q1).
- Locate the compensation network components near the MCP1632 case.

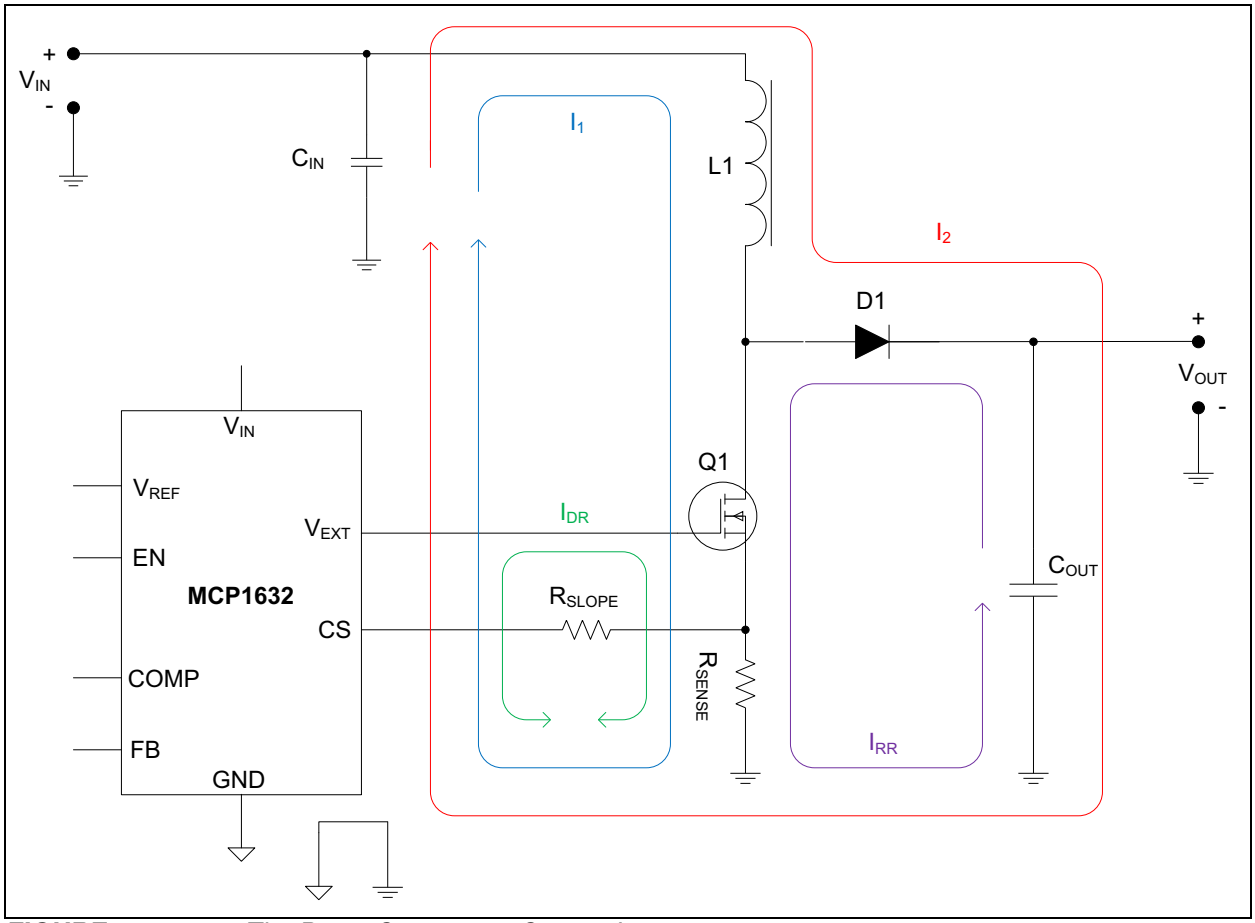


FIGURE 5-5: *The Boost Converter's Current Loops.*

NOTES:

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

8-Lead DFN (2x3x0.9 mm)

Part Number	Code
MCP1632-AAE/MC	ACD
MCP1632-BAE/MC	ACY
MCP1632T-AAE/MC	ACD
MCP1632T-BAE/MC	ACY

Example

8-Lead MSOP (3x3 mm)

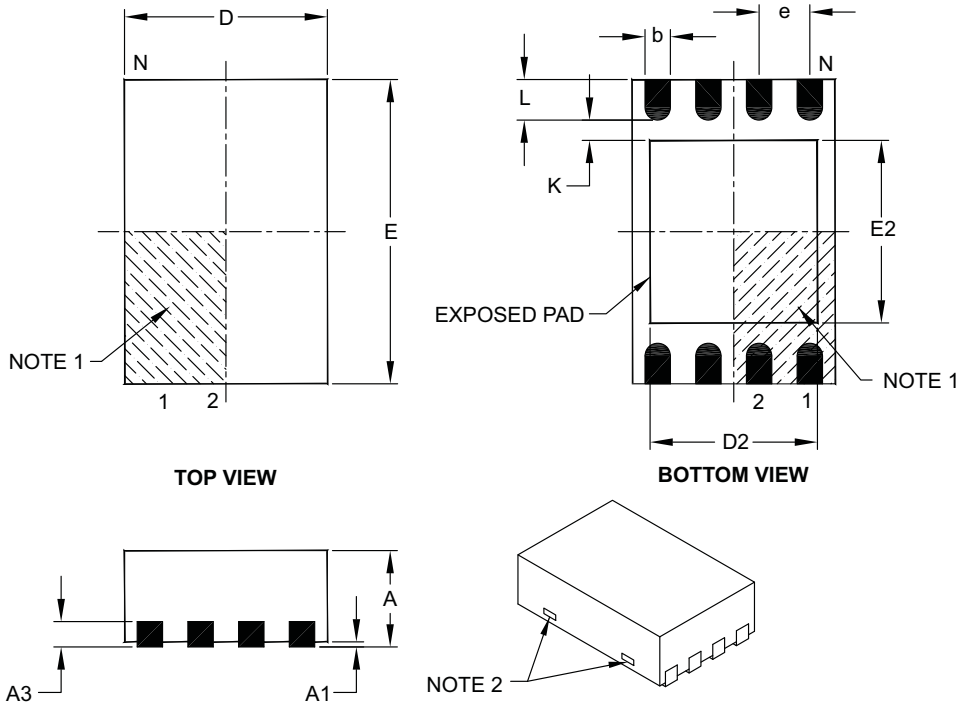
Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

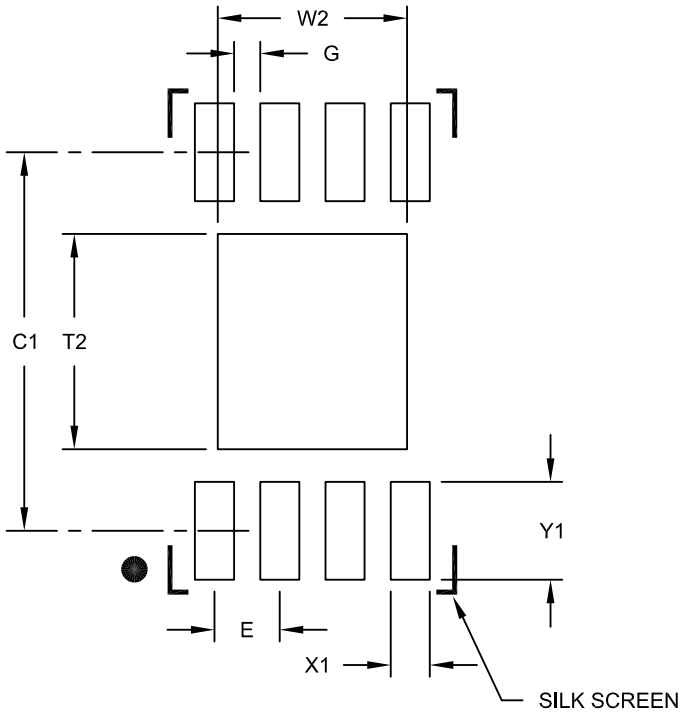
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B