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MCP1755/1755S

300 mA, 16V, High-Performance LDO

Features:

- High PSRR: >70 dB @ 1 kHz, typical
- 68.0 µA Typical Quiescent Current
- Input Operating Voltage Range: 3.6V to 16.0V
- 300 mA Output Current for all Output Voltages
- Low Dropout Voltage, 300 mV typical @ 300 mA
- Standard Output Voltage Options (1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 4.0V, 5.0V)
- Output Voltage Range 1.8V to 5.5V in 0.1V Increments (tighter increments are also possible per design)
- Output Voltage Tolerances of ±2.0% over entire Temperature Range
- Stable with Minimum 1.0 µF Output Capacitance
- Power Good Output
- Shutdown Input
- True Current Foldback Protection
- Short-Circuit Protection
- Overtemperature Protection

Applications:

- Battery-powered Devices
- Battery-powered Alarm Circuits
- Smoke Detectors
- CO_2 Detectors
- Pagers and Cellular Phones
- Smart Battery Packs
- Portable Digital Assistant (PDA)
- Digital Cameras
- Microcontroller Power
- Consumer Products
- Battery-powered Data Loggers

Related Literature:

- AN765, *"Using Microchip's Micropower LDOs"* (DS00765), Microchip Technology Inc., 2007
- AN766, *"Pin-Compatible CMOS Upgrades to BiPolar LDOs"* (DS00766), Microchip Technology Inc., 2003
- AN792, *"A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application"* (DS00792), Microchip Technology Inc., 2001

Description:

The MCP1755/1755S is a family of CMOS low-dropout (LDO) voltage regulators that can deliver up to 300 mA of current while consuming only 68.0 µA of quiescent current (typical). The input operating range is specified from 3.6V to 16.0V, making it an ideal choice for four to six primary cell battery-powered applications, 12V mobile applications and one to three cell Li-Ion-powered applications.

The MCP1755/1755S is capable of delivering 300 mA with only 300 mV (typical) of input-to-output voltage differential. The output voltage tolerance of the MCP1755 is typically +0.85% at +25°C and ±2.0% maximum over the operating junction temperature range of -40°C to +125°C. Line regulation is ±0.01% typical at +25°C.

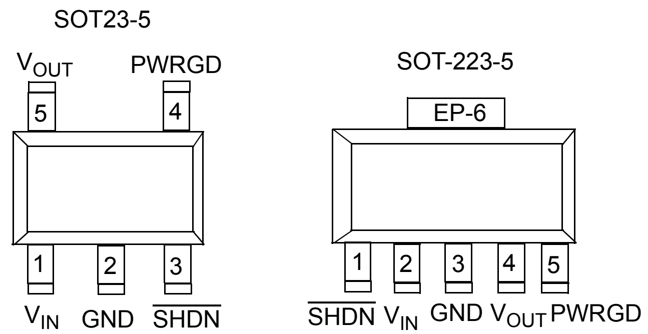
Output voltages available for the MCP1755/1755S range from 1.8V to 5.5V. The LDO output is stable when using only 1 µF of output capacitance. Ceramic, tantalum or aluminum electrolytic capacitors may all be used for input and output. Overcurrent limit and overtemperature shutdown provide a robust solution for any application.

The MCP1755/1755S family has a true current foldback feature. When the load impedance decreases beyond the MCP1755/1755S load rating, the output current and voltage will gracefully foldback towards 30 mA at about 0V output. When the load impedance increases and returns to the rated load, the MCP1755/1755S will follow the same foldback curve as the device comes out of current foldback.

Package options for the MCP1755 include the SOT-23-5, SOT-223-5 and 8-lead 2 x 3 DFN.

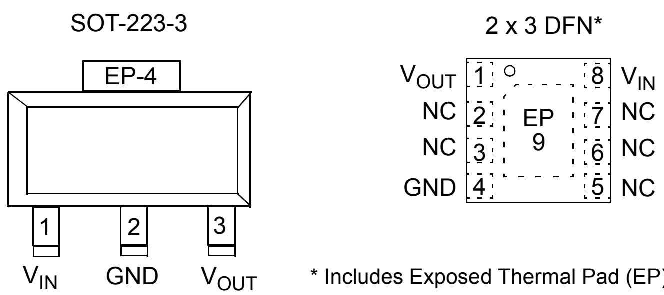
Package options for the MCP1755S device include the SOT-223-3 and 8-lead 2 x 3 DFN.

Package Types – MCP1755



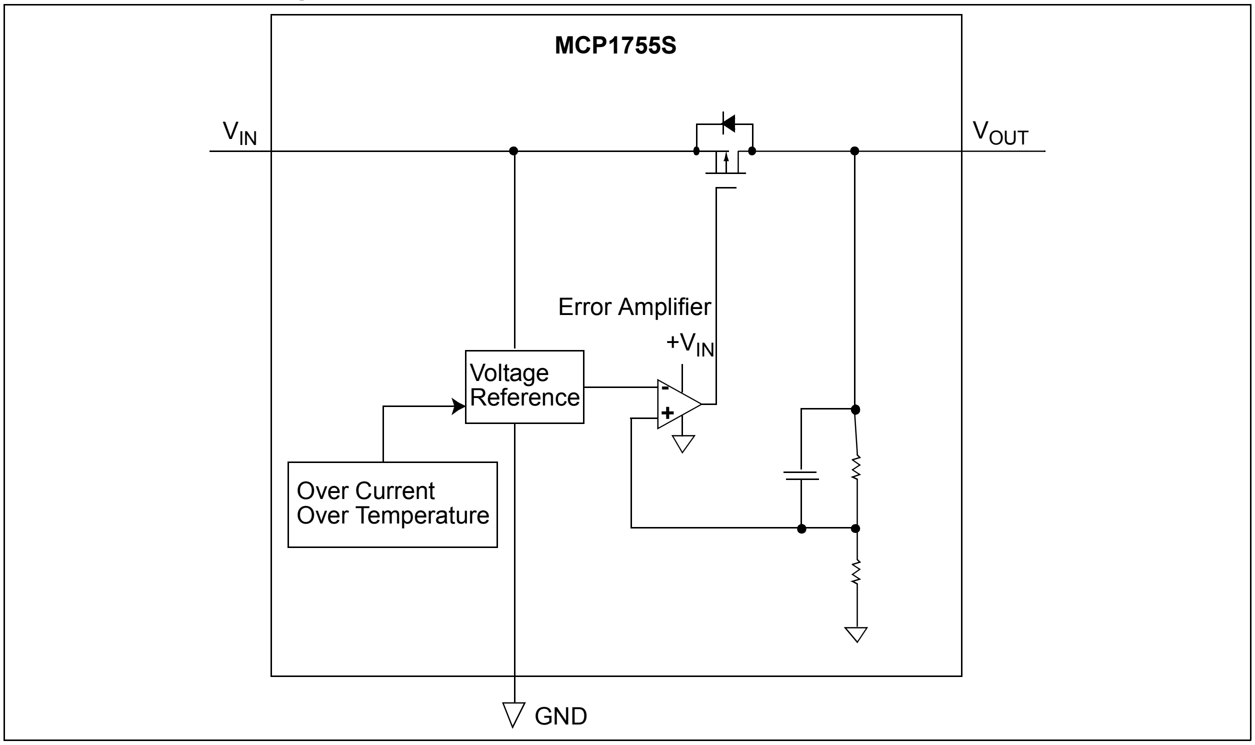
* Includes Exposed Thermal Pad (EP); see Table 3-1

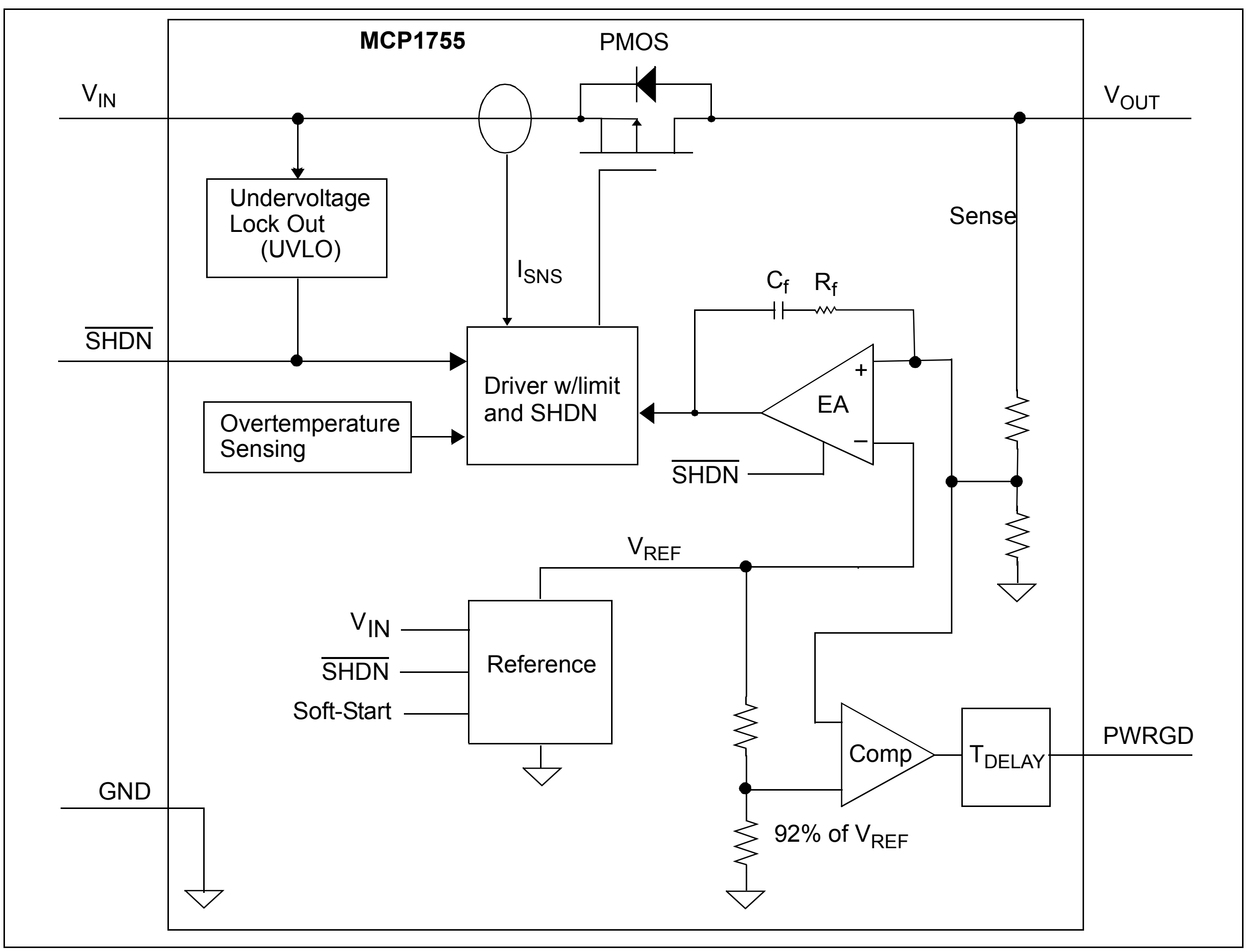
Package Types – MCP1755S



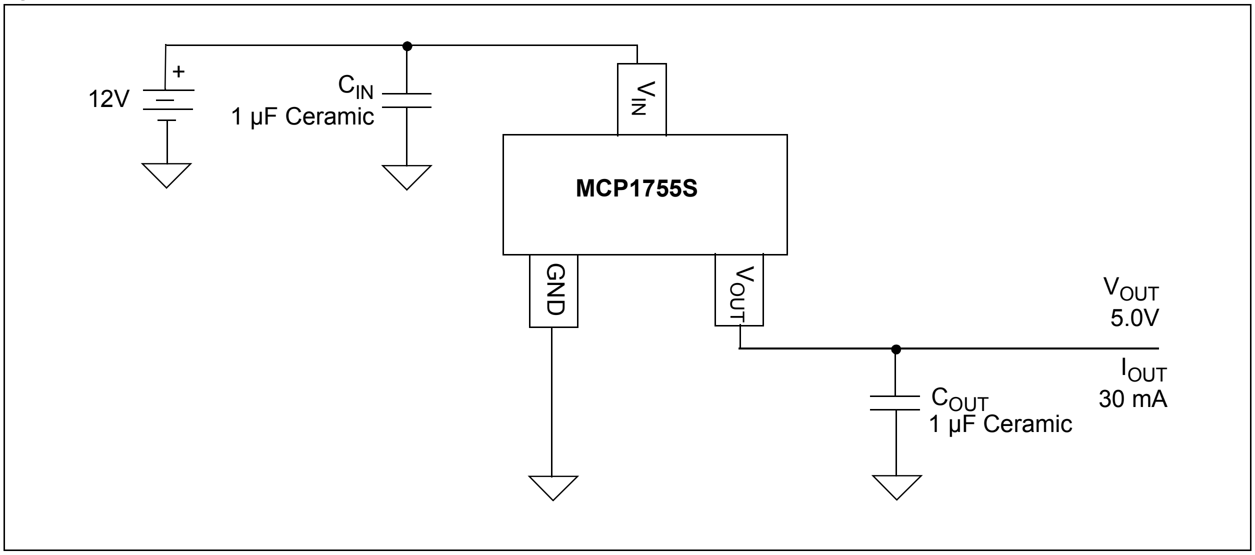
* Includes Exposed Thermal Pad (EP); see Table 3-2

Functional Block Diagrams





Typical Application Circuits



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN} .... +17.6V
V_{IN}, PWRGD, $\overline{SHDN}$ .... (GND – 0.3V) to (V_{IN} + 0.3V)
V_{OUT} .... (GND – 0.3V) to (+5.5V)
Internal Power Dissipation .... Internally-Limited (**Note 6**)
Output Short Circuit Current .... Continuous
Storage temperature .... -55°C to +150°C
Maximum Junction Temperature .... +165°C(**Note 7**)
Operating Junction Temperature .... -40°C to +150°C
ESD protection on all pins .... ≥3 kV HBM and ≥400V MM

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R$ + 1V, **Note 1**, I_{LOAD} = 1 mA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C, $t_{r(VIN)}$ = 0.5 V/µs, $\overline{SHDN} = V_{IN}$, PWRGD = 10K to V_{OUT}. **Boldface** type applies for junction temperatures, T_J (**Note 7**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input/Output Characteristics						
Input Operating Voltage	V_{IN}	**3.6**	—	**16.0**	V	
Output Voltage Operating Range	$V_{OUT-RANGE}$	**1.8**	—	**5.5**	V	
Input Quiescent Current	I_q	—	68	**100**	µA	I_L = 0 mA
Input Quiescent Current for $\overline{SHDN}$ mode	$I_{\overline{SHDN}}$	—	0.1	**4**	µA	$\overline{SHDN}$ = GND
Ground Current	I_{GND}	—	300	**400**	µA	I_{LOAD} = 300 mA
Maximum Output Current	I_{OUT_mA}	**300**	—	—	mA	
Output Soft Current Limit	SCL	—	450	—	mA	$V_{OUT} \geq 0.1V$, $V_{IN} = V_{IN(MIN)}$, Current measured 10 ms after the load is applied
Output Pulse Current Limit	PCL	—	350	—	mA	Pulse Duration < 100 ms, Duty Cycle < 50%, $V_{OUT} \geq 0.1V$, **Note 6**
Output Short Circuit Foldback Current	I_{OUT_SC}	—	30	—	mA	$V_{IN} = V_{IN(MIN)}$, V_{OUT} = GND
Output Voltage Overshoot on Start-up	V_{OVER}	—	0.5	—	$\%V_{OUT}$	V_{IN} = 0 to 16V, I_{LOAD} = 300 mA

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 3.6V$ and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage when the input voltage $V_{IN} = V_{Rated} + V_{DROPOUT(MAX)}$ or V_{IN} = 3.6V (whichever is greater); I_{OUT} = 1 mA.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) \times 10^6/(V_R \times \Delta_{Temperature})$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R$ + 1V or V_{IN} = 3.6V (whichever is greater).

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

8: See **Section 4.6 “Shutdown Input (SHDN)”** and Figure 2-34.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, **Note 1**, I_{LOAD} = 1 mA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C, $t_{r(VIN)}$ = 0.5 V/µs, $\overline{SHDN} = V_{IN}$, PWRGD = 10K to V_{OUT}. **Boldface** type applies for junction temperatures, T_J (**Note 7**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Voltage Regulation	V_{OUT}	**V_R – 2.0%**	V_R +0.85%	**V_R +2.0 %**	V	**Note 2**
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	35		ppm/°C	**Note 3**
Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	**-0.05**	±0.01	**+0.05**	%/V	$V_R + 1V \le V_{IN} \le 16V$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-0.5**	±0.1	**+0.5**	%	I_L = 1.0 mA to 300 mA, **Note 4**
Dropout Voltage (**Note 5**)	$V_{DROPOUT}$	—	300	**500**	mV	I_L = 300 mA
Dropout Current	I_{DO}	—	75	**120**	µA	$V_{IN} = 0.95V_R$, I_{OUT} = 0 mA
Undervoltage Lockout						
Undervoltage Lockout	UVLO	—	3.0	—	V	Rising V_{IN}
Undervoltage Lockout Hysterisis	$UVLO_{HYS}$	—	300	—	mV	Falling V_{IN}
Shutdown Input						
Logic High Input	$V_{SHDN-HIGH}$	**2.4**	—	$V_{IN(MAX)}$	V	
Logic Low Input	$V_{SHDN-LOW}$	0.0	—	**0.8**	V	
Shutdown Input Leakage Current	$\overline{SHDN}_{ILK}$	—	0.02	**0.2**	µA	$\overline{SHDN}$ = 16V
Power Good Output						
PWRGD Input Voltage Operating Range	V_{PWRGD_VIN}	**1.7**	—	V_{IN}	V	I_{SINK} = 1 mA
PWRGD Threshold Voltage (Referenced to V_{OUT})	V_{PWRGD_TH}	**90**	92	**94**	$\%V_{OUT}$	Falling Edge of V_{OUT}
PWRGD Threshold Hysteresis	V_{PWRGD_HYS}	—	2.0	—	$\%V_{OUT}$	Rising Edge of V_{OUT}
PWRGD Output Voltage Low	V_{PWRGD_L}	—	0.2	**0.45**	V	I_{PWRGD_SINK} = 5.0 mA, V_{OUT} = 0V
PWRGD Output Sink Current	I_{PWRGD_L}	**5.0**	—	—	mA	$V_{PWRGD} \le 0.45V$

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge 3.6V$ and $V_{IN} \ge V_R + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage when the input voltage $V_{IN} = V_{Rated} + V_{DROPOUT(MAX)}$ or V_{IN} = 3.6V (whichever is greater); I_{OUT} = 1 mA.

3: $TCV_{OUT} = (V_{OUT-HIGH} – V_{OUT-LOW}) \times 10^6/(V_R \times \Delta_{Temperature})$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R + 1V$ or V_{IN} = 3.6V (whichever is greater).

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

8: See **Section 4.6 "Shutdown Input (SHDN)"** and Figure 2-34.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 1V$, **Note 1**, I_{LOAD} = 1 mA, C_{OUT} = 1 µF (X7R), C_{IN} = 1 µF (X7R), T_A = +25°C, $t_{r(VIN)}$ = 0.5 V/µs, $\overline{SHDN} = V_{IN}$, PWRGD = 10K to V_{OUT}. **Boldface** type applies for junction temperatures, T_J (**Note 7**) of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PWRGD Leakage Current	I_{PWRGD_LK}	—	50	**200**	nA	V_{PWRGD} Pullup = 10 kΩ to V_{IN} V_{IN} = 16V
PWRGD Time Delay	T_{PG}	—	100	—	µs	Rising Edge of V_{OUT}
Detect Threshold to PWRGD Active Time Delay	T_{VDET_PWRGD}	—	200	—	µs	Falling Edge of V_{OUT} after Transition from $V_{OUT} = V_{PRWRGD\_TH}$ + 50 mV to V_{PWRGD_TH} – 50 mV, R_{PULLUP} = 10 kΩ to V_{IN}
AC Performance						
Output Delay from V_{IN} to V_{OUT} = 90% V_{REG}	T_{DELAY}	—	200	—	µs	V_{IN} = 0V to 16V, V_{OUT} = 90% V_R, $t_{r(VIN)}$ = 5 V/µs,
Output Delay From V_{IN} to V_{OUT} > 0.1V	T_{DELAY_START}	—	80	—	µs	V_{IN} = 0V to 16V, $V_{OUT} \geq$ 0.1V, $t_{r(VIN)}$ = 5 V/µs,
Output Delay From $\overline{SHDN}$ (**Note 8**)	T_{DELAY_SHDN}	—	235	—	µs	V_{IN} = 6V, V_{OUT} = 90% V_R, V_R=5V,$\overline{SHDN}$ = GND to V_{IN}
		—	940	—	µs	V_{IN} = 7V, V_{OUT} = 90% V_R, V_R=5V, $\overline{SHDN}$ = GND to V_{IN}
		—	210	—	µs	V_{IN} = 16V,V_{OUT} = 90% V_R, V_R=5V, $\overline{SHDN}$ = GND to V_{IN}
Output Noise	e_N	—	0.3	—	µV/(√Hz)	I_L = 50 mA, f = 1 kHz,
Power Supply Ripple Rejection Ratio	PSRR	—	80	—	dB	V_R = 5V, f = 1 kHz, I_L = 100 mA, V_{INAC} = 1V_{PK-PK}, C_{IN} = 0 µF, $V_{IN} \geq V_R$ + 1.5V ≥ 3.6V
Thermal Shutdown Temperature	T_{SD}	—	150	—	°C	**Note 6**
Thermal Shutdown Hysteresis	ΔTSD	—	10	—	°C	

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq$ 3.6V and $V_{IN} \geq V_R + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage when the input voltage $V_{IN} = V_{Rated} + V_{DROPOUT(MAX)}$ or V_{IN} = 3.6V (whichever is greater); I_{OUT} = 1 mA.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) \times 10^6/(V_R \times \Delta_{Temperature})$, $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification TCV_{OUT}.

5: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below the output voltage value that was measured with an applied input voltage of $V_{IN} = V_R$ + 1V or V_{IN} = 3.6V (whichever is greater).

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

8: See **Section 4.6 "Shutdown Input (SHDN)"** and Figure 2-34.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_J	-40	—	+150	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Thermal Package Resistance						
Thermal Resistance, SOT-223-3	θ_{JA}	—	62	—	°C/W	
	θ_{JC}	—	15	—		
Thermal Resistance, SOT-223-5	θ_{JA}	—	62	—	°C/W	
	θ_{JC}	—	15	—		
Thermal Resistance, SOT-23-5	θ_{JA}	—	256	—	°C/W	
	θ_{JC}	—	81	—		
Thermal Resistance, 2 x 3 DFN-8	θ_{JA}	—	70	—	°C/W	
	θ_{JC}	—	13.4	—		

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223.

2: Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

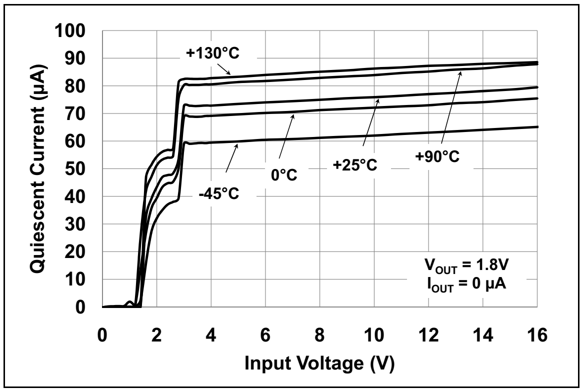


FIGURE 2-1: *Quiescent Current vs. Input Voltage.*

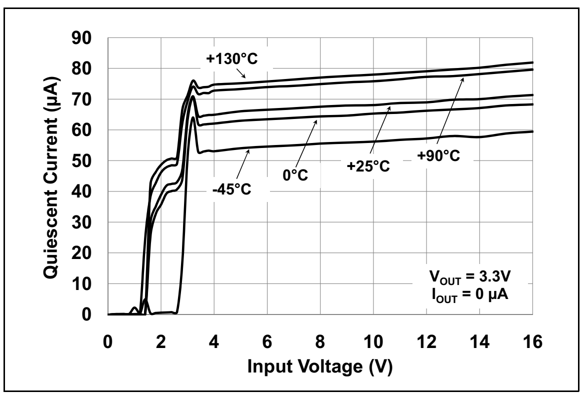


FIGURE 2-2: *Quiescent Current vs. Input Voltage.*

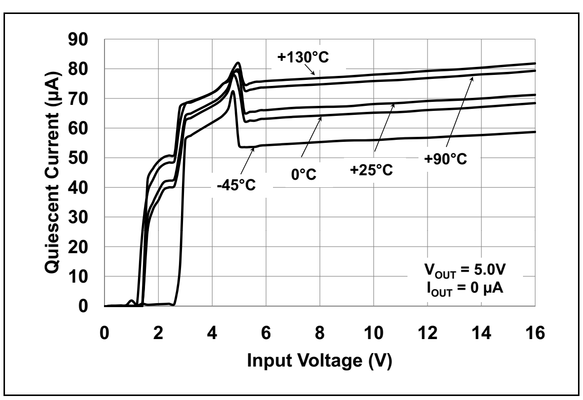


FIGURE 2-3: *Quiescent Current vs. Input Voltage.*

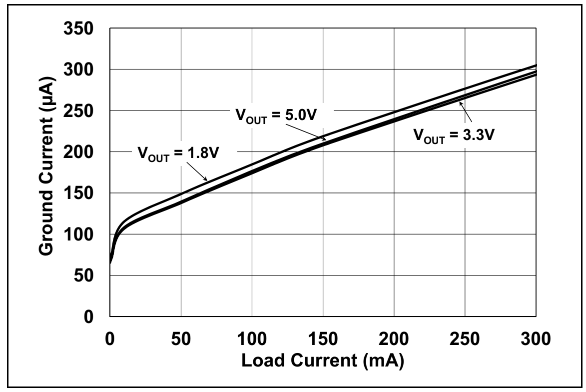


FIGURE 2-4: *Ground Current vs. Load Current.*

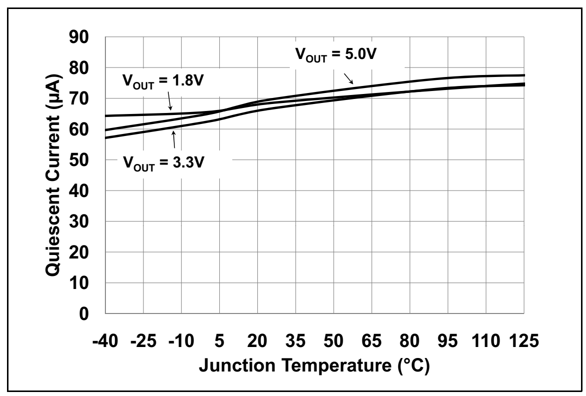


FIGURE 2-5: *Quiescent Current vs. Junction Temperature.*

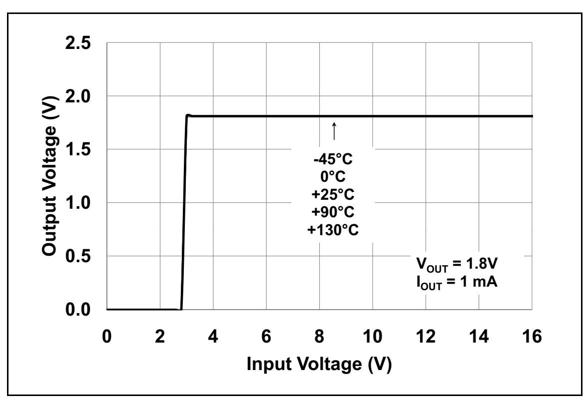


FIGURE 2-6: *Output Voltage vs. Input Voltage.*

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223

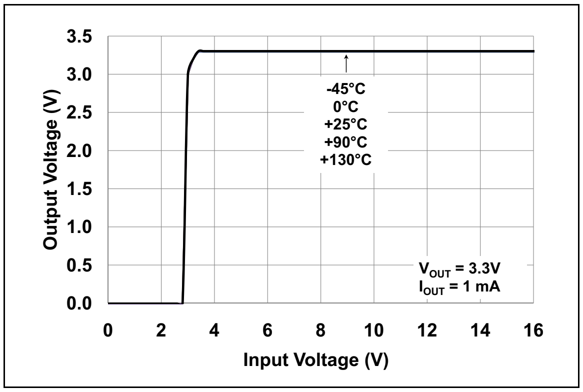


FIGURE 2-7: *Output Voltage vs. Input Voltage.*

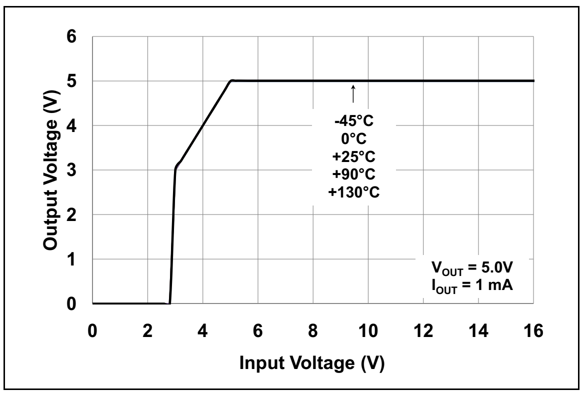


FIGURE 2-8: *Output Voltage vs. Input Voltage.*

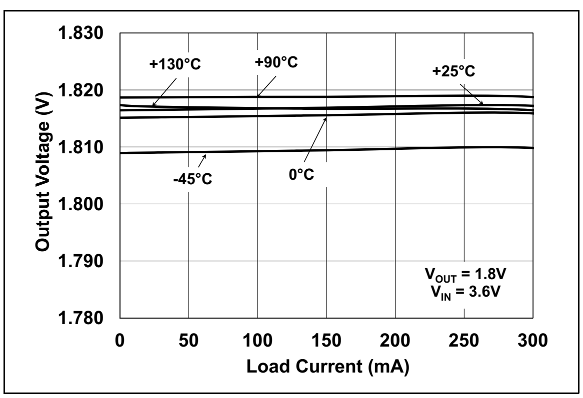


FIGURE 2-9: *Output Voltage vs. Load Current.*

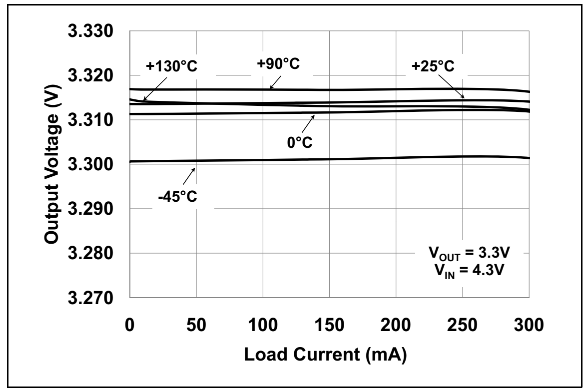


FIGURE 2-10: *Output Voltage vs. Load Current.*

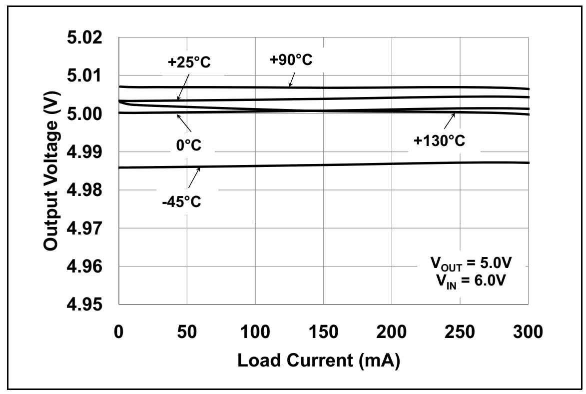


FIGURE 2-11: *Output Voltage vs. Load Current.*

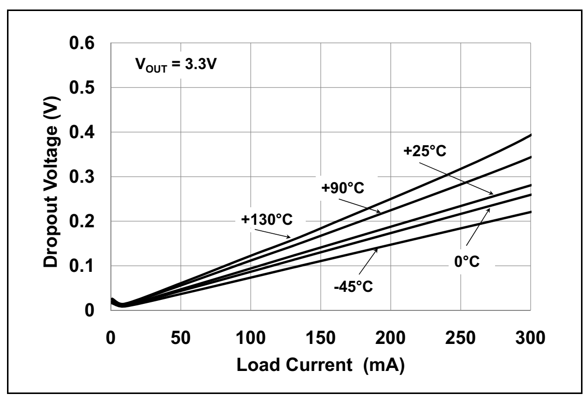


FIGURE 2-12: *Dropout Voltage vs. Load Current.*

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223

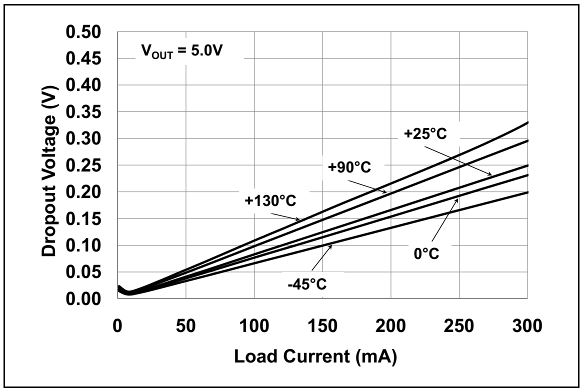


FIGURE 2-13: Dropout Voltage vs. Load Current.

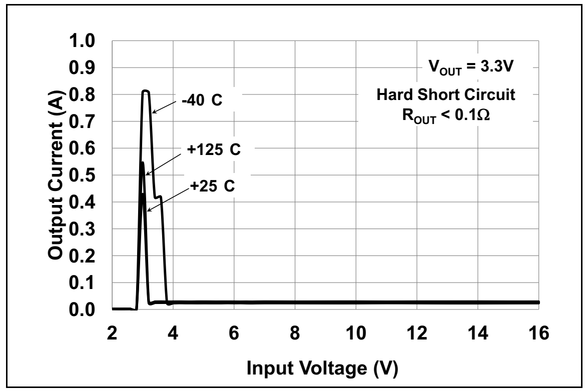


FIGURE 2-16: Short Circuit Current vs. Input Voltage.

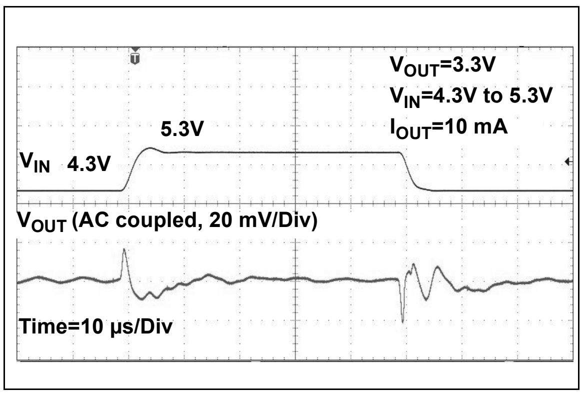


FIGURE 2-14: Dynamic Line Response.

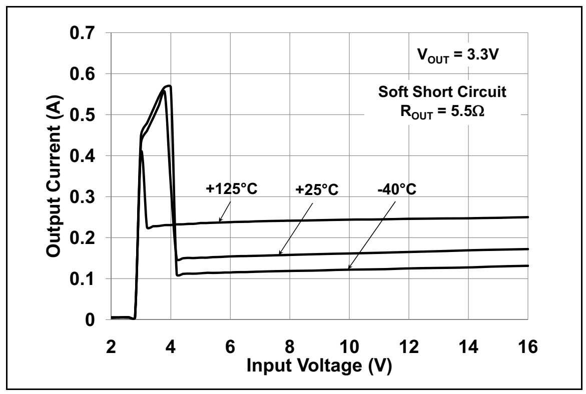


FIGURE 2-17: Short Circuit Current vs. Input Voltage.

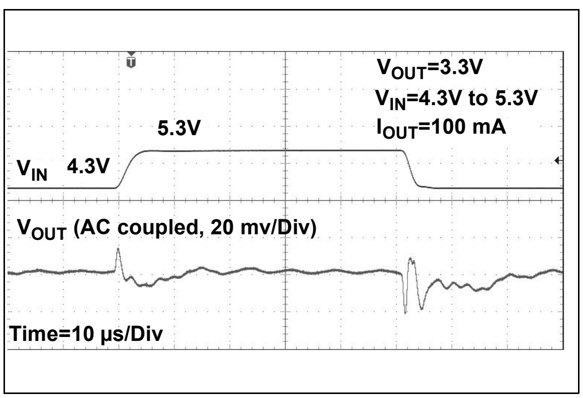


FIGURE 2-15: Dynamic Line Response.

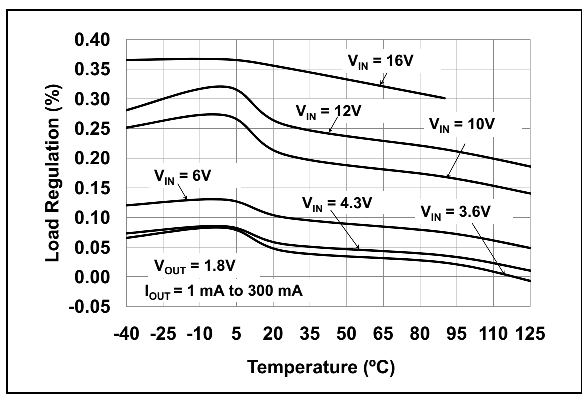


FIGURE 2-18: Load Regulation vs. Temperature.

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223

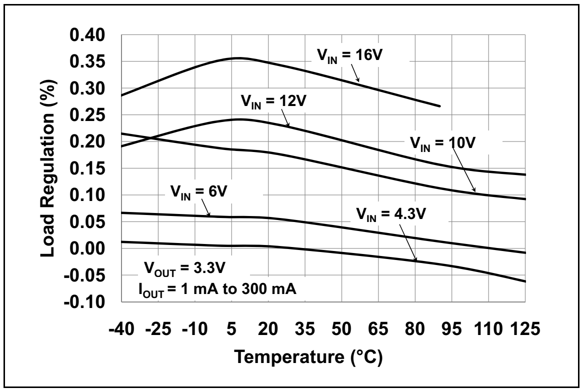


FIGURE 2-19: *Load Regulation vs. Temperature.*

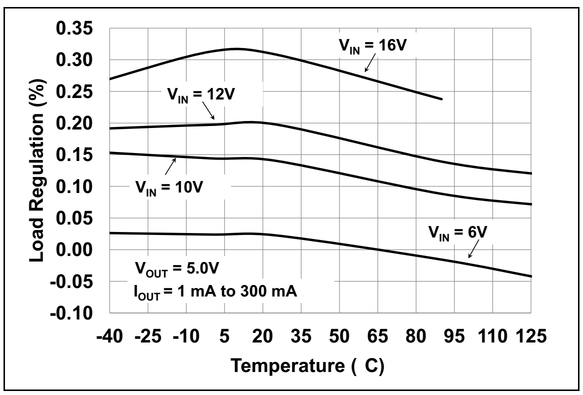


FIGURE 2-20: *Load Regulation vs. Temperature.*

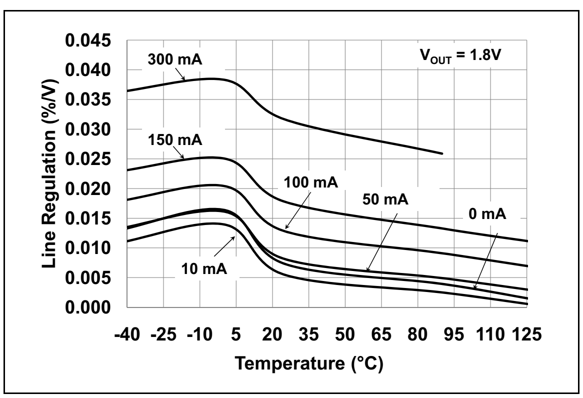


FIGURE 2-21: *Line Regulation vs. Temperature.*

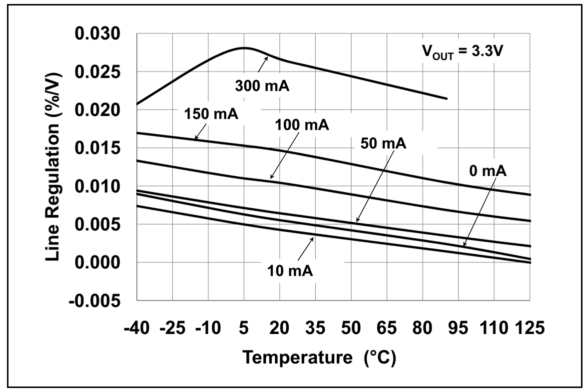


FIGURE 2-22: *Line Regulation vs. Temperature.*

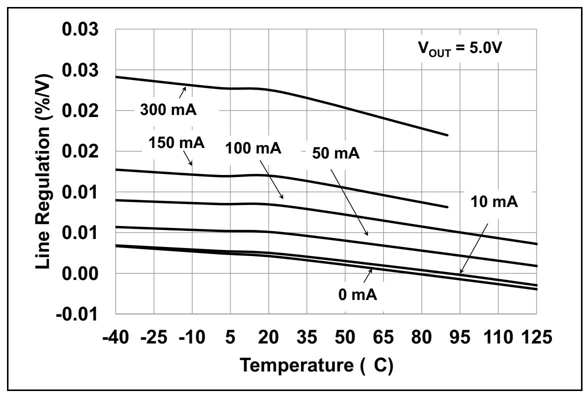


FIGURE 2-23: *Line Regulation vs. Temperature.*

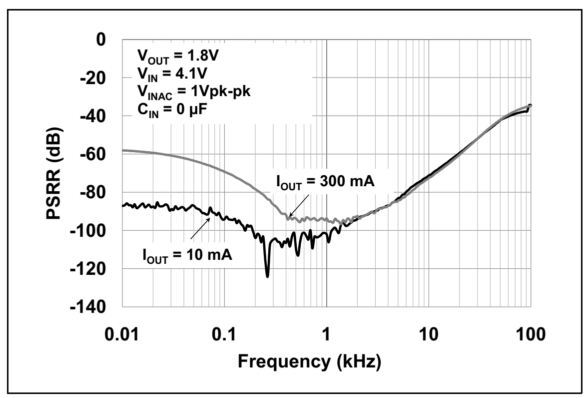


FIGURE 2-24: *Power Supply Ripple Rejection vs. Frequency.*

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223

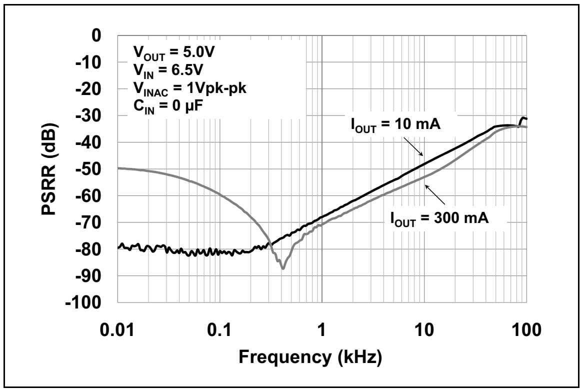


FIGURE 2-25: *Power Supply Ripple Rejection vs. Frequency.*

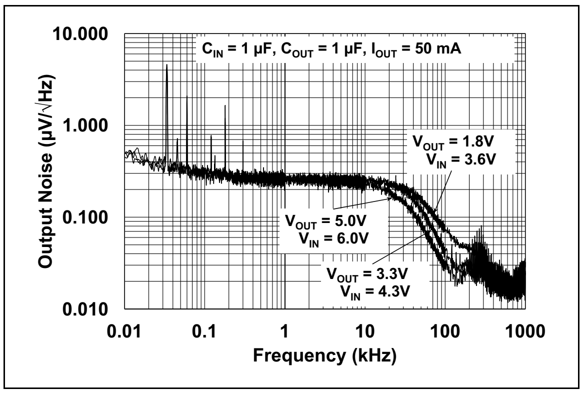


FIGURE 2-26: *Output Noise vs. Frequency (3 lines, V_R = 1.8V, 3.3V, 5.0V).*

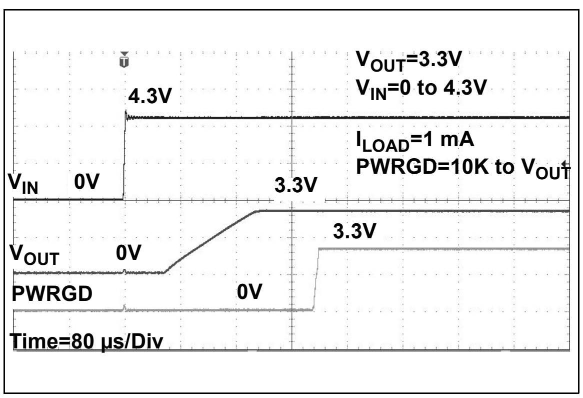


FIGURE 2-27: *Start-up from V_{IN}.*

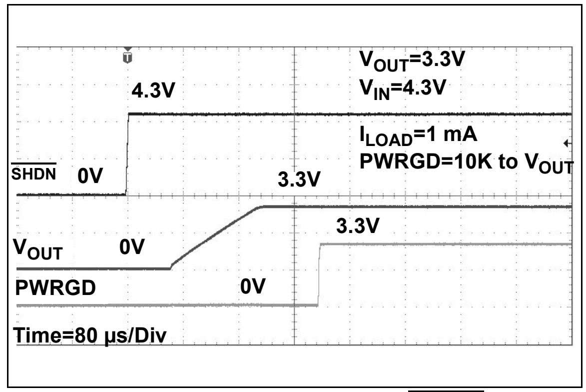


FIGURE 2-28: *Start-up from $\overline{SHDN}$.*

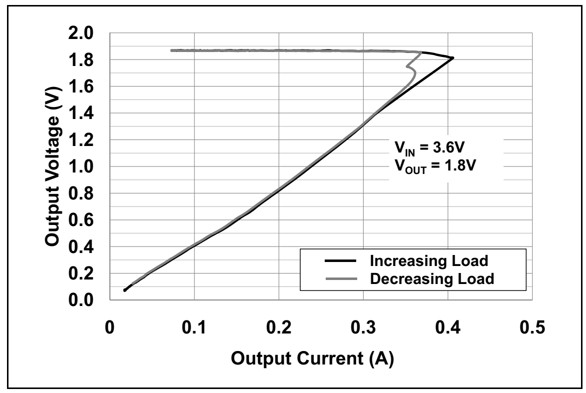


FIGURE 2-29: *Short Circuit Current Foldback.*

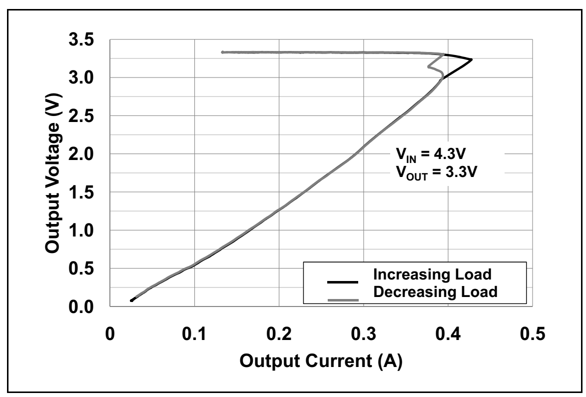


FIGURE 2-30: *Short Circuit Current Foldback.*

Note 1: Unless otherwise indicated V_R = 3.3V, C_{OUT} = 1 µF Ceramic (X7R), C_{IN} = 1 µF Ceramic (X7R), I_L = 1 mA, T_A = +25°C, V_{IN} = V_R + 1V or V_{IN} = 3.6V (whichever is greater), $\overline{SHDN}$ = V_{IN}, package = SOT-223

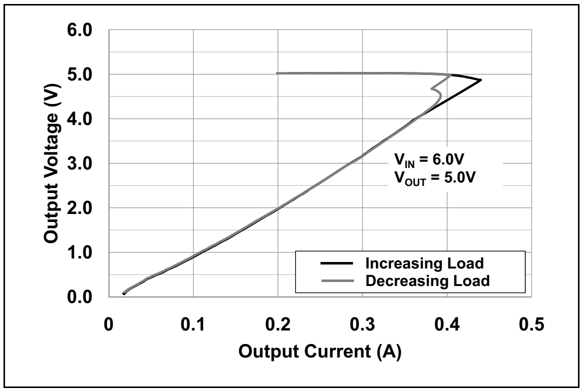


FIGURE 2-31: Short Circuit Current Foldback.

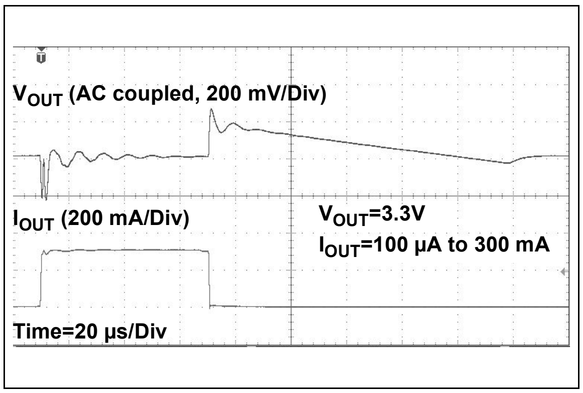


FIGURE 2-32: Dynamic Load Response.

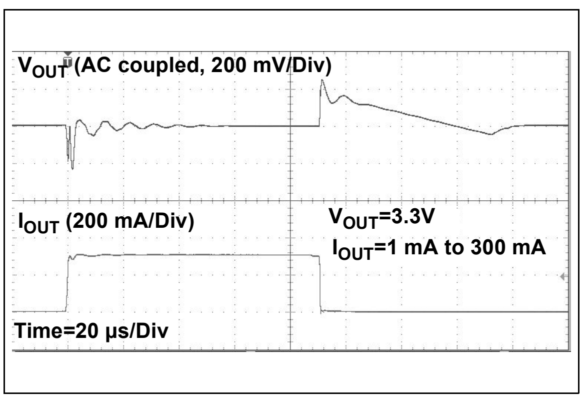


FIGURE 2-33: Dynamic Load Response.

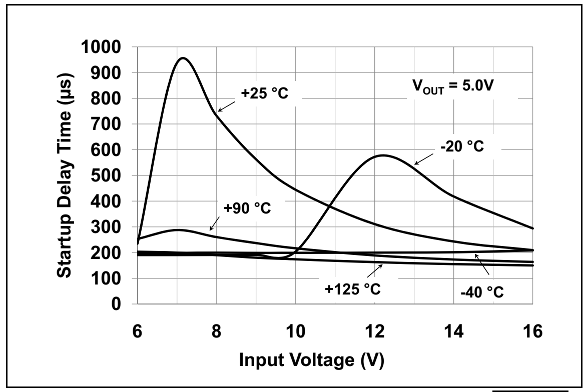


FIGURE 2-34: Start-up Delay From $\overline{SHDN}$ to 90% V_{OUT}.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1 and Table 3-2.

TABLE 3-1: MCP1755 PIN FUNCTION TABLE

SOT-223-5	SOT-23-5	2 x 3 DFN	Name	Function
4	5	1	V_{OUT}	Regulated Voltage Output
5	4	2	PWRGD	Open Drain Power Good Output
—	—	3, 6, 7	NC	No connection
3	2	4	GND	Ground Terminal
1	3	5	$\overline{SHDN}$	Shutdown Input
2	1	8	V_{IN}	Unregulated Supply Voltage
6	—	9	EP	Exposed Pad, Connected to GND

TABLE 3-2: MCP1755S PIN FUNCTION TABLE

SOT-223-3	2 x 3 DFN	Name	Function
3	1	V_{OUT}	Regulated Voltage Output
—	2, 3, 5, 6, 7	NC	No connection
2	4	GND	Ground Terminal
1	8	V_{IN}	Unregulated Supply Voltage
4	9	EP	Exposed Pad, Connected to GND

3.1 Regulated Output Voltage (V_{OUT})

Connect V_{OUT} to the positive side of the load and the positive side of the output capacitor. The positive side of the output capacitor should be physically located as close to the LDO V_{OUT} pin as is practical. The current flowing out of this pin is equal to the DC load current.

3.2 Power Good Output (PWRGD)

The PWRGD output is an open-drain output used to indicate when the LDO output voltage is within 92% (typically) of its nominal regulation value. The PWRGD threshold has a typical hysteresis value of 2%. The PWRGD output is delayed by 100 µs (typical) from the time the LDO output is within 92% + 3% (maximum hysteresis) of the regulated output value on power-up. This delay time is internally fixed. The PWRGD pin may be pulled up to V_{IN} or V_{OUT}. Pulling up to V_{OUT} conserves power when the device is in Shutdown ($\overline{SHDN}$ = 0V) mode.

3.3 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output capacitor and also to the negative side of the input capacitor. Only the LDO bias current flows out of this pin; there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.4 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is used to turn the LDO output voltage on and off. When the $\overline{SHDN}$ input is at a logic-high level, the LDO output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic-low level, the LDO output voltage is disabled. When the $\overline{SHDN}$ input is pulled low, the PWRGD output also goes low and the LDO enters a low quiescent current shutdown state.

3.5 Unregulated Input Voltage (V_{IN})

Connect V_{IN} to the input unregulated source voltage. Like all low dropout linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. For most applications, 1 µF of capacitance will ensure stable operation of the LDO circuit. The input capacitor should have a capacitance value equal to or larger than the output capacitor for performance applications. The input capacitor will supply the load current during transients and improve performance. For applications that have load currents below 10 mA, the input capacitance requirement can be lowered. The type of capacitor used may be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.6 Exposed Pad (EP)

Some of the packages have an exposed metal pad on the bottom of the package. The exposed metal pad gives the device better thermal characteristics by providing a good thermal path to either the PCB or heatsink to remove heat from the device. The exposed pad of the package is internally connected to GND.

4.0 DEVICE OVERVIEW

The MCP1755/1755S is a 300 mA output current, low-dropout (LDO) voltage regulator. The low-dropout voltage of 300 mV typical at 300 mA of current makes it ideal for battery-powered applications. The input voltage range is 3.6V to 16.0V. Unlike other high output current LDOs, the MCP1755/1755S typically draws only 300 µA of quiescent current for a 300 mA load. The MCP1755 adds a shutdown control input pin and a power good output pin. The output voltage options are fixed.

4.1 LDO Output Voltage

The MCP1755 LDO has a fixed output voltage. The output voltage range is 1.8V to 5.5V. The MCP1755S LDO is available as a fixed voltage device.

4.2 Output Current and Current Limiting

The MCP1755/1755S LDO is tested and ensured to supply a minimum of 300 mA of output current. The MCP1755/1755S has no minimum output load, so the output load current can go to 0 mA and the LDO will continue to regulate the output voltage to within tolerance.

The MCP1755/1755S also incorporates a true output current foldback. If the output load presents an excessive load due to a low-impedance short circuit condition, the output current and voltage will fold back towards 30 mA and 0V, respectively. The output voltage and current will resume normal levels when the excessive load is removed. If the overload condition is a soft overload, the MCP1755/1755S will supply higher load currents of up to typically 350 mA. This allows for device usage in applications that have pulsed load currents having an average output current value of 300 mA or less.

Output overload conditions may also result in an overtemperature shutdown of the device. If the junction temperature rises above +150°C (typical), the LDO will shut down the output. See **Section 4.8, Overtemperature Protection** for more information on overtemperature shutdown.

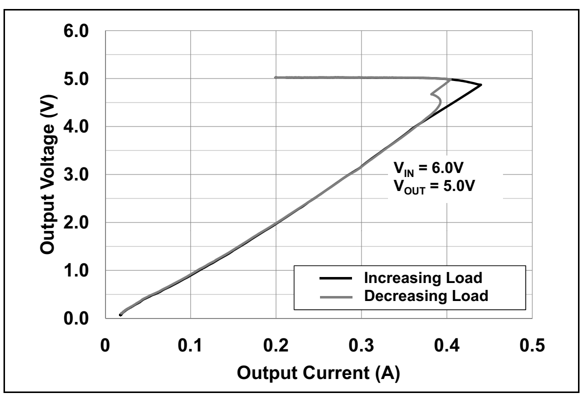


FIGURE 4-1: *Typical Current Foldback.*

4.3 Output Capacitor

The MCP1755/1755S requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The Equivalent Series Resistance (ESR) of the electrolytic output capacitor should be no greater than 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 milli-ohms.

Larger LDO output capacitors can be used with the MCP1755/1755S to improve dynamic performance and power supply ripple rejection performance. A maximum of 1000 µF is recommended. Aluminum-electrolytic capacitors are not recommended for low temperature applications of < -25°C.

4.4 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from, in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent or higher value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.5 Power Good Output (PWRGD)

The open drain PWRGD output is used to indicate when the output voltage of the LDO is within 92% (typical value, see **Section 1.0 "Electrical Characteristics"** for Minimum and Maximum specifications) of its nominal regulation value.

As the output voltage of the LDO rises, the open-drain PWRGD output will actively be held low until the output voltage has exceeded the power good threshold plus the hysteresis value. Once this threshold has been exceeded, the power good time delay is started (shown as T_{PG} in the **AC/DC Characteristics** table). The power good time delay is fixed at 100 µs (typical). After the time delay period, the PWRGD open-drain output becomes inactive and may be pulled high by an external pullup resistor, indicating that the output voltage is stable and within regulation limits. The power good output is typically pulled up to V_{IN} or V_{OUT}. Pulling the signal up to V_{OUT} conserves power during Shutdown mode.

If the output voltage of the LDO falls below the power good threshold, the power good output will transition low. The power good circuitry has a 200 µs delay when detecting a falling output voltage, which helps to increase noise immunity of the power good output and avoid false triggering of the power good output during fast output transients. See Figure 4-2 for power good timing characteristics.

When the LDO is put into Shutdown mode using the $\overline{SHDN}$ input, the power good output is pulled low immediately, indicating that the output voltage will be out of regulation. The timing diagram for the power good output when using the shutdown input is shown in Figure 4-3.

The power good output is an open-drain output that can be pulled up to any voltage that is equal to or less than the LDO input voltage. This output is capable of sinking a minimum of 5 mA (V_{PWRGD} < 0.45V).

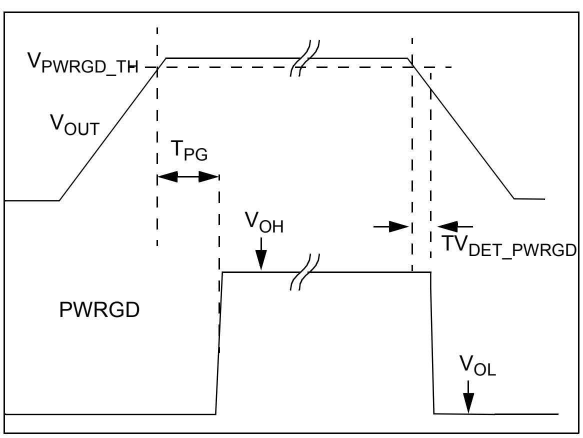


FIGURE 4-2: *Power Good Timing.*

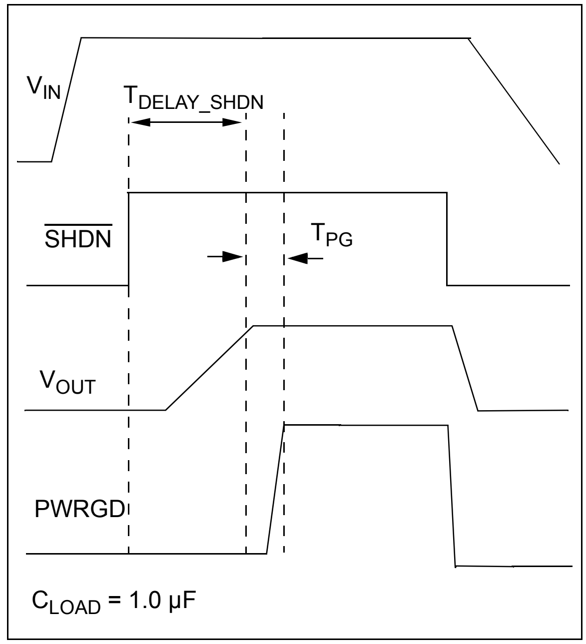


FIGURE 4-3: *Power Good Timing from Shutdown.*

4.6 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The $\overline{SHDN}$ threshold is a fixed voltage level. The minimum value of this shutdown threshold required to turn the output ON is 2.4V. The maximum value required to turn the output OFF is 0.8V.

The $\overline{SHDN}$ input will ignore low-going pulses (pulses meant to shut down the LDO) that are up to 400 ns in pulse width. If the shutdown input is pulled low for more than 400 ns, the LDO will enter Shutdown mode. This small bit of filtering helps to reject any system noise spikes on the shutdown input signal.

On the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry has a 135 µs delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{SHDN}$ input signal. After the 135 µs delay, the LDO output enters its soft-start period as it rises from 0V to its final regulation value. If the $\overline{SHDN}$ input signal is pulled low during the 135 µs delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. The total time from the $\overline{SHDN}$ input going high (turn-on) to the LDO output being in regulation is typically 235 µs. See Figure 4-4 for a timing diagram of the $\overline{SHDN}$ input.

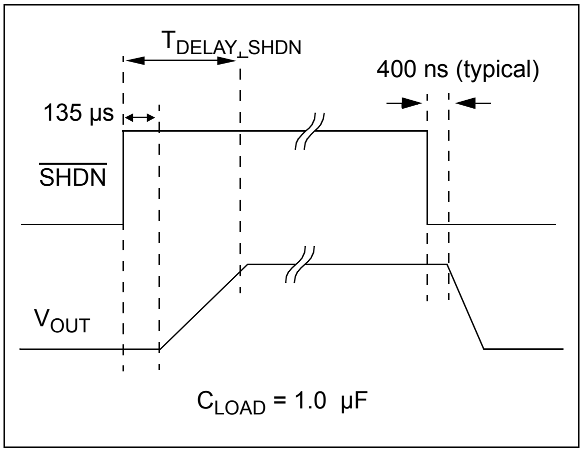


FIGURE 4-4: *Shutdown Input Timing Diagram.*

4.7 Dropout Voltage and Undervoltage Lockout

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a V_R + 1.0V differential applied. The MCP1755/1755S LDO has a very low dropout voltage specification of 300 mV (typical) at 300 mA of output current. See **Section 1.0 "Electrical Characteristics"** for maximum dropout voltage specifications.

The MCP1755/1755S LDO operates across an input voltage range of 3.6V to 16.0V and incorporates input undervoltage lockout (UVLO) circuitry that keeps the LDO output voltage off until the input voltage reaches a minimum of 3.00V (typical) on the rising edge of the input voltage. As the input voltage falls, the LDO output will remain on until the input voltage level reaches 2.70V (typical).

For high-current applications, voltage drops across the PCB traces must be taken into account. The trace resistances can cause significant voltage drops between the input voltage source and the LDO. For applications with input voltages near 3.0V, these PCB trace voltage drops can sometimes lower the input voltage enough to trigger a shutdown due to undervoltage lockout.

4.8 Overtemperature Protection

The MCP1755/1755S LDO has temperature-sensing circuitry to prevent the junction temperature from exceeding approximately +150°C. If the LDO junction temperature does reach +150°C, the LDO output will be turned off until the junction temperature cools to approximately +140°C, at which point the LDO output will automatically resume normal operation. If the internal power dissipation continues to be excessive, the device will again shut off. The junction temperature of the die is a function of power dissipation, ambient temperature and package thermal resistance. See **Section 5.0 "Application Circuits and Issues"** for more information on LDO power dissipation and junction temperature.

NOTES:

5.0 APPLICATION CIRCUITS AND ISSUES

5.1 Typical Application

The MCP1755/1755S is most commonly used as a voltage regulator. The low quiescent current and low dropout voltage make it ideal for many battery-powered applications.

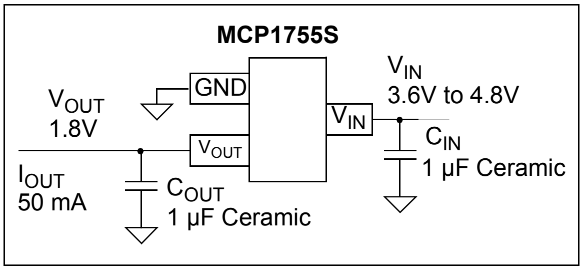


FIGURE 5-1: Typical Application Circuit.

5.1.1 APPLICATION INPUT CONDITIONS

Package Type = SOT-23
Input Voltage Range = 3.6V to 4.8V
V_{IN} maximum = 4.8V
V_{OUT} typical = 1.8V
I_{OUT} = 50 mA maximum

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1755/1755S is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low, it is insignificant (68.0 µA x V_{IN}). The following equation can be used to calculate the internal power dissipation of the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

P_{LDO} = LDO Pass device internal power dissipation
$V_{IN(MAX)}$ = Maximum input voltage
$V_{OUT(MIN)}$ = LDO minimum output voltage

The maximum continuous operating junction temperature specified for the MCP1755/1755S is +150°C. To estimate the internal junction temperature of the MCP1755/1755S, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$). The thermal resistance from junction to ambient for the SOT-23 package is estimated at 336°C/W.

EQUATION 5-2:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

$T_{J(MAX)}$ = Maximum continuous junction temperature
P_{TOTAL} = Total device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction to ambient
T_{AMAX} = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 5-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
$T_{J(MAX)}$ = Maximum continuous junction temperature
$T_{A(MAX)}$ = Maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION 5-4:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
$P_{D(MAX)}$ = Maximum device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION 5-5:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction temperature
$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
T_A = Ambient temperature

5.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

EXAMPLE 5-1: POWER DISSIPATION

Package

Package Type = SOT-23

Input Voltage

V_{IN} = 3.6V to 4.8V

LDO Output Voltages and Currents

V_{OUT} = 1.8V

I_{OUT} = 50 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = +40°C

Internal Power Dissipation

Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (V_{IN} to V_{OUT}).

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

P_{LDO} = (4.8V – (0.97 x 1.8V)) x 50 mA

P_{LDO} = 152.7 mW

5.3.1 DEVICE JUNCTION TEMPERATURE RISE

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, *"High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages"*. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, "*A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application"* (DS00792), for more information regarding this subject.

EXAMPLE 5-2:

$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$

T_{JRISE} = 152.7 mW x 336.0°C/Watt

T_{JRISE} = 51.3°C

5.3.2 JUNCTION TEMPERATURE ESTIMATE

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

EXAMPLE 5-3:

$T_J = T_{JRISE} + T_{A(MAX)}$

T_J = 91.3°C

Maximum Package Power Dissipation Examples at +40°C Ambient Temperature

SOT-23 (336.0°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C – 40°C)/336°C/W

$P_{D(MAX)}$ = 253 mW

SOT-89 (153.3°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C – 40°C)/153.3°C/W

$P_{D(MAX)}$ = 554 mW

5.4 Voltage Reference

The MCP1755/1755S can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1755/1755S LDO. The low-cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1755/1755S as a voltage reference.

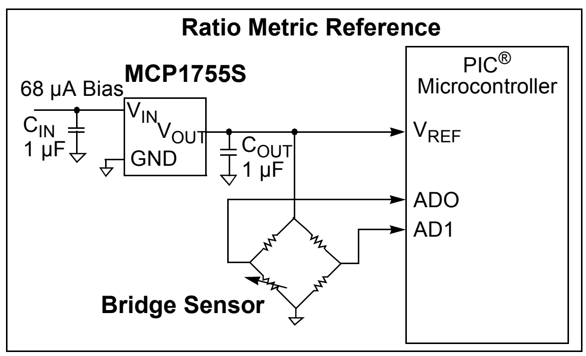


FIGURE 5-2: *Using the MCP1755/1755S as a Voltage Reference.*

5.5 Pulsed Load Applications

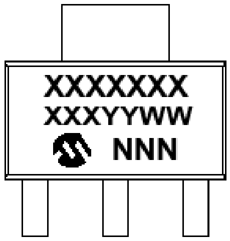
For some applications, there are pulsed load current events that may exceed the specified 300 mA maximum specification of the MCP1755/1755S. The internal current limit of the MCP1755/1755S will prevent high peak load demands from causing non-recoverable damage. The 300 mA rating is a maximum average continuous rating. As long as the average current does not exceed 300 mA, higher pulsed load currents can be applied to the MCP1755/1755S. The typical foldback current limit for the MCP1755/1755S is 350 mA (T_A = +25°C).

NOTES:

6.0 PACKAGING INFORMATION

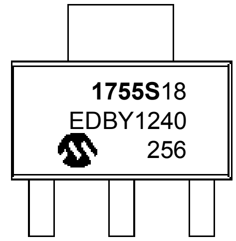
6.1 Package Marking Information

3-Lead SOT-223 **(MCP1755S only)**

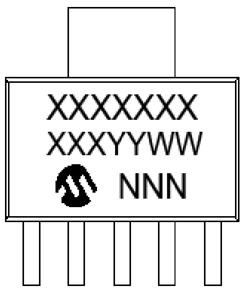


Part Number	First Line Code
MCP1755S-1802E/DB	1755S18
MCP1755ST-1802E/DB	1755S18
MCP1755S-3302E/DB	1755S33
MCP1755ST-3302E/DB	1755S33
MCP1755S-5002E/DB	1755S50
MCP1755ST-5002E/DB	1755S50

Example:

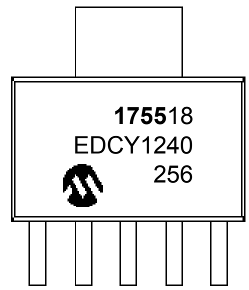


5-Lead SOT-223 **(MCP1755 only)**

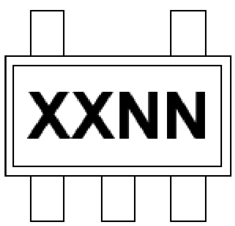


Part Number	First Line Code
MCP1755T-1802E/DC	175518
MCP1755T-3302E/DC	175533
MCP1755T-5002E/DC	175550

Example:

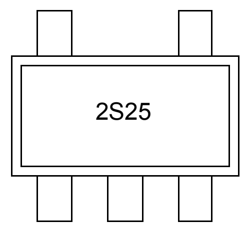


5-Lead SOT-23 **(MCP1755 only)**



Part Number	Code
MCP1755T-1802E/OT	2SNN
MCP1755T-3302E/OT	3CNN
MCP1755T-5002E/OT	3DNN

Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.