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MCP18480

-48V Hot Swap Controller

Features

- Allows safe board removal and insertion from a live backplane
- Accurate (<1.5%) internal voltage reference for fault detection and precision timing
- Programmable foldback current limiting
- Programmable circuit breaker current limiting
- Auto restart option for all faults
- Adjustable Undervoltage lockout thresholds
- Adjustable Overvoltage protection threshold
- Adjustable Power Good delay
- Configurable Power Good output polarity
- Low-side drive of an external N-channel FET

CMOS Technology

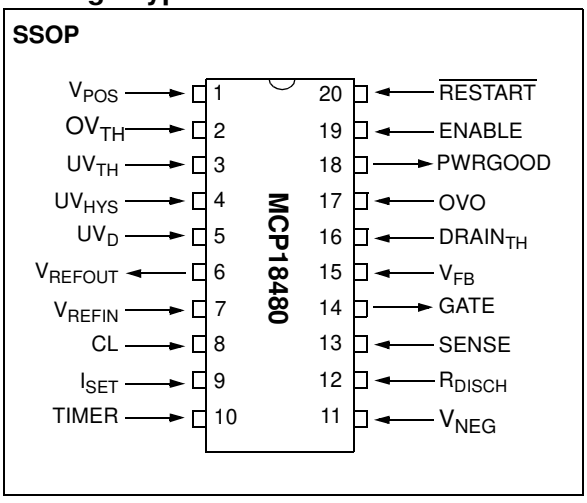
- High-Voltage Operation
- Temperature range: Industrial (I): -40°C to +85°C

Packaging

- 20-lead SSOP

Package Type

SSOP



Description

The MCP18480 is a Hot Swap controller that allows boards to be safely removed or inserted from an active backplane using -48V.

When PCBs are inserted into a live backplane, high-peak or transient currents from the source are generated due to the charging of the bypass capacitors on the supply. The high transient currents can destroy connectors and capacitors. The high inrush current can pull the input voltage BUS down and reset the system.

The MCP18480 solves this problem by controlling the slew rate of the backplane voltage to the board so that these transients are eliminated. This allows boards to be removed and inserted without causing damage to connector pins and input bulk capacitors, in addition to preventing false resets to the other boards on the backplane.

The MCP18480 can be used in applications in several areas including:

- Telecom Line Cards
- Network Switches
- Network Routers and Servers
- Base Station Line Cards
- Power-Over-LAN
- Power-Over-MDI
- IP Phone Switches/Routers
- Mid-Span, Power-Over-MDI

Two forms of current limit are provided in the MCP18480. These are:

- Foldback
- Circuit breaker

The foldback current-limiting circuit uses an external sense resistor and a voltage that is proportional to the external MOSFET's drain voltage. These are used to keep the MOSFET in its Safe Operating Area (SOA).

If the device remains in current limit for a programmed time period, the external N-channel FET is turned off. The option exists to configure the device to automatically restart after a programmed time delay. A programmable catastrophic current limit threshold shuts down the switch (circuit breaker) if excessive current is sensed due to a short-circuit condition.

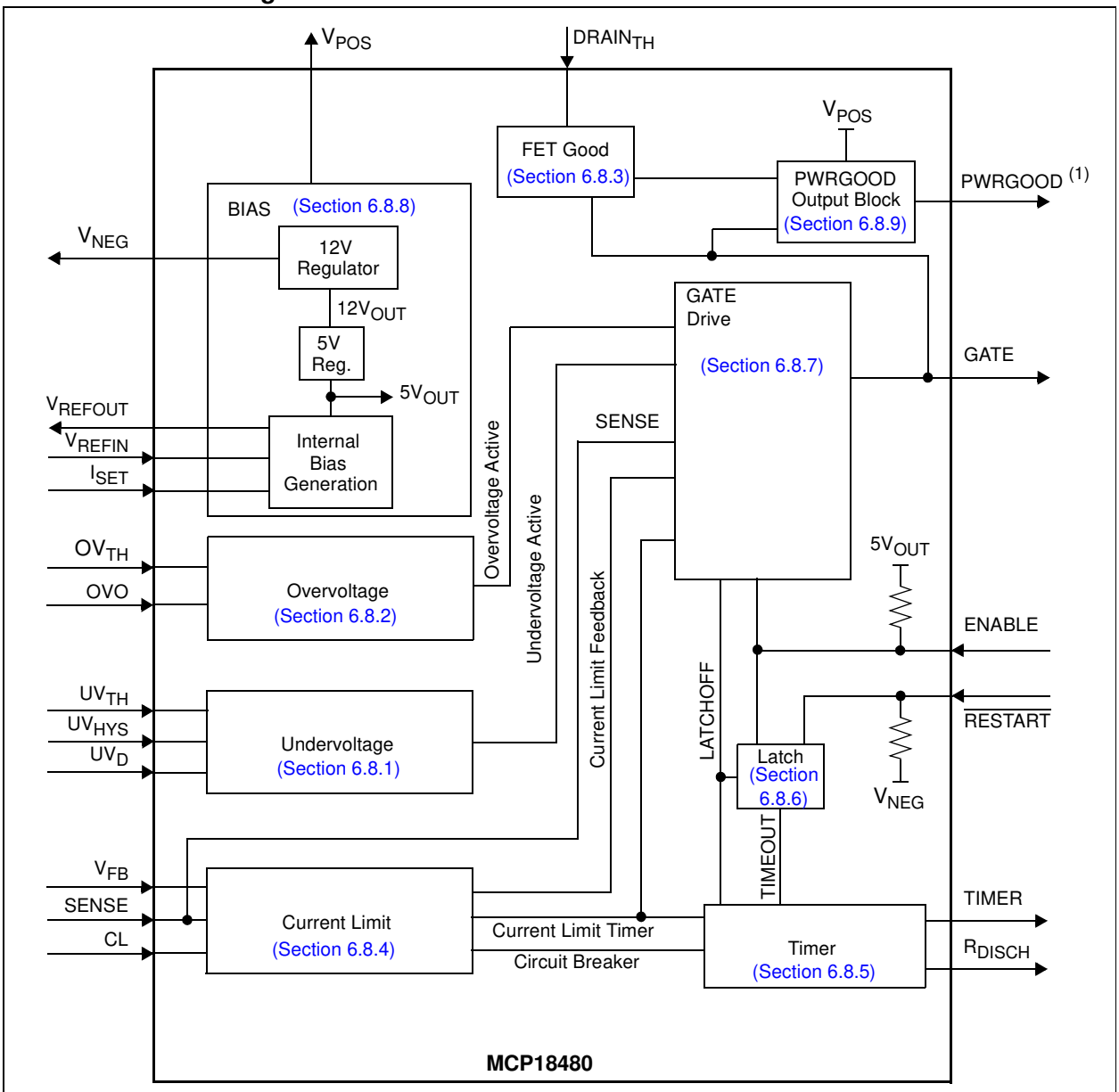
Internal comparators are incorporated to add hysteresis for adjusting the Undervoltage Lockout (UVLO) threshold. The external N-channel MOSFET is turned on when the input is below the user-programmable, Overvoltage threshold and above the user-programmable, Undervoltage threshold.

The PWRGOOD pin indicates the status of the MCP18480 and is active when the device has completed power-up and the system is not in an Undervoltage, Overvoltage or current-limit condition.

PWRGOOD can be externally configured to either active-high or active-low to accommodate external circuitry (power supplies) that have either enabling logic.

A block diagram of the MCP18480 is shown below.

MCP18480 Block Diagram



Note 1: The PWRGOOD output pin can be either active-high or active-low. This polarity is determined by the voltage (either the level on the V_{REFIN} pin or level on the V_{NEG} pin) on the I_{SET} pin:

- Connecting the external R_{ISET} resistor to V_{REFIN} configures the PWRGOOD pin as active-low
- Connecting the external R_{ISET} resistor to V_{NEG} configures the PWRGOOD pin as active-high

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –40°C to +85°C

Storage Temperature ..... –65°C to +150°C

Voltage on V_{POS} with respect to V_{NEG} -0.3V to +15.0V

Voltage on DV_{TH}, UV_{TH}, V_{FB}, OVO and UV_{HYS} pins with respect to V_{NEG} ..... V_{NEG} – 0.3V to (V_{POS} + 0.3V)

Voltage on V_{REFIN}, CL, SENSE, $DRAIN_{TH}$, ENABLE and RESTART pins with respect to V_{NEG} ..... V_{NEG} - 0.3V to 6V.

Total Power Dissipation **(Note 1)** ..... 800 mW

Max. Current out of V_{NEG} pin ..... 80 mA

Max. Current into V_{POS} pin ..... 50 mA

Max. Output Current sunk by Gate pin..... 80 mA

Max. Output Current sunk by V_{REFOUT} pin ..... 5 mA

Max. Output Current sunk by any other Output pin..... 25 mA

Max. Output Current sourced by Gate pin ..... 200 µA

Max. Output Current sourced by V_{REFOUT} pin ..... 5 mA

Max. Output Current sourced by any other Output pin..... 25 mA

Junction to Ambient, Θ_{JA} (20 pin SSOP Package) Derating ..... 108.1°C/W

Junction to Case, Θ_{JC} (20 pin SSOP Package) Derating ..... 32.2°C/W

Lead Temperature, Soldering, 10 seconds ..... 300°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power Dissipation is calculated as follows:

$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma\{(V_{DD}-V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, operating temperature: –40°C ≤ T_A ≤ +85°C (Industrial), Supply Current: 5 mA ≤ I_{POS} ≤ 25 mA, R_{ISET} = 125 kΩ, C_{BYP} = 2 µF.

Param. No.	Parameter		Sym	Min	Typ (1)	Max	Units	Conditions
MD001	Current into shunt regulator that produces V_{POS} output voltage that meets MD001A specification		I_{POS1}	5	—	25	mA	ENABLE pin = 5V
				5	—	25		ENABLE pin = V_{NEG}
MD001A	Regulated Output Voltage Differential of V_{POS} to V_{NEG}		V_{POS}	10.4	12.0	13.4	V	See MD001
MD002	V_{REFOUT} pin output voltage		V_{REFOUT}	2.463	2.5	2.538	V	Load = 50 µA
MD010	V_{GATE} pin output voltage		V_{GATE}	V_{POS} - 2	V_{POS} -1	V_{POS}	V	
MD011	Voltage on I_{SET} pin		V_{ISET}	(V_{REFIN}/2) - 0.02	V_{REFIN}/2	(V_{REFIN}/2) +0.02	V	
MD012A	Voltage on SENSE pin to trigger current-limiting		V_{SENSE}	40	50	60	mV	$V_{FB} = V_{NEG}$
MD012B				25	31.0	40	mV	$V_{FB} = V_{NEG}$ + 0.25V
MD012C				7	12	17	mV	$V_{FB} = V_{NEG}$ + 0.5V
MD013	Undervoltage Threshold		UV_{TH}	V_{REFIN} - 0.03	V_{REFIN}	V_{REFIN} + 0.03	V	
MD014A	Overvoltage Threshold	rising	OV_{TH}	V_{REFIN} - 0.05	V_{REFIN}	V_{REFIN} + 0.05	V	V_{REFIN} = 2.5V
MD014B		falling	OV_{TH}	V_{REFIN} - 0.035	V_{REFIN} - 0.02	V_{REFIN} - 0.005	V	V_{REFIN} = 2.5V
MD015	DRAIN Pin Input Threshold Voltage		V_{DTH}	90	100	130	mV	

Note 1: Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

2: Negative current is defined as current sourced by the pin.

3: All voltages are with respect to the V_{NEG} pin voltage.

DC Characteristics (Continued)

Electrical Specification: Unless otherwise specified, operating temperature: –40°C ≤ T_A ≤ +85°C (Industrial), Supply Current: 5 mA ≤ I_{POS} ≤ 25 mA, R_{ISET} = 125 kΩ, C_{BYP} = 2 µF

Param. No.	Parameter		Sym	Min	Typ (1)	Max	Units	Conditions
MD020	DRAIN pin current		I_{DRAIN}	—	—	0.1	µA	$DRAIN_{TH}$ pin = V_{NEG}
MD021	SENSE pin current		I_{SENSE}	—	—	0.1	µA	
MD022	GATE pin current	Pull-up	I_{GATE}					SENSE pin = V_{NEG} GATE pin = V_{NEG} +4V
MD022A				-30	-50	-75	µA	V_{FB} = V_{NEG}
MD022B				-9	-17	-33	µA	V_{FB} = V_{NEG} + 500 mV
MD022C		Pull-down	I_{GATE}	31	49	72	mA	Any fault condition
MD023	UV_D pin current		I_{UVD}	-7	-10	-15	µA	UV_{TH} < V_{REFIN}
MD024A	TIMER pin current	Pull-up	I_{TIMER}	-100	-160	-200	µA	R_{ISET} = 125 kΩ, V_{REFIN} = 2.5V
MD024B		Pull-down		52	78	104	nA	R_{ISET} = 125 kΩ, V_{REFIN} = 2.5V R_{DISCH} = 1.6 MΩ
MD025	I_{SET} pin current		I_{ISET}	$V_{ISET(MIN)}$ $R_{ISET(MAX)}$	—	$V_{ISET(MAX)}$ $R_{ISET(MIN)}$	A	**See MD011**

Note 1: Data in the Typical ("Typ") column is based on characterization results at +25°C. This data is for design guidance only and is not tested.

2: Negative current is defined as current sourced by the pin.

3: All voltages are with respect to the V_{NEG} pin voltage.

DC Characteristics (Continued)

Electrical Specifications: Unless otherwise specified, operating temperature: –40°C ≤ T_A ≤ +85°C (Industrial), Supply Current: 5 mA ≤ I_{POS} ≤ 25 mA, R_{ISET} = 125 kΩ, C_{BYP} = 2 µF.

Param #	Parameter	Sym	Min	Typ	Max	Units	Conditions
MD030	Input Low Voltage	V_{IL}					
MD031	ENABLE pin		V_{NEG}	—	0.8	V	
MD032	$\overline{\text{RESTART}}$ pin		V_{NEG}	—	0.8		
MD040	Input High Voltage	V_{IH}					
MD041	ENABLE pin		2.0	—	5.0	V	
MD042	$\overline{\text{RESTART}}$ pin		2.0	—	5.0	V	
MD050	Internal Resistance on UV_{HYS} pin	R_{UVHYS}	500	1200	2100	Ω	$V_{UVTH} < V_{REFIN}$, I_{UVHYS} = 30 µA
			50	100	—	MΩ	$V_{UVTH} > V_{REFIN}$, I_{UVHYS} = 30 µA
	Input Leakage Current (Notes 2, 3)						
MD060A	OV_{TH}, UV_{TH}, V_{FB}, OVO and UV_{HYS} pins	I_{IL}	-1	—	+1	µA	$V_{NEG} \le V_{PIN} \le 11V$, Pin at high-impedance
MD060B	V_{REFIN}, CL, SENSE, $DRAIN_{TH}$, ENABLE and RESTART pins		—	—	±1	µA	$V_{NEG} \le V_{PIN} \le 5V$, Pin at hi-impedance
MD070	Minimum current into ENABLE pin to disable MCP18480	I_{EN}	—	10	30	µA	I_{POS} = 5 mA, ENABLE = 0.8V
	Output Low Voltage	V_{OL}					
MD080	PWRGOOD pin		0	—	0.4	V	I_{OL} = 5 mA
	Output High Voltage	V_{OH}		—			
MD090	PWRGOOD pin		0.8 V_{POS}	0.96 V_{POS}	V_{POS}	V	I_{OH} = 2 mA, 7 mA ≤ I_{POS} ≤ 12 mA
MD100	Offset Voltage at the internal comparator input that is connected to the CL pin.	V_{CL}	-15	—	+15	mV	V_{FB} = 0

Note 1: All voltages are with respect to the V_{NEG} pin voltage.

2: The leakage currents on the ENABLE and $\overline{\text{RESTART}}$ pins are strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

1.1 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created using one of the following formats:

1.1.1 TIMING CONDITIONS

The temperature and voltages specified in Table 1-2 apply to all timing specifications, unless otherwise noted. Figure 1-1 specifies the load conditions for the timing specifications.

TABLE 1-1: SYMBOLOGY

1. TppS2ppS

T	
F	Frequency
E	Error

2. TppS

T	Time

Lowercase letters (pp) indicate the device pin.

Uppercase letters and their meanings:

S			
F	Fall	P	Period
FR	Fast Ramp	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low		

TABLE 1-2: AC TEMPERATURE AND VOLTAGE SPECIFICATIONS

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated) Operating temperature: –40°C ≤ T_A ≤ +85°C (industrial) Operating voltage V_{DD} range as described in DC spec Section 1.0.

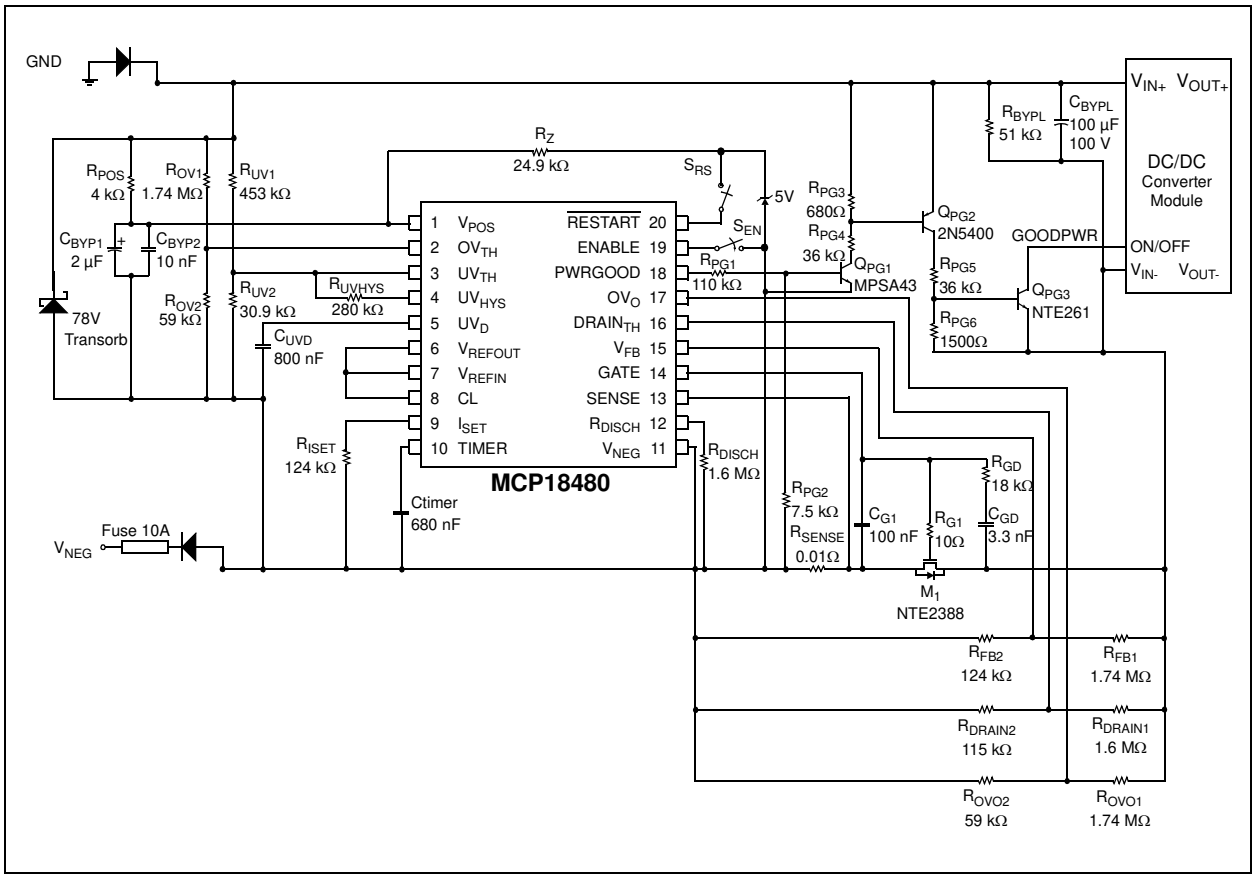
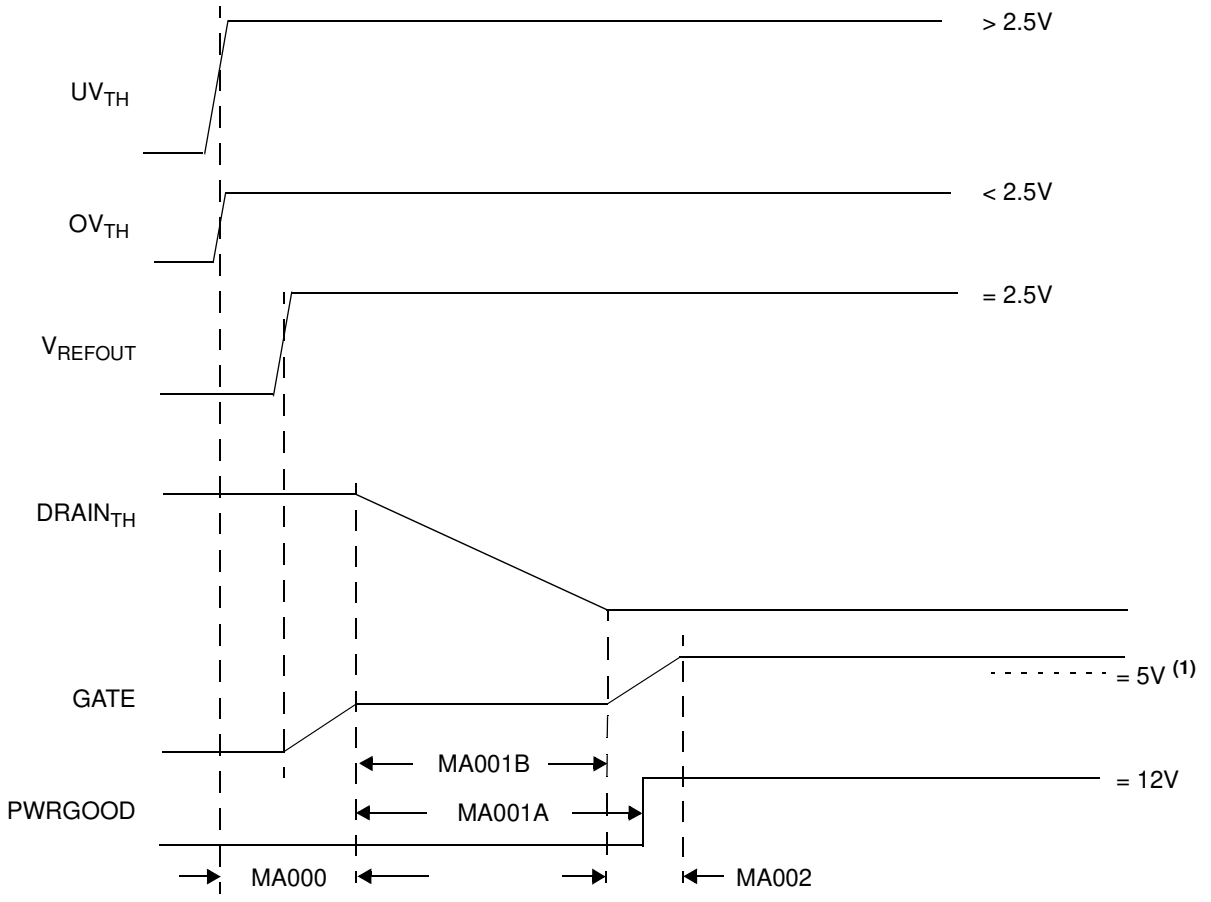


FIGURE 1-1: *Load Conditions for Device Timing Specifications.*

1.2 Timing Diagrams and Specifications



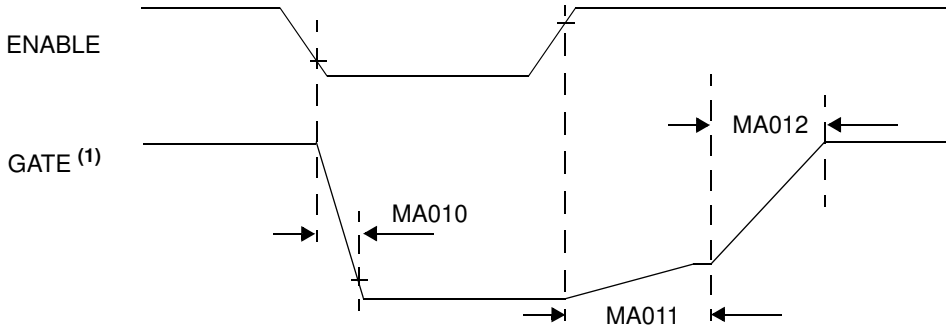
Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

FIGURE 1-2: *Startup Waveforms.*

TABLE 1-3: STARTUP TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA000	UV_{TH}/OV_{TH} High (V_{POS} applied) to $DRAIN_{TH}$ falling	$T_{UVOV}H2_{DTH}F$	—	20.2	—	ms	
MA001A	$DRAIN_{TH}$ falling to PWRGOOD High	$T_{DTH}F2_{GATE}PGH$	—	19.3	—	ms	
MA001B	$DRAIN_{TH}$ falling to GATE Fast Ramp	$T_{DTH}F2_{GATE}FR$	—	13.1	—	ms	
MA002	GATE Fast Ramp to external FET fully enhanced	$T_{GATE}FR2FET_E$	—	16.1	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.



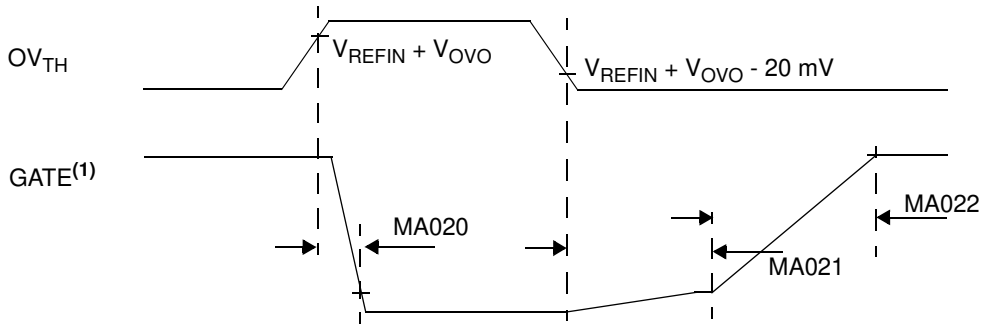
Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

FIGURE 1-3: *ENABLE-to-GATE Waveforms.*

TABLE 1-4: ENABLE-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA010	ENABLE Low to GATE Low	$T_{EN}L2_{GATE}L$	—	23.6	—	µs	
MA011	ENABLE High to GATE Fast Ramp	$T_{EN}H2_{GATE}FR$	—	41	—	ms	
MA012	GATE Fast Ramp to GATE High	$T_{GATE}FR2_{GATE}H$	—	17.8	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.



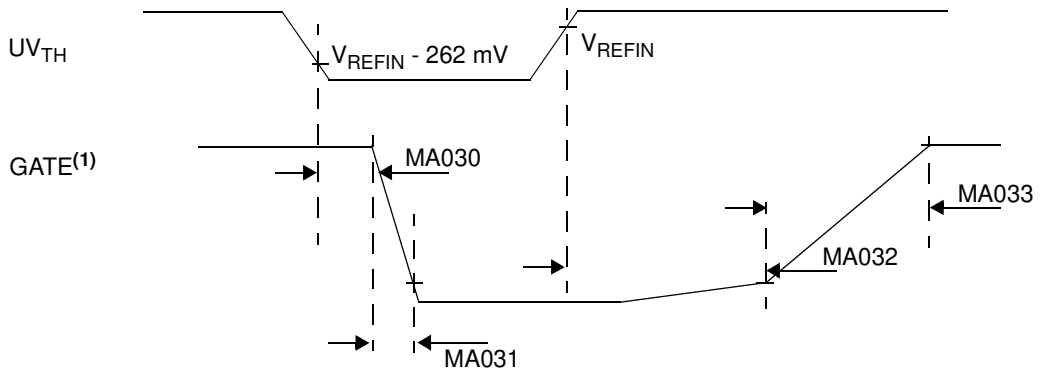
Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

FIGURE 1-4: *OV_{TH}-to-gate Waveform.*

TABLE 1-5: OV_{TH}-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA020	OV_{TH} High to GATE Low	$T_{OV}H2_{GATE}L$	—	58.4	—	µs	
MA021	OV_{TH} Low to GATE Fast Ramp	$T_{OV}L2_{GATE}FR$	—	40.8	—	µs	
MA022	GATE Fast Ramp to GATE High	$T_{GATE}FR2_{GATE}H$	—	17.8	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.



Note 1: This voltage is determined by the threshold voltage of the external FET. This voltage needs to ensure the external FET is fully enhanced.

FIGURE 1-5: *UV_{TH}-to-gate Waveform*

TABLE 1-6: UVTH-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ(1)	Max	Units	Conditions
MA030	UV_{TH} Low to GATE Falling Edge	$T_{UV}L2_{GATE}F$	—	108	—	µs	C_{UVD} = 800 nF
MA031	GATE High to GATE Low	$T_{GATE}H2_{GATE}L$	—	25.8	—	µs	
MA032	ENABLE High to GATE Fast Ramp	$T_{UV}H2_{GATE}FR$	—	40.4	—	ms	
MA033	GATE Fast Ramp to GATE High	$T_{GATE}FR2_{GATE}H$	—	58.4	—	ms	

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C, unless otherwise stated.
2: Minimum and maximum specifications will be provided in future revisions of this data sheet.

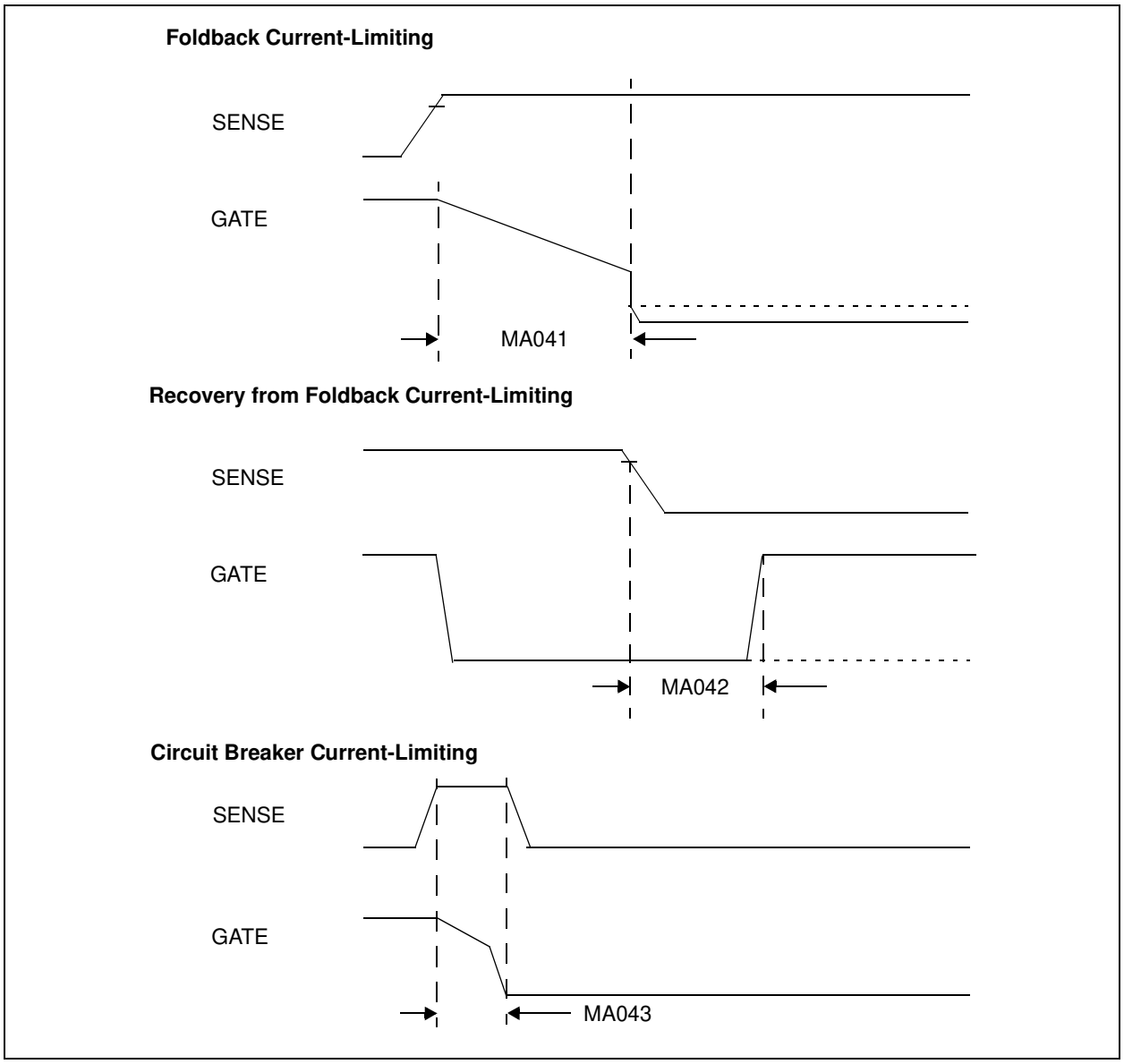


FIGURE 1-6: *Sense-to-gate Waveform.*

TABLE 1-7: SENSE-TO-GATE TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA041	GATE Current Limit to GATE Off	$T_{GATE}CL2_{GATE}O$	—	5.5	—	ms	C_{TIMER} = 0.68 µF R_{ISET} = 124 kΩ
MA042	GATE Current Limit Recovery	$T_{GATE}CL$	—	10.2	—	ms	C_{TIMER} = 0.68 µF R_{ISET} = 124 kΩ
MA043	SENSE High to GATE Off	$T_{SENSE}H2_{GATE}O$	—	3.6	—	ms	

Note: Minimum and maximum specifications will be provided in future revisions of this data sheet.

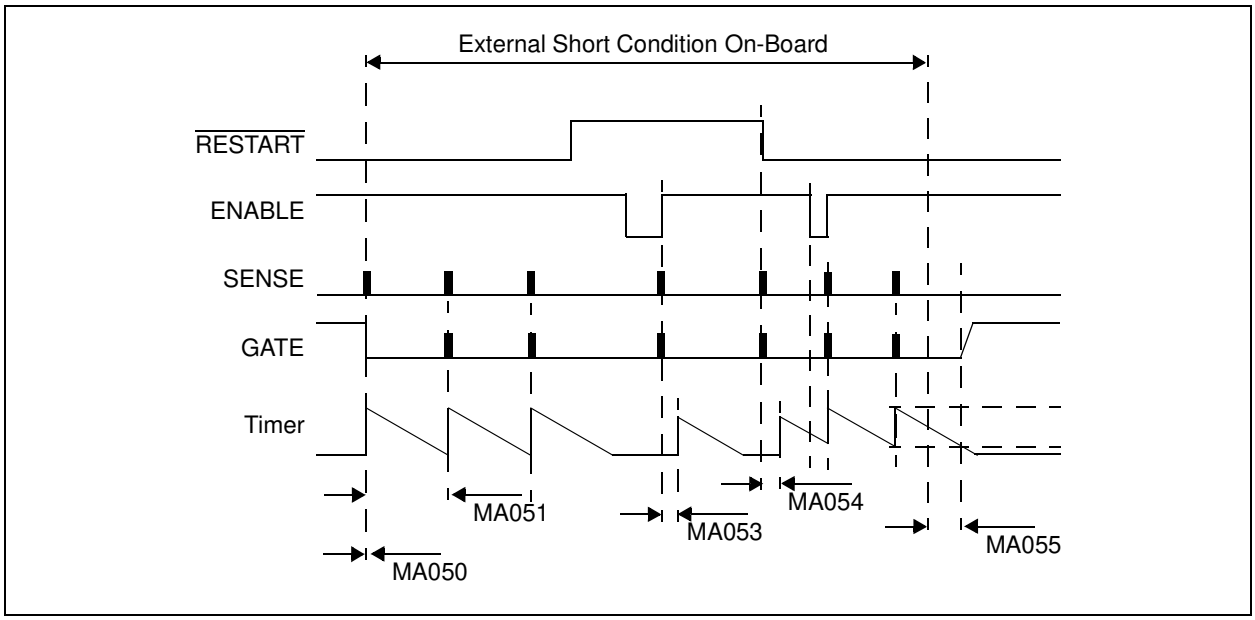


FIGURE 1-7: *Current Limit Waveform.*

TABLE 1-8: CURRENT LIMIT TIMING REQUIREMENTS

Param. No.	Parameter	Sym	Min	Typ	Max	Units	Conditions
MA050	External Short to Timer period start	$T_{SHORT}2_{TIMER}S$	—	171	—	mS	
MA051	Timer period	$T_{TIMER}P$	—	5.8	—	sec	C_{TIMER} = 0.68 µF R_{DISCH} = 1.6 MΩ
MA053	ENABLE High to Timer period start	$T_{ENABLE}H2_{TIMER}S$	—	30.5	—	mS	C_{TIMER} = 0.68 µF R_{DISCH} = 1.6 MΩ
MA054	$\overline{\text{RESTART}}$ Low to Timer period start	$T_{\overline{RESTART}}L2_{TIMER}S$	—	30.9	—	mS	C_{TIMER} = 0.68 µF R_{DISCH} = 11.6 MΩ
MA055	External Short removed to Timer off **Note 2**	$T_{NOSHORT}2_{TIMER}O$	—	5.8	—	sec	C_{TIMER} = 0.68 µF R_{DISCH} = 1.6 MΩ

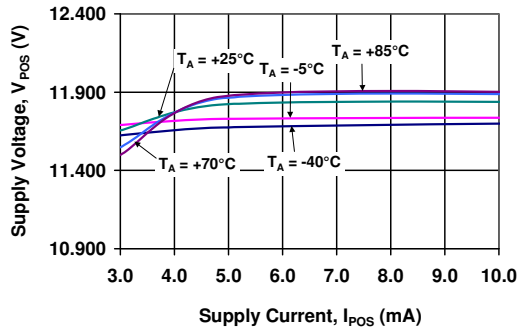
Note 1: Minimum and maximum specifications will be provided in future revisions of this data sheet.

2: This is up to one additional timer period because the external short circuit is removed asynchronously to the timer. The timer must time out before normal operation returns.

NOTES:

2.0 DC CHARACTERISTIC CURVES

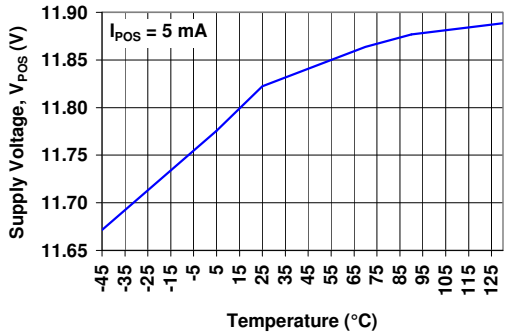
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.



Data taken with the minimum following conditions:

V_{REFIN} = 2.5V, I_{SET} = 10 µA

FIGURE 2-1: *Supply Current (I_{POS}) vs. Supply Voltage (V_{POS}).*

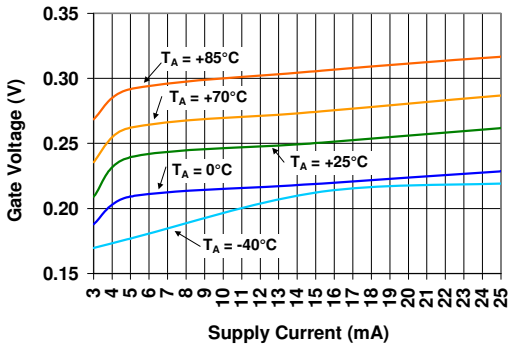


Data taken with the minimum following conditions:

Minimum Supply Current to bring V_{POS} into regulation

V_{REFIN} = 2.5V, I_{SET} = 10 µA

FIGURE 2-2: *Minimum Supply Current vs. Temperature.*



Data taken with the minimum following conditions:

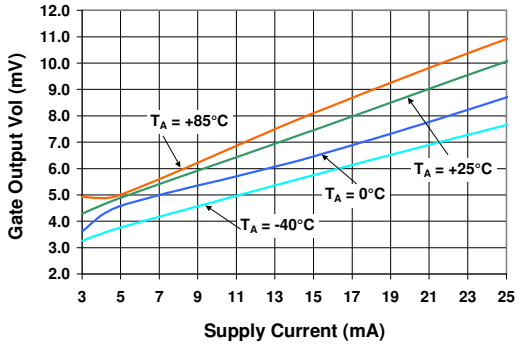
3 mA ≤ I_{POS} ≤ 30 mA

V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-3: *GATE Output High-Voltage (V_{POS}- V_{GATE}) vs. Supply Current (I_{POS}).*



Data taken with the minimum following conditions:

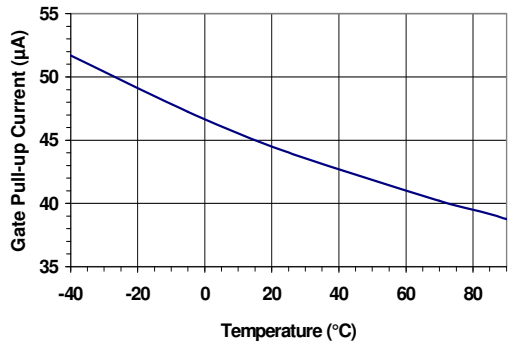
3 mA ≤ I_{POS} ≤ 30 mA

V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
$V_{ENABLE} = V_{VNEG}$
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-4: *GATE Output Low-Voltage (V_{GATE} - V_{NEG}) vs. Supply Current (I_{POS}).*



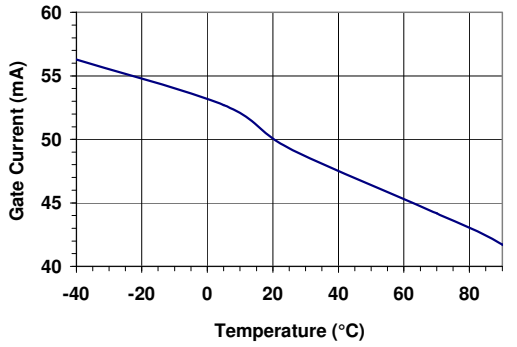
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)

FIGURE 2-5: *GATE Source (Pull-Up) Current vs. Temperature.*



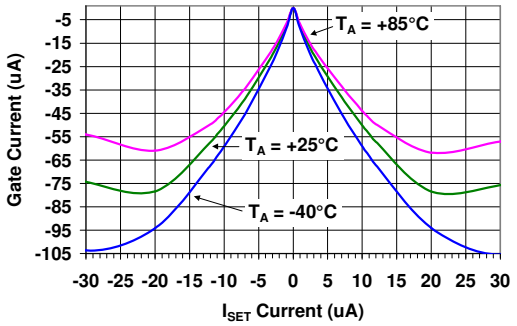
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{GATE} > 0.5V$
$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
$V_{ENABLE} = V_{VNEG}$
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-6: *GATE Sink (Pull-Down) Current vs. Temperature.*



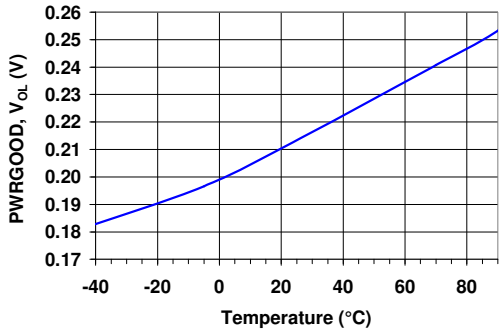
Data taken with the minimum following conditions:

-50 µA µA < I_{ISET} < 50 µA ($I_{ISET} \neq 0$)
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

Note 1:

V_{GATE} > 0.5V
$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-7: *GATE Source Current vs. I_{SET} Pin Current.*



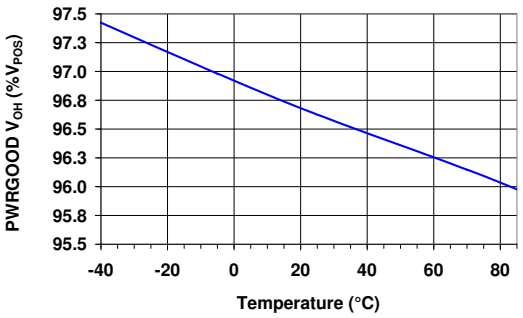
Data taken with the minimum following conditions:

I_{LOAD} = 1 mA
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-8: *PWRGOOD Output Low Voltage (V_{OL}) vs. Temperature.*



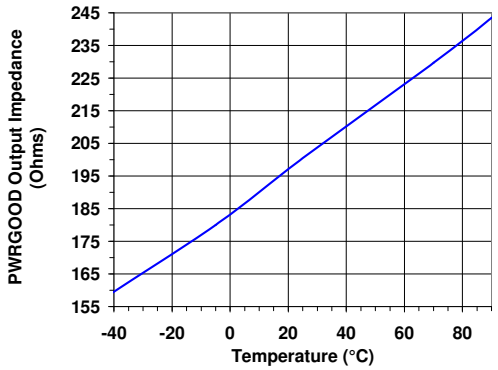
Data taken with the minimum following conditions:

I_{LOAD} = -1 mA
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-9: *PWRGOOD Output High-Voltage (V_{OH}) vs. Temperature.*



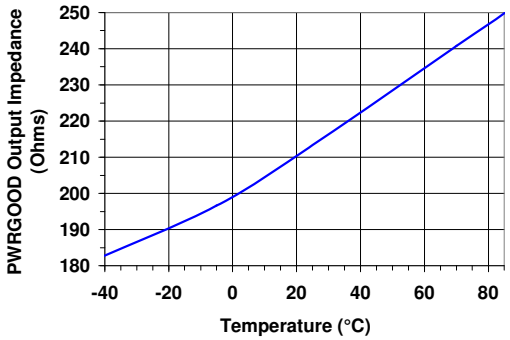
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-10: *PWRGOOD Output High-Impedance vs. Temperature.*



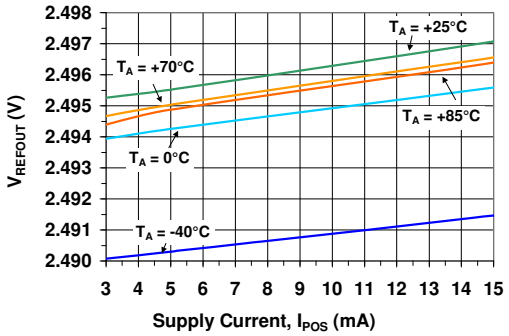
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-11: *PWRGOOD Output Low-Impedance vs. Temperature.*

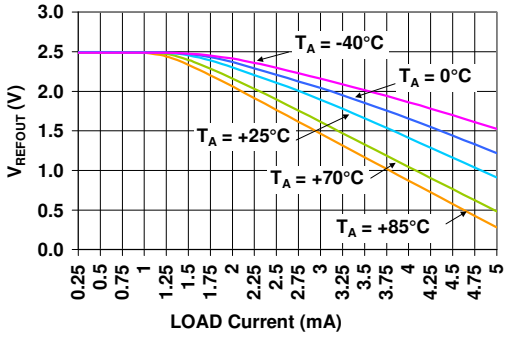


Data taken with the minimum following conditions:

3 mA ≤ I_{POS} ≤ 30 mA

V_{REFIN} = 2.5V, I_{SET} = 10 µA

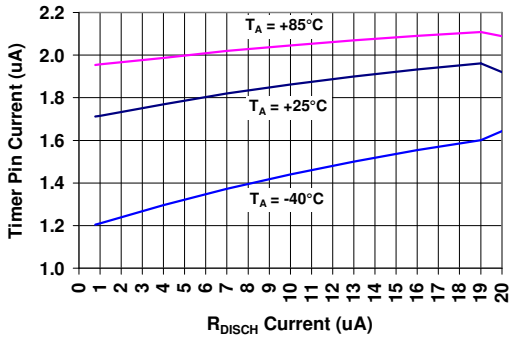
FIGURE 2-12: *V_{REFOUT} vs. Supply Current (I_{POS}).*



Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, Iset = 10 µA

FIGURE 2-13: *V_{REFOUT} vs. LOAD.*



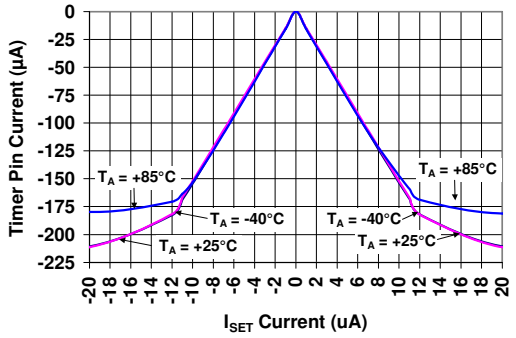
Data taken with the minimum following conditions:

-50 µA < I_{ISET} < 50 µA ($I_{ISET} \neq 0$)
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-14: *TIMER Pin Output Low Current vs. R_{DISCH} Current.*



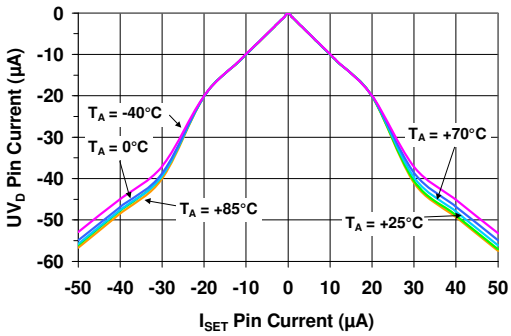
Data taken with the minimum following conditions:

-50 µA < I_{ISET} < 50 µA ($I_{ISET} \neq 0$)
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} \geq 100mV$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-15: *TIMER Pin Output High Current vs. I_{SET} Current.*



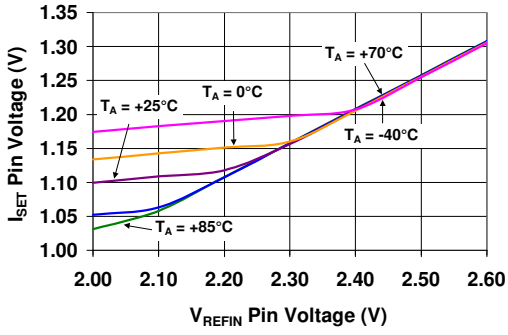
Data taken with the minimum following conditions:

$-50\ \mu A < I_{ISET} < 50\ \mu A$ ($I_{ISET} \neq 0$)
I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V

Note 1:

$V_{UVTH} < V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

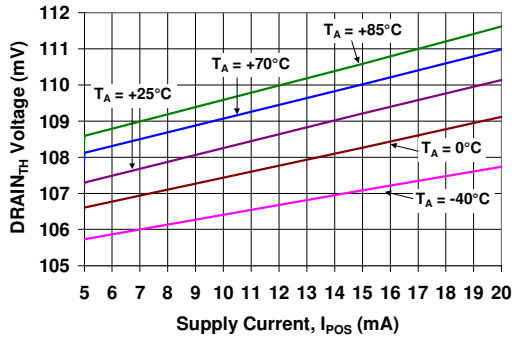
FIGURE 2-16: *UV_D Pin Current vs. I_{SET} Pin Current.*



Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
Iset = 10 µA

FIGURE 2-17: *I_{SET} Pin Voltage vs. V_{REFIN} Pin Voltage.*



Data taken with the minimum following conditions:

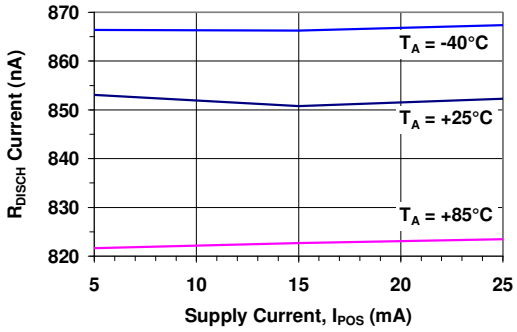
$3\ mA \leq I_{POS} \leq 30\ mA$

V_{REFIN} = 2.5V, I_{SET} = 10 µA
Determined by PWRGOOD signal

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-18: *DRAINTH Threshold Voltage vs. Supply current (I_{POS}).*



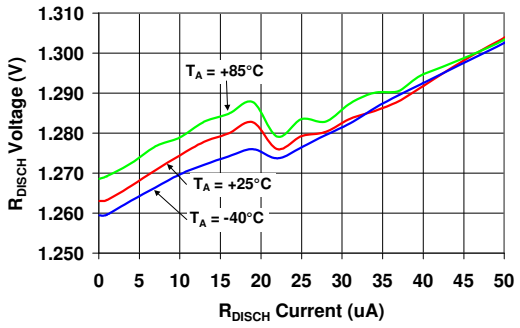
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
R_{DISCH} = 16 MΩ

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-19: *R_{DISCH} Current vs. Supply Current (I_{POS}).*



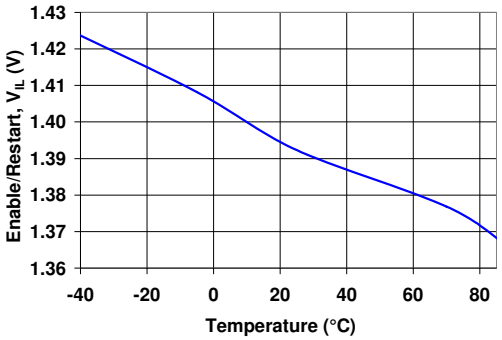
Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
I_{RDISCH} from 100 nA to 10 µA (500 nA steps)

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
V_{ENABLE} = 5V (open)
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-20: *R_{DISCH} Voltage vs. R_{DISCH} Current.*



Data taken with the minimum following conditions:

I_{POS} = 5 mA
(Enables V_{POS} at its self-regulating voltage)
V_{REFIN} = 2.5V, I_{SET} = 10 µA
Determined by GATE voltage

Note 1:

$V_{UVTH} > V_{VREFIN}$
$V_{OVTH} < V_{VREFIN}$
$V_{SENSE} = V_{VNEG}$
$V_{VFB} = V_{VNEG}$
$V_{DRAINTH} = V_{VNEG}$
$V_{OVO} = V_{VNEG}$
$V_{CL} = V_{VREFIN}$
$V_{RESTART} = V_{VNEG}$ (open)

FIGURE 2-21: *ENABLE/$\overline{\text{RESTART}}$ Pin Trip Point Voltage vs. Temperature.*