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MCP19114/5

Digitally Enhanced Power Analog Synchronous Low-Side PWM Controller

Features

- Input Voltage: 4.5V to 42V
- Can be Configured with Multiple Topologies Including but not Limited to:
  - Flyback
  - Ćuk
  - Boost
  - SEPIC (Single-Ended Primary-Inductor Converter)
- Capable of Quasi-Resonant or Fixed-Frequency Operation
- Low Quiescent Current: 5 mA Typical
- Low Sleep Current: 30 µA Typical
- Low-Side Gate Drivers:
  - +5V gate drive
  - 0.5A sink/source current
  - +10V gate drive
  - 1A sink/source current
- Peak Current Mode Control
- Differential Remote Output Sense
- Multiple Output Systems:
  - Master or Slave
- AEC-Q100 Qualified
- Configurable Parameters:
  - V_{REF}, Precision I_{OUT}/V_{OUT} Set Point (DAC)
  - Input Undervoltage Lockout (UVLO)
  - Input Overvoltage Lockout (OVLO)
  - Detection and protection
  - Primary current leading edge blanking (0, 50 ns, 100 ns and 200 ns)
  - Gate drive dead time (16 ns to 256 ns)
  - Fixed switching frequency range: 31.25 kHz to 2.0 MHz
  - Slope compensation
  - Quasi-resonant configuration with built-in comparator and programmable offset voltage adjustment
  - Primary current offset adjustment
  - Configurable GPIO pin options
- Integrated Low-Side Differential Current Sense Amplifier
- ±5% Current Regulation
- Thermal Shutdown

Microcontroller Features

- Precision 8 MHz Internal Oscillator Block:
  - Factory-calibrated to ±1%, typical
- Interrupt-Capable
  - Firmware
  - Interrupt-on-change pins
- Only 35 Instructions to Learn
- 4096 Words On-Chip Program Memory
- High-Endurance Flash:
  - 100,000 write Flash endurance
  - Flash retention: >40 years
- Watchdog Timer (WDT) with Independent Oscillator for Reliable Operation
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- Eight I/O Pins and One Input-Only Pin
  - Two open-drain pins
- Analog-to-Digital Converter (ADC):
  - 10-bit resolution
  - Five external channels
- Timer0: 8-bit Timer/Counter with 8-bit Prescaler
- Enhanced Timer1:
  - 16-bit timer with prescaler
  - Two selectable clock sources
- Timer2: 8-Bit Timer with Prescaler
  - 8-bit period register
- I^2C™ Communication:
  - 7-bit address masking
  - Two dedicated address registers

Pin Diagram – 24-Pin QFN (MCP19114)

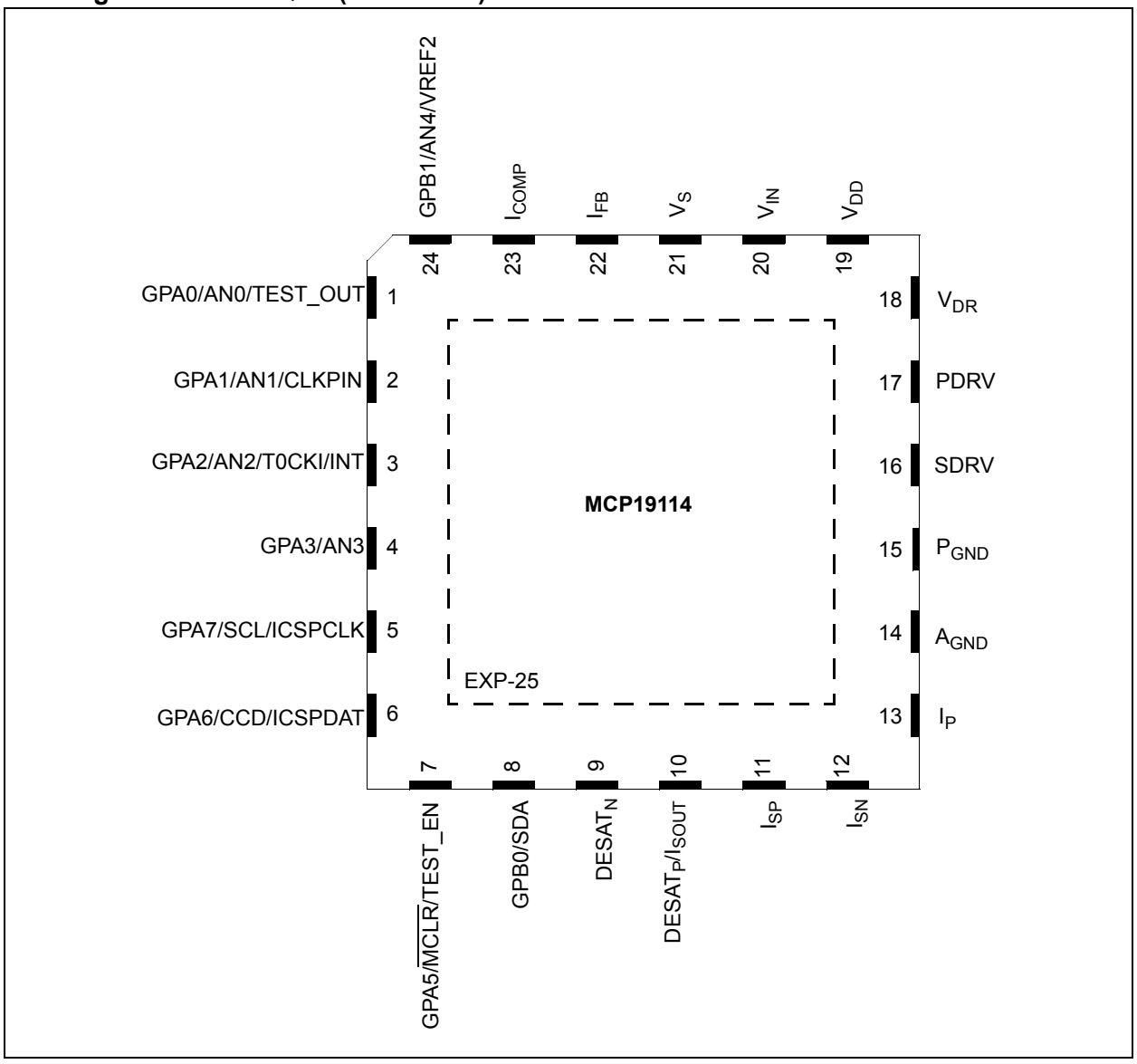

TABLE 1: 24-PIN SUMMARY

I/O	24-Pin QFN	ANSEL	A/D	Timers	MSSP	Interrupt	Pull-Up	Basic	Additional
GPA0	1	Y	AN0	—	—	IOC	Y	—	Analog/Digital Debug Output(1)
GPA1	2	Y	AN1	—	—	IOC	Y	—	Sync Signal In/Out(2)
GPA2	3	Y	AN2	T0CKI	—	IOC INT	Y	—	—
GPA3	4	Y	AN3	—	—	IOC	Y	—	—
GPA5	7	N	—	—	—	IOC(4)	Y(5)	$\overline{MCLR}$	Test Enable Input
GPA6	6	N	—	—	—	IOC	Y	ICSPDAT	Dual Capture/Compare Input
GPA7	5	N	—	—	SCL	IOC	N	ICSPCLK	—
GPB0	8	N	—	—	SDA	IOC	N	—	—
GPB1	24	Y	AN4	—	—	IOC	Y	—	V_{REF2}(3)
$DESAT_N$	9	N	—	—	—	—	—	—	DESAT Negative Input
$DESAT_P$/ I_{SOUT}	10	N	—	—	—	—	—	—	$DESAT_P$ Input or I_{SOUT} Output(6)
I_{SP}	11	N	—	—	—	—	Y	—	Current Sense Amplifier Positive Input
I_{SN}	12	N	—	—	—	—	—	—	Current Sense Amplifier Negative Input
I_P	13	N	—	—	—	—	—	—	Primary Input Current Sense
A_{GND}	14	N	—	—	—	—	—	A_{GND}	Small Signal Ground
P_{GND}	15	N	—	—	—	—	—	P_{GND}	Large Signal Ground
SDRV	16	N	—	—	—	—	—	—	Secondary LS Gate Drive Output
PDRV	17	N	—	—	—	—	—	—	Primary LS Gate Drive Output
V_{DR}	18	N	—	—	—	—	—	V_{DR}	Gate Drive Supply Voltage
V_{DD}	19	N	—	—	—	—	—	V_{DD}	V_{DD} Output
V_{IN}	20	N	—	—	—	—	—	V_{IN}	Input Supply Voltage
V_S	21	N	—	—	—	—	—	—	Output Voltage Sense
I_{FB}	22	N	—	—	—	—	—	—	Error Amplifier Feedback Input
I_{COMP}	23	N	—	—	—	—	—	—	Error Amplifier Output

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON register.

2: Selected when functioning as master or slave by proper configuration of the MSC<1:0> bits in the MODECON register.

3: V_{REF2} output selected when configured as master by proper configuration of the MSC<1:0> bits in the MODECON register.

4: The IOC is disabled when $\overline{MCLR}$ is enabled.

5: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

6: When RFB of MODECON<5> = 0, the internal feedback resistor and $DESAT_P$ input are enabled. When RFB = 1, I_{SOUT} is enabled.

Pin Diagram – 28-Pin QFN (MCP19115)

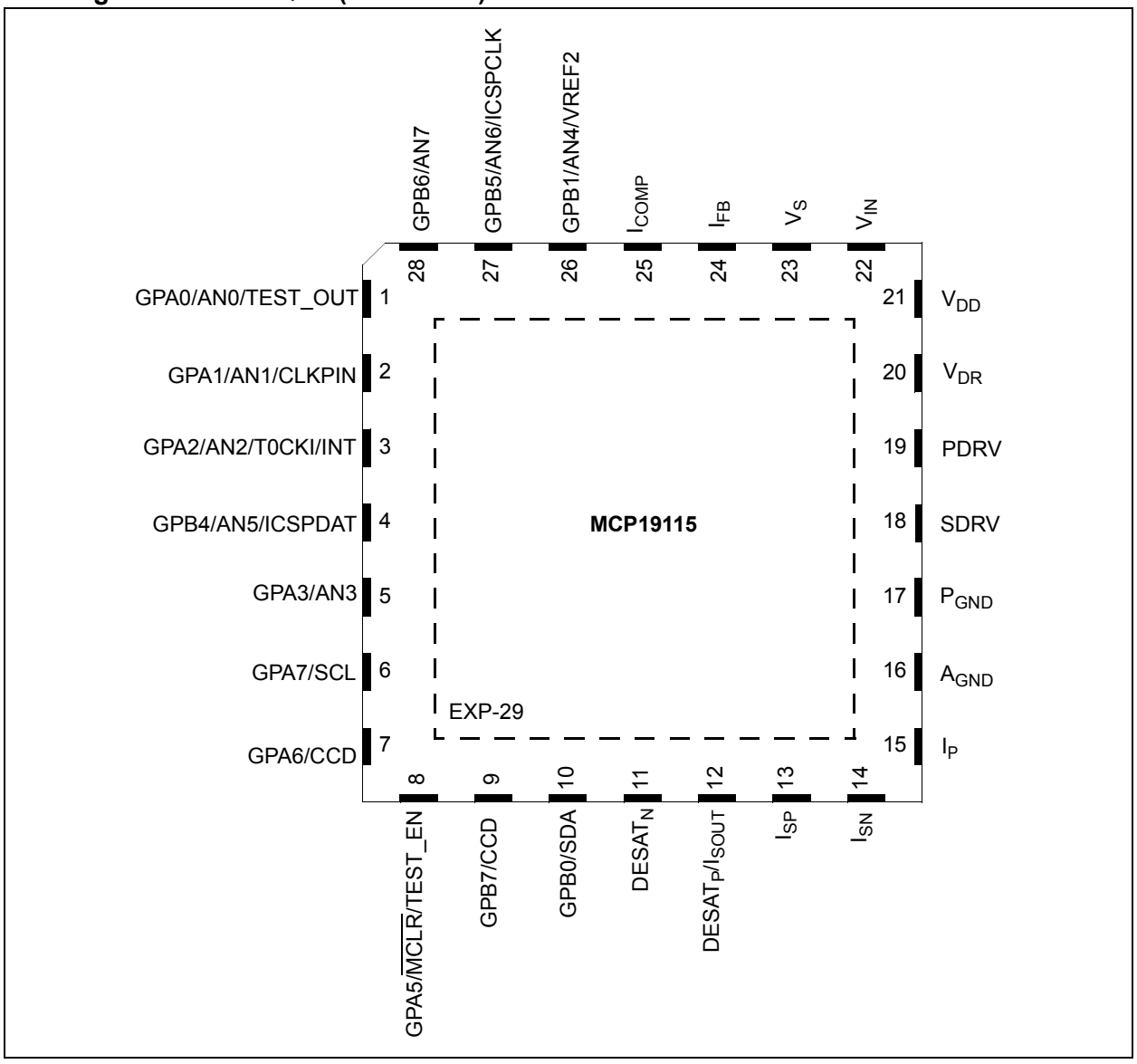

TABLE 2: 28-PIN SUMMARY

I/O	28-Pin QFN	ANSEL	A/D	Timers	MSSP	Interrupt	Pull-Up	Basic	Additional
GPA0	1	Y	AN0	—	—	IOC	Y	—	Analog/Digital Debug Output(1)
GPA1	2	Y	AN1	—	—	IOC	Y	—	Sync Signal In/Out(2)
GPA2	3	Y	AN2	T0CKI	—	IOC INT	Y	—	—
GPA3	5	Y	AN3	—	—	IOC	Y	—	—
GPA5	8	N	—	—	—	IOC(4)	Y(5)	$\overline{MCLR}$	Test Enable Input
GPA6	7	N	—	—	—	IOC	Y	—	Dual Capture/Single Compare1 Input
GPA7	6	N	—	—	SCL	IOC	N	—	—
GPB0	10	N	—	—	SDA	IOC	N	—	—
GPB1	26	Y	AN4	—	—	IOC	Y	—	V_{REF2}(3)
GPB4	4	Y	AN5	—	—	IOC	Y	ICSPDAT	—
GPB5	27	Y	AN6	—	—	IOC	Y	ICSPCLK	—
GPB6	28	Y	AN7	—	—	IOC	Y	—	—
GPB7	9	Y	—	—	—	IOC	Y	—	Single Compare2 Input
$DESAT_P$/ I_{SOUT}	12	N	—	—	—	—	—	—	$DESAT_P$ input or I_{SOUT} Output(6)
$DESAT_N$	11	N	—	—	—	—	—	—	DESAT Negative Input
I_{SP}	13	N	—	—	—	—	Y	—	Current Sense Amplifier Noninverting Input
I_{SN}	14	N	—	—	—	—	—	—	Current Sense Amplifier Inverting Input
I_P	15	N	—	—	—	—	—	—	Primary Input Current Sense
A_{GND}	16	N	—	—	—	—	—	A_{GND}	Small Signal Ground
P_{GND}	17	N	—	—	—	—	—	P_{GND}	Large Signal Ground
SDRV	18	N	—	—	—	—	—	—	Secondary LS Gate Drive Output
PDRV	19	N	—	—	—	—	—	—	Primary LS Gate Drive Output
V_{DR}	20	N	—	—	—	—	—	V_{DR}	Gate Drive Supply Voltage
V_{DD}	21	N	—	—	—	—	—	V_{DD}	V_{DD} Output
V_{IN}	22	N	—	—	—	—	—	V_{IN}	Input Supply Voltage
V_S	23	N	—	—	—	—	—	—	Output Voltage Sense
I_{FB}	24	N	—	—	—	—	—	—	Error Amplifier Feedback input
I_{COMP}	25	N	—	—	—	—	—	—	Error Amplifier Output

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON register.

2: Selected when functioning as master or slave by proper configuration of the MSC<1:0> bits in the MODECON register.

3: VREF2 output selected when configured as master by proper configuration of the MSC<1:0> bits in the MODECON register.

4: The IOC is disabled when $\overline{MCLR}$ is enabled.

5: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

6: When RFB of MODECON<6> = 0, the internal feedback resistor is enabled allow with $DESAT_P$ input. When RFB = 1, I_{SOUT} is enabled.

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NOTES:

1.0 DEVICE OVERVIEW

The MCP19114/5 are highly integrated, mixed-signal low-side synchronous controllers that operate from 4.5V to 42V. The family features an analog PWM controller with an integrated microcontroller core used for LED lighting systems, battery chargers and other low-side switch PWM applications. The devices feature an analog internal PWM controller similar to the MCP1631, and a standard PIC® microcontroller similar to the PIC12F617.

Complete customization of device operating parameters, start-up or shutdown profiles, protection levels and fault handling procedures are accomplished by setting digital registers using Microchip's MPLAB® X Integrated Development Environment software and one of Microchip's many in-circuit debugger and device programmers.

The MCP19114/5 mixed-signal low-side synchronous controllers feature integrated programmable input UVLO/OVLO, programmable output overvoltage (OV), two low-side gate drive outputs with independent programmable dead time, programmable leading edge blanking (four steps), programmable 6-bit slope compensation and an integrated internal programmable oscillator for fixed-frequency applications. An integrated 8-bit reference voltage (V_{REF}) is used for setting output voltage or current. An internal comparator supports quasi-resonant applications. Additional Capture and Compare modules are integrated for additional control, including enhanced dimming capability. The MCP19114/5 devices contain two internal LDOs. A 5V LDO is used to power the internal processor and provide 5V externally. This 5V external output can be used to supply the gate drive. An analog filter between the V_{DD} output and the V_{DR} input is recommended when implementing a 5V gate drive supplied from V_{DD}. Two 4.7 µF capacitors are recommended with one placed as close as possible to V_{DD} and one as close as possible to V_{DR}, separated by a 10Ω isolation resistor. DO NOT exceed 10 µF on the V_{DD}. An external supply is required to implement higher gate drive voltages. By utilizing Microchip's TC1240A voltage doubler supplied from V_{DD} to provide V_{DR}, a 10V gate drive can be achieved. A 4V LDO is used to power the internal analog circuitry. The two low-side drivers can be used to operate the power converter in bidirectional mode, enabling the "shaping" of LED dimming current in LED applications or developing bidirectional power converters for battery-powered applications.

The MCP19114 is packaged in a 24-lead 4 mm x 4 mm QFN and offers an alternate-bonded 28-lead 5 mm x 5 mm QFN. The MCP19115 is packaged in a 28-lead 5 mm x 5 mm QFN.

The ability for system designers to configure application-specific features allows the MCP19114/5 to be offered in smaller packages than currently available in integrated devices today. The General Purpose Input/Output (GPIO) of the MCP19114/5 can be configured to offer a status output; a device enable, to control an external switch; a switching frequency synchronization output or input or even a device status or "heartbeat" indicator. This flexibility allows the MCP19114/5 packages and complete solutions to be smaller, thereby saving size and cost of the system printed circuit boards.

With integrated features like output current adjustment and dynamic output voltage positioning, the MCP19114/5 family has the best in-class performance and highest integration level currently available.

Power trains supported by this architecture include but are not limited to boost, flyback, quasi-resonant flyback, SEPIC, Ćuk, etc. Two low-side gate drivers are capable of sinking and sourcing 1A at 10V V_{DR}. With a 5V gate drive, the driver is capable of 0.5A sink and source. The user has the option to allow the V_{IN} UVLO to shut down the drivers by setting the UVLOEN bit. When this bit is not set, the device drivers will ride through the UVLO condition and continue to operate until V_{DR} reaches the gate drive UVLO value. This value is selectable at 2.7V or 5.4V and is always enabled. An internal reset for the microcontroller core is set to 2.0V. An internal comparator module is used to sense the desaturation of the flyback transformer to synchronize switching for quasi-resonant applications. The operating input voltage for normal device operation ranges from 4.5V to 42V with an absolute maximum of 44V. The maximum transient voltage is 48V for 500 ms. An I^2C serial bus is used for device communications from the PWM controller to the system.

FIGURE 1-1: MCP19114/5 FLYBACK SYNCHRONOUS QUASI-RESONANT BLOCK DIAGRAM

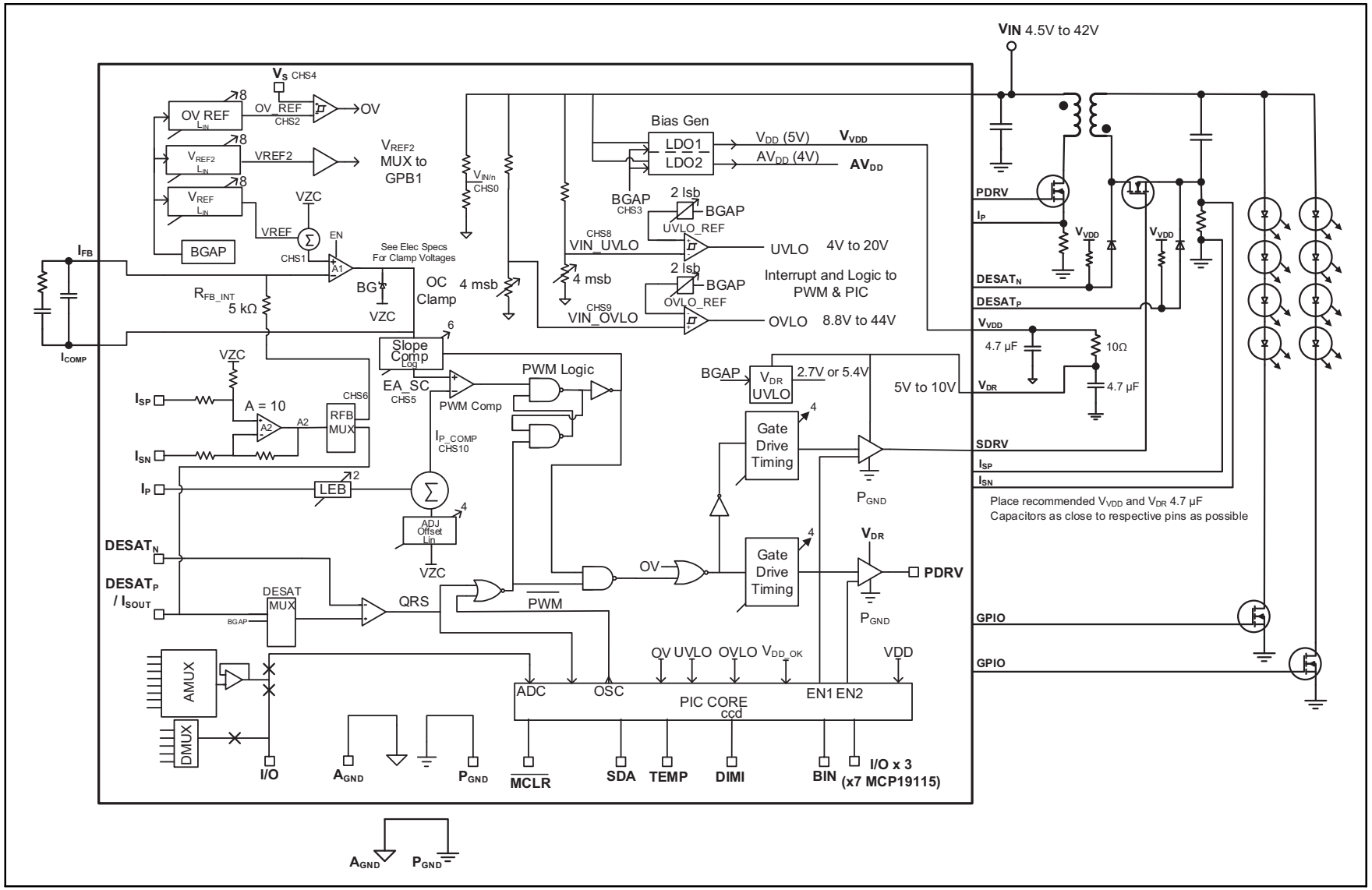


FIGURE 1-2: MCP19114 ĆUK SYNCHRONOUS POSITIVE OUTPUT APPLICATION DIAGRAM

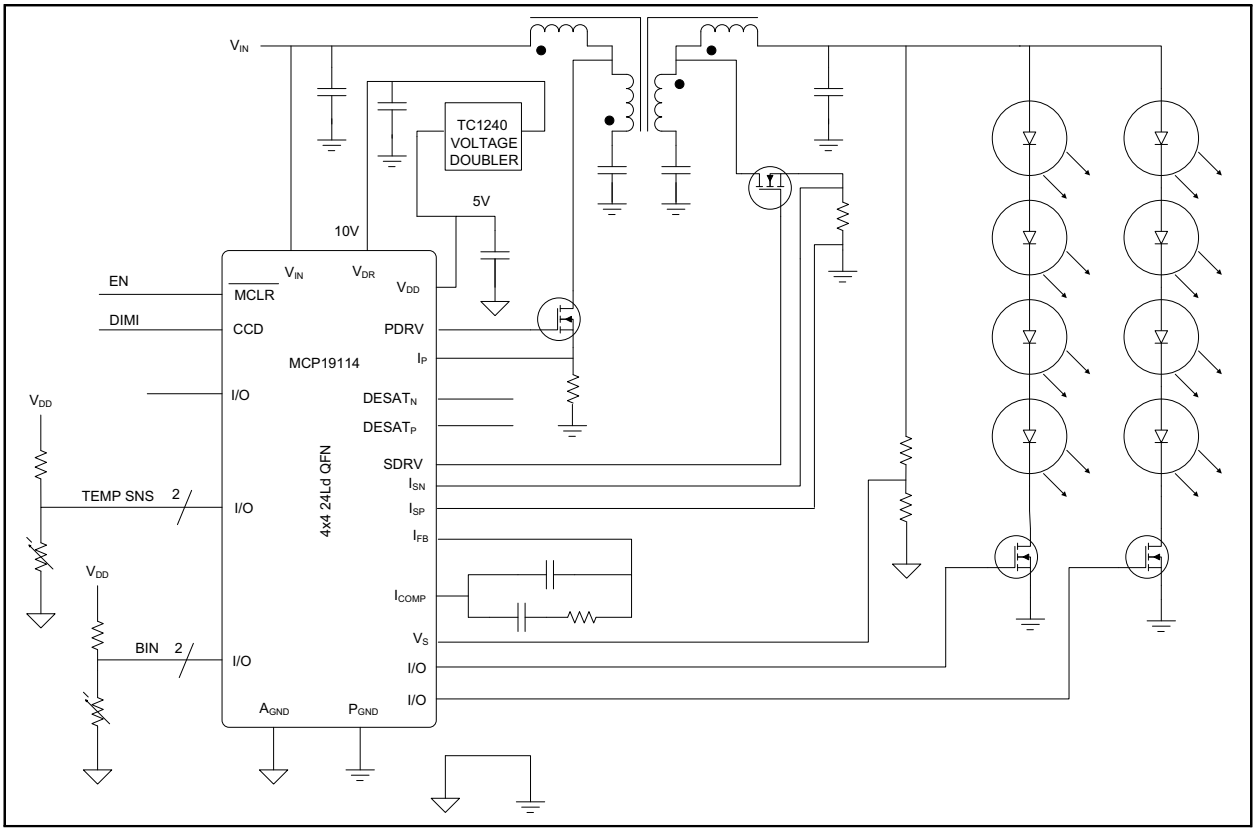


FIGURE 1-3: MCP19114 BOOST QUASI-RESONANT APPLICATION DIAGRAM

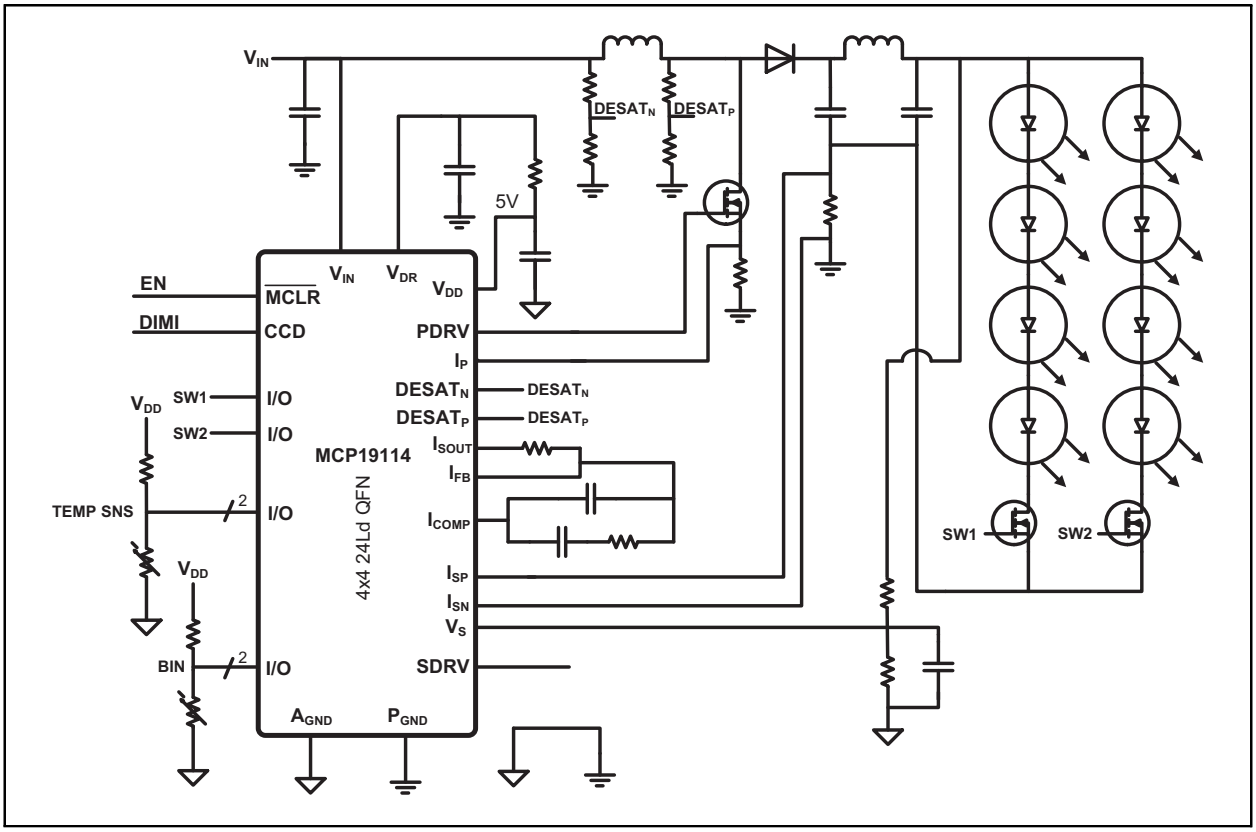
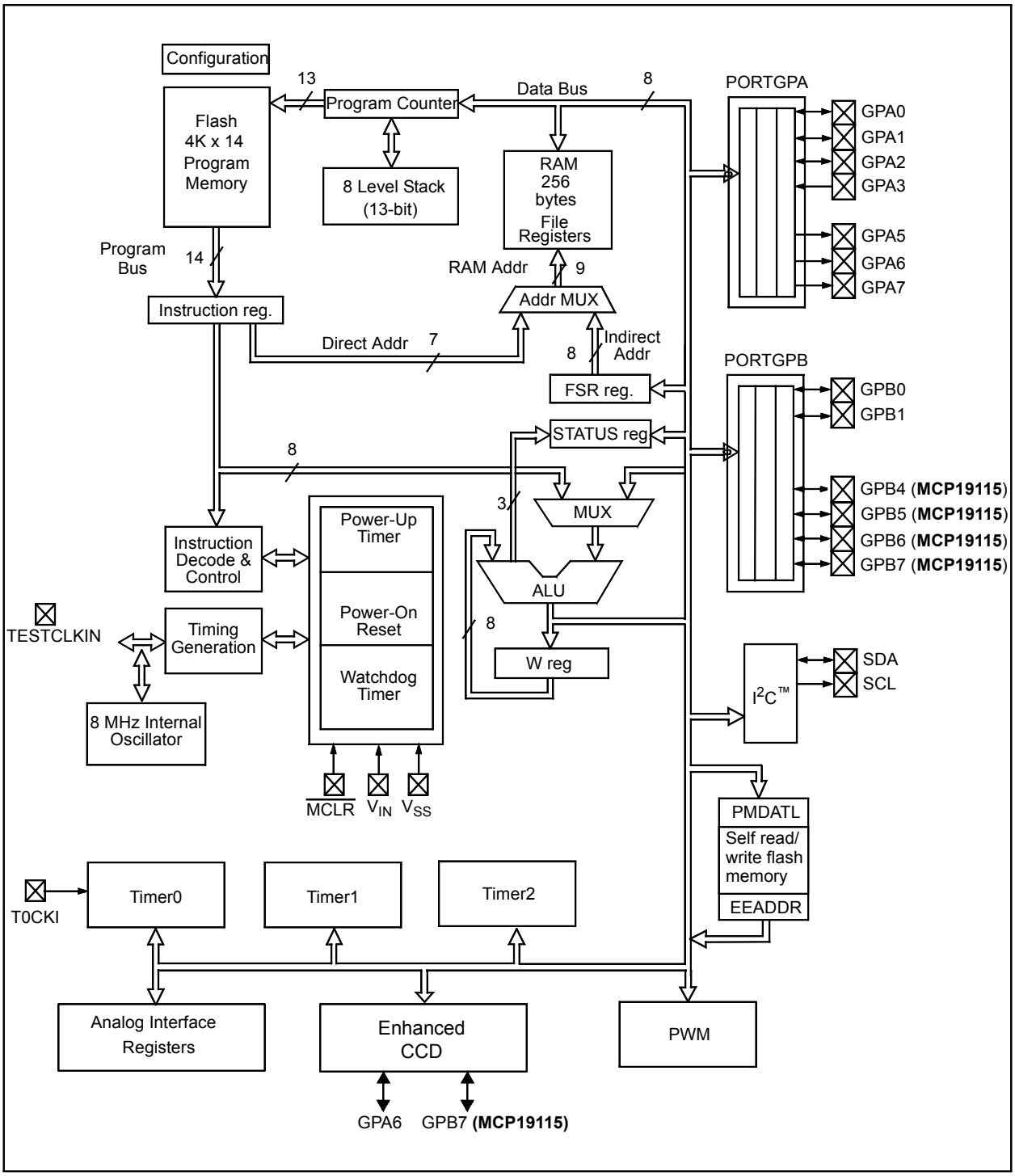


FIGURE 1-4: MICROCONTROLLER CORE BLOCK DIAGRAM



2.0 PIN DESCRIPTION

The 24-lead MCP19114 and 28-lead MCP19115 devices feature pins that have multiple functions associated with each pin. Table 2-1 provides a description of the different functions. Refer to **Section 2.1 "Detailed Pin Functional Description"** for more detailed information.

TABLE 2-1: MCP19114/5 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GPA0/AN0/TEST_OUT	GPA0	TTL	CMOS	General-purpose I/O
	AN0	AN	—	A/D Channel 0 input
	TEST_OUT	—	—	Internal analog/digital signal multiplexer output(1)
GPA1/AN1/CLKPIN	GPA1	TTL	CMOS	General-purpose I/O
	AN1	AN	—	A/D Channel 1 input
	CLKPIN	ST	CMOS	Switching frequency clock input or output(2)
GPA2/AN2/T0CKI/INT	GPA2	ST	CMOS	General-purpose I/O
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External interrupt
GPA3/AN3	GPA3	TTL	CMOS	General-purpose I/O
	AN3	AN	—	A/D Channel 3 input
GPA5/$\overline{\text{MCLR}}$	GPA5	TTL	—	General-purpose input only
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
GPA6/CCD/ICSPDAT	GPA6	ST	CMOS	General-purpose I/O
	ICSPDAT	ST	CMOS	Serial Programming Data I/O
	CCD	ST	CMOS	Single Compare output. Dual Capture input
GPA7/SCL/ICSPCLK	GPA7	ST	OD	General-purpose open drain I/O
	SCL	I^2C™	OD	I^2C clock
	ICSPCLK	ST	—	Serial Programming Clock
GPB0/SDA	GPB0	TTL	OD	General-purpose I/O
	SDA	I^2C™	OD	I^2C data input/output
GPB1/AN4/VREF2	GPB1	TTL	CMOS	General-purpose I/O
	AN4	AN	—	A/D Channel 4 input
	VREF2	—	AN	VREF2 DAC Output(3)
GPB4/AN5/ICSPDAT (**MCP19115** Only)	GPB4	TTL	CMOS	General-purpose I/O
	AN5	AN	—	A/D Channel 5 input
	ICSPDAT	ST	CMOS	Primary Serial Programming Data I/O
GPB5/AN6/ICSPCLK (**MCP19115** Only)	GPB5	TTL	CMOS	General-purpose I/O
	AN6	AN	—	A/D Channel 6 input
	ISCPCLK	ST	—	Primary Serial Programming Clock

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON register.

2: Selected when functioning as master or slave by proper configuration of the MSC<1:0> bits in the MODECON register.

3: VREF2 output selected when configured as master by proper configuration of the MSC<1:0> bits in the MODECON register.

TABLE 2-1: MCP19114/5 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
GPB6/AN7 (**MCP19115** Only)	GPB6	TTL	CMOS	General-purpose I/O
	AN7	AN	—	A/D Channel 7 input
GPB7/CCD (**MCP19115** Only)	GPB7	TTL	CMOS	General-purpose I/O
	CCD	ST	CMOS	Single Compare output. Dual Capture input.
V_{IN}	V_{IN}	—	—	Device input supply voltage
V_{DD}	V_{DD}	—	—	Internal +5V LDO output pin
V_{DR}	V_{DR}	—	—	Gate drive supply voltage
A_{GND}	A_{GND}	—	—	Small signal quiet ground
P_{GND}	P_{GND}	—	—	Large signal power ground
PDRV	PDRV	—	—	Primary Low-Side MOSFET gate drive
SDRV	SDRV	—	—	Secondary Low-Side MOSFET gate drive
I_P	I_P	—	—	Primary input current sense
I_{SN}	I_{SN}	—	—	Secondary current sense amplifier negative input
I_{SP}	I_{SP}	—	—	Secondary current sense amplifier positive input
V_S	V_S	—	—	Sense voltage compared to overvoltage DAC
I_{FB}	I_{FB}	—	—	Error amplifier feedback input
I_{COMP}	I_{COMP}	—	—	Error amplifier output
$DESAT_P/I_{SOUT}$	$DESAT_P/I_{SOUT}$	—	—	$DESAT_P$: DESAT detect comparator positive input I_{SOUT}: Secondary current sense amplifier output
$DESAT_N$	$DESAT_N$	—	—	$DESAT_N$: DESAT detect comparator negative input

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON register.

2: Selected when functioning as master or slave by proper configuration of the MSC<1:0> bits in the MODECON register.

3: VREF2 output selected when configured as master by proper configuration of the MSC<1:0> bits in the MODECON register.

2.1 Detailed Pin Functional Description

2.1.1 GPA0 PIN

GPA0 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN0 is an input to the A/D. To configure this pin to be read by the A/D on channel 0, bits TRISA0 and ANSA0 must be set.

The ABECON register can be configured to set this pin to the TEST_OUT function. It is a buffered output of the internal analog or digital signal multiplexers. Analog signals present on this pin are controlled by the ADCON0 register. Digital signals present on this pin are controlled by the ABECON register.

2.1.2 GPA1 PIN

GPA1 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN1 is an input to the A/D. To configure this pin to be read by the A/D on channel 1, bits TRISA1 and ANSA1 must be set.

When the MCP19114/5 are configured as a master or slave, this pin is configured to be the switching frequency synchronization input or output (CLKPIN).

2.1.3 GPA2 PIN

GPA2 is a general-purpose ST input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN2 is an input to the A/D. To configure this pin to be read by the A/D on channel 2, bits TRISA2 and ANSA2 must be set.

When bit T0CS is set in the OPTION_REG register, the T0CKI function is enabled. Refer to **Section 22.0 "Timer0 Module"** for more information.

GPA2 can also be configured as an external interrupt by setting the INTE bit. Refer to **Section 14.2 "GPA2/INT Interrupt"** for more information.

2.1.4 GPA3 PIN

GPA3 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN3 is an input to the A/D. To configure this pin to be read by the A/D on channel 3, bits TRISA3 and ANSA3 must be set.

2.1.5 GPA5 PIN

GPA5 is a general-purpose TTL input only pin. An internal weak pull-up and interrupt-on-change are also available.

For programming purposes, this pin is to be connected to the $\overline{\text{MCLR}}$ pin of the serial programmer. Refer to **Section 30.0 "In-Circuit Serial Programming™ (ICSP™)"** for more information.

This pin is $\overline{\text{MCLR}}$ when the MCLRE bit is set in the CONFIG register.

2.1.6 GPA6 PIN

GPA6 is a general-purpose CMOS output ST input pin whose data direction is controlled in TRISGPA.

ICSPDAT is a serial programming data I/O function. This can be used in conjunction with ICSPCLK to serial program the device.

GPA6 is part of the CCD Module. For more information, refer to **Section 26.0 "Dual Capture/Compare (CCD) Module"**.

2.1.7 GPA7 PIN

GPA7 is a true open drain general-purpose pin whose data direction is controlled in TRISGPA. There is no internal connection between this pin and device V_{DD}. This pin does not have a weak pull-up, but interrupt-on-change is available.

This pin is the primary ICSPCLK input. This can be used in conjunction with ICSPDAT to serial program the device.

When the MCP19114/5 is configured for I^2C communication, **Section 28.2 "I2C Mode Overview"**, GPA7 functions as the I^2C clock (SCL). This pin must be configured as an input to allow proper operation.

2.1.8 GPB0 PIN

GPB0 is a true open-drain general-purpose pin whose data direction is controlled in TRISGPB. There is no internal connection between this pin and device V_{DD}. This pin does not have a weak pull-up, but interrupt-on-change is available. When the MCP19114/5 are configured for I^2C communication, **Section 28.2 "I2C Mode Overview"**, GPB0 functions as the I^2C clock (SDA). This pin must be configured as an input to allow proper operation.

2.1.9 GPB1 PIN

GPB1 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN4 is an input to the A/D. To configure this pin to be read by the A/D on channel 4, bits TRISB1 and ANSB1 must be set.

When the MCP19114/5 are configured as a master, this pin is configured to be the V_{REF2} DAC output.

2.1.10 GPB4 PIN **(MCP19115 ONLY)**

GPB4 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN5 is an input to the A/D. To configure this pin to be read by the A/D on channel 5, bits TRISB4 and ANSB4 must be set.

ICSPDAT is the primary serial programming data I/O function. This is used in conjunction with ICSPCLK to serial program the device.

2.1.11 GPB5 PIN **(MCP19115 ONLY)**

GPB5 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN6 is an input to the A/D. To configure this pin to be read by the A/D on channel 6, bits TRISB5 and ANSB5 must be set.

ICSPCLK is the primary serial programming clock function. This is used in conjunction with ICSPDAT to serial program the device.

2.1.12 GPB6 PIN **(MCP19115 ONLY)**

GPB6 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN7 is an input to the A/D. To configure this pin to be read by the A/D on channel 7, bits TRISB6 and ANSB6 must be set.

2.1.13 GPB7 PIN **(MCP19115 ONLY)**

GPB7 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

GPB7 is part of the CCD Module. For more information, refer to **Section 26.0 "Dual Capture/Compare (CCD) Module"**.

2.1.14 $DESAT_N$ PIN

Internal comparator inverting input. Used during quasi-resonant operation for desaturation detection.

2.1.15 $DESAT_P/I_{SOUT}$ PIN

When using the internal comparator for desaturation detection during quasi-resonant operation, this pin connects to the comparator's noninverting input. The output of the remote sense current sense amplifier gets configured to utilize the 5 kΩ internal feedback resistor. When not utilizing the internal comparator and not configured to use the 5 kΩ internal feedback resistor, the current sense amplifier gets connected to this pin and is I_{SOUT}.

2.1.16 I_{SP} PIN

The noninverting input to internal current sense amplifier, typically used to differentially remote sense secondary current. This pin can be internally pulled-up to V_{DD} by setting the <ISPUEN> bit in the PE1 register.

2.1.17 I_{SN} PIN

The inverting input to internal current sense amplifier, typically used to differentially remote sense secondary current.

2.1.18 I_P PIN

Primary input current sense for current mode control and peak current limit. For voltage mode control, this pin can be connected to an artificial ramp.

2.1.19 A_{GND} PIN

A_{GND} is the small signal ground connection pin. This pin should be connected to the exposed pad on the bottom of the package.

2.1.20 P_{GND} PIN

Connect all large signal level ground returns to P_{GND}. These large-signal level ground traces should have a small loop area and minimal length to prevent coupling of switching noise to sensitive traces.

2.1.21 SDRV PIN

The gate of the low-side secondary MOSFET is connected to SDRV. The PCB trace connecting SDRV to the gate must be of minimal length and appropriate width to handle the high-peak drive current and fast voltage transitions.

2.1.22 PDRV PIN

The gate of the low-side primary MOSFET is connected to PDRV. The PCB tracing connecting PDRV to the gate must be of minimal length and appropriate width to handle the high-peak drive currents and fast voltage transitions.

2.1.23 V_{DR} PIN

The supply for the low-side drivers is connected to this pin and has an absolute maximum rating of +13.5V. This pin can be connected by an RC filter to the V_{DD} pin.

2.1.24 V_{DD} PIN

The output of the internal +5.0V regulator is connected to this pin. It is recommended that a 1.0 µF minimum/ 10 µF maximum bypass capacitor be connected between this pin and the GND pin of the device. The bypass capacitor should be physically placed close to the device.

2.1.25 V_{IN} PIN

Input power connection pin of the device. It is recommended that capacitance be placed between this pin and the GND pin of the device.

2.1.26 V_S PIN

Analog input connected to the noninverting input of the overvoltage comparator. Typically used as output voltage overvoltage protection. The inverting input of the overvoltage comparator is controlled by the OV REF DAC.

2.1.27 I_{FB} PIN

Error amplifier inverting feedback connection.

2.1.28 I_{COMP} PIN

Error amplifier output signal.

2.1.29 EXPOSED PAD (EP)

It is recommended to connect the exposed pad to A_{GND}.

Note: Upon initial power-up, the device may apply a weak pull-up effect on GPIO pads that can be configured as analog inputs. Once the external capacitance on the 5V (V_{DD}) is charged and the external 5V regulator exceeds the internal 4V regulator (AV_{DD}) the pull-up effect is shut off. To prevent this parasitic power-up effect, a pull-down resistor of 10 kΩ maximum is recommended for GPIO with analog input capability. This applies to GPA0, GPA1, GPA2, GPA3, GPB1, GPB4 (MCP19115 only), GPBD (MCP19115 only), GPB6 (MCP19115 only).

NOTES:

3.0 FUNCTIONAL DESCRIPTION

3.1 Linear Regulators

The operating input voltage for the MCP19114/5 ranges from 4.5V to 42V. There are two internal Low Dropout (LDO) voltage regulators. A 5V LDO is used to power the internal processor and provide a 5V output for external usage. A second LDO (AV_{DD}) is a 4V regulator and is used to power the remaining analog internal circuitry. Using an LDO to power the MCP19114/5, the input voltage is monitored using a resistor divider. The MCP19114/5 also incorporate brown-out protection. Refer to **Section 13.3 "Brown-Out Reset (BOR)"** for details. The PIC core will reset at 2.0V V_{DD}.

3.2 Output Drive Circuitry

The MCP19114/5 integrate two low-side drivers used to drive the external low-side N-Channel power MOSFETs for synchronous applications, such as synchronous flyback and synchronous Ćuk converters. Both converter types can be configured for nonsynchronous control by replacing the synchronous FET with a diode. The flyback is also capable of quasi-resonant operation. The MCP19114/5 can also be configured as a Boost or SEPIC switch-mode power supply (SMPS). In Boost mode, nonsynchronous fixed-frequency or nonsynchronous quasi-resonant control can be utilized. This device can also be used as a SEPIC SMPS in fixed-frequency nonsynchronous mode. The low-side drive is capable of switching the MOSFET at high frequency in typical SMPS applications. The gate drive (V_{DR}) can be supplied from 5V to 10V. The drive strength is capable of up to 1A sink/source with 10V gate drive and down to 0.5A sink/source with 5V gate drive. A programmable delay is used to set the gate turn-on dead time. This prevents overlap and shoot-through currents that can decrease the converter efficiency. Each driver shall have its own EN input controlled by the microcontroller core.

3.3 Current Sense

The output current is differentially sensed by the MCP19114/5. In low-current applications, this helps maintain high system efficiency by minimizing power dissipation in current sense resistors. Differential current sensing also minimizes external ground shift errors. The internal differential amplifier has a typical gain of 10 V/V.

3.4 Peak Current Mode

The MCP19114/5 is a peak current mode controlled device with the current sensing element in series with the primary side MOSFET. Programmable leading edge blanking can be implemented to blank current spikes resulting from turn on. The blank time is controlled from the ICLEBCON register.

Primary input current offset adjust is also available via user programmability, thus limiting peak primary input current. This offset adjustment is controlled by the ICOACON register.

3.5 Magnetic Desaturation Detection

An internal comparator module is used to detect power train magnetic desaturation for quasi-resonant applications. The comparator output is used as a signal to synchronize the start of the next switching cycle. This operation differs from the traditional fixed-frequency application. The DESAT comparator output can be enabled and routed into the PWM circuitry or disabled for fixed-frequency applications. During Quasi-Resonant (QR) operation, the DESAT comparator output is enabled and combined with a pair of one-shot timers and a flip-flop to sustain PWM operation. Timer2 (TMR2) must be initialized and set to run at a frequency lower than the minimum QR operating frequency. When the CDSWDE bit is set in the DESATCON register, TMR2 serves as a watchdog.

An example of the order of events for a Flyback SMPS in synchronous QR operation is as follows:

The primary gate drive (PDRV) goes high. The output of the DESAT comparator is high. The primary current increases until I_P reaches the level of the Error Amp and causes PWM comparator output to go low. The PDRV goes low and the secondary gate drive (SDRV) goes high (after programmed dead time). This triggers the first one-shot to send a 200 ns pulse that resets the flip-flop and TMR2 (WDM_RESET). The 200 ns one-shot pulse design is implemented to mask out any spurious transitions at the DESAT comparator output caused by switching noise. The SDRV stays high until the secondary winding completely runs out of energy, at which time the output capacitance begins to source current back through the winding and secondary MOSFET. The DESAT comparator detects this and its output goes low. This sets the flip-flop and triggers the second one-shot to send a 33 ns pulse to the control logic, causing the SDRV to go low and the PDRV to go high (after programmed dead time). The cycle then repeats. If, for any reason, the reset one-shot does not fire, the WDM_RESET signal stays low and TMR2 is allowed to run until the PWM signal kicks off a new cycle.

The desaturation comparator module is controlled by the DESATCON register.

3.6 Start-Up

To control the output current during start-up, the MCP19114/5 have the capability to monotonically increase system current, at the user's discretion. This is accomplished through the control of the reference voltage DAC (V_{REF}). The entire start-up profile is under user control via software.

3.7 Driver Control Circuitry

The internal driver control circuitry of the MCP19114/5 is comprised of an error amplifier (EA), a high-speed comparator and a latch similar to the MCP1631.

The error amplifier generates the control voltage used by the high-speed PWM comparator. There is an internally generated reference voltage, V_{REF}. The difference or error between this internal reference voltage and the actual feedback voltage is the control voltage. Some applications will implement parked times where the gate drives are not active. For example, when changing between LED strings and after voltage repositioning, the user can disable the gate drives and park the error amplifier output low. During the time when the EA is parked, its output will be clamped low (1 * BG) such that it is in a known state when reactivated. Before the output switches are re-enabled, it may be necessary to re-enable the EA some time prior to enabling the output drivers. This prior-EA enable time will allow the EA to slew towards the intended target and prevent the secondary switch from turning on for an extensive period of time, unintentionally discharging the output capacitance and pulling the output voltage down. External compensation is used to stabilize the control system.

Since the MCP19114/5 are peak current mode controlled, the comparator compares the primary peak current waveform (I_P) that is based upon the current flowing in the primary side with the error amplifier control output voltage. This error amplifier control output voltage also has user-programmable slope compensation subtracted from it. In fixed-frequency applications, the slope compensation signal is generated to be greater than 1/2 the down slope of the inductor current waveform and is controlled by the SLPCRCON register. Offset adjust ability is also available to set the peak current limit of the primary switch for overcurrent protection. The range of the slope compensation ramp is specified. When the current sense signal reaches the level of the control voltage minus slope compensation, the on cycle is terminated and the external switch is latched off until the beginning of the next cycle which begins at the next clock cycle.

To improve current regulation at low levels, a pedestal voltage (VZC) set to the BG (1.23V) is implemented. This virtual ground serves as the reference for the error amplifier (A1), slope compensation, current sense amplifier (A2) and the I_P offset adjustment.

An S-R latch (Set-Rest-Flip-Flop) is used to prevent the PWM circuitry from turning the external switch on until the beginning of the next clock cycle.

3.8 Fixed PWM Frequency

The switching frequency of the MCP19114/5 while not controlled by the DESAT comparator output is generated by using a single edge of the 8 MHz internal clock. The user sets the MCP19114/5 switching frequency by configuring the PR2 register. The maximum allowable PDRV duty cycle is adjustable and is controlled by the PWMRL register. The programmable range of the switching frequency will be 31.25 kHz to 2 MHz. The available switching frequency below 2 MHz is defined as F_{SW} = 8 MHz/N, where N is a whole number between $4 \leq N \leq 256$. Refer to **Section 25.0 "Enhanced PWM Module"** for details.

3.9 V_{REF}

This reference is used to generate the voltage connected to the noninverting input of the error amplifier. The entire analog control loop is raised to a virtual ground pedestal equal to the Band Gap voltage (1.23V).

3.10 OV REF

This reference is used to set the output overvoltage set point. It is compared to the V_S input pin, which is typically proportional to the output voltage based on a resistor divider. OV protection, when enabled, can be set to a value for the protection of system circuitry or it can be used to "ripple" regulate the converter output voltage for repositioning purposes. For details, refer to Register 6-4.

3.11 Independent Gate Drive with Programmable Delay

Two independent low-side gate drives are integrated for synchronous applications. Programmable delay has been implemented to improve efficiency and prevent shoot-through currents. Each gate drive has an independent enable input controlled by the PE1 register and programmable dead time controlled by the DEADCON register.

3.12 Temperature Management

3.12.1 THERMAL SHUTDOWN

To protect the MCP19114/5 from overtemperature conditions, a 150°C junction temperature thermal shutdown has been implemented. When the junction temperature reaches this limit, the device disables the output drivers. In Shutdown mode, both PDRV and SDRV outputs are disabled and the overtemperature flag (OTIF) is set in the PIR2 register. When the junction temperature is reduced by 20°C to 130°C, the MCP19114/5 can resume normal output drive switching.

3.12.2 TEMPERATURE REPORTING

The MCP19114/5 have a second on-chip temperature monitoring circuit that can be read by the ADC through the analog test MUX. Refer to **Section 20.0 "Internal Temperature Indicator Module"** for details on this internal temperature monitoring circuit.

4.0 ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS †

V_{IN} - V_{GND} (operating) ..... -0.3V to +44V
V_{IN} (transient < 500 ms) ..... +48V
PDRV ..... (GND - 0.3V) to (V_{DR} + 0.3V)
SDRV ..... (GND - 0.3V) to (V_{DR} + 0.3V)
V_{DD} Internally Generated ..... +6.5V
V_{DR} Externally Generated ..... +13.5V
Voltage on $\overline{MCLR}$ with respect to GND ..... -0.3V to +13.5V
Maximum voltage: any other pin ..... +(V_{GND} - 0.3V) to (V_{DD} + 0.3V)
Maximum output current sunk by any single I/O pin ..... 25 mA
Maximum output current sourced by any single I/O pin ..... 25 mA
Maximum current sunk by all GPIO ..... 90 mA
Maximum current sourced by all GPIO ..... 35 mA
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C
Operating Junction Temperature ..... -40°C to +125°C
ESD protection on all pins (HBM) ..... 2.0 kV
ESD protection on all pins (MM) 200V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.2 Electrical Characteristics

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 150 kHz, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage	V_{IN}	**4.5**	—	**42**	V	
Input Quiescent Current	I_Q	—	5	**6.5**	mA	V_{IN} = 12V, Not switching
		—	5	**6.75**		V_{IN} = 20V, Not switching
Shutdown Current	I_{SHDN}	—	30	**150**	µA	V_{IN} = 12V **(Note 1)**
Linear Regulator V_{DD}						
Internal Circuitry Bias Voltage	V_{DD}	**4.75**	5.0	**5.5**	V	V_{IN} = 6.0V to 42V
Maximum External V_{DD} Output Current	I_{DD_OUT}	**35**	—	—	mA	V_{IN} = 6.0V to 42V **(Note 4)**
Line Regulation	ΔV_{DD-OUT}/ (V_{DD-OUT} * ΔV_{IN})	**-0.1**	0.002	**0.1**	%/V	(V_{DD} + 1.0V) ≤ V_{IN} ≤ 20V **(Note 4)**
Load Regulation	ΔV_{DD-OUT}/ V_{DD-OUT}	**-0.65**	0.1	**+0.65**	%	I_{DD_OUT} = 1 mA to 20 mA **(Note 4)**
Output Short-Circuit Current	I_{DD_SC}	—	50	—	mA	V_{IN} = (V_{DD} + 1.0V) **(Note 4)**

Note 1: Refer to **Section 15.0 “Power-Down Mode (Sleep)”**.
2: These parameters are characterized, but not production tested.
3: Ensured by design, not production tested.
4: V_{DD} is the voltage present at the V_{DD} pin.
5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.
6: The V_{DD} LDO will limit the total source current to a maximum of 35 mA. Individually each pin can source a maximum of 15 mA.

4.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 150 kHz, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dropout Voltage	V_{IN} - V_{DD}	—	0.3	**0.5**	V	I_{DD_OUT} = 20 mA, (**Notes 4** and **5**)
Power Supply Rejection Ratio	$PSRR_{LDO}$	—	60	—	dB	f ≤ 1000 Hz, I_{DD_OUT} = 25 mA C_{IN} = 0 µF, C_{DD} = 1 µF
Linear Regulator AV_{DD}						
Internal Analog Supply Voltage	AV_{DD}	—	4.0	—	V	
Band Gap Voltage	BG	—	1.23	—	V	Trimmed at 1.0% tolerance
Band Gap Tolerance	BG_{TOL}	**-2.5**	—	**+2.5**	%	
Input UVLO Voltage						
UVLO Range	$UVLO_{ON}$	**4.0**	—	**20**	V	V_{IN} Falling
$UVLO_{ON}$ Trip Tolerance	$UVLO_{TOL}$	**-14**	—	**14**	%	V_{IN} Falling UVLO trip set to 9V VINUVLO = 0x21h
UVLO Hysteresis	$UVLO_{HYS}$	**1**	4	**8**	%	Hysteresis is based upon the $UVLO_{ON}$ setting UVLO trip set to 9V VINUVLO = 0x21h
Resolution	nbits	—	6	—	Bits	Logarithmic Steps
UVLO Comparator						
Input-to-Output Delay	TD	—	5	—	µs	100 ns rise time to 1V overdrive on V_{IN} V_{IN} > UVLO to flag set
Input OVLO Voltage						
OVLO Range	$OVLO_{ON}$	**8.8**	—	**44**	V	V_{IN} Rising
$OVLO_{ON}$ Trip Tolerance	$OVLO_{TOL}$	**-14**	—	**14**	%	V_{IN} Rising OVLO trip set to 18V VINOVLO = 0x1Fh
OVLO Hysteresis	$OVLO_{HYS}$	**1**	5	**8**	%	Hysteresis is based upon the $OVLO_{ON}$ setting OVLO trip set to 18V VINOVLO = 0x1Fh
Resolution	nbits	—	6	—	Bits	Logarithmic Steps
OVLO Comparator						
Input-to-Output Delay	TD	—	5	—	µs	100 ns rise time to 1V overdrive on V_{IN} V_{IN} > OVLO to flag set
Output OV DAC						

Note 1: Refer to **Section 15.0 "Power-Down Mode (Sleep)"**.

2: These parameters are characterized, but not production tested.

3: Ensured by design, not production tested.

4: V_{DD} is the voltage present at the V_{DD} pin.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

6: The V_{DD} LDO will limit the total source current to a maximum of 35 mA. Individually each pin can source a maximum of 15 mA.

4.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 150 kHz, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Resolution	nbits	—	8	—	Bits	Linear DAC
Full Scale Range	FSR	0	—	2 * BG	V	
Tolerance	$OVREF_{TOL}$	**-10**	—	**+10**	%	Full Scale, Code = 0xFF
Output OV Comparator						
OV Hysteresis	OV_{HYS}	—	50	—	mV	
Input Bias Current	I_{BIAS}	—	±1	—	µA	
Common-Mode Input Voltage Range	V_{CMR}	0	—	3.0	V	**Note 3**
Input-to-Output Delay	TD	—	200	—	ns	**Note 3** 100 ns rise time to 1V overdrive on V_S V_S > OV to flag set
Voltage Reference DAC (V_{REF})						
Resolution	nbits	—	8	—	V/V	Linear DAC
Full-Scale Range	FSR	BG	—	2 * BG	V	Pedestal set to BG
Voltage Reference DAC (V_{REF2})						
Resolution	nbits	—	8	—	Bits	Linear DAC
Full-Scale Range	FSR	0	—	BG	V	
Sink Current	I_{SINK}	**-3**	—	—	mA	V_{REF2} = 0V, R_L = 300Ω to BG
Source Current	I_{SOURCE}	**3**	—	—	mA	V_{REF2} = BG, R_L = 300Ω to GND
Tolerance	$VREF2_{TOL}$	**-10**	—	**+10**	%	Full Scale, Code = 0xFF
Current Sense Amplifier (A2)						
Amplifier PSRR	PSRR	—	65	—	dB	V_{CM} = 2 * BG
Closed-Loop Voltage Gain	$A2_{VCL}$	—	10	—	V/V	R_L = 5 kΩ to 2.048V, 100 mV < A2 < AV_{DD} – 100 mV, V_{CM} = BG
Low-Level Output	V_{OL}	—	300	—	mV	R_L = 5 kΩ to 2.048V
Gain-Bandwidth Product	GBWP	—	10	—	MHz	AV_{DD} = 4V
Input Impedance	R_{IN}	—	10	—	kΩ	
Sink Current	I_{SINK}	**-3**	—	—	mA	I_{SP} = I_{SN} = GND R_L = 300Ω to 2 * BG
Source Current	I_{SOURCE}	**3**	—	—	mA	I_{SP} = I_{SN} = GND R_L = 300Ω to GND

Note 1: Refer to **Section 15.0 "Power-Down Mode (Sleep)"**.

2: These parameters are characterized, but not production tested.

3: Ensured by design, not production tested.

4: V_{DD} is the voltage present at the V_{DD} pin.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

6: The V_{DD} LDO will limit the total source current to a maximum of 35 mA. Individually each pin can source a maximum of 15 mA.

4.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 150 kHz, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Common-Mode Range	V_{CMR}	GND – 0.3	—	V_{BG} + 0.3	V	**Note 3**
Common-Mode Rejection Ratio	CMRR	—	70	—	dB	
Internal Feedback Resistor	R_{FB_INT}	—	5	—	kΩ	
Internal Feedback Resistor Tol	$R_{FB\_INT\_TOL}$	—	2	—	%	Trimmed
Pedestal Voltage						
Pedestal Voltage Level	VZC	—	BG	—	V	
Error Amplifier (EA)						
Input Offset Voltage	V_{OS}	—	2	—	mV	
Common-Mode Rejection Ratio	CMRR	—	65	—	dB	V_{CM} = 0V to BG
Open-Loop Voltage Gain	A_{VOL}	—	70	—	dB	**Note 3**
Low-Level Clamp Value	V_{OL}	**BG - 0.35**	BG - 0.22	**BG - 0.1**	V	R_L = 5 kΩ to 2.048V
Gain-Bandwidth Product	GBWP	—	3.5	—	MHz	
Error Amplifier Sink Current	I_{SINK}	**-3**	—	—	mA	V_{REF} = BG, I_{FB} = I_{COMP} R_L = 150Ω to 1.5 * BG
Error Amplifier Source Current	I_{SOURCE}	**3**	—	—	mA	V_{REF} = 2 * BG, I_{FB} = I_{COMP} R_L = 150Ω to 1.5 * BG
Maximum Error Amplifier Output High-Level Clamp	V_{EA_MAX}	—	2 x BG	—	V	EA Output clamped to 2 x BG Voltage
Peak Current Sense Input						
Maximum Primary Current Sense Signal Voltage	V_{IP_MAX}	—	BG	1.5	V	**Note 3**
PWM Comparator						
Input-to-Output Delay	TD	—	11	**20**	ns	**Note 3**
Peak Current Leading Edge Blanking						
Resolution	LEB	—	2	—	Bits	
Blanking Time Adjustable Range	LEB_{RANGE}	0	—	256	ns	4-Step Programmable Range (0, 50,100, and 200 ns) **(Note 3)**

Note 1: Refer to **Section 15.0 "Power-Down Mode (Sleep)"**.

2: These parameters are characterized, but not production tested.

3: Ensured by design, not production tested.

4: V_{DD} is the voltage present at the V_{DD} pin.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

6: The V_{DD} LDO will limit the total source current to a maximum of 35 mA. Individually each pin can source a maximum of 15 mA.