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MCP19122/3

Digitally Enhanced Power Analog Controller with Integrated Synchronous Driver

Synchronous Buck Features

- Input Voltage: 4.5V to 40V (operating), 48V (non-operating)
- Output Voltage: 0.3V to 16V
  - 0.1% typical output voltage accuracy
  - Greater than 16V requires external divider
- Switching Frequency: 100 kHz to 1.6 MHz
- Shutdown Quiescent Current: 50 µA Typical
- High-Drive:
  - +5V Gate Drive
  - 2A Source Current
  - 2A Sink Current
- Low-Drive:
  - +5V Gate Drive
  - 2A Source Current
  - 4A Sink Current
- Emulated Average Current Mode Control
- Differential Remote Output Sense
- Multi-Phase Systems:
  - Master or Slave
  - Frequency Synchronized
  - Common Current Sense Signal
- Multiple Output Systems:
  - Master or Slave
  - Frequency Synchronized
- AEC-Q100 Qualified
- Configureable Parameters:
  - Overcurrent Limit
  - Input Undervoltage Lockout
  - Input Overvoltage
  - Output Overvoltage
  - Output Undervoltage
  - Internal Analog Compensation
  - Soft Start Profile
  - Synchronous Driver Dead Time
  - Switching Frequency
- Thermal Shutdown

Microcontroller Features

- Precision 8 MHz Internal Oscillator Block:
  - Factory Calibrated
- Interrupt Capable
  - Firmware
  - Interrupt-on-Change Pins
- Only 35 Instructions to Learn
- 4096 Words On-Chip Program Memory
- High Endurance Flash:
  - 100,000 Write Flash Endurance
  - Flash Retention: >40 years
- Watchdog Timer (WDT) with Independent Oscillator for Reliable Operation
- Programmable Code Protection
- In-Circuit Debug (ICD) via Two Pins (MCP19123)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- 12 I/O Pins and One Input-Only Pin (MCP19122)
  - 3 Open Drain Pins
  - 2 Weak Current Source Pins
- 16 I/O Pins and One Input-Only Pin (MCP19123)
  - 3 Open Drain Pins
  - 2 Weak Current Source Pins
- Analog-to-Digital Converter (ADC):
  - 10-bit Resolution
  - 24 Internal Channels
  - 8 External Channels
- Timer0: 8-bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - 16-bit Timer/Counter with Prescaler
  - 2 Selectable Clock Sources
  - External Gate Input Mode
- Timer2: 8-Bit Timer/Counter with Prescaler
  - 8-bit Period Register
- Capture, Compare Module
- I^2C™ Communication:
  - 7-bit Address Masking
  - 2 Dedicated Address Registers
  - SMBus/PMBus™ Compatibility

Pin Diagram – 24-Pin 4X4 QFN (MCP19122)

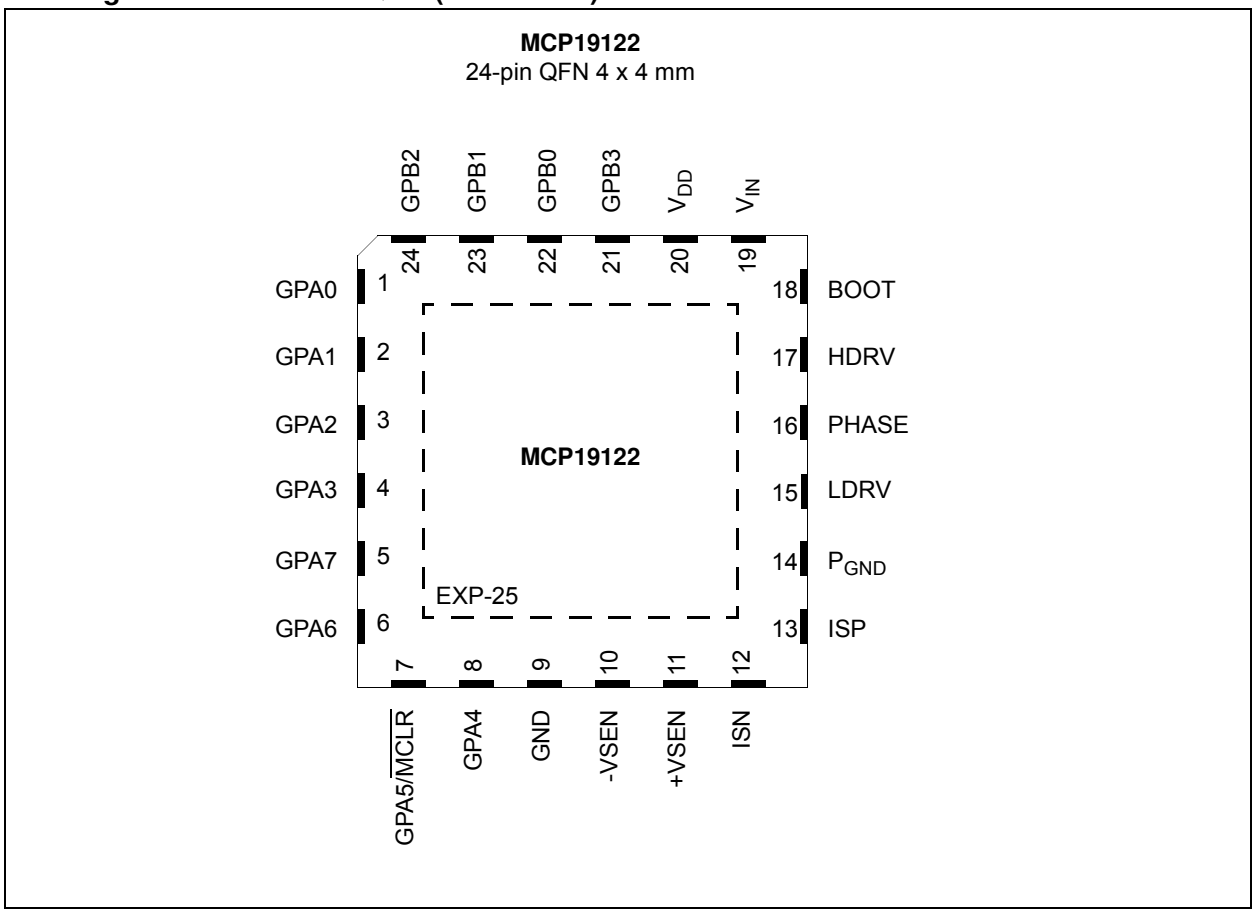

TABLE 1: 24-PIN QFN (MCP19122) SUMMARY

I/O	24-Pin QFN	ANSEL	A/D	Timers	MSSP	Interrupt	Pull-up	Basic	Additional
GPA0	1	Y	AN0	—	—	IOC	Y	—	Analog Debug Output (1)
GPA1	2	Y	AN1	—	—	IOC	Y	—	Sync Signal In/Out (2, 3)
GPA2	3	Y	AN2	T0CKI	—	IOC INT	—	—	Weak Current Source
GPA3	4	Y	AN3		—	IOC	—	—	Weak Current Source Timer1 Gate Input 1
GPA4	8	N	—	—	—	IOC	N	—	—
GPA5	7	N	—	—	—	IOC(4)	Y(5)	$\overline{\text{MCLR}}$	—
GPA6	6	N	—	—	—	IOC	N	ICSPDAT	—
GPA7	5	N	—	—	SCL	IOC	N	ICSPCLK	—
GPB0	22	N	—	—	SDA	IOC	N	—	—
GPB1	23	Y	AN4	—	—	IOC	Y	—	Current Sense Output Current Reference Input (3)
GPB2	24	Y	AN5	—	—	IOC	Y	—	Timer1 Gate Input 2
GPB3	21	N	—	—	—	IOC	Y	—	Clock Signal In/Out (2, 3)
V_{IN}	19	N	—	—	—	—	—	V_{IN}	Device Input Voltage
V_{DD}	20	N	—	—	—	—	—	V_{DD}	Internal Regulator Output
GND	9	N	—	—	—	—	—	GND	Small Signal Ground
P_{GND}	14	N	—	—	—	—	—	—	Large Signal Ground
LDRV	15	N	—	—	—	—	—	—	Low-Side MOSFET Connection
HDRV	17	N	—	—	—	—	—	—	High-Side MOSFET Connection
PHASE	16	N	—	—	—	—	—	—	Switch Node
BOOT	18	N	—	—	—	—	—	—	Floating Bootstrap Supply
$+V_{SEN}$	11	N	—	—	—	—	—	—	Output Voltage Differential Sense
$-V_{SEN}$	10	N	—	—	—	—	—	—	Output Voltage Differential Sense
ISP	13	N	—	—	—	—	—	—	Current Sense Input
ISN	12	N	—	—	—	—	—	—	Current Sense Input
EP	—	—	—	—	—	—	—	—	Exposed Pad

Note 1: The Analog Debug Output is selected when the BUFFCON<BNCHEN> bit is set.

2: Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

4: The IOC is disabled when $\overline{\text{MCLR}}$ is enabled.

5: Weak pull-up always enabled when $\overline{\text{MCLR}}$ is enabled, otherwise the pull-up is under user control.

Pin Diagram – 28-Pin 5X5 QFN (MCP19123)

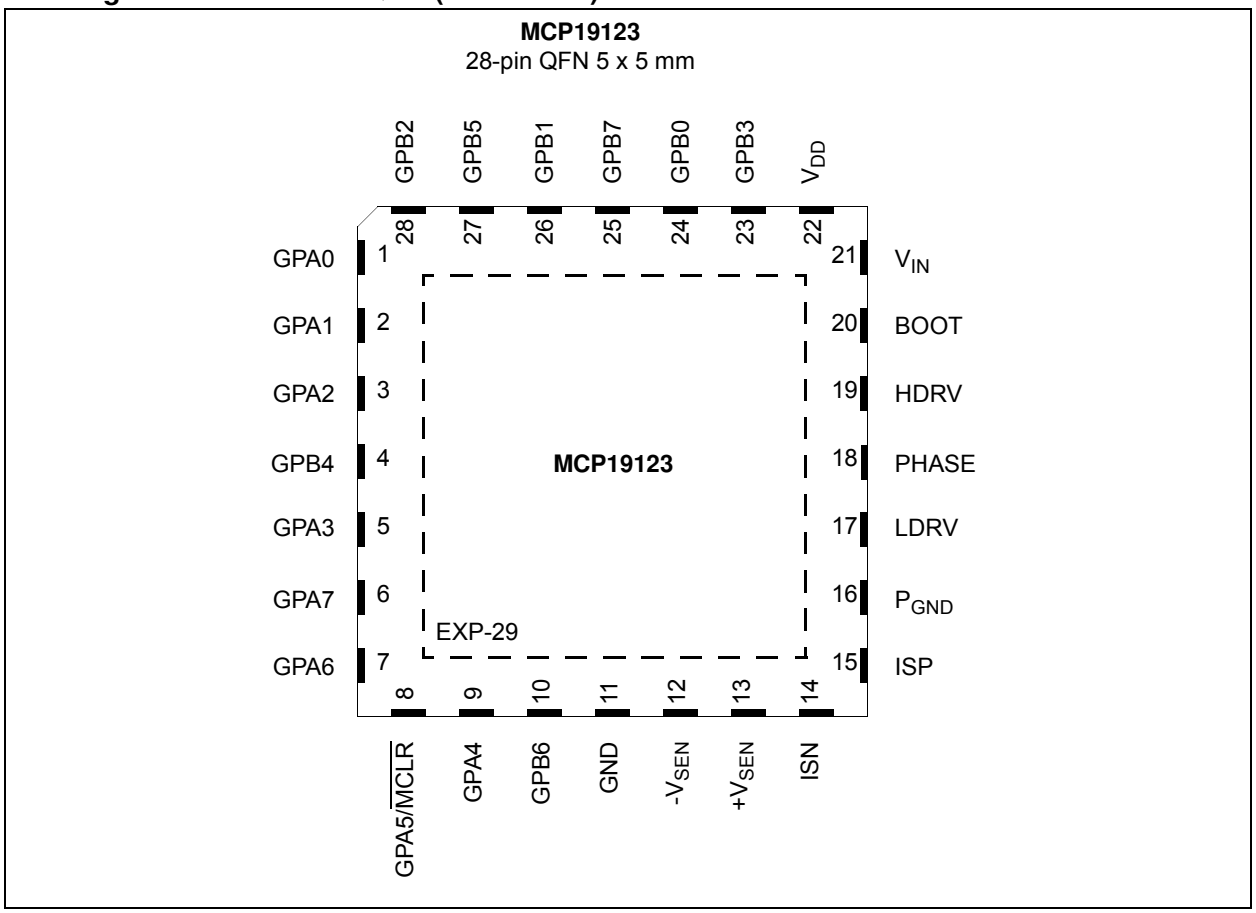

TABLE 2: 28-PIN QFN (MCP19123) SUMMARY

I/O	28-Pin QFN	ANSEL	A/D	Timers	MSSP	Interrupt	Pull-up	Basic	Additional
GPA0	1	Y	AN0	—	—	IOC	Y	—	Analog Debug Output (1)
GPA1	2	Y	AN1	—	—	IOC	Y	—	Sync Signal In/Out (2, 3)
GPA2	3	Y	AN2	T0CKI	—	IOC INT	Y	—	Weak Current Source
GPA3	5	Y	AN3	—	—	IOC	Y	—	Weak Current Source Timer1 Gate Input 1
GPA4	9	N	—	—	—	IOC	N	—	—
GPA5	8	N	—	—	—	IOC(4)	Y(5)	$\overline{\text{MCLR}}$	—
GPA6	7	N	—	—	—	IOC	N	—	CCD Input 1
GPA7	6	N	—	—	SCL	IOC	N	—	—
GPB0	24	N	—	—	SDA	IOC	N	—	—
GPB1	26	Y	AN4	—	—	IOC	Y	—	Current Sense Output Current Reference Input(3)
GPB2	28	Y	AN5	—	—	IOC	Y	—	Timer1 Gate Input 2
GPB3	23	N	—	—	—	IOC	Y	—	Clock Signal In/Out (2, 3)
GPB4	4	Y	AN6	—	—	IOC	Y	ICSPDAT ICDDAT	—
GPB5	27	Y	AN7	—	—	IOC	Y	ICSPCLK ICDCLK	—
GPB6	10	N	—	—	—	IOC	Y	—	CCD Input 2
GPB7	25	N	—	—	—	IOC	Y	—	External A/D Reference
V_{IN}	21	N	—	—	—	—	—	V_{IN}	Device Input Voltage
V_{DD}	22	N	—	—	—	—	—	V_{DD}	Internal Regulator Output
GND	11	N	—	—	—	—	—	GND	Small Signal Ground
P_{GND}	16	N	—	—	—	—	—	—	Large Signal Ground
LDRV	17	N	—	—	—	—	—	—	Low-Side MOSFET Connection
HDRV	19	N	—	—	—	—	—	—	High-Side MOSFET Connection
PHASE	18	N	—	—	—	—	—	—	Switch Node
BOOT	20	N	—	—	—	—	—	—	Floating Bootstrap Supply
$+V_{SEN}$	13	N	—	—	—	—	—	—	Output Voltage Differential Sense
$-V_{SEN}$	12	N	—	—	—	—	—	—	Output Voltage Differential Sense
ISP	15	N	—	—	—	—	—	—	Current Sense Input
ISN	14	N	—	—	—	—	—	—	Current Sense Input
EP	—	—	—	—	—	—	—	—	Exposed Pad

Note 1: The Analog Debug Output is selected when the BUFFCON<BNCHEN> bit is set.

2: Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

4: The IOC is disabled when $\overline{\text{MCLR}}$ is enabled.

5: Weak pull-up always enabled when $\overline{\text{MCLR}}$ is enabled, otherwise the pull-up is under user control.

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NOTES:

1.0 DEVICE OVERVIEW

The MCP19122/3 is a stand-alone mixed signal synchronous buck pulse-width modulated (PWM) current mode controller that features an integrated microcontroller core, high-endurance flash memory, communication and configurable analog circuitry. It features integrated synchronous drivers, bootstrap device, internal linear regulator and 4k words of nonvolatile memory. The devices are capable of efficiently converting 4.5V-40V to 0.3V-16V.

Since the MCP19122/3 uses traditional analog control circuitry to regulate the output of the DC/DC converter, the integration of the PIC® microcontroller mid-range core is used to provide complete customization of device operating parameters, start-up and shut-down profiles, protection levels and fault handling procedures.

After initial device configuration using Microchip's MPLAB® X Integrated Development Environment (IDE) software, PMBus commands or I^2C can be used by a host to communicate with, or modify, the operation of the MCP19122/3.

FIGURE 1-1: TYPICAL APPLICATION CIRCUIT

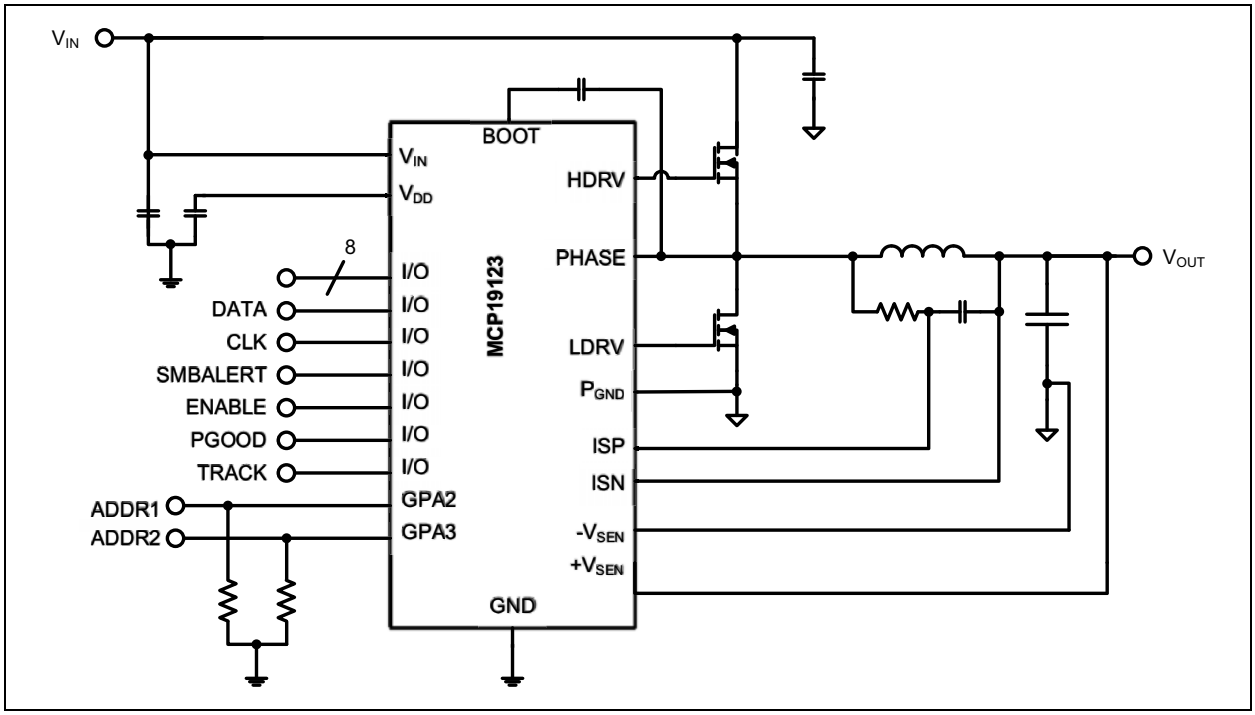


FIGURE 1-2: MCP19122/3 SYNCHRONOUS BUCK BLOCK DIAGRAM

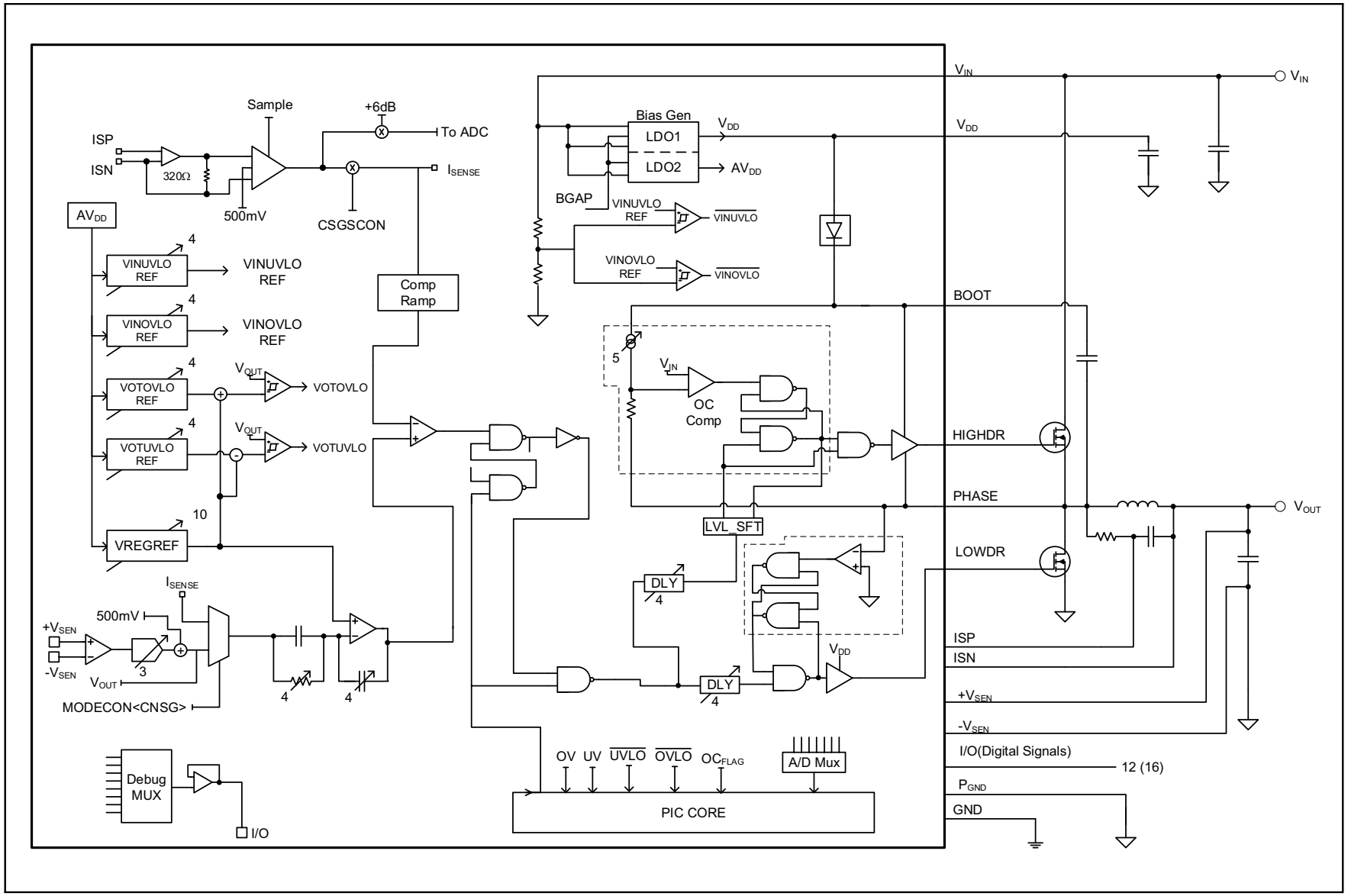
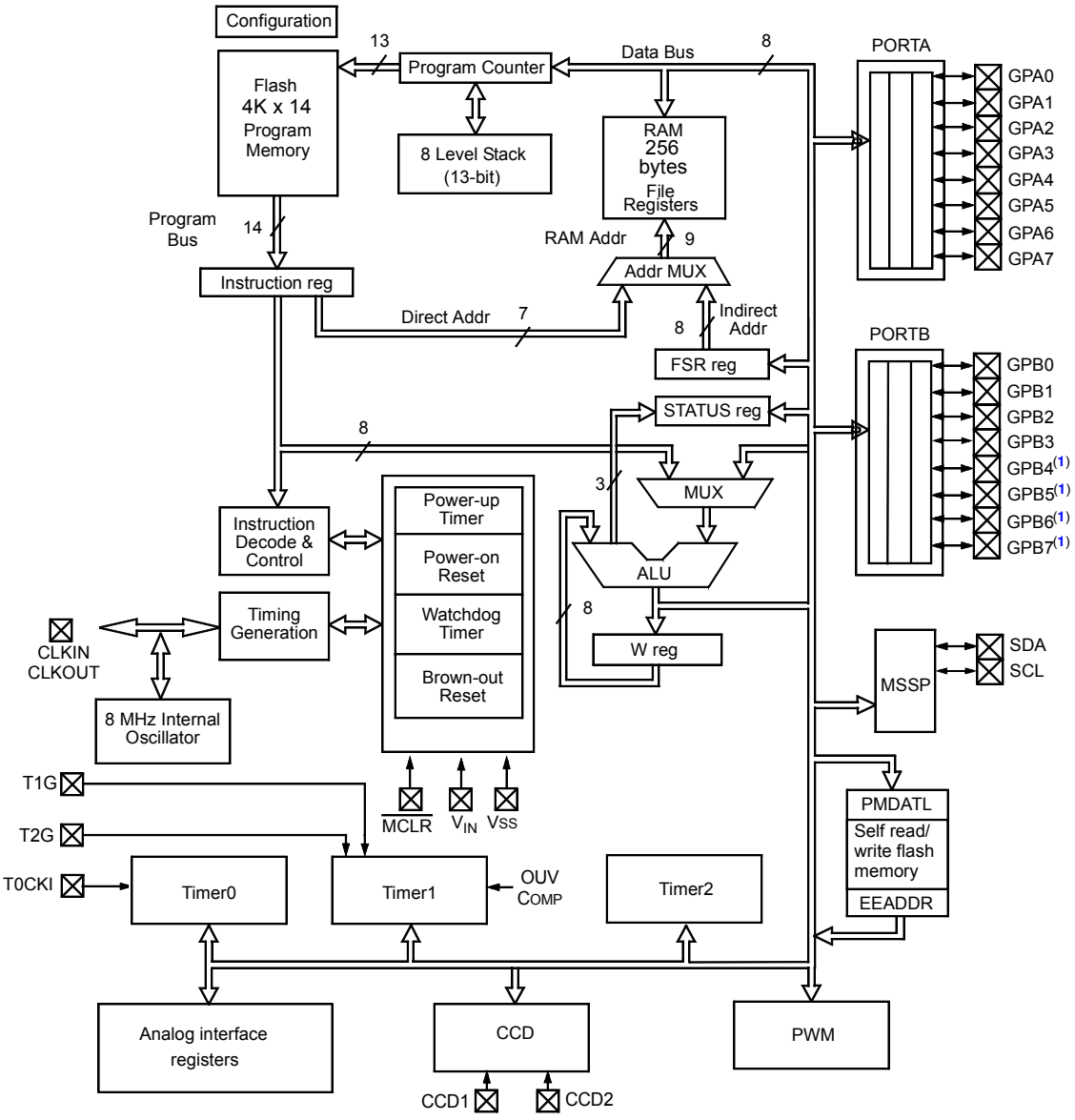


FIGURE 1-3: MICROCONTROLLER CORE BLOCK DIAGRAM



Note 1: Not implemented on the MCP19122.

2.0 PIN DESCRIPTION

The MCP19122/3 family of devices features pins that have multiple functions associated with each pin. Table 2-1 provides a description of the different functions. See **Section 2.1 "Detailed Pin Description"** for more detailed information.

TABLE 2-1: MCP19122/3 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GPA0/AN0/ANALOG_TEST	GPA0	TTL	CMOS	General purpose I/O
	AN0	AN	—	A/D Channel 0 input.
	ANALOG_TEST	—	—	Internal analog signal multiplexer output (1)
GPA1/AN1/SYC_SIGNAL	GPA1	TTL	CMOS	General purpose I/O
	AN1	AN	—	A/D Channel 1 input
	SYC_SIGNAL	—	—	Switching clock synchronization signal input and output (2,3)
GPA2/AN2/T0CKI/INT	GPA2	TTL	CMOS	General purpose I/O
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External interrupt
GPA3/AN3/T1G1	GPA3	TTL	CMOS	General purpose I/O
	AN3	AN	—	A/D Channel 3 input
	T1G1	ST	—	Timer1 gate input 1
GPA4	GPA4	TTL	OD	General purpose I/O
GPA5/$\overline{\text{MCLR}}$	GPA5	TTL	—	General purpose input only
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
GPA6/CCD1(4)/ICSPDAT(5)	GPA6	ST	CMOS	General purpose I/O
	CCD1	ST	CMOS	Capture/Compare input 1 (4)
	ICSPDAT		CMOS	Serial Programming Data I/O (5)
GPA7/SCL/ICSPCLK(5)	GPA7	ST	OD	General purpose open drain I/O
	SCL	I^2C	OD	I^2C clock
	ICSPCLK	ST	—	Serial Programming Clock (5)
GPB0/SDA	GPB0	TTL	OD	General purpose I/O
	SDA	I^2C	OD	I^2C data input/output
GPB1/AN4/CON_SIGNAL	GPB1	TTL	CMOS	General purpose I/O
	AN4	AN	—	A/D Channel 4 input
	CON_SIGNAL	—	—	Current sense output or current reference input (3)

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST =Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: Analog Test is selected when the BUFFCON<BNCHEN> bit is set.

2: Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

4: Feature only available on the MCP19123.

5: Feature only available on the MCP19122.

TABLE 2-1: MCP19122/3 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
GPB2/AN5/T1G2	GPB2	TTL	CMOS	General purpose I/O
	AN5	AN	—	A/D Channel 5 input
	T1G2	ST	—	Timer1 gate input 2
GPB3/CLOCK	GPB3	TTL	CMOS	General purpose I/O
	CLOCK	—	—	Clock signal input/output (2,3)
GPB4(4)/AN6(4)/ICSPDAT(4)/ ICDDAT(4)	GPB4	TTL	CMOS	General purpose I/O(4)
	AN6	AN	—	A/D Channel 6 input(4)
	ICSPDAT	ST	—	Serial Programming Data I/O(4)
	ICDDAT	ST	—	In-circuit debug data(4)
GPB5(4)/AN7(4)/ICSPCLK(4)/ ICDCLK(4)	GPB5	TTL	CMOS	General purpose I/O(4)
	AN7	AN	—	A/D Channel 7 input(4)
	ISCPCLK	ST	—	Serial Programming Clock(4)
	ICDCLK	ST	—	In-circuit debug clock(4)
GPB6/CCD2(4)	GPB6	TTL	CMOS	General purpose I/O
	CCD2	ST	CMOS	Capture/Compare input 2(4)
GPB7/VADC(4)	GPB7	TTL	CMOS	General purpose I/O
	VADC	AN		External voltage reference for A/D(4)
V_{IN}	V_{IN}	—	—	Device input supply voltage
V_{DD}	V_{DD}	—	—	Internal +5V LDO output pin
GND	GND	—	—	Small signal quiet ground
P_{GND}	P_{GND}	—	—	Large signal power ground
LDRV	LDRV	—	—	High-current drive signal connected to the gate of the low-side MOSFET
HDRV	HDRV	—	—	Floating high-current drive signal connected to the gate of the high-side MOSFET
PHASE	PHASE	—	—	Synchronous buck switch node connection
BOOT	BOOT	—	—	Floating bootstrap supply
$+V_{SEN}$	$+V_{SEN}$	—	—	Positive input of the output voltage sense differential amplifier
$-V_{SEN}$	$-V_{SEN}$	—	—	Negative input of the output voltage sense differential amplifier
ISP	ISP	—	—	Current sense input
ISN	ISN	—	—	Current sense input
EP	—	—	—	Exposed Thermal Pad

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST =Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: Analog Test is selected when the BUFFCON<BNCHEN> bit is set.

2: Selected when device is functioning as multiple output master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MSC<2:0> bits in the MODECON register.

4: Feature only available on the MCP19123.

5: Feature only available on the MCP19122.

2.1 Detailed Pin Description

2.1.1 GPA0 PIN

GPA0 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN0 is an input to the A/D. To configure this pin to be read by the A/D on channel 0, bits TRISA0 and ANSA0 must be set.

When the BUFFCON<BNCHEN> bit is set, this pin is configured as the ANALOG_TEST function. It is a buffered output of the internal analog and digital signal multiplexer. Analog signals present on this pin are controlled by the ADCON0 register; see Register 19-1. Digital signals present on this pin are controlled by the BUFFCON register; see Register 7-1.

2.1.2 GPA1 PIN

GPA1 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN1 is an input to the A/D. To configure this pin to be read by the A/D on channel 1, bits TRISA1 and ANSA1 must be set.

When the MCP19122/3 is configured as a multiple output or multi-phase MASTER or SLAVE, this pin is configured to be the switching frequency synchronization input or output, SYN_SIGNAL. See **Section 3.12 "System Configuration Control"** for more information.

2.1.3 GPA2 PIN

GPA2 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak current source and interrupt-on-change are also available.

AN2 is an input to the A/D. To configure this pin to be read by the A/D on channel 2, bits TRISA2 and ANSA2 must be set.

When bit T0CS is set, the T0CKI function is enabled. See **Section 21.0 "Timer0 Module"** for more information.

GPA2 can also be configured as an external interrupt by setting of the INTE bit. See **Section 13.0.1 "GPA2/INT Interrupt"** for more information.

2.1.4 GPA3 PIN

GPA3 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak current source and interrupt-on-change are also available.

AN3 is an input to the A/D. To configure this pin to be read by the A/D on channel 3, bits TRISA3 and ANSA3 must be set.

T1G1 is an input to the TIMER1 gate. To configure this pin to be an external source to the TIMER1 gate circuitry, see **Section 22.0 "Timer1 Module With Gate Control"**.

2.1.5 GPA4 PIN

GPA4 is a true open drain general purpose pin whose data direction is controlled in TRISGPA. There is no internal connection between this pin and device V_{DD}, making this pin ideal to be used as an SMBus Alert pin. This pin does not have a weak pull-up, but interrupt-on-change is available.

2.1.6 GPA5 PIN

GPA5 is a general purpose TTL input-only pin. An internal weak pull-up and interrupt-on-change are also available.

For programming purposes, this pin is to be connected to the $\overline{MCLR}$ pin of the serial programmer. See **Section 29.0 "In-Circuit Serial Programming™ (ICSP™)"** for more information.

2.1.7 GPA6 PIN

GPA6 is a general purpose CMOS input/output pin whose data direction is controlled in TRISGPA. An interrupt-on-change is also available.

On the MCP19122, the ISCPDAT is the primary serial programming data input function. This is used in conjunction with ICSPCLK to serial program the device. This pin function is only implemented on the MCP19122.

On the MCP19123, this pin can be configured as an input to the CCD module. For more information refer to **Section 24.0 "Dual Capture/Compare (CCD) Module"**.

2.1.8 GPA7 PIN

GPA7 is a true open drain general purpose pin whose data direction is controlled in TRISGPA. There is no internal connection between this pin and device V_{DD}. This pin does not have a weak pull-up, but interrupt-on-change is available.

When the MCP19122/3 is configured for I^2C communication (see **Section 27.2 "I^2C Mode Overview"**), GPA7 functions as the I^2C clock, SCL.

On the MCP19122, the ISCPCLK is the serial programming clock function. This is used in conjunction with ICSPDAT to serial program the device. This pin function is only implemented on the MCP19122.

2.1.9 GPB0 PIN

GPB0 is a true open drain general purpose pin whose data direction is controlled in TRISGPB. There is no internal connection between this pin and device V_{DD}. This pin does not have a weak pull-up, but interrupt-on-change is available.

When the MCP19122/3 is configured for I^2C communication (see **Section 27.2 "I^2C Mode Overview"**), GPB0 functions as the I^2C clock, SDA.

2.1.10 GPB1 PIN

GPB1 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN4 is an input to the A/D. To configure this pin to be read by the A/D on channel 4, bits TRISB1 and ANSB1 must be set.

When the MCP19122/3 is configured as a multi-phase MASTER or SLAVE, this pin is configured to be the sensed current input or output signal. On a device configured to be a MASTER, this is an output signal of the sensed current that is to be shared with the SLAVE devices. On a device configured as a SLAVE, this is an input signal used to as a current regulation point. See **Section 3.12 "System Configuration Control"**, for more information.

2.1.11 GPB2 PIN

GPB2 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN5 is an input to the A/D. To configure this pin to be read by the A/D on channel 5, bits TRISB2 and ANSB2 must be set.

T1G2 is an input to the TIMER1 gate. To configure this pin to be an external source to the TIMER1 gate circuitry, see **Section 22.0 "Timer1 Module With Gate Control"**.

2.1.12 GPB3 PIN

GPB3 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

When the MCP19122/3 is configured as a multiple output or multi-phase Master or Slave, this pin is configured to be the switching frequency clock input or output. See **Section 3.12 "System Configuration Control"**.

2.1.13 GPB4 PIN

This pin and associated functions are only available on the MCP19123 device.

GPB4 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN6 is an input to the A/D. To configure this pin to be read by the A/D on channel 6, bits TRISB4 and ANSB4 must be set.

On the MCP19123, the ISCPDAT is the primary serial programming data input function. This is used in conjunction with ICSPCLK to serial program the device.

The ICDDAT is the in-circuit debug data function. This pin function is only implemented on the MCP19123. See **Section 29.2 "In-Circuit Debugger"**

2.1.14 GBP5 PIN

This pin and associated functions is only available on the MCP19123 device.

GPB5 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN7 is an input to the A/D. To configure this pin to be read by the A/D on channel 7, bits TRISB5 and ANSB5 must be set.

On the MCP19123, the ISCPCLK is the primary serial programming clock function. This is used in conjunction with ICSPDAT to serial program the device.

The ICDDLK is the in-circuit debug clock function. This pin function is only implemented on the MCP19123. See **Section 29.2 "In-Circuit Debugger"**

2.1.15 GPB6 PIN

This pin and associated functions is only available on the MCP19123 device.

GPB6 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

CCD2 is an input to the CCD module. For more information refer to **Section 24.0 "Dual Capture/Compare (CCD) Module"**.

2.1.16 GPB7 PIN

This pin and associated functions is only available on the MCP19123 device.

GPB7 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

VADC is an external A/D reference voltage input. See **Section 19.0 "Analog-to-Digital Converter (ADC) Module"**.

2.1.17 V_{IN} PIN

Device input power connection pin. It is recommended that capacitance be placed between this pin and the GND pin of the device.

2.1.18 V_{DD} PIN

The output of the internal +5.0V regulator is connected to this pin. It is recommended that a 1.0 µF bypass capacitor be connected between this pin and the GND pin of the device. The bypass capacitor should be placed physically close to the device.

2.1.19 GND PIN

GND is the small signal ground connection pin. This pin should be connected to the exposed pad, on the bottom of the package.

2.1.20 P_{GND} PIN

Connect all large signal level ground returns to P_{GND}. These large-signal level ground traces should have a small loop area and minimal length to prevent coupling of switching noise to sensitive traces.

2.1.21 LDRV PIN

The gate of the low-side or rectifying MOSFET is connected to LDRV. The PCB trace connecting LDRV to the gate must be of minimal length and appropriate width to handle the high peak drive currents and fast voltage transitions.

2.1.22 HDRV PIN

The gate of the high-side MOSFET is connected to HDRV. This is a floating driver referenced to PHASE. The PCB trace connecting HDRV to the gate must be of minimal length and appropriate width to handle the high peak drive current and fast voltage transitions.

2.1.23 PHASE PIN

The PHASE pin provides the return path for the high-side gate driver. The source of the high-side MOSFET, drain of the low-side MOSFET and the inductor are connected to this pin.

2.1.24 BOOT PIN

The BOOT pin is the floating bootstrap supply pin for the high-side gate driver. A capacitor is connected between this pin and the PHASE pin to provide the necessary charge to turn on the high-side MOSFET.

2.1.25 $+V_{SEN}$ PIN

The non-inverting input of the unity gain amplifier used for output voltage remote sensing is connected to the $+V_{SEN}$ pin.

2.1.26 $-V_{SEN}$ PIN

The inverting input of the unity gain amplifier used for output voltage remote sensing is connected to the $–V_{SEN}$ pin.

2.1.27 ISP PIN

The non-inverting input of the current sense amplifier is connected to the ISP pin.

2.1.28 ISN PIN

The inverting input of the current sense amplifier is connected to the ISN pin.

2.1.29 EXPOSED PAD (EP)

There is no internal connection to the Exposed Thermal Pad. The EP should be connected to the GND pin and to the GND PCB plane to aid in the removal of the heat.

3.0 FUNCTIONAL DESCRIPTION

3.1 Internal Supplies

The operating input voltage of the MCP19122/3 ranges from 4.5V to 40V. There are two internal Low Dropout (LDO) voltage regulators. A 5V LDO (V_{DD}) is used to power the internal microcontroller, the internal gate driver circuitry and provide a 5V output for external use. It is recommended that a 1 µF ceramic capacitor be placed between the V_{DD} pin and the P_{GND} pin.

The MODECON<VDDEN> bit controls the state of the 5V V_{DD} LDO when the `SLEEP` command is issued to the MCP19122/3. See **Section 3.12.3 "VDD LDO Control"** for more information.

The gate drive current required to drive the external power MOSFETs must be added to the MCP19122/3 quiescent current $I_{Q(max)}$. This total current must be less than the maximum current, I_{DD-OUT}, available from V_{DD} that is specified in **Section 4.0 "Electrical Characteristics"**.

A second 4V LDO (AV_{DD}) is used to power the internal analog circuitry. The AV_{DD} is not available externally. AV_{DD} is calibrated to 4.096V and is the default ADC reference voltage.

EQUATION 3-1: TOTAL REGULATOR CURRENT

$$I_{DD-OUT} > (I_Q + I_{DRIVE} + I_{EXT})$$

Where:

- I_{DD-OUT} is the total current available from V_{DD}
- I_Q is the device quiescent current
- I_{DRIVE} is the current required to drive the external MOSFETs
- I_{EXT} is the amount of current used to power additional external circuitry.

EQUATION 3-2: GATE DRIVE CURRENT

$$I_{DRIVE} = (Q_{gHIGH} + Q_{gLOW}) \times F_{SW}$$

Where:

- I_{DRIVE} is the current required to drive the external MOSFETs
- Q_{gHIGH} is the total gate charge of the high-side MOSFET
- Q_{gLOW} is the total gate charge of the low-side MOSFET
- F_{SW} is the switching frequency

3.2 Switching Frequency

The switching frequency is configurable over the range of 100 kHz to 1.6 MHz. The Timer2 module is used to generate the HDRV/LDRV switching frequency. Refer to Section 26.0, Enhanced PWM Module for more information. Example 3-1 shows how to configure the MCP19122/3 for a switching frequency of 300 kHz.

EXAMPLE 3-1: CONFIGURING F_{SW}

```
BANKSEL     T2CON
CLRF        T2CON   ;Turn off Timer2
CLRF        TMR2    ;Initialize module
MOVLW       0x19    ;Fsw=300 kHz
MOVWF       PR2
MOVLW       0x0A    ;Max duty cycle=40%
MOVWF       PWMRL
MOVWF       PWMRH
MOVLW       0x00    ;No phase shift
MOVWF       PWMPHL
MOVWF       PWMPHH
MOVLW       0x04    ;Turn on Timer2
MOVWF       T2CON
```

3.3 Input Voltage Monitoring

The input voltage to the MCP19122/3 is monitored to determine an input undervoltage or an input overvoltage. It can also be measured by the ADC and reported as telemetry data.

3.3.1 INPUT UNDERVOLTAGE LOCKOUT

The VINUVLO register contains the digital value that sets the input under voltage lockout. When the input voltage on the V_{IN} pin to the MCP19122/3 is below this programmed level, the PIR2<UVLOIF> status flag will be set. This bit is automatically cleared when the MCP19122/3 V_{IN} voltage rises above this programmed level. The VINUVLO shall operate on a rising or falling input voltage. Hysteresis shall exist between the rising threshold that clears the flag and the failing threshold that sets the flag.

A hardware under voltage lockout path can be enabled by setting the VINCON<UVLOEN> bit. When this bit is set and the voltage on the V_{IN} pin is below the threshold set by the VINUVLO register, hardware will keep the high-side and low-side MOSFET drivers off. Once the voltage on the V_{IN} pin is greater than the threshold set by the VINUVLO register, the high-side and low-side MOSFET drivers are enabled.

To function properly, the V_{IN} under voltage lockout setting must be lower than the V_{IN} over voltage lockout setting. The state of the VINUVLO and VINOVLO registers are unknown at power-up. Therefore if only the V_{IN} under voltage lockout is desired, the V_{IN} over voltage lockout threshold still must be set in the VINOVLO register.

Note:	The UVLOIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register.
Note:	The UVLOIF interrupt flag bit is set when an interrupt condition occurs regardless of the state of the VINCON<UVLOEN> bit.

REGISTER 3-1: VINUVLO: INPUT UNDER VOLTAGE LOCKOUT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	UVLO3	UVLO2	UVLO1	UVLO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **UVLO<3:0>:** Under Voltage Lockout Configuration bits
0000 = 4.0V
0001 = 6.0V
0010 = 8.0V
0011 = 10.0V
0100 = 12.0V
0101 = 14.0V
0110 = 16.0V
0111 = 18.0V
1000 = 20.0V
1001 = 22.0V
1010 = 24.0V
1011 = 26.0V
1100 = 28.0V
1101 = 30.0V
1110 = 32.0V
1111 = 34.0V

3.3.2 INPUT OVER VOLTAGE LOCKOUT

The VINOVLO register contains the digital value that sets the input over voltage lockout. When the input voltage on the V_{IN} pin to the MCP19122/3 is above this programmed level, the PIR2<OVLOIF> status flag will be set. This bit is automatically cleared when the MCP19122/3 V_{IN} voltage falls below this programmed level. The VINOVLO shall operate on a rising or falling input voltage. Hysteresis shall exist between the rising threshold that sets the flag and the failing threshold that clears the flag.

A hardware over voltage lockout path can be enabled by setting the VINCON<OVLOEN> bit. When this bit is set and the voltage on the V_{IN} pin is above the threshold set by the VINOVLO register, hardware will keep the high-side and low-side MOSFET drivers off. Once the voltage on the V_{IN} pin is lower than the threshold set by the VINOVLO register, the high-side and low-side MOSFET drivers are enabled.

To function properly, the V_{IN} overvoltage lockout setting must be lower than the V_{IN} undervoltage lockout setting. The state of the VINUVLO and VINOVLO registers are unknown at power-up. Therefore if only the V_{IN} overvoltage lockout is desired, the V_{IN} undervoltage lockout threshold still must be set in the VINUVLO register.

Note:	The OVLOIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register.
Note:	The OVLOIF interrupt flag bit is set when an interrupt condition occurs regardless of the state of the VINCON<OVLOEN> bit.

REGISTER 3-2: VINOVLO: INPUT OVERVOLTAGE LOCKOUT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	OVLO3	OVLO2	OVLO1	OVLO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **OVLO<3:0>:** Overvoltage Lockout Configuration bits
0000 = 12.0V
0001 = 14.0V
0010 = 16.0V
0011 = 18.0V
0100 = 20.0V
0101 = 22.0V
0110 = 24.0V
0111 = 26.0V
1000 = 28.0V
1001 = 30.0V
1010 = 32.0V
1011 = 34.0V
1100 = 36.0V
1101 = 38.0V
1110 = 40.0V
1111 = 42.0V

3.3.3 INPUT UNDER/OVERVOLTAGE CONTROL REGISTER

The VINCON register is the comparator control register for both the input undervoltage lockout and input overvoltage lockout. It contains the enable bits, the polarity edge detection bits and the status output bits for both protection circuits. The interrupt flags <UVLOIF> and <OVLOIF> in the PIR2 register are independent of the enable <UVLOEN> and <OVLOEN> bits in the VINCON register. The <UVLOOUT> undervoltage lockout status output bit in the VINCON register indicates if an UVLO event has occurred. The <OVLOOUT> overvoltage lockout status output bit in the VINCON register indicates if an OVLO event has occurred.

When the input voltage on the V_{IN} pin to the MCP19122/3 is below the threshold programmed by the VINUVLO register and the <UVLOEN> bit is set, both the HDRV and LDRV gate drivers are disabled.

When the input voltage on the V_{IN} pin to the MCP19122/3 is above the threshold programmed by the VINOVLO register and the <OVLOEN> bit is set, both the HDRV and LDRV gate drivers are disabled.

REGISTER 3-3: VINCON: INPUT VOLTAGE UVLO AND OVLO CONTROL REGISTER

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0
UVLOEN	UVLOOUT	UVLOINTP	UVLOINTN	OVLOEN	OVLOOUT	OVLOINTP	OVLOINTN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **UVLOEN:** UVLO Comparator Module Logic Enable bit
1 = UVLO Comparator Module Logic enabled
0 = UVLO Comparator Module Logic disabled

bit 6 **UVLOOUT:** Undervoltage Lock Out Status bit
1 = UVLO event has occurred
0 = UVLO event has not occurred

bit 5 **UVLOINTP:** UVLO Comparator Interrupt-on-Positive Going Edge Enable bit
1 = UVLOIF will be set upon a positive going edge of the UVLO
0 = No UVLOIF will be set upon a positive going edge of the UVLO

bit 4 **UVLOINTN:** UVLO Comparator Interrupt on Negative Going Edge Enable bit
1 = UVLOIF will be set upon a negative going edge of the UVLO
0 = No UVLOIF will be set upon a negative going edge of the UVLO

bit 3 **OVLOEN:** OVLO Comparator Module Logic Enable bit
1 = OVLO Comparator Module Logic enabled
0 = OVLO Comparator Module Logic disabled

bit 2 **OVLOOUT:** Overvoltage Lock Out Status bit
1 = OVLO event has occurred
0 = OVLO event has not occurred

bit 1 **OVLOINTP:** OVLO Comparator Interrupt on Positive Going Edge Enable bit
1 = OVLOIF will be set upon a positive going edge of the OVLO
0 = No OVLOIF will be set upon a positive going edge of the OVLO

bit 0 **OVLOINTN:** OVLO Comparator Interrupt on Negative Going Edge Enable bit
1 = OVLOIF will be set upon a negative going edge of the OVLO
0 = No OVLOIF will be set upon a negative going edge of the OVLO

3.4 Output Overcurrent

The MCP19122/3 features a cycle-by-cycle peak current limit. By monitoring the OCIF interrupt flag, custom over current fault handling can be implemented.

To detect an output overcurrent, the MCP19122/3 senses the voltage drop across the high-side MOSFET while it is conducting. Leading-edge blanking is incorporated to mask the overcurrent measurement for a given amount of time. This helps prevent false overcurrent readings.

When an output overcurrent is sensed, the OCIF flag is set and the high-side drive signal is immediately terminated. Without any custom overcurrent handling implemented, the high-side drive signal will be asserted high at the beginning of the next clock cycle. If the overcurrent condition still exists, the high-drive signal will again be terminated.

The OCIF interrupt flag must be cleared in software. It can only be cleared once a switching cycle without an overcurrent condition has occurred.

Register OCCON contains the bits used to configure both the output overcurrent limit and the amount of leading edge blanking (see Register 3-4).

The OCCON<OCEN> bit must be set to enable the input overcurrent circuitry.

Note:	The OCIF interrupt flag bit is set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register.

REGISTER 3-4: OCCON: OUTPUT OVERCURRENT CONTROL REGISTER

R/W-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
OCEN	OCLEB1	OCLEB0	OOC4	OOC3	OOC2	OOC1	OOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **OCEN:** Output Overcurrent Control bit
1 = Output Overcurrent comparator is enabled
0 = Output Overcurrent comparator is disabled

bit 6-5 **OCLEB<1:0>:** Leading Edge Blanking
00 = 110 ns blanking
01 = 200 ns blanking
10 = 380 ns blanking
11 = 740 ns blanking

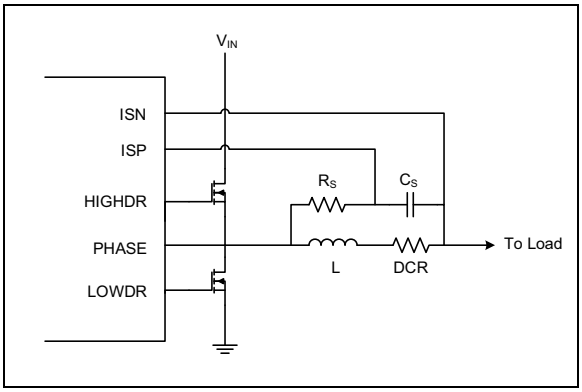
bit 4-0 **OOC<4:0>:** Output Overcurrent Configuration bits
00000 = 91 mV drop
00001 = 112 mV drop
00010 = 134 mV drop
00011 = 155 mV drop
00100 = 177 mV drop
00101 = 198 mV drop
00110 = 220 mV drop
00111 = 241 mV drop
01000 = 263 mV drop
01001 = 284 mV drop
01010 = 306 mV drop
01011 = 327 mV drop
01100 = 350 mV drop
01101 = 370 mV drop
01110 = 392 mV drop
01111 = 413 mV drop
10000 = 435 mV drop
10001 = 456 mV drop
10010 = 478 mV drop
10011 = 500 mV drop
10100 = 521 mV drop
10101 = 542 mV drop
10111 = 585 mV drop
11000 = 607 mV drop
11001 = 628 mV drop
11010 = 650 mV drop
11011 = 671 mV drop
11100 = 693 mV drop
11101 = 714 mV drop
11110 = 736 mV drop
11111 = 757 mV drop

3.5 Current Sensing

The system output current can be sensed by using either a low value resistor placed in series with the output or for applications that require the highest possible efficiency the series resistance (DCR) of the inductor.

For applications that use DCR sensing, a resistor in series with a capacitor are placed around the inductor, as shown in Figure 3-1. If the value of R_S and C_S are chosen so the RC time constant matches the inductor time constant, the voltage appearing across C_S will equal the voltage across the DCR and therefore the current flowing through the inductor. Equation 3-3 can be used to select R_S and C_S.

FIGURE 3-1: INDUCTOR CURRENT SENSE FILTER



EQUATION 3-3: CALCULATING FILTER VALUES

$$\frac{L}{DCR} = (R_S \times C_S)$$

Where:

- L is the inductance value of the output inductor
- DCR is the series resistance of the output inductor
- R_S is the current sense filter resistor
- C_S is the current sense filter capacitor

3.5.1 CURRENT SENSE GAIN

The entire current sense path has a fixed gain of 32. Additional gain or attenuation can be added. The amount added is controlled by the CSGSCON register, Register 3-5. The gain added to this current sense signal does not change the +6 dB of current sense gain added before being read by the A/D.

3.5.2 INDUCTOR OR SENSE RESISTOR SELECTION

The DCR of the inductor or the value of the sense resistor are to be selected so the output of the internal current sense amplifier output does not exceed 3.0V at full load current. The internal current sense amplifier has a fixed gain of 32. See Equation 3-4.

EQUATION 3-4: SENSE ELEMENT RESISTANCE

$$R_{SENSE} = \frac{AMP_{VOUT}}{AMP_{GAIN} \times I_{MAX}}$$

Where:

- R_{SENSE} is the resistance of the sense element
- AMP_{VOUT} is the maximum output voltage of the current sense amplifier
- AMP_{GAIN} is the fixed gain of the current sense amplifier
- I_{MAX} is the maximum application load current

3.5.3 MEASURING SYSTEM LOAD CURRENT

The system load current can be measured by the internal ADC. Before being measured by the ADC, the sampled current is gained by a fixed +6 dB. It is recommended that multiple ADC readings of the sampled current be taken and averaged together to provide a more uniform measurement.

REGISTER 3-5: CSGSCON: CURRENT SENSE GAIN CONTROL REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	CSGS4	CSGS3	CSGS2	CSGS1	CSGS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **CSGS<4:0>:** Current Sense Gain Setting bits

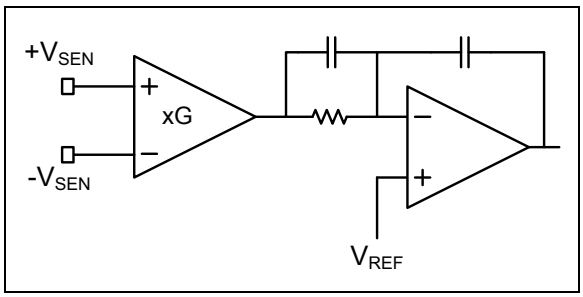
000000 = -3.0 dB
000001 = -2.8 dB
000010 = -2.6 dB
000011 = -2.4 dB
000100 = -2.2 dB
000101 = -2.0 dB
000110 = -1.8 dB
000111 = -1.6 dB
001000 = -1.4 dB
001001 = -1.2 dB
001010 = -1.0 dB
001011 = -0.8 dB
001100 = -0.6 dB
001101 = -0.4 dB
001110 = -0.2 dB
001111 = 0.0 dB
010000 = 0.2 dB
010001 = 0.4 dB
010010 = 0.6 dB
010011 = 0.8 dB
010100 = 1.0 dB
010101 = 1.2 dB
010110 = 1.4 dB
010111 = 1.6 dB
011000 = 1.8 dB
011001 = 2.0 dB
011010 = 2.2 dB
011011 = 2.4 dB
011100 = 2.6 dB
011101 = 2.8 dB
011110 = 3.0 dB
011111 = 3.2 dB

3.6 Control Parameters

3.6.1 COMPENSATION SETTING

The MCP19122/3 is an emulated current mode controller with integrated compensation. The desired response of the overall loop can be tuned by proper placement of the compensation zero frequency and gain. The CMPZCON register, Register 3-6, is used to adjust the compensation zero frequency and gain. Figure 3-2 shows a simplified drawing of the internal compensation with and the adjustable gain differential amplifier.

FIGURE 3-2: SIMPLIFIED COMPENSATION



REGISTER 3-6: CMPZCON: COMPENSATION SETTING CONTROL REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
CMPZF3	CMPZF2	CMPZF1	CMPZF0	CMPZG3	CMPZG2	CMPZG1	CMPZG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **CMPZF<3:0>:** Compensation Zero Frequency Setting bits
0000 = 1500 Hz
0001 = 1850 Hz
0010 = 2300 Hz
0011 = 2840 Hz
0100 = 3460 Hz
0101 = 4300 Hz
0110 = 5300 Hz
0111 = 6630 Hz
1000 = 8380 Hz
1001 = 9950 Hz
1010 = 12200 Hz
1011 = 14400 Hz
1100 = 18700 Hz
1101 = 23000 Hz
1110 = 28400 Hz
1111 = 35300 Hz

bit 3-0 **CMPZG<3:0>:** Compensation Gain Setting bits
0000 = 30.13 dB
0001 = 27.73 dB
0010 = 24.66 dB
0011 = 22.41 dB
0100 = 20.08 dB
0101 = 17.78 dB
0110 = 15.42 dB
0111 = 13.06 dB
1000 = 10.75 dB
1001 = 8.30 dB
1010 = 6.02 dB
1011 = 3.52 dB
1100 = 1.21 dB
1101 = –1.41 dB
1110 = –3.74 dB
1111 = –6.02 dB