Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MCP19214/5

Digitally Enhanced Power Analog, Dual Channel, Low-Side PWM Controller

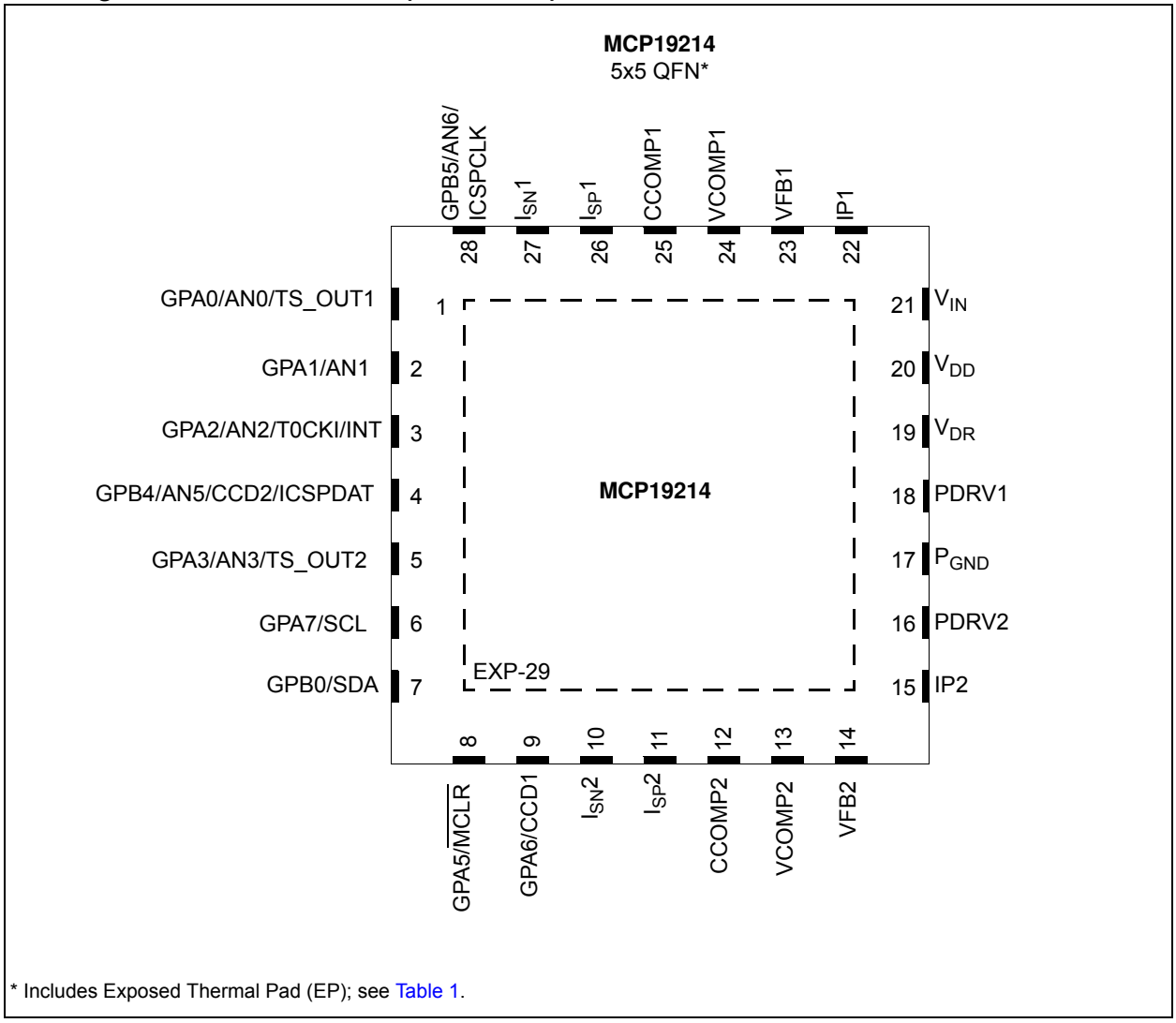
Features

- AEC Q100 Qualified and PPAP Capable
- Input Voltage Range: 4.5V-42V
- Two Independent High-Performance PWM Controllers
- Two Independent Control Loops per Channel allowing the User to Simultaneously Control the Output Voltage and Current
- Can Be Configured to Control Multiple Topologies including but Not Limited To:
  - Boost
  - Flyback
  - Ćuk
  - Single-Ended Primary-Inductor Converter (SEPIC)
- Peak Current Mode Control
- Master/Slave Operation of the PWM Controllers with Adjustable Phase Shift
- Differential Output Current Sense Capability
- Integrated Low-Side Current Sense Differential Amplifier (10X)
- Integrated Low-Side Gate Drivers:
  - 0.5A Sink/Source Current Capability at 5V Supply Voltage
  - 1A Sink/Source Current Capability at 10V Supply Voltage
- Special Events Generator (the state of regulating loops can be monitored without firmware overhead)
- Configurable Parameters:
  - Reference Voltages for Regulating Loops (four internal DACs)
  - Input Undervoltage Lockout (UVLO)
  - Input Overvoltage Lockout (OVLO)
  - Primary Current Leading Edge Blanking: 0 ns, 50 ns, 100 ns and 200 ns
  - Fixed Switching Frequency Range: 31.25 kHz-2.0 MHz
  - Slope Compensation
  - Primary Current Sense Offset Adjustment
  - Configurable GPIO Pin Options
- Low Quiescent Current: 10 mA Typical
- Low Sleep Current: 120 µA Typical
- Thermal Shutdown

Microcontroller Features

- Precision 8 MHz Internal Oscillator Block:
  - Factory-Calibrated to ±1%, Typical
- Interrupt-Capable
  - Firmware
  - Interrupt-on-Change Pins
- Only 35 Instructions to Learn
- 8192 Words On-Chip Program Memory
- 336 bytes of Internal RAM
- High-Endurance Flash:
  - 100,000 Write Flash Endurance
  - Flash Retention: > 40 Years
- Watchdog Timer (WDT) with Independent Oscillator for Reliable Operation
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- Up to 12 I/O Pins and One Input-Only Pin
- Analog-to-Digital Converter (ADC):
  - 10-Bit Resolution
  - Internal 4096 mV Precision Reference Generator
  - Up to 8 External Channels
- Timer0: 8-Bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - 16-bit Timer with Prescaler
  - Two Selectable Clock Sources
- Timer2: 8-Bit Timer with Prescaler
  - 8-Bit Period Register
- I^2C Communication:
  - 7-bit Address Masking
  - Two Dedicated Address Registers
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART) (only MCP19215):
  - 8 and 9-Bit Data Operations
  - Address Detect
  - Asynchronous and Synchronous Operating Modes

Pin Diagram – 28-Pin 5x5 QFN (MCP19214)



* Includes Exposed Thermal Pad (EP); see Table 1.

TABLE 1: 28-PIN QFN (MCP19214) SUMMARY

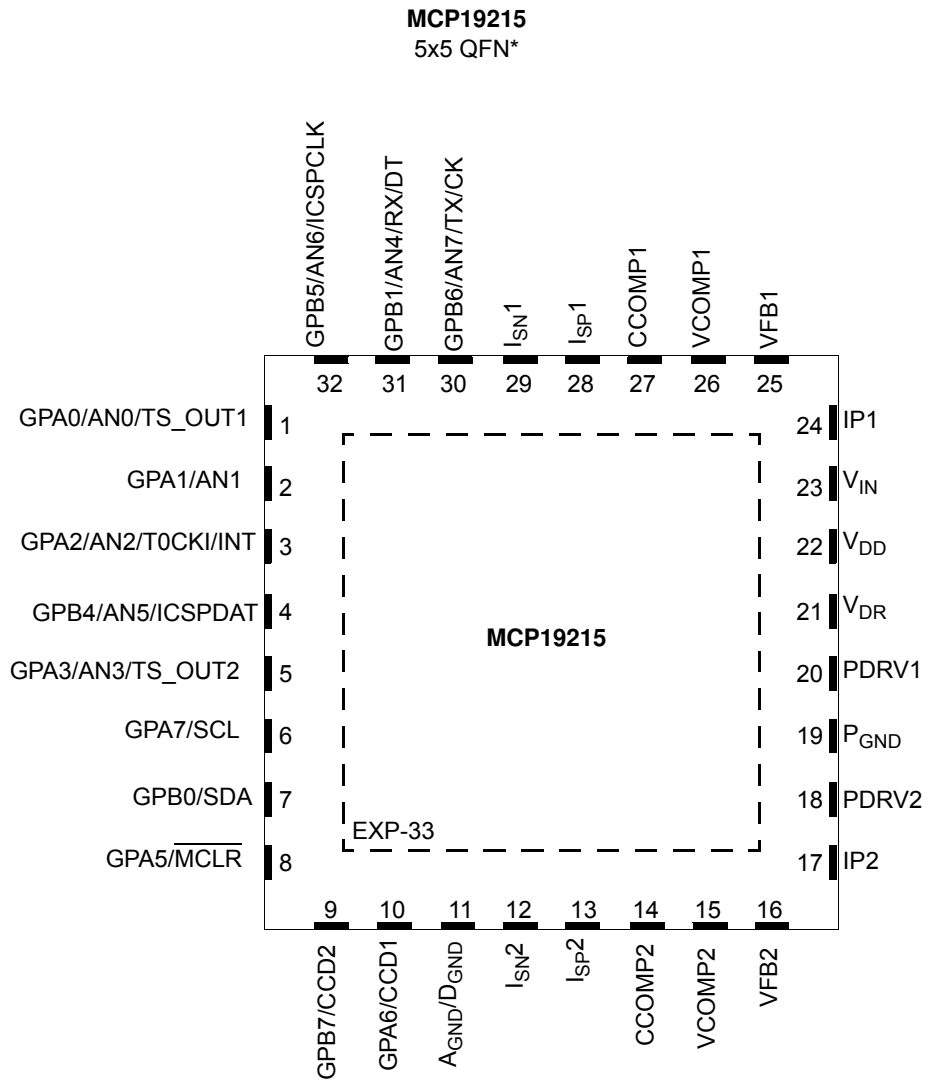
I/O	28-Pin QFN	ANSEL	A/D	Timers	MSSP	AUSART	Interrupt	Pull-Up	Basic	Additional
GPA0	1	Y	AN0	—	—	—	IOC	Y	—	Analog Circuitry Debug Out(1)
GPA1	2	Y	AN1	—	—	—	IOC	Y	—	—
GPA2	3	Y	AN2	T0CKI	—	—	IOC INT	Y	—	—
GPB4	4	Y	AN5	—	—	—	IOC	Y	—	Dual Capture/Compare Input 2
GPA3	5	Y	AN3	—	—	—	IOC	Y		Digital Circuitry Debug Out(1)
GPA7	6	N	—	—	SCL	—	IOC	Y	ICSPDAT	—
GPB0	7	N	—	—	SDA	—	IOC	Y		—
GPA5	8	N	—	—	—	—	IOC(2)	Y(3)	$\overline{MCLR}$	Test Enable Input
GPA6	9	N	—	—	—	—	IOC	Y	—	Dual Capture/Compare Input 1
$I_{SN}2$	10	—	—	—	—	—	—	—	—	Current Sense Amplifier Negative Input for PWM Channel 2
$I_{SP}2$	11	—	—	—	—	—	—	—	—	Current Sense Amplifier Positive Input for PWM Channel 2
CCOMP2	12	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Current Loop of PWM Channel 2
VCOMP2	13	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Voltage Loop of PWM Channel 2
VFB2	14	—	—	—	—	—	—	—	—	Feedback Input of the Voltage Loop of PWM Channel 2
IP2	15	—	—	—	—	—	—	—	—	Primary Input Current Sense of PWM Channel 2
PDRV2	16	—	—	—	—	—	—	—	—	Gate Drive Output of PWM Channel 2
P_{GND}	17	—	—	—	—	—	—	—	—	Power Ground
PDRV1	18	—	—	—	—	—	—	—	—	Gate Drive Output of PWM Channel 1
V_{DR}	19	—	—	—	—	—	—	—	—	Gate Drive Supply Voltage
V_{DD}	20	—	—	—	—	—	—	—	—	V_{DD} Output (+5V)
V_{IN}	21	—	—	—	—	—	—	—	—	Input Supply Voltage
IP1	22	—	—	—	—	—	—	—	—	Primary Input Current Sense of PWM Channel 1
VFB1	23	—	—	—	—	—	—	—	—	Feedback Input of the Voltage Loop of PWM Channel 1
VCOMP1	24	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Voltage Loop of PWM Channel 1
CCOMP1	25	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Current Loop of PWM Channel 1
$I_{SP}1$	26	—	—	—	—	—	—	—	—	Current Sense Amplifier Positive Input for PWM Channel 1
$I_{SN}1$	27	—	—	—	—	—	—	—	—	Current Sense Amplifier Negative Input for PWM Channel 1
GPB5	28	Y	AN6	—		—	IOC	Y	ICSPCLK	—
EP	29	—	—	—	—		—	—	A_{GND}	Small Signal Ground and Digital Ground

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON1 register.

2: The IOC is disabled when $\overline{MCLR}$ is enabled.

3: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

Pin Diagram – 32-PIN 5X5 QFN (MCP19215)



* Includes Exposed Thermal Pad (EP); see Table 2.

TABLE 2: 32-PIN QFN (MCP19215) SUMMARY

I/O	32-Pin QFN	ANSEL	A/D	Timers	MSSP	AUSART	Interrupt	Pull-Up	Basic	Additional
GPA0	1	Y	AN0	—	—	—	IOC	Y	—	Analog Circuitry Debug Out(1)
GPA1	2	Y	AN1	—	—	—	IOC	Y	—	—
GPA2	3	Y	AN2	T0CKI	—	—	IOC INT	Y	—	—
GPB4	4	Y	AN5	—	—	—	IOC	Y	ICSPDAT	—
GPA3	5	Y	AN3	—	—	—	IOC	Y	—	Digital Circuitry Debug Out(1)
GPA7	6	N	—	—	SCL	—	IOC	Y	—	Dual Capture/Single Compare1 Input
GPB0	7	N	—	—	SDA	—	IOC	Y	—	—
GPA5	8	N	—	—	—	—	IOC(2)	Y(3)	$\overline{MCLR}$	—
GPB7	9	N	—	—	—	—	IOC	Y	—	—
GPA6	10	N	—	—	—	—	IOC	Y	—	—
A_{GND}/D_{GND}	11	—	—	—	—	—	—	—	—	—
$I_{SN}2$	12	—	—	—	—	—	—	—	—	Current Sense Amplifier Negative Input for PWM Channel 2
$I_{SP}2$	13	—	—	—	—	—	—	—	—	Current Sense Amplifier Positive Input for PWM Channel 2
CCOMP2	14	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Current Loop of PWM Channel 2
VCOMP2	15	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Voltage Loop of PWM Channel 2
VFB2	16	—	—	—	—	—	—	—	—	Feedback Input of the Voltage Loop of PWM Channel 2
IP2	17	—	—	—	—	—	—	—	—	Primary Input Current Sense of PWM Channel 2
PDRV2	18	—	—	—	—	—	—	—	—	Gate Drive Output of PWM Channel 2
P_{GND}	19	—	—	—	—	—	—	—	—	Power Ground
PDRV1	20	—	—	—	—	—	—	—	—	Gate Drive Output of PWM Channel 1
V_{DR}	21	—	—	—	—	—	—	—	—	Gate Drives Supply Voltage
V_{DD}	22	—	—	—	—	—	—	—	—	V_{DD} Output (+5V)
V_{IN}	23	—	—	—	—	—	—	—	—	Input Supply Voltage
IP1	24	—	—	—	—	—	—	—	—	Primary Input Current Sense of PWM Channel 1
VFB1	25	—	—	—	—	—	—	—	—	Feedback Input of the Voltage Loop of PWM Channel 1

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON1 register.

2: The IOC is disabled when $\overline{MCLR}$ is enabled.

3: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

TABLE 2: 32-PIN QFN (MCP19215) SUMMARY (CONTINUED)

I/O	32-Pin QFN	ANSEL	A/D	Timers	MSSP	AUSART	Interrupt	Pull-Up	Basic	Additional
VCOMP1	26	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Voltage Loop of PWM Channel 1
CCOMP1	27	—	—	—	—	—	—	—	—	The Output of the Error Amplifier of the Current Loop of PWM Channel 1
$I_{SP}1$	28	—	—	—	—	—	—	—	—	Current Sense Amplifier Positive Input for PWM Channel 1
$I_{SN}1$	29	—	—	—	—	—	—	—	—	Current Sense Amplifier Negative Input for PWM Channel 1
GPB6	30	Y	AN7	—	—	TX/CK	IOC	Y	—	—
GPB1	31	Y	AN4	—	—	RX/DT	IOC	Y	—	—
GPB5	32	Y	AN6	—	—	—	IOC	Y	ICSPCLK	—
EP	33	—	—	—	—	—	—	—	—	—

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON1 register.

2: The IOC is disabled when $\overline{\text{MCLR}}$ is enabled.

3: Weak pull-up always enabled when $\overline{\text{MCLR}}$ is enabled, otherwise the pull-up is under user control.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via e-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our web site at:

www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's web site; **www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

1.0 DEVICE OVERVIEW

The MCP19214/5 devices are highly integrated, digitally enhanced PWM controllers, used for battery chargers, bidirectional converters, LED lighting systems and other low-side switch PWM applications.

These devices feature two independent analog PWM controllers, and the internal architecture is optimized for applications that require precise control of the output parameters. Like the other members of the digitally enhanced PWM controllers family, MCP19214/5 includes a fully programmable microcontroller core and a 10-bit analog-to-digital converter.

Each PWM channel includes two error amplifiers with independent adjustable reference voltage generators, current sense input with programmable leading edge blanking, programmable slope compensation ramp generator, integrated internal programmable oscillator, current sense differential amplifier and an integrated MOSFET driver.

An internal LDO (+5V) is used to power the PIC core, the analog circuitry and to provide 5V externally. This 5V external output can also be used to supply the internal MOSFET drivers. The internal MOSFET drivers have the option to be powered from an external voltage source (up to 10V) in order to accommodate applications that require higher voltages for gate driving.

The MCP19214/5 controllers offer a very high degree of integration, allowing the user to develop complex applications without additional circuitry. Some unique features, like simultaneous control of the converter's output current and voltage, make MCP19214/5 devices ideally suited for battery chargers, LED drivers and bidirectional converters. Additionally, the General Purpose Inputs/Outputs (GPIOs) can be used to drive various switches, to enable/disable additional circuitry, or to indicate a typical state.

The MCP19214 is packaged in a 28-lead 5 mm x 5 mm QFN, and the MCP19215 in a 32-lead 5 mm x 5 mm QFN. The operating input voltage for normal device operation is 4.5V-42V, with an absolute maximum of 44V. The maximum transient voltage is 48V for 500 mS.

Power trains supported by this architecture include, but are not limited to, Boost, Buck-Boost, Flyback, SEPIC and Cuk.

MCP19214/5 integrates an I^2C controller and an Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART) module (only for MCP19215). The user can develop specific communication protocols using the internal interfaces. A PMBus compatible protocol, specific for power converters, can be implemented using the provided I^2C serial bus.

Complete customization of the device operating parameters, start-up or shutdown profiles, protection levels and fault handling procedures are accomplished by firmware that can be developed using Microchip's MPLAB® X Integrated Development Environment. Programming the MCP19214/5 is done using one of Microchip's many in-circuit debugger and device programmers.

FIGURE 1-1: MCP19214/5 SIMPLIFIED INTERNAL BLOCK DIAGRAM

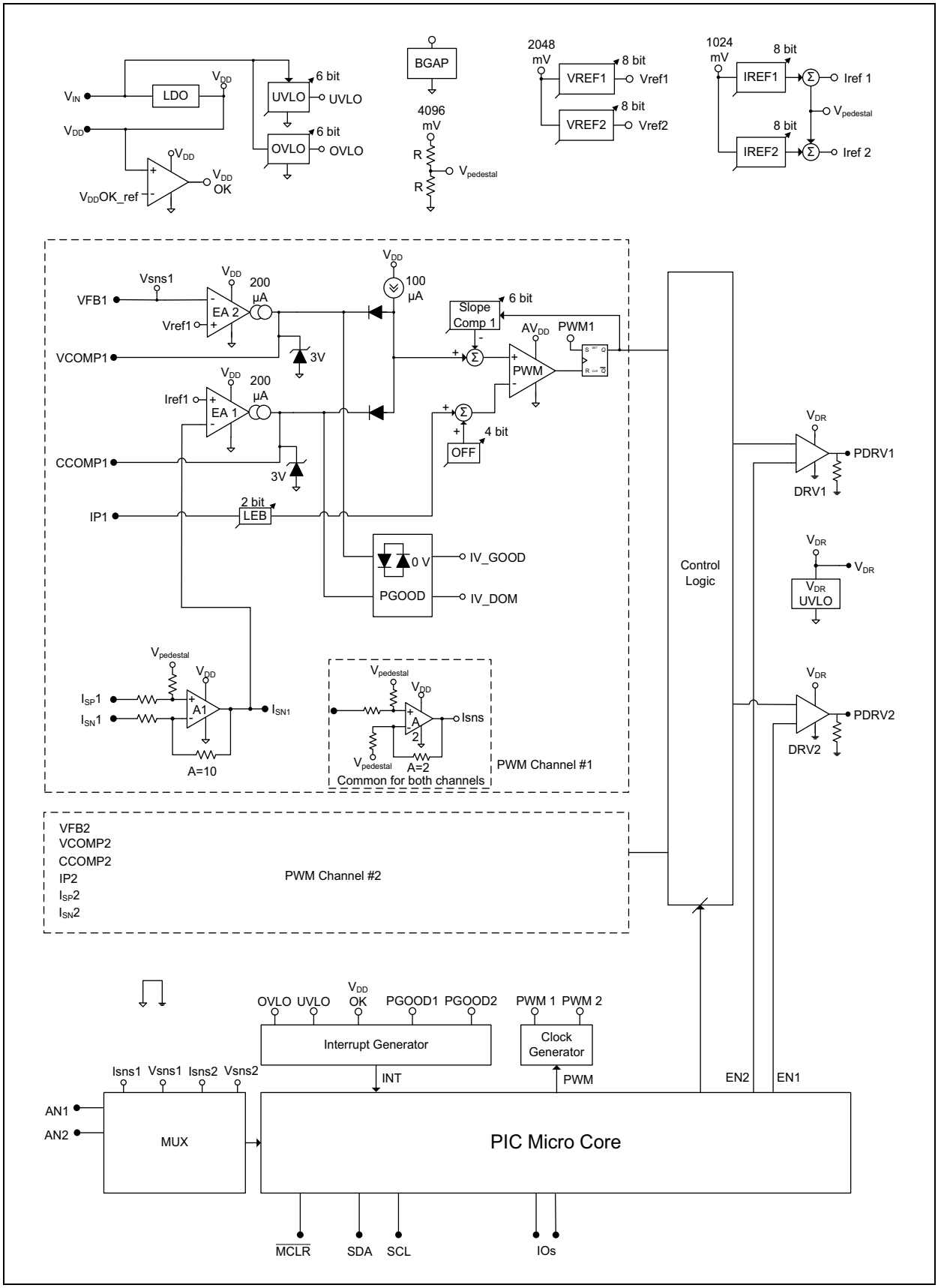


FIGURE 1-2: MCP19214 DUAL LED STRING APPLICATION DIAGRAM

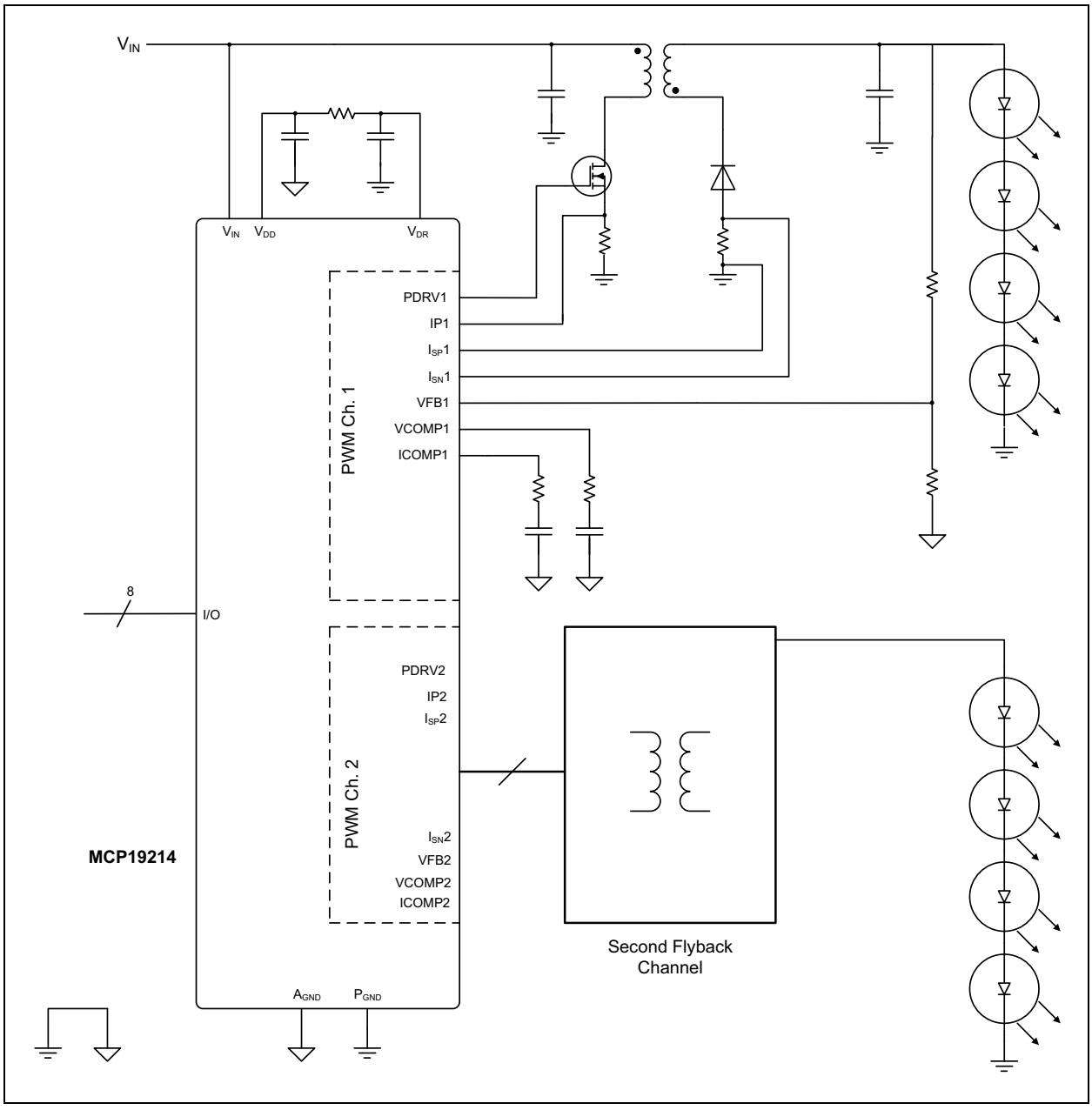


FIGURE 1-3: MCP19214 BIDIRECTIONAL CONVERTER APPLICATION DIAGRAM

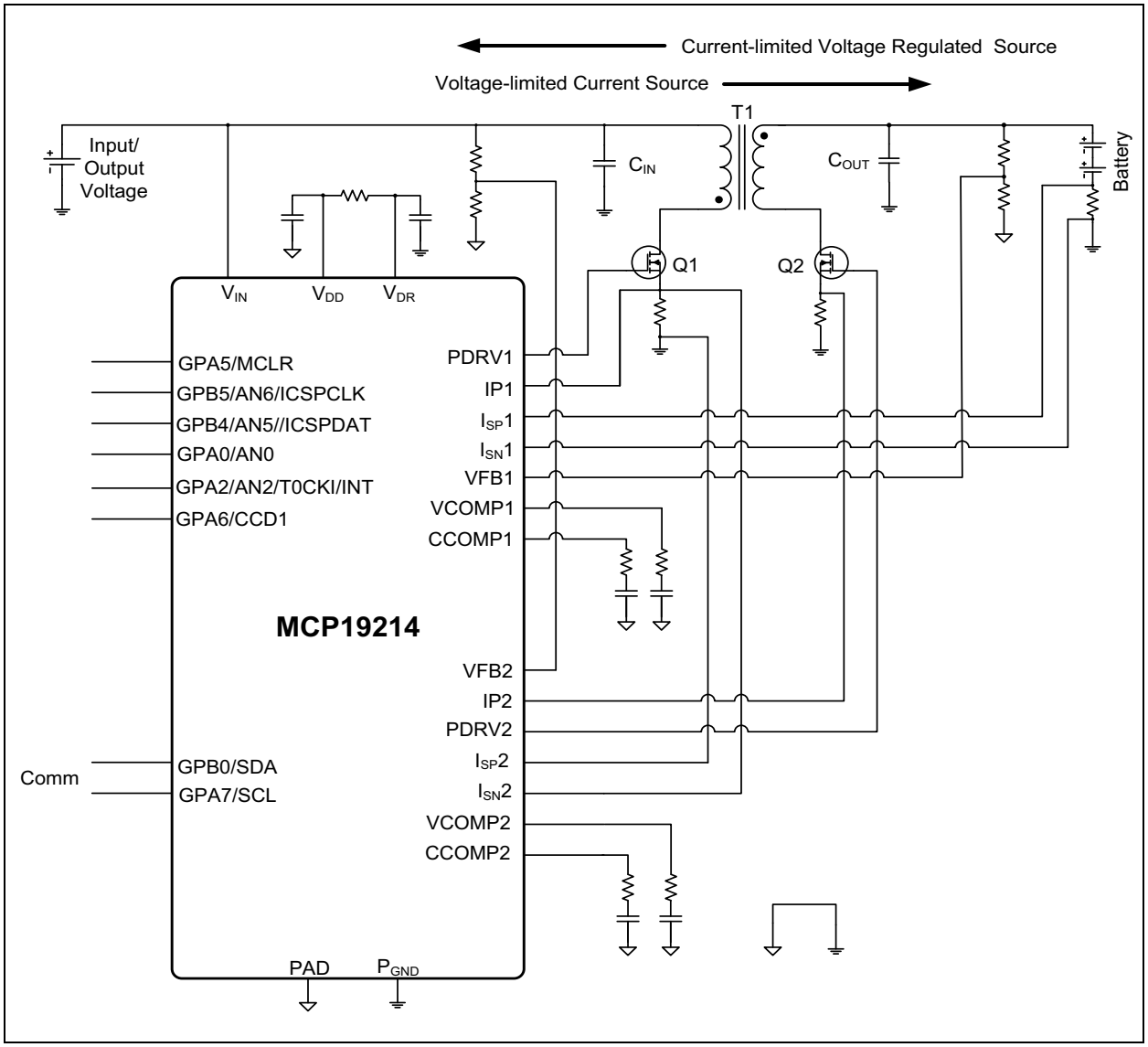
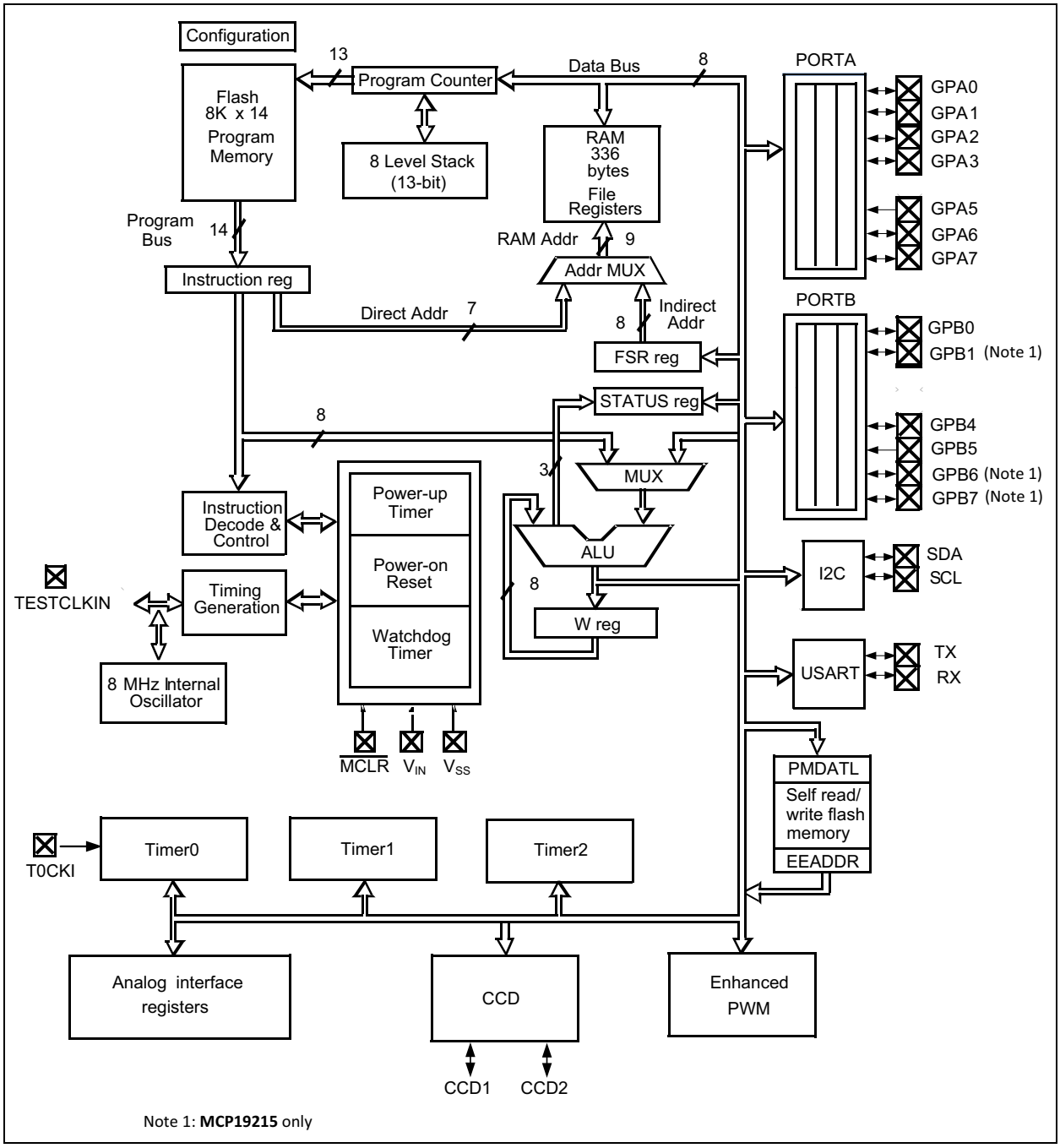


FIGURE 1-4: MICROCONTROLLER CORE BLOCK DIAGRAM



2.0 PIN DESCRIPTION

The 28-lead MCP19214 and 32-lead MCP19215 devices feature pins that have multiple functions associated with each pin. Table 2-1 provides a description of the different functions. Refer to **Section 2.1 "Detailed Pin Functional Description"** for more detailed information.

TABLE 2-1: MCP19214/5 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GPA0/AN0/TS_OUT1	GPA0	TTL	CMOS	General-purpose I/O
	AN0	AN	—	A/D Channel 0 input
	TS_OUT1	—	—	Internal analog signal multiplexer output(1)
GPA1/AN1	GPA1	TTL	CMOS	General-purpose I/O
	AN1	AN	—	A/D Channel 1 input
GPA2/AN2/T0CKI/INT	GPA2	ST	CMOS	General-purpose I/O
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External interrupt
GPA3/AN3/TS_OUT2	GPA3	TTL	CMOS	General-purpose I/O
	AN3	AN	—	A/D Channel 3 input
	TS_OUT2			Internal digital signals multiplexer output(1)
GPA5/$\overline{\text{MCLR}}$	GPA5	TTL	—	General-purpose input only
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
GPA6/CCD1	GPA6	ST	CMOS	General-purpose I/O
	CCD1	ST	CMOS	Single Compare output of PWM channel 1. Dual Capture input of PWM channel 1.
GPA7/SCL	GPA7	ST	CMOS	General-purpose open drain I/O
	SCL	I^2C	OD	I^2C clock
GPB0/SDA	GPB0	TTL	CMOS	General-purpose I/O
	SDA	I^2C	OD	I^2C data input/output
GPB1/AN4/RX/DT (**MCP19215** Only)	GPB1	TTL	CMOS	General-purpose I/O
	AN4	AN	—	A/D Channel 4 input
	RX	ST	—	AUSART asynchronous receive input
	DT	TTL	CMOS	AUSART synchronous data input/output
GPB4/AN5/ICSPDAT	GPB4	TTL	CMOS	General-purpose I/O
	AN5	AN	—	A/D Channel 5 input
	ICSPDAT	ST	CMOS	In-Circuit Debugger and ICSP programming data
GPB5/AN6/ICSPCLK	GPB5	TTL	CMOS	General-purpose I/O
	AN6	AN	—	A/D Channel 6 input
	ISCPCLK	ST	—	In-Circuit Debugger and ICSP programming clock

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON1 register.

TABLE 2-1: MCP19214/5 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
GPB6/AN7/TX/CK (**MCP19215** Only)	GPB6	TTL	CMOS	General-purpose I/O
	AN7	AN	—	A/D Channel 7 input
	TX	—	CMOS	AUSART asynchronous transmit output
	CK	TTL	CMOS	AUSART synchronous clock input/output
GPB7/CCD2 (**MCP19215** Only)	GPB7	TTL	CMOS	General-purpose I/O
	CCD2	ST	CMOS	Single Compare output of PWM channel 2 Dual Capture input of PWM channel 2
V_{IN}	V_{IN}	—	—	Device input supply voltage
V_{DD}	V_{DD}	—	—	Internal +5V LDO output pin
V_{DR}	V_{DR}	—	—	Gate drivers supply voltage
A_{GND}/D_{GND}	A_{GND}	—	—	Small signal quiet ground
P_{GND}	P_{GND}	—	—	Large signal power ground
PDRV1	PDRV1	—	—	Primary PWM channel MOSFET gate drive
PDRV2	PDRV2	—	—	Secondary PWM channel MOSFET gate drive
IP1	IP1	—	—	Primary input current sense for PWM channel 1
IP2	IP2	—	—	Primary input current sense for PWM channel 2
$I_{SN}1$	$I_{SN}1$	—	—	Differential current sense amplifier negative input of PWM channel 1
$I_{SN}2$	$I_{SN}2$	—	—	Differential current sense amplifier negative input of PWM channel 2
$I_{SP}1$	$I_{SP}1$	—	—	Differential current sense amplifier positive input of PWM channel 1
$I_{SP}2$	$I_{SP}2$	—	—	Differential current sense amplifier positive input of PWM channel 2
CCOMP1	CCOMP1	—	—	Output of the current loop error amplifier of PWM channel 1
CCOMP2	CCOMP2	—	—	Output of the current loop error amplifier of PWM channel 2
VCOMP1	VCOMP1	—	—	Output of the voltage loop error amplifier of PWM channel 1
VCOMP2	VCOMP2	—	—	Output of the voltage loop error amplifier of PWM channel 2
VFB1	VFB1	—	—	Feedback input of the voltage loop of PWM channel 1
VFB2	VFB2	—	—	Feedback input of the voltage loop of PWM channel 2
EP				Exposed Pad. The A_{GND} and D_{GND} internal nodes close here. Connect this to the PCBs ground plane using multiple vias.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: The Analog/Digital Debug Output is selected through the control of the ABECON1 register.

2.1 Detailed Pin Functional Description

2.1.1 GPA0 PIN

GPA0 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN0 is an input to the A/D. To configure this pin to be read by the A/D on channel 0, bits TRISA0 and ANSA0 must be set.

The ABECON1/2 registers can be configured to set this pin to the TS_OUT1 function. It is a buffered output of the internal analog signals multiplexer. Analog signals present on this pin are controlled by the ADCON0 register.

2.1.2 GPA1 PIN

GPA1 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN1 is an input to the A/D. To configure this pin to be read by the A/D on channel 1, bits TRISA1 and ANSA1 must be set.

2.1.3 GPA2 PIN

GPA2 is a general-purpose ST input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN2 is an input to the A/D. To configure this pin to be read by the A/D on channel 2, bits TRISA2 and ANSA2 must be set.

When bit T0CS is set in the OPTION_REG register, the T0CKI function is enabled. Refer to **Section 21.0 "Timer0 Module"** for more information.

GPA2 can also be configured as an external interrupt by setting the INTE bit. Refer to **Section 13.2 "GPA2/INT Interrupt"** for more information.

2.1.4 GPA3 PIN

GPA3 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN3 is an input to the A/D. To configure this pin to be read by the A/D on channel 3, bits TRISA3 and ANSA3 must be set.

The ABECON1/2 registers can be configured to set this pin to the TS_OUT2 function. It is a buffered output of the internal digital signals multiplexer. Digital signals present on this pin are controlled by the ABECON2 register.

2.1.5 GPA5 PIN

GPA5 is a general-purpose TTL input only pin. An internal weak pull-up and interrupt-on-change are also available.

For programming purposes, this pin is to be connected to the $\overline{\text{MCLR}}$ pin of the serial programmer. Refer to **Section 32.0 "In-Circuit Serial Programming™ (ICSP™)"** for more information.

This pin is $\overline{\text{MCLR}}$ when the $\overline{\text{MCLR}}$E bit is set in the CONFIG register. When the $\overline{\text{MCLR}}$ is active, the interrupt-on-change is disabled and the weak pull-up is always enabled.

2.1.6 GPA6 PIN

GPA6 is a general-purpose CMOS output ST input pin whose data direction is controlled in TRISGPA.

GPA6 is part of the CCD Module. For more information, refer to **Section 31.0 "Dual Capture/Compare (CCD) Module"**.

2.1.7 GPA7 PIN

GPA7 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

When the MCP19214/5 is configured for I^2C communication, **Section 27.2 "I^2C Mode Overview"**, GPA7 functions as the I^2C clock (SCL). This pin must be configured as an input to allow proper operation.

2.1.8 GPB0 PIN

GPB0 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

When the MCP19214/5 are configured for I^2C communication, **Section 27.2 "I^2C Mode Overview"**, GPB0 functions as the I^2C clock (SDA). This pin must be configured as an input to allow proper operation.

2.1.9 GPB1 PIN **(MCP19215 ONLY)**

GPB1 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN4 is an input to the A/D. To configure this pin to be read by the A/D on channel 4, bits TRISB1 and ANSB1 must be set.

RX is the receiver's input of the AUSART block for asynchronous operation.

DT is the input/output pin of the AUSART block for synchronous operation

2.1.10 GPB4 PIN

GPB4 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN5 is an input to the A/D. To configure this pin to be read by the A/D on channel 5, bits TRISB4 and ANSB4 must be set.

ICSPDAT is the serial programming data I/O function. This is used in conjunction with ICSPCLK to serial program the device. Refer to **Section 32.0 "In-Circuit Serial Programming™ (ICSP™)"** for more information.

2.1.11 GPB5 PIN

GPB5 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN6 is an input to the A/D. To configure this pin to be read by the A/D on channel 6, bits TRISB5 and ANSB5 must be set.

ICSPCLK is the serial programming/debugging clock function. This is used in conjunction with ICSPDAT to serial program the device. Refer to **Section 32.0 "In-Circuit Serial Programming™ (ICSP™)"** for more information.

2.1.12 GPB6 PIN **(MCP19215 ONLY)**

GPB6 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN7 is an input to the A/D. To configure this pin to be read by the A/D on channel 7, bits TRISB6 and ANSB6 must be set.

TX is the transmitter's output of the AUSART block during asynchronous operation.

CK is the input/output clock of the AUSART block during synchronous operation.

2.1.13 GPB7 PIN **(MCP19215 ONLY)**

GPB7 is a general-purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

GPB7 is part of the CCD Module. For more information, refer to **Section 31.0 "Dual Capture/Compare (CCD) Module"**.

2.1.14 V_{IN} PIN

V_{IN} is the input voltage pin of the MCP19214/5 controller. This pin is connected to the input of the +5V internal voltage regulator. A bypass capacitor of minimum 100 nF must be connected between this pin and GND. This capacitor should be physically placed close to the device.

2.1.15 V_{DD} PIN

The output of the internal +5.0V regulator is connected to this pin. It is recommended that a minimum 4.7 µF ceramic bypass capacitor be connected between this pin and the GND pin of the device. The bypass capacitor should be physically placed close to the device.

2.1.16 V_{DR} PIN

The supply for the MOSFET drivers is connected to this pin and has an absolute maximum rating of +13.5V. A decoupling capacitor of 1.0 µF should be placed between this pin and P_{GND} pin. This pin can be connected by an RC filter to the V_{DD} pin.

2.1.17 A_{GND}/D_{GND} PIN **(MCP19215 ONLY)**

A_{GND}/D_{GND} is the small signal ground connection pin. This pin should be connected to a low noise ground.

2.1.18 P_{GND} PIN

This is the large signal ground pin. P_{GND} is the return path for the internal MOSFET drivers. This pin should be connected to the power train ground using short, low impedance connection.

2.1.19 PDRV1 PIN

The output of the internal MOSFET driver of PWM channel 1. Connect this pin to the gate of the power MOSFET using short, low-impedance trace.

2.1.20 PDRV2 PIN

The output of the internal MOSFET driver of PWM channel 2. Connect this pin to the gate of the power MOSFET using short, low-impedance trace.

2.1.21 IP1 PIN

This pin is the primary current sense input of the PWM channel 1. IP1 is connected to the main PWM comparator via a blanking circuit.This input is sensitive to high-frequency noise. Keep the associated trace away from noise sources like the main switch node of the converter or the MOSFET's gate drive signals. It is recommended to insert an RC low-pass filter between this input and the shunt resistor used to sense the inductor's current.

2.1.22 IP2 PIN

This pin is the primary current sense input of the PWM channel 2. IP2 is connected to the main PWM comparator via a blanking circuit.This input is sensitive to high-frequency noise. Keep the associated trace away from noise sources like the main switch node of the converter or the MOSFETs gate drive signals. It is recommended to insert an RC low-pass filter between this input and the shunt resistor used to sense the inductor's current.

2.1.23 $I_{SN}1$ PIN

This pin is the inverting input of the internal differential current sense amplifier of PWM channel 1.

2.1.24 $I_{SN}2$ PIN

This pin is the inverting input of the internal differential current sense amplifier of PWM channel 2.

2.1.25 $I_{SP}1$ PIN

This pin is the noninverting input of the internal differential current sense amplifier of PWM channel 1.

2.1.26 $I_{SP}2$ PIN

This pin is the noninverting input of the internal differential current sense amplifier of PWM channel 2.

2.1.27 CCOMP1

The CCOMP1 pin is the output of the current loop error amplifier of PWM channel 1. The loop's compensation network is connected between this pin and GND. This is a high-impedance node, and the traces associated with this pin must be kept far from the noise sources like the main switch node of the converter or the MOSFET's gate drive signals.

2.1.28 CCOMP2

The CCOMP2 pin is the output of the current loop error amplifier of PWM channel 2. The loop's compensation network is connected between this pin and GND. This is a high-impedance node, and the traces associated with this pin must be kept far from the noise sources like the main switch node of the converter or the MOSFETs gate drive signals.

2.1.29 VCOMP1

The VCOMP1 pin is the output of the voltage loop error amplifier of PWM channel 1. The compensation network is connected between this pin and GND. This is a high-impedance node, and the traces associated with this pin must be kept far from the noise sources like the main switch node of the converter or the MOSFET's gate drive signals.

2.1.30 VCOMP2

The VCOMP2 pin is the output of the voltage loop error amplifier of PWM channel 2. The compensation network is connected between this pin and GND. This is a high-impedance node, and the traces associated with this pin must be kept far from the noise sources like the main switch node of the converter or the MOSFET's gate drive signals.

2.1.31 VFB1 PIN

The inverting input of the error amplifier of the voltage loop for PWM channel 1. This is a high-impedance input and is sensitive to noise. Keep the trace associated with this pin far from noise sources like the main switch node of the converter or MOSFETs gate drive signals.

2.1.32 VFB2 PIN

The inverting input of the error amplifier of the voltage loop for PWM channel 2. This is a high-impedance input and is sensitive to noise. Keep the trace associated with this pin far from noise sources like the main switch node of the converter or MOSFET's gate drive signals.

2.1.33 EXPOSED PAD (EP)

This pad should be connected to a solid ground plane using multiple vias.The connection must provide low thermal impedance as well as low electrical noise. In case of MCP19214, this pad is associated with analog and digital internal grounds (A_{GND}/D_{GND}).

3.0 FUNCTIONAL DESCRIPTION

3.1 Linear Regulator

The operating input voltage for the MCP19214/5 devices ranges from 4.5V-42V. The internal 5V LDO provides bias voltage for the microcontroller core and for the analog circuitry. The output of this LDO can be used for bias additional external low-power circuitry, as well as for the integrated MOSFET drivers. Care should be exercised to avoid an overload of the LDO. The output of this LDO is monitored using a comparator and a specific interrupt is generated in case of malfunction. The thresholds of this comparator are adjustable. Bits that control the functionality of the V_{DD} UVLO comparator are located in the VDDCON register.

In order to minimize the current consumption during Sleep mode, the output voltage of the LDO can be adjusted in two steps: 3V and 5V (typical). There are also two operating modes during sleep: Normal mode and Low-Power mode. Bits that control the functionality of the LDO during Sleep mode are located in PE1 register.

The MCP19214/5 also incorporate a brown-out protection. Refer to **Section 12.3 "Brown-out Reset (BOR)"** for details. The PIC core will reset at 2.0V V_{DD}.

3.2 Output Drive Circuitry

The MCP19214/5 integrates two low-side drivers, one per PWM channel used to drive the external low-side N-Channel power MOSFETs. MCP19214/5 directly controls only topologies that involve low-side MOSFET drivers like boost, buck-boost, flyback, SEPIC or Cuk. For topologies that require high-side MOSFET drive (e.g., buck or synchronous buck) an external, specialized MOSFET driver can be used.

The gate drive (V_{DR}) can be supplied from 5V-10V. The drive strength is capable of up to 1A sink/source with 10V gate drive and down to 0.5A sink/source with 5V gate drive. The supply voltage of the MOSFET drivers is monitored by a UVLO circuit in order to prevent damage to the external power switches. The MOSFET driver's UVLO circuit has two thresholds: 2.7V and 5.4V (typical).

Each driver has its own enable bit, controlled by the microcontroller core. These bits are located in PE1 register.

3.3 PWM Controller

MCP19214/5 integrates two independent PWM controllers. Each PWM channel comprises a set of two error amplifiers with independent reference voltage generators, a PWM comparator with latched output, a current sense input with adjustable leading-edge blanking time, and a ramp generator for slope compensation. See Figure 3-1 for details.

The error amplifiers are of transconductance type (OTA) with separate, external compensation network connected between the output and the ground (A_{GND}). The outputs of the OTAs are tied together through diodes in order to allow the simultaneous control of the output voltage and current. The typical sink current is 200 uA. This type of amplifier makes possible the usage of high-valued resistors for the feedback divider without affecting the frequency response of the amplifier, as these resistors are out of the compensation loop. Only one inverting input is accessible outside the chip (VFBx), the other being internally connected to the output of the 10X differential amplifier. The error signal is clamped at a certain level (3V, typical) in order to prevent overcurrent in the main switching MOSFET of the converter.

The output of the error amplifiers (CCOMP and VCOMP) are equipped with switches (S1 and S2 in Figure 3-1) in order to reset the compensation networks before the soft start or before the activation of a certain loop. These switches are under the software control (VLRES and CLRES bits), and it is the responsibility of the user to ensure proper operation.

The internal 10X differential amplifier is used to improve the accuracy of the current regulated loops and reduce the power dissipation in the external current sensing element (shunt).

A second amplifier (common for both PWM channels) with a gain of 2X is connected between the ADC input and the output of the 10X amplifier. This second amplifier increases the dynamic range of the current measurement circuitry.

In order to prevent any inherent errors that may occur when the output of the amplifier goes near ground or input rail, a special circuit centers the common mode voltage at a specified level (pedestal voltage, typical 2.048V). This technique allows the microcontroller core to read the current in both directions (as with the bidirectional converters): the forward direction when the converter charges the battery, and the reverse direction when the converter delivers constant output voltage from the battery. The output of the 10X differential amplifier as well as the output of the second 2X amplifier will be at the pedestal voltage if the sensed current is zero. The same pedestal voltage is added tothe value of the reference voltage generator of the current loop in order to compensate the DC offset introduced by the pedestal voltage. The 2X amplifier output can be connected via the analog multiplexer to the ADC input for current monitoring purposes (Isnsx signal). The pedestal voltage is fixed at 2.048V.

The loop implements the Peak Current mode control. The IPx input is used to sense the inductor's current. A leading-edge blanking circuit (LEB) is used to prevent false reset of the PWM circuitry. The LEB can be set to four steps (0 ns, 50 ns, 100 ns and 200 ns). The blank time is controlled from the ICLEBCON register. External resistor capacitor filtering techniques can still be used to filter the leading edge if desired. An adjustable offset voltage generator is used to add a certain amount of DC offset (programmable) on top of the IPx signal. This offset prevents the effects of the nonlinearities associated with the error amplifiers outputs at very low-voltage levels, and can also be used for overcurrent protection purposes (cycle-by-cycle current limit). This offset adjustment is controlled by the ICOACON register.

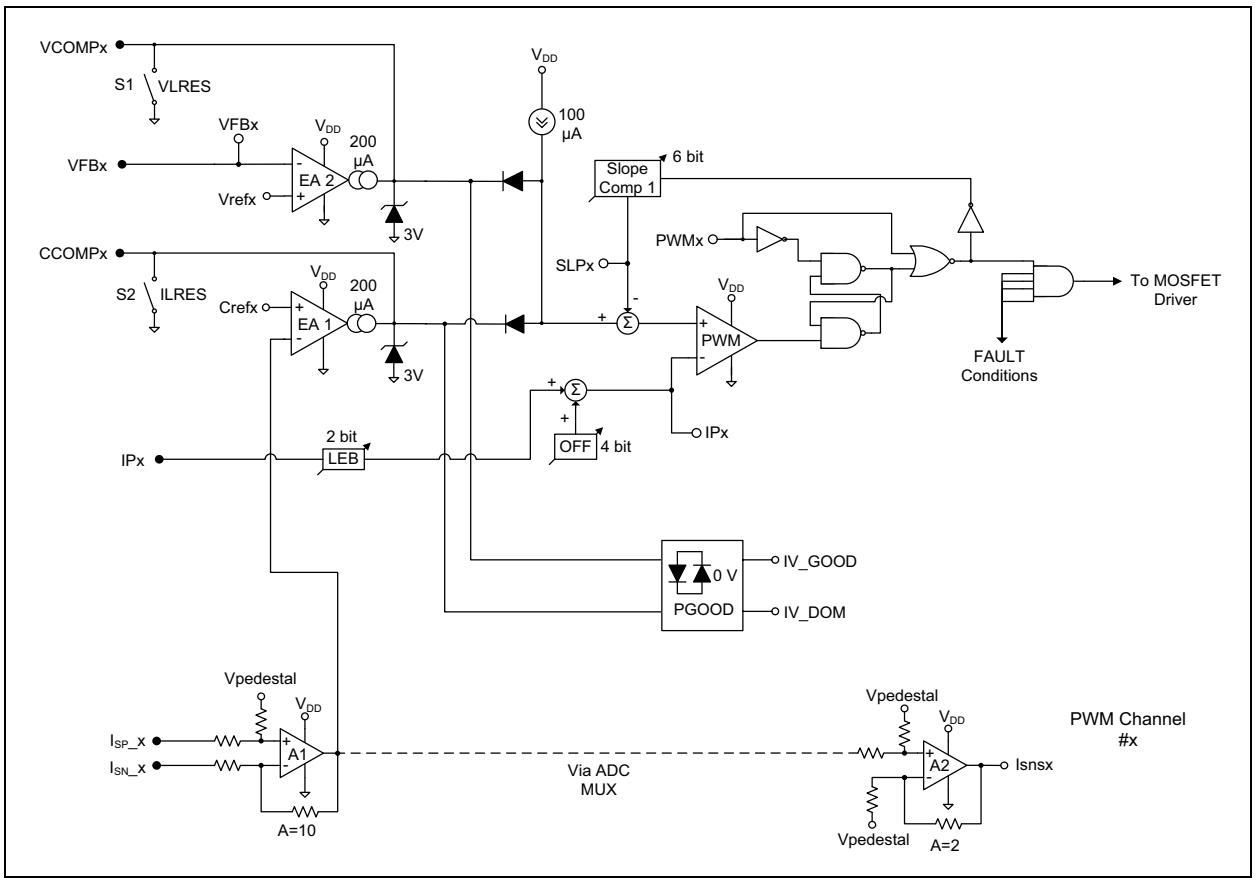
The Peak Current mode control requires slope compensation in order to avoid subharmonic oscillations. A programmable (6-bit) ramp generator is provided and its output is subtracted from the error signal.

When the current sense signal reaches the level of the control voltage minus slope compensation, the on cycle is terminated and the external switch is latched off until the beginning of the next cycle, which begins at the next clock cycle.

A S-R Latch (Set-Reset Latch) is used to prevent the PWM circuitry from turning the external switch on until the beginning of the next clock cycle.

In order to avoid severe overshoots of the controlled parameter (current or voltage) when the loop switches between operating modes (constant current or constant voltage), the outputs of the error amplifiers are clamped together.

FIGURE 3-1: THE PWM CONTROLLER BLOCK DIAGRAM



3.4 Current Sense

The output current is differentially sensed by the MCP19214/5. In high-current applications, this helps to maintain high-system efficiency by minimizing power dissipation in current sense resistors. Differential current sensing also minimizes external ground shift errors. The internal differential amplifier has a typical gain of 10 V/V (typical).

3.5 Power Good Circuitry

The Power Good circuitry monitors the outputs of the error amplifiers to detect an open-loop condition. The IV_GOOD signal will generate an interrupt and the PIC core will read the status of the IV_GOOD and IV_DOM bits. The IV_GOOD signal indicates if one of the loops is active, and IV_DOM indicates which loop is dominant. The associated bits are located in LOOPCON1 and LOOPCON2.

3.6 PWM Frequency

The MCP19214/5 device uses a fixed frequency PWM control strategy. Both PWM channels will have the same switching frequency, but the phase difference between them is adjustable. The first PWM channel is considered the master channel, while the second is the slave channel. The user sets the MCP19214/5 switching frequency by configuring the PR2 register. The maximum allowable PDRVx duty cycle is adjustable and is controlled by the PWMRL register. The programmable range of the switching frequency will be 31.25 kHz to 2 MHz. The available switching frequency below 2 MHz is defined as F_{SW} = 8 MHz/N, where N is a whole number between $4 \leq N \leq 256$. Refer to **Section 24.0 "Enhanced PWM Module"** for details.

3.7 Reference Voltage Generators

There are four internal reference generators, two for each PWM channel. The digital-to-analog converters that control these reference have 8-bit resolution and are controlled by firmware.

The output voltage range of the DACs that set the reference voltage for the voltage loops is 0 mV to 2.048 mV (typical). Thus, the reference voltage of the voltage loops can be adjusted with a step of 8 mV. The associated registers that hold the DAC value are VREFCON1 and VREFCON2.

The output voltage range of the DACs that set the reference voltage for the current loops is 0 mV to 1.024 mV (typical). Thus, the reference voltage of the current loops can be adjusted with a step of 4 mV. The associated registers that hold the DAC value are CREFCON1 and CREFCON2.

3.8 Start-Up

To control the output current during start-up, the MCP19214/5 has the capability to monotonically increase system voltage or current at the user's discretion. This is accomplished through the control of the reference voltage DACs for each control loop. The entire start-up profile is under user control via software.

3.9 Temperature Management

3.9.1 THERMAL SHUTDOWN

To protect the MCP19214/5 from overtemperature conditions, a 150°C (typical) junction temperature thermal shutdown has been implemented. When the junction temperature reaches this limit, the device disables the output drivers. In Shutdown mode, both PDRV1 and PDRV1 outputs are disabled and the overtemperature flag (OTIF) is set in the PIR2 register. The internal LDO is also disabled during thermal shutdown phase. When the junction temperature is reduced by 20°C to 130°C (typical), the MCP19214/5 can resume normal output drive switching.

3.9.2 TEMPERATURE REPORTING

The MCP19214/5 has a second on-chip temperature monitoring circuit that can be read by the ADC through the analog test MUX. Refer to **Section 25.0 "Internal Temperature Indicator Module"** for details on this internal temperature monitoring circuit.

4.0 ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS †

V_{IN} - V_{GND} (operating) ..... –0.3V to +44V
V_{IN} (transient < 500 ms) ..... +48V
PDRVx ..... (GND - 0.3V) to (V_{DR} + 0.3V)
V_{DD} Internally Generated ..... +6.5V
V_{DR} Externally Generated ..... +13.5V
Voltage on $\overline{MCLR}$ with respect to GND ..... –0.3V to +13.5V
Maximum voltage: any other pin ..... +(V_{GND} - 0.3V) to (V_{DD} + 0.3V)
Maximum output current sunk by any single I/O pin ..... 25 mA
Maximum output current sourced by any single I/O pin ..... 25 mA
Maximum current sunk by all GPIO ..... 90 mA
Maximum current sourced by all GPIO ..... 35 mA
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature ..... +150°C
Operating Junction Temperature ..... –40°C to +125°C
ESD protection on all pins (CDM) ..... 2.0 kV
ESD protection on all pins (HBM) ..... 1.0 kV
ESD protection on all pins (MM) 100V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.2 Electrical Characteristics

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 300 kHz, T_A = +25°C, **Boldface** specifications apply over the T_A range of –40°C to +125°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Input Voltage	V_{IN}	**4.5**	—	**42**	V	Steady State
Input Quiescent Current	I_Q	—	6	**10**	mA	Not Switching, Analog circuitry disabled
Shutdown Current	I_{SHDN}	—	110	**400**	µA	Depends on the selected mode; see **Section 19.0 “Power-Down Mode (Sleep)”**
Linear Regulator V_{DD}						
Internal Circuitry Bias Voltage	V_{DD}	**4.75**	5.0	**5.25**	V	V_{IN} = 6.0V to 42V
Maximum External V_{DD} Output Current	I_{DD_OUT}	**35**	—	—	mA	V_{IN} = 6.0V to 42V, V_{DD} = 5.0V, (**Note 1**)
Line Regulation	$\Delta V_{DD-OUT}/(V_{DD-OUT}*\Delta V_{IN})$	—	0.02	**0.1**	%/V	(V_{DD} + 1.0V) ≤ V_{IN} ≤ 20V (**Note 1**)
Load Regulation	$\Delta V_{DD-OUT}/V_{DD-OUT}$	**-1**	±0.1	**+1**	%	I_{DD_OUT} = 1 mA to 35 mA (**Note 1**)
Output Short Circuit Current	I_{DD_SC}	—	60	**90**	mA	V_{IN} = (V_{DD} + 1.0V) (**Note 1**)

Note 1: V_{DD} is the voltage present at the V_{DD} pin.

2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

3: Characterized during validation phase, not production tested.

4: The V_{DD} LDO will limit the total source current to less than 90 mA. Each pin individually can source a maximum of 15 mA.

4.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 300 kHz, T_A = +25°C, **Boldface** specifications apply over the T_A range of –40°C to +125°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dropout Voltage	V_{IN} - V_{DD}	—	0.3	**0.6**	V	I_{DD_OUT} = 35 mA, (**Notes 1** and **2**)
Power Supply Rejection Ratio	$PSRR_{LDO}$	40	60	—	dB	f ≤ 1000 Hz, I_{DD_OUT} = 25 mA C_{IN} = 0 µF, C_{DD} = 4.7 µF
Band Gap Voltage	BG	**1.215**	1.23	**1.245**	V	Trimmed at 1.0% tolerance
Input UVLO Voltage DAC						
UVLO Range (***VIN_ON***)	$UVLO_{ON}$	4.0	—	20	V	V_{IN} Falling
UVLO Hysteresis (***VIN_OFF***)	$UVLO_{HYS}$	—	5	—	%	Hysteresis is based upon $UVLO_{ON}$ setting
Resolution	nbits	—	6	—	Bits	Logarithmic DAC
Input UVLO Comparator						
Input Offset Voltage	V_{OS}	—	+/-10	20	mV	Ensure by design
Input-to-Output Delay	TD	—	5	—	µs	100 ns rise time to 1V overdrive on V_{IN}. V_{IN} > UVLO to flag set.
Input OVLO Voltage DAC						
OVLO (V_{IN} Rising) Range (***VIN_ON***)	$OVLO_{ON}$	**8.8**	—	**44**	V	V_{IN} Rising
OVLO Hysteresis (***VIN_OFF***)	$OVLO_{HYS}$	—	5	—	%	Hysteresis is based upon $OVLO_{ON}$ setting
Resolution	nbits	—	6	—	Bits	Logarithmic DAC
Input OVLO Comparator						
Input Offset Voltage	V_{OS}	—	+/-10	20	mV	
Input-to-Output Delay	TD	—	5	—	µs	100 nS rise time to 1V overdrive on V_{IN} V_{IN} > OVLO to flag set
V_{DD} UVLO Comparator						
Input Offset Voltage	V_{OS}	—	20	50	mV	
Input-to-Output Delay	TD	—	5	—	µs	**Note 3**
Voltage Loop Reference DAC(PWM #1/2)						
Resolution	nbits	—	8	—	Bits	Linear DAC
Full Scale Range	FSR	—	2048	—	mV	
Tolerance	$VVREF_{TOL}$	**-2**	+/-1	**+2**	%	Trimmed
Current Loop Reference DAC(PWM #1/2)						
Resolution	nbits	—	8	—	Bits	Linear DAC
Full Scale Range	FSR	—	1024	—	mV	The pedestal voltage is added on top of this voltage
Tolerance	$CVREF_{TOL}$	**-2**	+/-1	**+2**	%	Trimmed

Note 1: V_{DD} is the voltage present at the V_{DD} pin.

2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

3: Characterized during validation phase, not production tested.

4: The V_{DD} LDO will limit the total source current to less than 90 mA. Each pin individually can source a maximum of 15 mA.

4.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 300 kHz, T_A = +25°C, **Boldface** specifications apply over the T_A range of –40°C to +125°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Differential Current Sense Amplifiers (A1)						
Input Offset Voltage	V_{OS}	—	+/-1	+/-2	mV	Trimmed, 6 bits adjustable
Amplifier PSRR	PSRR	60	—	—	dB	V_{CM} = 2V
Voltage Gain	$A1_{VCL}$	**9.5**	10	**10.5**	V/V	V_{CM} = ±0.1V
Low-Level Output	V_{OL}	—	50	—	mV	
Gain Bandwidth Product	GBWP	7	10		MHz	V_{VDD} = 5V
Input Impedance	R_{IN}		20		kΩ	
Common Mode Range	V_{CMR}	GND-0.3	—	2	V	
Common Mode Rejection Ratio	CMRR	30	—	—	dB	**Note 3**
Auxiliary Measuring Amplifier						
Input Offset Voltage	V_{OS}	—	1	**5**	mV	Trimmed
Voltage Gain	V_G	—	1/2	—	V/V	Programmable
Pedestal Voltage						
Pedestal Voltage Level	V_{PD}	**2028**	2048	**2068**	mV	Trimmed, 6 bits
Current loop Error Amplifiers (EA1)						
Input Current Offset	I_{OS}	**–4**	0	**+4**	µA	Trimmed, 4 bits
Error Amplifier PSRR	PSRR	80	—	—	dB	V_{CM} = 2.048V
Common Mode Input Range	V_{CM}	0.8	—	3	V	
Common Mode Rejection Ratio	CMRR	60	—		dB	V_{CM} = 0.8V-2.5V
Transconductance	g_m	**180**	200	**220**	µS	V_{CM} = 0.8V-3V, Trimmed, 4 bits
Gain Bandwidth Product	GBWP	—	3.5	—	MHz	
Low-Level Output	V_{OL}	—	100	—	mV	
Voltage Loop Error Amplifiers (EA2)						
Input Current Offset	I_{OS}	**–4**	0	**+4**	µA	Trimmed, 4 bits
Error Amplifier PSRR	PSRR	80	—	—	dB	V_{CM} = 1.024V
Common Mode Input Range	V_{CM}	0.8	—	3	V	
Common Mode Rejection Ratio	CMRR	60	—	—	dB	V_{CM} = 0.8V to 3V (**Note 3**)
Transconductance	g_m	**180**	200	**220**	µS	V_{CM} = 0.8V to 3.0V, Trimmed, 4 bits
Gain Bandwidth Product	GBWP	—	3.5	—	MHz	
Low-Level Output	V_{OL}	—	100	—	mV	
Peak Current Sense Input						
Maximum Current Sense Signal Voltage	V_{IP_MAX}	—	1.2	1.5	V	

Note 1: V_{DD} is the voltage present at the V_{DD} pin.

2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

3: Characterized during validation phase, not production tested.

4: The V_{DD} LDO will limit the total source current to less than 90 mA. Each pin individually can source a maximum of 15 mA.

4.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 300 kHz, T_A = +25°C, **Boldface** specifications apply over the T_A range of –40°C to +125°C

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PWM Comparator						
Common-Mode Input Voltage Range	V_{CMR}	GND-0.3	—	3	V	
Input-to-Output Delay	TD	—	20	**50**	ns	**Note 3**
Peak Current Leading Edge Blanking						
Resolution	LEB	—	2	—	Bits	
Blanking Time Adjustable Range	LEB_{RANGE}	0	—	200	ns	4 Step Programmable Range (0, 50,100 and 200 ns)
Offset Adjustment (I_P Sense)						
Resolution	OS_{ADJ}	—	4	—	Bits	
Offset Adjustment Range	OS_{ADJ_RANGE}	0		750	mV	
Offset Adjustment Step Size	OS_{ADJ_STEP}	—	50	—	mV	Linear Steps
Adjustable Slope Compensation						
Resolution	SC_{RES}		6		Bits	Log steps
Slope	m	4		437	mV/µs	
Slope Step Size	SC_{STEP}	—	8	—	%	Log Steps
Ramp Set Point Tol	m_{TOL}	—	+/-10	+/-32	%	
V_{DR} UVLO						
V_{DR} UVLO (2.7V V_{DR} Falling)	$V_{DR\_UVLO\_2.7}$	2.6	2.7	2.8	V	
V_{DR} UVLO (2.7 V_{DR} Rising)	$V_{DR\_UVLO\_2.7}$	2.9	3.05	3.2	V	
V_{DR} UVLO (2.7V) Hysteresis	$V_{DR\_UVLO\ 2.7\ HYS}$	300	350	400	mV	
V_{DR} UVLO (5.4V V_{DR} Falling)	$V_{DR\_UVLO\_5.4}$	5.2	5.4	5.6	V	
V_{DR} UVLO (5.4V V_{DR} Rising)	$V_{DR\_UVLO\_5.4}$	5.8	6.1	6.4	V	
V_{DR} UVLO (5.4V) Hysteresis	$V_{DR\_UVLO\ 5.4\ HYS}$	600	700	800	mV	
Output Driver (PDRV 1/2)						
PDRV Gate Drive Source Resistance	$R_{DR\text{-}SCR}$	—	—	**12**	Ω	V_{DR} = 4.5V (**Note 3**)
PDRV Gate Drive Sink Resistance	$R_{DR\text{-}SINK}$	—	—	**12**	Ω	V_{DR} = 4.5V (**Note 3**)
PDRV Gate Drive Source Current	$I_{DR\text{-}SCR}$	— —	0.5 1.0	— —	A	V_{DR} = 5V V_{DR} = 1 0V (**Note 3**)
PDRV Gate Drive Sink Current	$I_{DR\text{-}SINK}$	— —	0.5 1.0	— —	A	V_{DR} = 5V V_{DR} = 10V (**Note 3**)

Note 1: V_{DD} is the voltage present at the V_{DD} pin.

2: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential between V_{IN} and V_{DD}.

3: Characterized during validation phase, not production tested.

4: The V_{DD} LDO will limit the total source current to less than 90 mA. Each pin individually can source a maximum of 15 mA.