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## LIN Transceiver

### Features

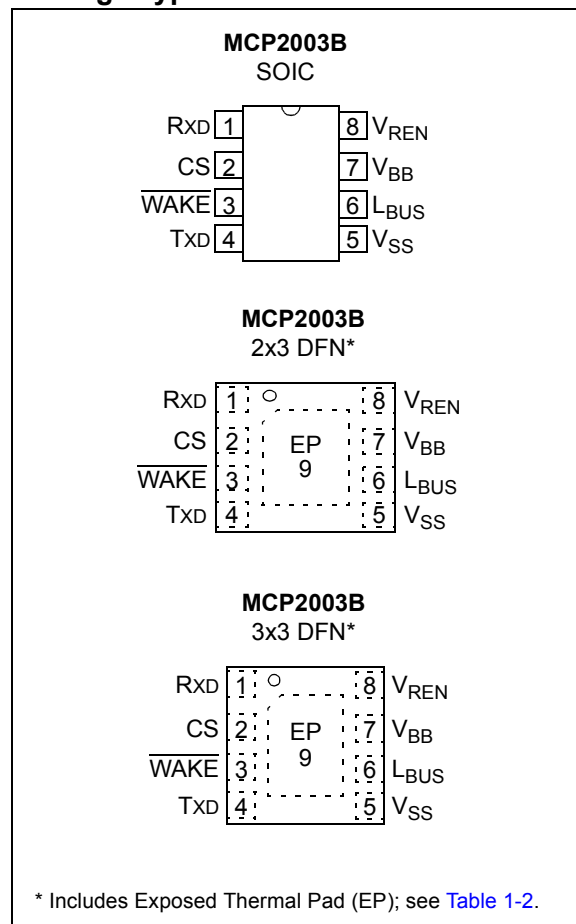
- The MCP2003B is Compliant with Local Interconnect Network (LIN) Bus Specifications 1.3, 2.0, 2.1, 2.2, SAE J2602, and ISO17987
- Supports Baud Rates up to 20 Kbaud with LIN-Compatible Output Driver
- 60V Load Dump Protected
- Very High Electromagnetic Immunity (EMI) Meets Stringent Original Equipment Manufacturers (OEM) Requirements
- Direct Capacitor Coupling Robustness without Transient Voltage Suppressor (TVS):
  - $\pm 35V$  on LBUS (SAE J2962-1)
  - $\pm 85V$  on LBUS (SAE J2962-1)
- High Electrostatic Discharge (ESD) Immunity without TVS:
  - $>25$  kV on LBUS (SAE J2962-1)
  - $>15$  kV on VBB (IEC 61000-4-2)
  - $>6$  kV on LBUS (IEC 61000-4-2)
- Very High Immunity to RF Disturbances Meets Stringent OEM Requirements
- Wide Supply Voltage: 5.5V – 30.0V Continuous
- Extended (E) Temperature Range:  $-40^{\circ}C$  to  $+125^{\circ}C$
- High (H) Temperature Range:  $-40^{\circ}C$  to  $+150^{\circ}C$
- Interfaces to PIC<sup>®</sup> MCU EUSART and Standard USARTs
- LIN Bus Pin:
  - Internal pull-up resistor and diode
  - Protected against battery shorts
  - Protected against loss of ground
  - High current drive:  $>40$  mA
- Automatic Thermal Shutdown
- Low-Power Mode:
  - Receiver monitoring bus and transmitter off: ( $\cong 5 \mu A$ )



### Description

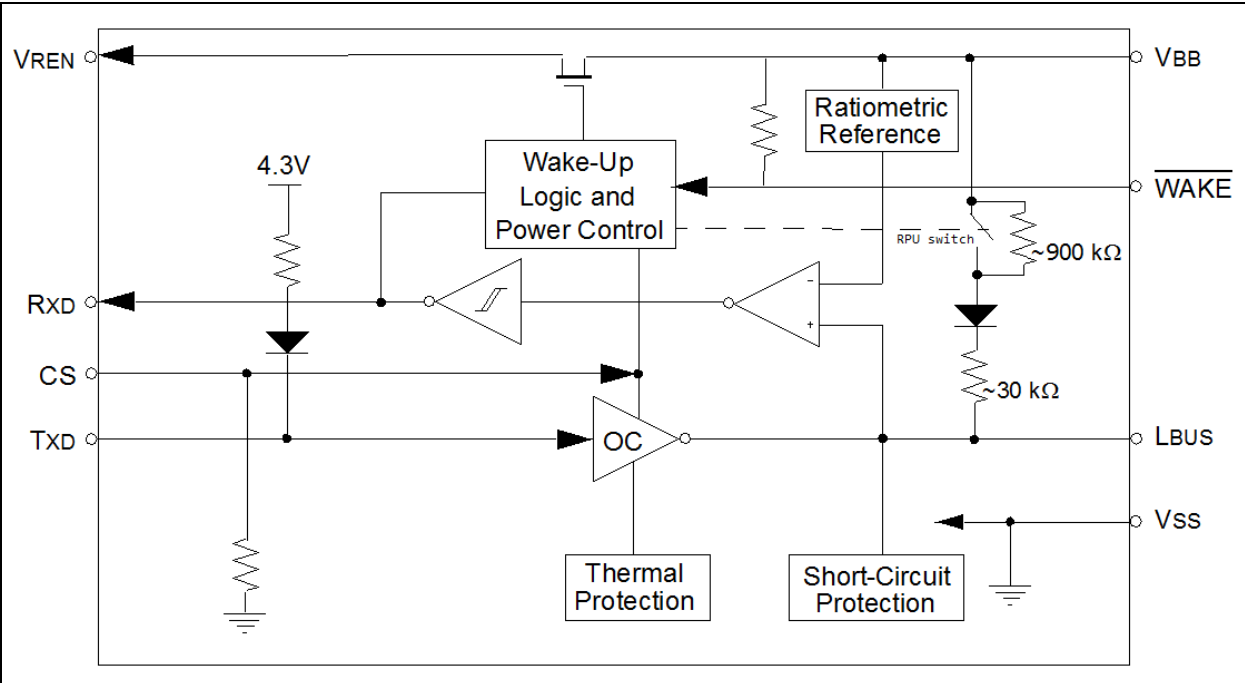
This device provides a bidirectional, half-duplex communication, physical interface to automotive and industrial LIN systems to meet the LIN Bus Specification Revision 2.2, SAE J2602, and ISO 17987. The device is both short-circuit and overtemperature protected by internal circuitry. The device has been specifically designed to operate in the automotive operating environment and will survive all specified transient conditions while meeting all of the stringent quiescent current requirements.

### Package Types



# MCP2003B

MCP2003B Block Diagram



## 1.0 DEVICE OVERVIEW

The MCP2003B devices provide a physical interface between a microcontroller and a LIN bus. These devices will translate the CMOS/TTL logic levels to LIN logic level, and vice versa. It is intended for automotive and industrial applications with serial bus speeds up to 20 Kbaud.

LIN Bus Specification Revision 2.2 requires that the transceiver of all nodes in the system is connected via the LIN pin, referenced to ground and with a maximum external termination resistance load of  $510\Omega$  from LIN bus to battery supply. The  $510\Omega$  corresponds to 1 master and 15 slave nodes.

The VREN pin can be used to drive the logic input of an external voltage regulator. This pin is high in all modes except for Power-Down mode.

### 1.1 External Protection

#### 1.1.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see [Example 1-1](#)).

#### 1.1.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 60V transient suppressor (TVS) diode, between VBB and ground, with a  $50\Omega$  transient protection resistor (RTP) in series with the battery supply and the VBB pin serve to protect the device from power transients (see [Example 1-1](#)) and ESD events. While this protection is optional, it is considered good engineering practice.

## 1.2 Internal Protection

### 1.2.1 ESD PROTECTION

For component-level ESD ratings, please refer to the maximum operation specifications.

### 1.2.2 GROUND LOSS PROTECTION

The LIN Bus specification states that the LIN pin must transition to the recessive state when ground is disconnected. Therefore, a loss of ground effectively forces the LIN line to a high-impedance level.

### 1.2.3 THERMAL PROTECTION

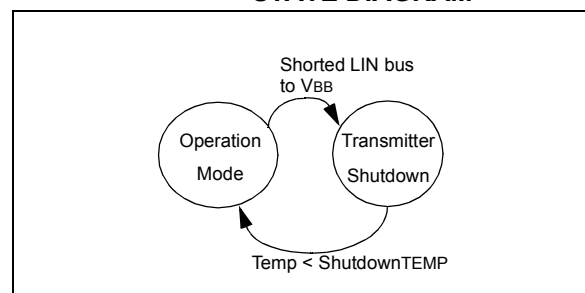
The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter.

There are two causes for a thermal overload. A thermal shutdown can be triggered by either, or both, of the following thermal overload conditions.

- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

Driving the TXD and checking the RXD pin makes it possible to determine whether there is a bus contention (Rx = low, Tx = high) or a thermal overload condition (Rx = high, Tx = low). After a thermal overload event, the device will automatically recover once the die temperature has fallen below the recovery temperature threshold (see [Figure 1-1](#)).

**FIGURE 1-1: THERMAL SHUTDOWN STATE DIAGRAM**



# MCP2003B

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## 1.3 Modes of Operation

For an overview of all operational modes, refer to [Table 1-1](#).

The device will go into Power-Down mode on the falling edge of CS, or return to Operation mode if all faults are resolved.

### 1.3.1 POWER-DOWN MODE

In Power-Down mode, everything is off except the wake-up section. The internal 30 k $\Omega$  pull-up resistor switch is open, which enables the high ohmic pull-up resistor (900 k $\Omega$  typical). This is the lowest power mode. The receiver is off, thus its output is open-drain.

On CS going to a high level or a falling edge on  $\overline{\text{WAKE}}$ , the device will enter Ready mode as soon as internal voltage stabilizes. Refer to [Section 2.4 “AC Specifications”](#) for further information. In addition, LIN bus activity will change the device from Power-Down mode to Ready mode; The MCP2003B wakes up on a rising edge on L<sub>BUS</sub> preceded by a low level lasting at least 70  $\mu\text{s}$  typically. See [Figure 1-2](#) about remote wake-up. If CS is held high as the device transitions from Power-Down to Ready mode, the device will transition to either Operation or Transmitter Off mode, depending on TXD input, as soon as internal voltages stabilize.

### 1.3.2 READY MODE

Transitioning from POR into Ready mode is achieved when  $V_{\text{BB}} > V_{\text{BBUV\_RISE}}$ . Upon entering Ready mode, VREN is enabled and the receiver detect circuit is powered-up. The transmitter remains disabled and the device is ready to receive data but not to transmit.

Upon V<sub>BB</sub> supply pin power-on, the device will remain in Ready mode as long as CS is low. When CS transitions high, the device will either enter Operation mode if the TXD pin is held high, or the device will enter Transmitter Off mode if the TXD pin is held low.

### 1.3.3 OPERATION MODE

In this mode, all internal modules are operational. Note that the part cannot transmit if the pull-up resistance is missing on RX pin. See [Section 1.5.1.1 “RxD Monitoring”](#) for details.

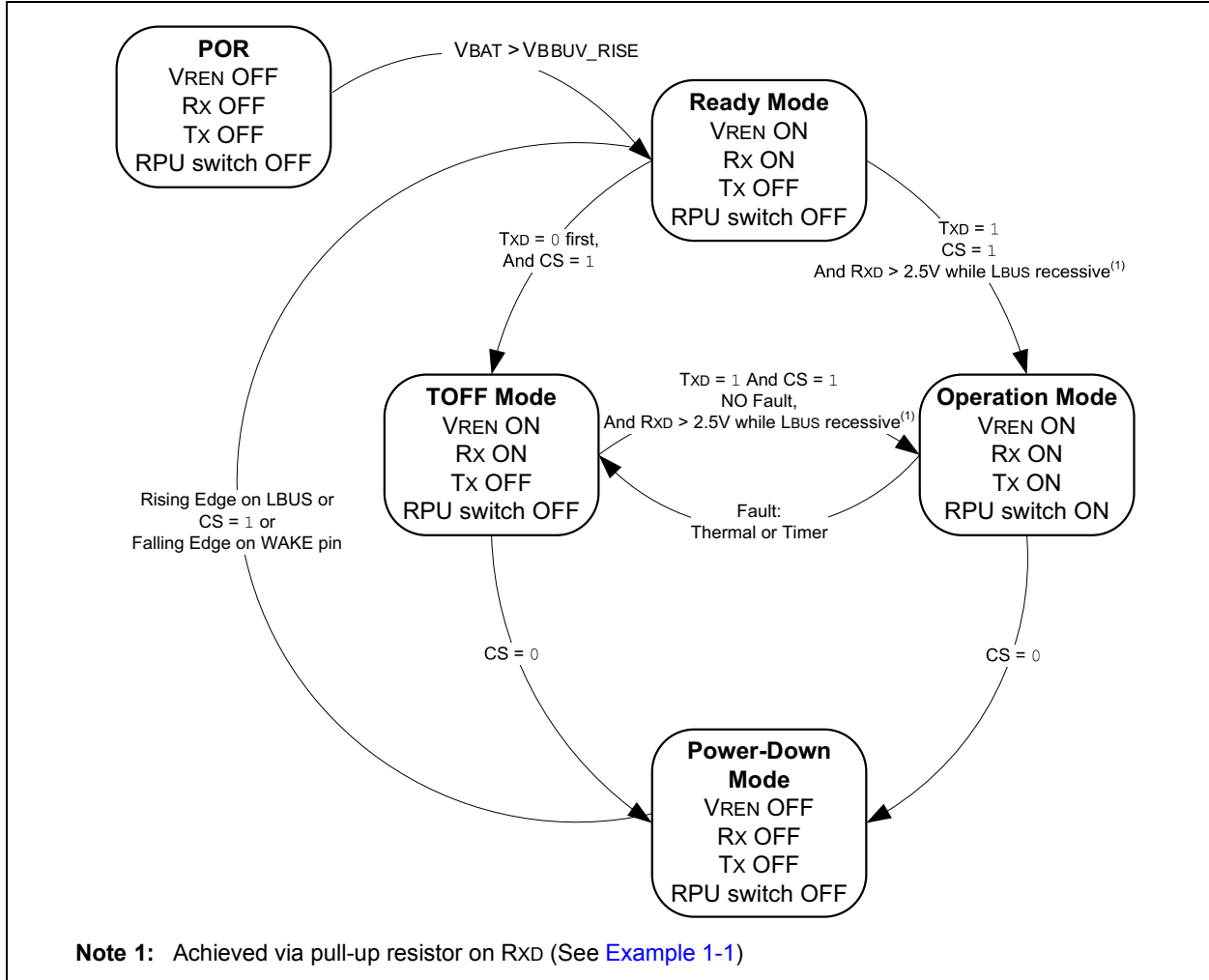
The device will go into Power-Down mode on the falling edge of CS and the TXD pin is held high. The device will enter Transmitter Off mode in the event of a Fault condition such as thermal overload, bus contention or TXD timer expiration.

The V<sub>BB</sub> to L<sub>BUS</sub> ~30 k $\Omega$  pull-up resistor (R<sub>SLAVE</sub>) is connected only in Operation mode.

### 1.3.4 TRANSMITTER OFF MODE

Transmitter Off mode is reached whenever the transmitter is disabled due to a Fault condition. Fault conditions include thermal overload, bus contention, RxD monitoring and TXD timer expiration.

**FIGURE 1-2: OPERATIONAL MODES STATE DIAGRAM – MCP2003B**



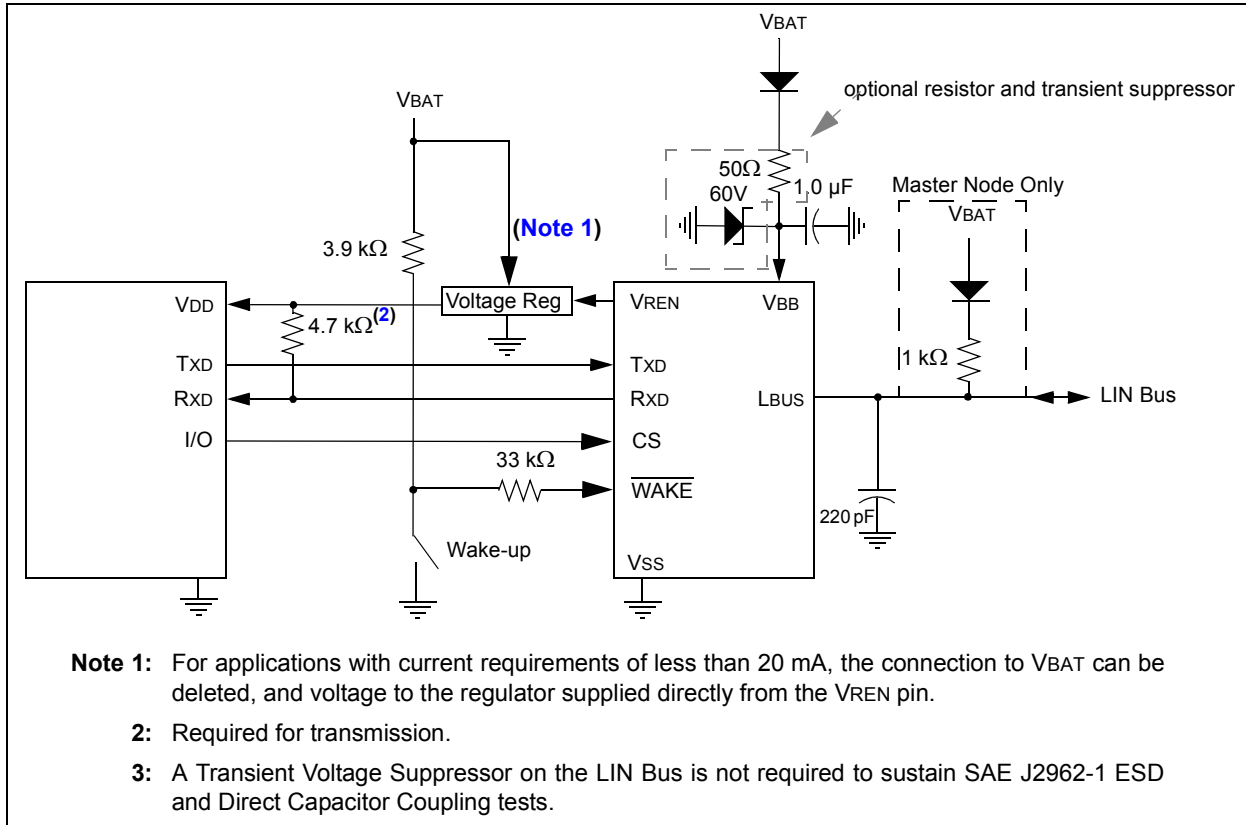
**TABLE 1-1: OVERVIEW OF OPERATIONAL MODES**

State	Transmitter	Receiver	VREN	Operation	Comments
POR	OFF	OFF	OFF	Check CS: if low, then proceed to Ready mode; If high, transition to either TOFF or Operation mode, depending on TXD.	VBB > VBB(MIN) and Internal Supply stable. High ohmic pull-up resistor enabled (900 kΩ typical).
Ready	OFF	ON	ON	On CS high level, proceed to Operation or TOFF mode.	Bus Off state. High ohmic pull-up resistor enabled (900 kΩ typical).
Operation	ON	ON	ON	On CS low level, proceed to Power-Down. On a fault condition, proceed to TOFF mode.	Normal Operation mode. RXD has to be at a high level (>2.5V typical) while LBUS is recessive.
Power-Down	OFF	Activity Detect	OFF	On CS high level, proceed to Ready mode then proceed to either Operation or TOFF mode. Falling edge on WAKE will put the device into Ready mode. Rising edge on LIN bus will put the device into Ready mode.	Low-Power mode. High ohmic pull-up resistor enabled (900 kΩ typical).
Transmitter Off	OFF	ON	ON	On CS low level, proceed to Power-Down mode; On TXD high and no fault condition, proceed to Operation mode.	High ohmic pull-up resistor enabled (900kΩ typical).

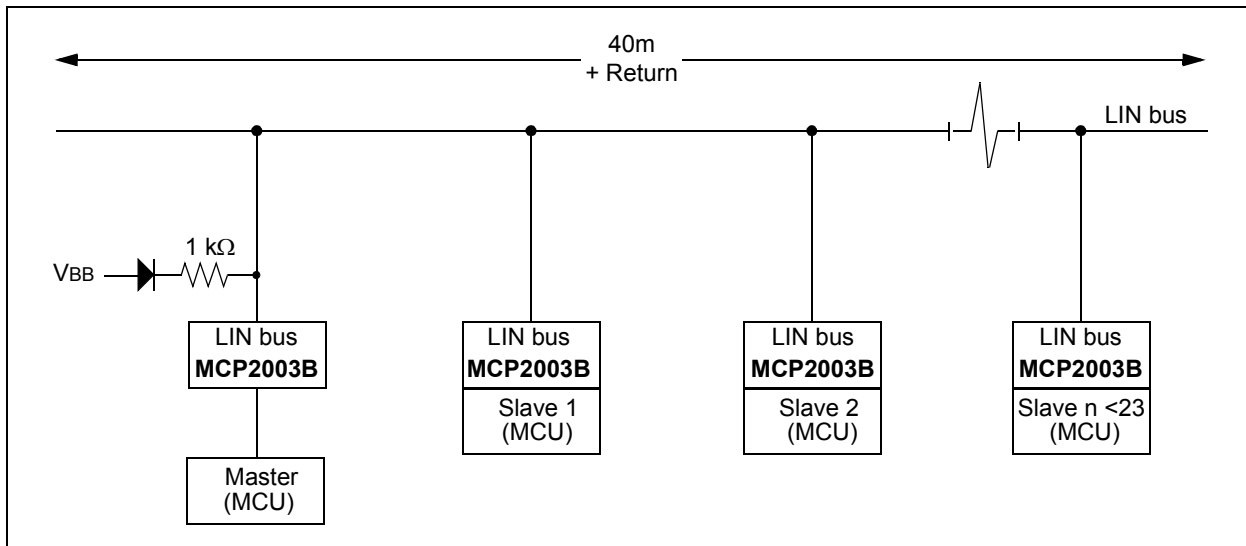
# MCP2003B

## 1.4 Typical Applications

### EXAMPLE 1-1: TYPICAL MCP2003B APPLICATION



### EXAMPLE 1-2: TYPICAL LIN NETWORK CONFIGURATION



## 1.5 Pin Descriptions

**TABLE 1-2: PINOUT DESCRIPTIONS**

Pin Name	8-Lead SOIC	2x3 DFN	3x3 DFN	Normal Operation
RXD	1	1	1	Receive Data Output (OD), HV tolerant
CS	2	2	2	Chip Select (TTL), HV tolerant
$\overline{\text{WAKE}}$	3	3	3	Wake-up, HV tolerant
TXD	4	4	4	Transmit Data Input (TTL), HV tolerant
VSS	5	5	5	Ground
LBUS	6	6	6	LIN Bus (bidirectional)
VBB	7	7	7	Battery Positive
VREN	8	8	8	Voltage Regulator Enable Output
EP	—	9	9	Exposed Thermal Pad. Do not electrically connect or connect to Vss.

**Legend:** TTL = TTL Input Buffer; OD = Open-Drain Output

### 1.5.1 RECEIVE DATA OUTPUT (RXD)

The Receive Data Output pin is an open-drain (OD) output and follows the state of the LIN pin, except in Power-Down mode.

#### 1.5.1.1 RXD Monitoring

The RXD pin is internally monitored. It has to be at a high level (> 2.5V typical) while LBUS is recessive in Operation mode. Otherwise, an internal fault will be created and the device will transition to Transmitter Off mode.

**Note:** A voltage regulator sensing circuit is connected to RXD. This sensing circuit internally monitors the RXD pin when LBUS is recessive (RXD = 1). It will not allow the device to switch (or stay) in Operation Mode if the RXD pin is left open. The RXD pin must be connected to a valid supply through a pull-up resistor as RXD is an open drain pin.

### 1.5.2 CHIP SELECT (CS)

This is the Chip Select Input pin. An internal pull-down resistor will keep the CS pin low. This is done to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-on Reset and an I/O initialization sequence. The pin must detect a high level to activate the transmitter. An internal Low-Pass filter, with a typical time constant of 10  $\mu$ s, prevents unwanted wake-up (or transition to Power-Down mode) on glitches.

If CS = 0 when the VBB supply is turned on, the device goes to Ready mode as soon as internal voltages stabilize, and stays there as long as the CS pin is held low (0). In Ready mode, the receiver is on and the LIN transmitter driver is off.

If CS = 1 when the VBB supply is turned on, the device will proceed to Operation mode, or TXOFF (refer to [Figure 1-2](#)), as soon as internal voltages stabilize.

This pin may also be used as a local wake-up input (refer to [Example 1-1](#)). In this implementation, the microcontroller I/O controlling the CS should be converted to a high-impedance input allowing the internal pull-down resistor to keep CS low. An external switch, or other source, can then wake-up both the transceiver and the microcontroller (if powered). Refer to [Section 1.3 “Modes of Operation”](#), for detailed operation of CS.

**Note:** It is not recommended to tie CS high, as this can result in the device entering Operation mode before the microcontroller is initialized and may result in unintentional LIN traffic. The CS pin is internally pulled down to ground with 190 k $\Omega$  when CS is less than V<sub>IL</sub>, and 2 M $\Omega$  when CS is greater than V<sub>IH</sub>. The current on CS is limited to about 2  $\mu$ A when CS is greater than V<sub>IH</sub>.

### 1.5.3 WAKE-UP INPUT ( $\overline{\text{WAKE}}$ )

The  $\overline{\text{WAKE}}$  pin has an internal 800 k $\Omega$  pull-up to VBB. A falling edge on the  $\overline{\text{WAKE}}$  pin causes the device to wake from Power-Down mode. Upon waking, the MCP2003B will enter Ready mode.

### 1.5.4 TRANSMIT DATA INPUT (TXD)

The Transmit Data Input pin has an internal pull-up. The LIN pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

For extra bus security, TXD is internally forced to '1' whenever the transmitter is disabled, regardless of external TXD voltage.



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## 1.5.4.1 TXD Dominant Timeout

If TXD is driven low for longer than approximately 25 ms, the LBUS pin is switched to Recessive mode and the part enters TOFF Mode. This is to prevent the LIN node from permanently driving the LIN Bus dominant. The transmitter is reenabled on TXD rising edge.

## 1.5.5 GROUND (VSS)

This is the Ground pin.

## 1.5.6 LIN BUS (LBUS)

The bidirectional LIN Bus pin (LBUS) is controlled by the TXD input. LBUS has a current limited open collector output. To reduce EMI, the edges during the signal changes are slope controlled and include corner rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus, and matches the output signal RXD to follow the state of the LBUS pin.

### 1.5.6.1 Bus Dominant Timer

The Bus Dominant Timer is an internal timer that deactivates the LBUS transmitter after approximately 25 ms of dominant state on the LBUS pin. The timer is reset on any recessive LBUS state.

The LIN bus transmitter will be reenabled after a recessive state on the LBUS pin as long as CS is high. Disabling can be caused by the LIN bus being externally held dominant, or by TXD being driven low.

## 1.5.7 BATTERY (VBB)

This is the Battery Positive Supply Voltage pin.

## 1.5.8 VOLTAGE REGULATOR ENABLE OUTPUT (VREN)

This is the External Voltage Regulator Enable pin. Open-drain output is pulled high to VBB in all modes except Power-Down.

## 1.5.9 EXPOSED THERMAL PAD (EP)

Do not electrically connect, or connect to VSS.

## 2.0 ELECTRICAL CHARACTERISTICS

### 2.1 Absolute Maximum Ratings†

V <sub>IN</sub> DC Voltage on RXD, TXD, CS .....	-0.3 to +50V
V <sub>IN</sub> DC Voltage on $\overline{\text{WAKE}}$ and VREN .....	-0.3 to +V <sub>BB</sub>
V <sub>BB</sub> Battery Voltage, continuous, non-operating <sup>(1)</sup> .....	-0.3 to +50V
V <sub>BB</sub> Battery Voltage, non-operating (LIN bus recessive) <sup>(2)</sup> .....	-0.3 to +60V
V <sub>BB</sub> Battery Voltage, transient ISO 7637 Test 1 .....	-200V
V <sub>BB</sub> Battery Voltage, transient ISO 7637 Test 2a .....	+150V
V <sub>BB</sub> Battery Voltage, transient ISO 7637 Test 3a .....	-300V
V <sub>BB</sub> Battery Voltage, transient ISO 7637 Test 3b .....	+200V
V <sub>LBUS</sub> Bus Voltage, continuous .....	-18 to +50V
V <sub>LBUS</sub> Bus Voltage, transient <sup>(3)</sup> .....	-27 to +60V
V <sub>LBUS</sub> Bus Voltage, Direct Capacitor Coupling without TVS (SAE J2962-1) .....	±35V and ±85V
I <sub>LBUS</sub> Bus Short-Circuit Current Limit .....	200 mA
ESD protection on LIN, without TVS (SAE J2962-1) .....	±25 kV
ESD protection on LIN, V <sub>BB</sub> , $\overline{\text{WAKE}}$ (IEC 61000-4-2) <sup>(4)</sup> .....	±6 kV
ESD protection on LIN, V <sub>BB</sub> , $\overline{\text{WAKE}}$ , CS (Human Body Model) <sup>(5)</sup> .....	±8 kV
ESD protection on all other pins (Human Body Model) <sup>(5)</sup> .....	±4 kV
ESD protection on all pins (Charge Device Model) <sup>(6)</sup> .....	±2 kV
ESD protection on all pins (Machine Model) <sup>(7)</sup> .....	±400V
Maximum Junction Temperature .....	+150°C
Storage Temperature .....	-65 to +150°C

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device, at those or any other conditions above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** LIN 2.x compliant specification.

**2:** SAE J2602 compliant specification.

**3:** ISO 7637/1 load dump compliant (t < 500 ms).

**4:** According to IEC 61000-4-2, 330Ω, 150 pF and Transceiver EMC Test Specifications [2] to [4]. For  $\overline{\text{WAKE}}$  pin to meet the specification, series resistor must be in place (refer to [Example 1-2](#)).

**5:** According to AEC-Q100-002/JESD22-A114.

**6:** According to AEC-Q100-011B.

**7:** According to AEC-Q100-003/JESD22-A115.

# MCP2003B

## 2.2 Nomenclature Used in This Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown in [Table 2-1](#).

**TABLE 2-1: EQUIVALENT VALUES**

LIN specifications Name	Term used in the following tables	Definition
VBAT	<i>not used</i>	ECU operating voltage
VSUP	V <sub>BB</sub>	Supply voltage at device pin
IBUS_LIM	I <sub>SC</sub>	Current Limit of driver
VBUSREC	V <sub>IH</sub> (L <sub>BUS</sub> )	Recessive state
VBUSDOM	V <sub>IL</sub> (L <sub>BUS</sub> )	Dominant state

## 2.3 DC Specifications

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for V <sub>BB</sub> = 5.5V to 30.0V Extended (E): TA = -40°C to +125°C High (H): TA = -40°C to +150°C					
	Parameter	Sym.	Min.	Typ.	Max.	Units
<b>Power</b>						
V <sub>BB</sub> Quiescent Operating Current	IBBQ	—	65	150	μA	Operating Mode, bus recessive
		—	—	160	μA	V <sub>BB</sub> > 18V
V <sub>BB</sub> Transmitter-off Current	IBBTO	—	60	120	μA	Transmitter off, bus recessive
		—	—	130	μA	V <sub>BB</sub> > 18V
V <sub>BB</sub> Power-Down Current	IBBPD	—	6	15	μA	
		—	—	20	μA	V <sub>BB</sub> > 18V
		—	14	20	μA	LIN bus shorted to GND V <sub>LIN</sub> = 0V, V <sub>BB</sub> < 12V
V <sub>BB</sub> Current with V <sub>SS</sub> Floating	IBBNOGND	-1	—	1	mA	V <sub>BB</sub> = 12V, GND to V <sub>BB</sub> , V <sub>LIN</sub> = 0-27V
V <sub>BB</sub> Undervoltage Threshold (switching from Operation mode to TOFF and V <sub>REN</sub> OFF)	V <sub>BBUV_FALL</sub>	3.8	4	4.4	V	V <sub>BB</sub> falling ( <b>Note 3</b> )
V <sub>BB</sub> Undervoltage Recovery Threshold (switching from POR to Ready mode)	V <sub>BBUV_RISE</sub>	5.5	5.6	6.0	V	V <sub>BB</sub> rising ( <b>Note 3</b> )
<b>Microcontroller Interface</b>						
High-Level Input Voltage (TxD)	V <sub>IH</sub>	2.0	—	30	V	
Low-Level Input Voltage (TxD)	V <sub>IL</sub>	-0.3	—	0.8	V	
High-Level Input Current (TxD)	I <sub>IH</sub>	-5	—	—	μA	Input voltage = 4.0V

**Note 1:** Internal current limited. 2.0 ms maximum recovery time (R<sub>L<sub>BUS</sub></sub> = 0Ω, T<sub>x</sub> = 0.4 V<sub>REG</sub>, V<sub>L<sub>BUS</sub></sub> = V<sub>BB</sub>).

**2:** Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

**3:** Characterized; not 100% tested.

## 2.3 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 5.5V$ to $30.0V$ Extended (E): $T_A = -40^{\circ}C$ to $+125^{\circ}C$ High (H): $T_A = -40^{\circ}C$ to $+150^{\circ}C$						
	Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Low-Level Input Current (TXD)	I <sub>IL</sub>	-12	—	—	—	μA	Input voltage = 0.5V
High-Level Voltage (VREN)	V <sub>HVREN</sub>	-0.3	—	—	$V_{BB} + 0.3$	V	
High-Level Output Current (VREN)	I <sub>HVREN</sub>	-40	—	—	-5	mA	Output voltage = $V_{BB} - 0.5V$
		-120	—	—	-20		Output voltage = $V_{BB} - 2.0V$
High-Level Input Voltage (CS)	V <sub>IH</sub>	2.0	—	—	30	V	Through a current limiting resistor
Low-Level Input Voltage (CS)	V <sub>IL</sub>	-0.3	—	—	0.8	V	
High-Level Input Current (CS)	I <sub>IH</sub>	—	—	—	10.0	μA	Input voltage = 4.0V
Low-Level Input Current (CS)	I <sub>IL</sub>	—	—	—	7.0	μA	Input voltage = 0.5V
Low-Level Input Voltage (WAKE)	V <sub>IL</sub>	$V_{BB} - 4.0V$	—	—	—	V	
High-Level Input Current (WAKE)	I <sub>IH</sub>	-12	—	—	—	μA	
		-15	—	—	—	μA	$V_{BB} > 18V$
Low-Level Input Current (WAKE)	I <sub>IL</sub>	-30	—	—	—	μA	
		-45	—	—	—	μA	$V_{BB} > 18V$
Low-Level Output Voltage (RXD)	V <sub>OL</sub>	—	—	—	0.4	V	I <sub>IN</sub> = 2 mA
Input Threshold Level (RXD)	V <sub>TH(RXD)</sub>	—	2.5	—	—	V	RXD > V <sub>TH</sub> ; LBUS recessive in Operating mode
High-Level Output Current (RXD)	I <sub>OH</sub>	-1	—	—	-1	μA	V <sub>LIN</sub> = $V_{BB}$ , V <sub>RXD</sub> = 5.5V
<b>Bus Interface</b>							
High-Level Input Voltage	V <sub>IH(LBUS)</sub>	$0.6 V_{BB}$	—	—	—	V	Recessive state
Low-Level Input Voltage	V <sub>IL(LBUS)</sub>	-8	—	—	$0.4 V_{BB}$	V	Dominant state
Input Hysteresis	V <sub>HYS</sub>	—	—	—	$0.175 V_{BB}$	V	V <sub>IH(LBUS)</sub> - V <sub>IL(LBUS)</sub>
Low-Level Output Current	I <sub>OL(LBUS)</sub>	40	—	—	200	mA	Output voltage = $0.2 V_{BB}$ , $V_{BB} = 12V$
		16.5	—	—	—		Output voltage = $0.2 V_{BB}$ , $V_{BB} = 18V$
High-Level Output Current	I <sub>OH(LBUS)</sub>	—	—	—	20	μA	
Short-Circuit Current Limit	I <sub>SC</sub>	50	—	—	200	mA	<b>(Note 1)</b>
High-Level Output Voltage	V <sub>OH(LBUS)</sub>	$0.8 V_{BB}$	—	—	$V_{BB}$	V	
Driver Dominant Voltage	V <sub>LOSUP</sub>	—	—	—	1.2	V	R <sub>LOAD</sub> = 500Ω
Input Leakage Current (at the receiver during dominant bus level)	I <sub>BUS_PAS_DO M</sub>	-1	-0.4	—	—	mA	Driver off, V <sub>BUS</sub> = 0V, $V_{BB} = 12V$

**Note 1:** Internal current limited. 2.0 ms maximum recovery time (R<sub>LBUS</sub> = 0Ω, T<sub>X</sub> = 0.4 V<sub>REG</sub>, V<sub>LBUS</sub> = V<sub>BB</sub>).

**2:** Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

**3:** Characterized; not 100% tested.

# MCP2003B

## 2.3 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for $V_{BB} = 5.5V$ to $30.0V$ Extended (E): $T_A = -40^{\circ}C$ to $+125^{\circ}C$ High (H): $T_A = -40^{\circ}C$ to $+150^{\circ}C$					
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Leakage Current (at the receiver during recessive bus level)	IBUS_PAS_REC	—	12	20	$\mu A$	Driver off, $8V < V_{BB} < 18V$ , $8V < V_{BUS} < 18V$ , $V_{BUS} \geq V_{BB}$
Leakage Current (disconnected from ground)	IBUS_NO_GND	-10	1.0	+10	$\mu A$	$GND_{DEVICE} = V_{BB}$ , $0V < V_{BUS} < 18V$ , $V_{BB} = 12V$
Leakage Current (disconnected from $V_{BB}$ )	IBUS_NO_VBB	—	—	10	$\mu A$	$V_{BB} = GND$ , $0 < V_{BUS} < 18V$ , <b>(Note 2)</b>
Receiver Center Voltage	VBUS_CNT	$0.475 V_{BB}$	$0.5 V_{BB}$	$0.525 V_{BB}$	V	$V_{BUS\_CNT} = (V_{IL} (LBUS) + V_{IH} (LBUS))/2$
Slave Termination	RSLAVE	20	30	60	$k\Omega$	
Capacitance of Slave Node	CSLAVE	—	—	100	pF	<b>(Note 3)</b>

- Note 1:** Internal current limited. 2.0 ms maximum recovery time ( $R_{LBUS} = 0\Omega$ ,  $T_X = 0.4 V_{REG}$ ,  $V_{LBUS} = V_{BB}$ ).
- 2:** Node has to sustain the current that can flow under this condition; bus must be operational under this condition.
- 3:** Characterized; not 100% tested.

## 2.4 AC Specifications

<b>AC Characteristics</b>						
<b>Electrical Characteristics:</b> Unless otherwise indicated, all limits are specified for $V_{BB} = 5.5V$ to $27.0V$ Extended (E): $T_A = -40^{\circ}C$ to $+125^{\circ}C$ High (H): $T_A = -40^{\circ}C$ to $+150^{\circ}C$						
Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
<b>Bus Interface – Constant Slope Time Parameters</b>						
Slope Rising and Falling Edges	$t_{SLOPE}$	3.5	—	22.5	$\mu s$	$7.3V \leq V_{BB} \leq 18V$
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	4.0	$\mu s$	$t_{TRANSPD} = \max(t_{TRANSPDR} \text{ or } t_{TRANSPDF})$
Propagation Delay of Receiver	$t_{RECPD}$	—	—	6.0	$\mu s$	$t_{RECPD} = \max(t_{RECPDR} \text{ or } t_{RECPDF})$
Symmetry of Propagation Delay of Receiver Rising Edge w.r.t. Falling Edge	$t_{RECSYM}$	-2.0	—	2.0	$\mu s$	$t_{RECSYM} = \max(t_{RECPDF} - t_{RECPDR})$ RRXD $2.4\Omega$ to $V_{CC}$ , CRXD $20 pF$
Symmetry of Propagation Delay of Transmitter Rising Edge w.r.t. Falling Edge	$t_{TRANSSYM}$	-2.0	—	2.0	$\mu s$	$t_{TRANSSYM} = \max(t_{TRANSPDF} - t_{TRANSPDR})$
Duty Cycle 1 @20.0 kbit/sec		0.396	—	—	—	CBUS; RBUS conditions: 1 nF; 1 k $\Omega$   6.8 nF; 660 $\Omega$   10 nF; 500 $\Omega$ THREC(MAX) = $0.744 \times V_{BB}$ , THDOM(MAX) = $0.581 \times V_{BB}$ , $V_{BB} = 7.0V - 18V$ ; tBIT = 50 $\mu s$ D1 = $t_{BUS\_REC(MIN)}/2 \times t_{BIT}$
Duty Cycle 2 @20.0 kbit/sec		—	—	0.581	—	CBUS; RBUS conditions: 1 nF; 1 k $\Omega$   6.8 nF; 660 $\Omega$   10 nF; 500 $\Omega$ THREC(MAX) = $0.284 \times V_{BB}$ , THDOM(MAX) = $0.422 \times V_{BB}$ , $V_{BB} = 7.6V - 18V$ ; tBIT = 50 $\mu s$ D2 = $t_{BUS\_REC(MAX)}/2 \times t_{BIT}$
Duty Cycle 3 @10.4 kbit/sec		0.417	—	—	—	CBUS; RBUS conditions: 1 nF; 1 k $\Omega$   6.8 nF; 660 $\Omega$   10 nF; 500 $\Omega$ THREC(MAX) = $0.778 \times V_{BB}$ , THDOM(MAX) = $0.616 \times V_{BB}$ , $V_{BB} = 7.0V - 18V$ ; tBIT = 96 $\mu s$ D3 = $t_{BUS\_REC(MIN)}/2 \times t_{BIT}$
Duty Cycle 4 @10.4 kbit/sec		—	—	0.590	—	CBUS; RBUS conditions: 1 nF; 1 k $\Omega$   6.8 nF; 660 $\Omega$   10 nF; 500 $\Omega$ THREC(max) = $0.251 \times V_{BB}$ , THDOM(MAX) = $0.389 \times V_{BB}$ , $V_{BB} = 7.6V - 18V$ ; tBIT = 96 $\mu s$ D4 = $t_{BUS\_REC(MAX)}/2 \times t_{BIT}$
<b>Wake-up Timing</b>						
Bus Activity Debounce time	$t_{BDB}$	30	70	125	$\mu s$	
Bus Activity to VREN on	$t_{BACTIVE}$	10	60	110	$\mu s$	
WAKE to VREN on	$t_{WAKE}$	—	—	150	$\mu s$	
Chip Select to VREN on	$t_{CSOR}$	—	—	150	$\mu s$	VREN floating
Chip Select to VREN off	$t_{CSPD}$	—	—	200	$\mu s$	VREN floating

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## 2.5 Thermal Specifications

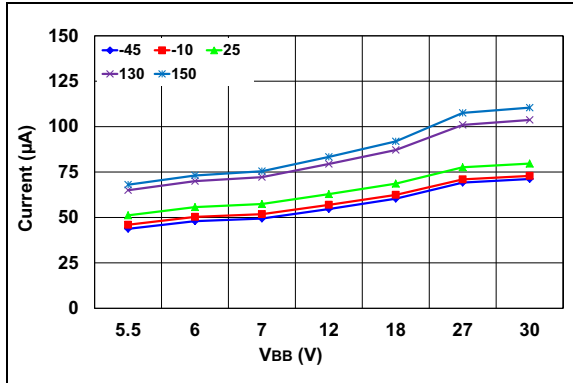
Parameter	Symbol	Typ.	Max.	Units	Test Conditions
Recovery Temperature	$\theta_{RECOVERY}$	+160	—	°C	
Shutdown Temperature	$\theta_{SHUTDOWN}$	+180	—	°C	
Short-Circuit Recovery Time	$t_{THERM}$	1.5	5.0	ms	
<b>Thermal Package Resistances</b>					
Thermal Resistance, 2x3 8L-DFN	$\theta_{JA}$	75	—	°C/W	
Thermal Resistance, 3x3 8L-DFN	$\theta_{JA}$	56.7	—	°C/W	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	149.5	—	°C/W	

**Note 1:** The maximum power dissipation is a function of  $T_{JMAX}$ ,  $\theta_{JA}$  and ambient temperature  $T_A$ . The maximum allowable power dissipation at an ambient temperature is  $P_D = (T_{JMAX} - T_A) \theta_{JA}$ . If this dissipation is exceeded, the die temperature will rise above 150°C and the device will go into thermal shutdown.

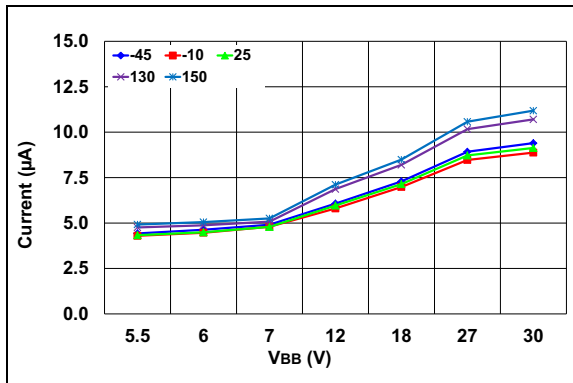
## 2.6 Typical Performance Curves

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

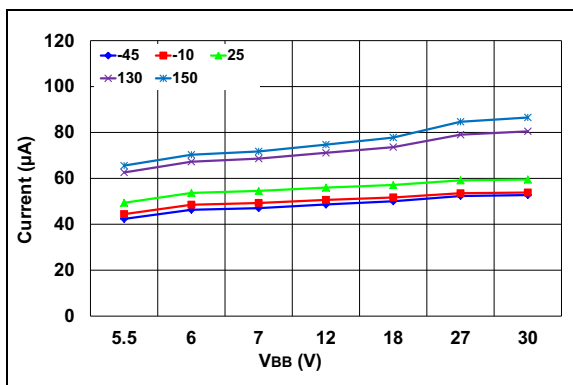
**Note:** Unless otherwise indicated,  $V_{BB} = 5.5V$  to  $18.0V$ , Extended (E):  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$  and High (H):  $T_A = -40^{\circ}C$  to  $+150^{\circ}C$ .



**FIGURE 2-1:** Typical IBBQ.



**FIGURE 2-2:** Typical IBBPD.



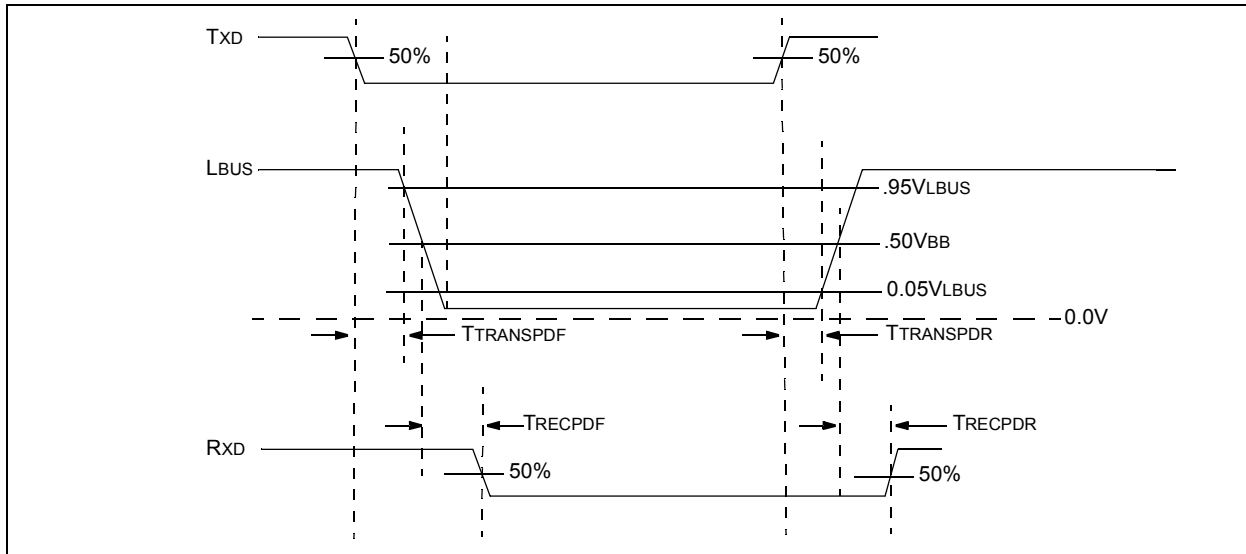
**FIGURE 2-3:** Typical IBBTO.



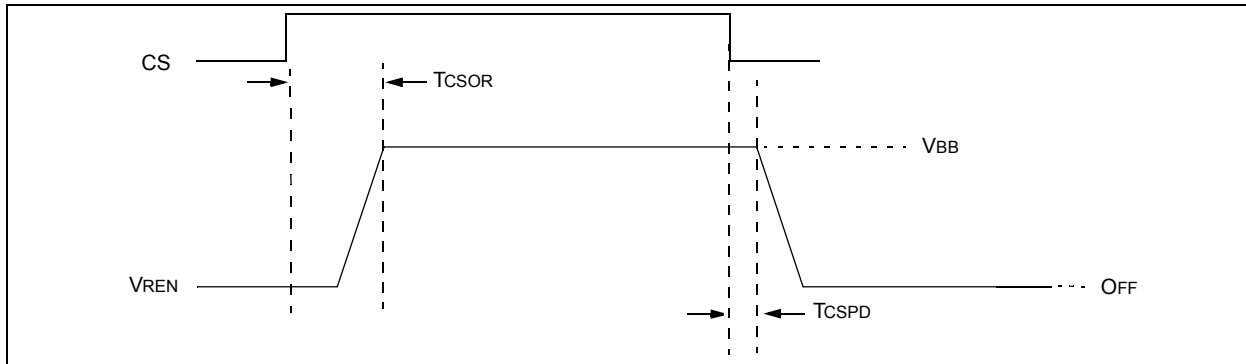
# MCP2003B

## 2.7 Timing Diagrams and Specifications

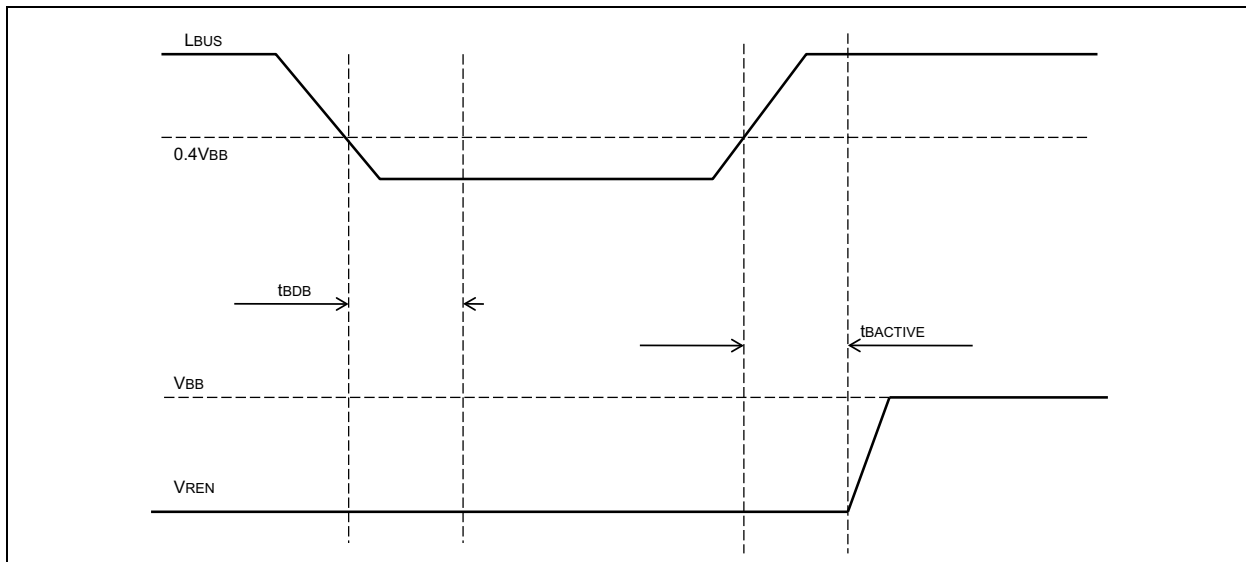
**FIGURE 2-4: BUS TIMING DIAGRAM**



**FIGURE 2-5: CS TO VREN TIMING DIAGRAM**



**FIGURE 2-6: REMOTE WAKE-UP**



## 3.0 PACKAGING INFORMATION

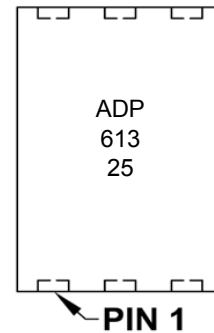
### 3.1 Package Marking Information

8-Lead DFN (2x3)

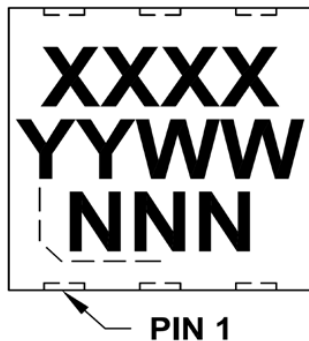


Device	Code
MCP2003B-E/MC	ADP
MCP2003BT-E/MC	ADP
MCP2003B-H/MC	ADR
MCP2003BT-H/MC	ADR

Examples:

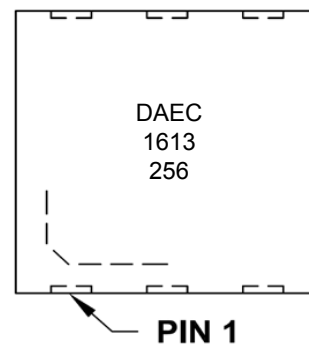


8-Lead DFN (3x3)

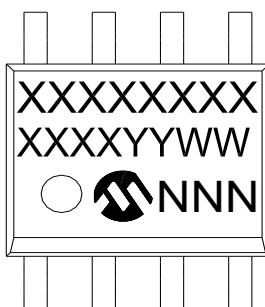


Device	Code
MCP2003B-E/MF	DAEC
MCP2003BT-E/MF	DAEC
MCP2003B-H/MF	DAEE
MCP2003BT-H/MF	DAEE

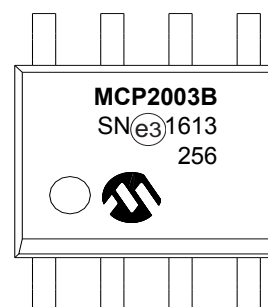
Examples:



8-Lead SOIC (150 mil)



Examples:



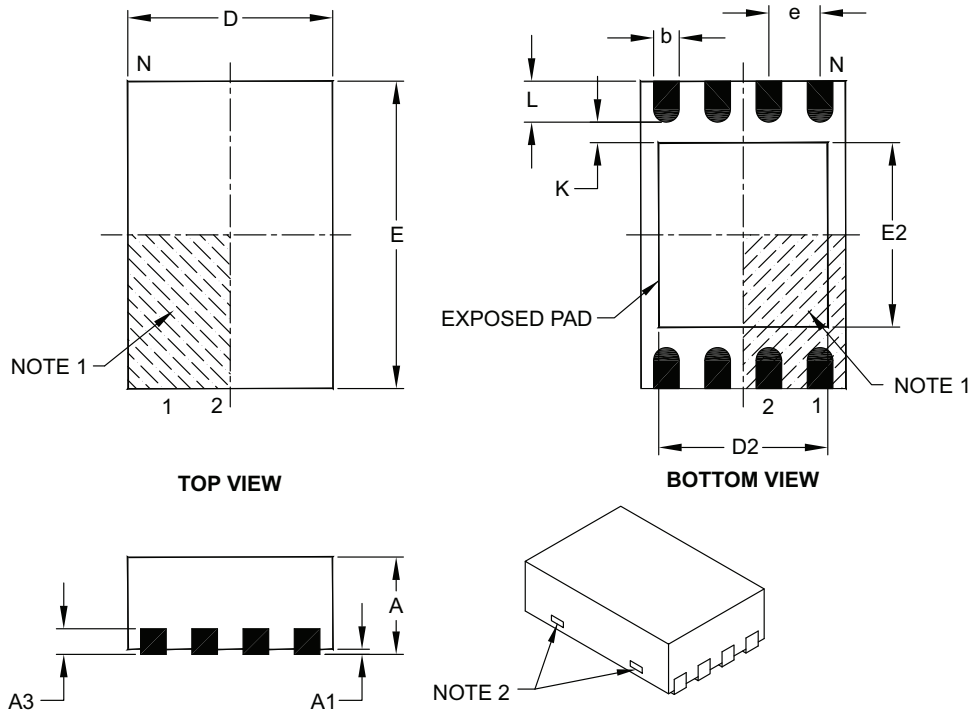
<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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## 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packageing>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package may have one or more exposed tie bars at ends.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

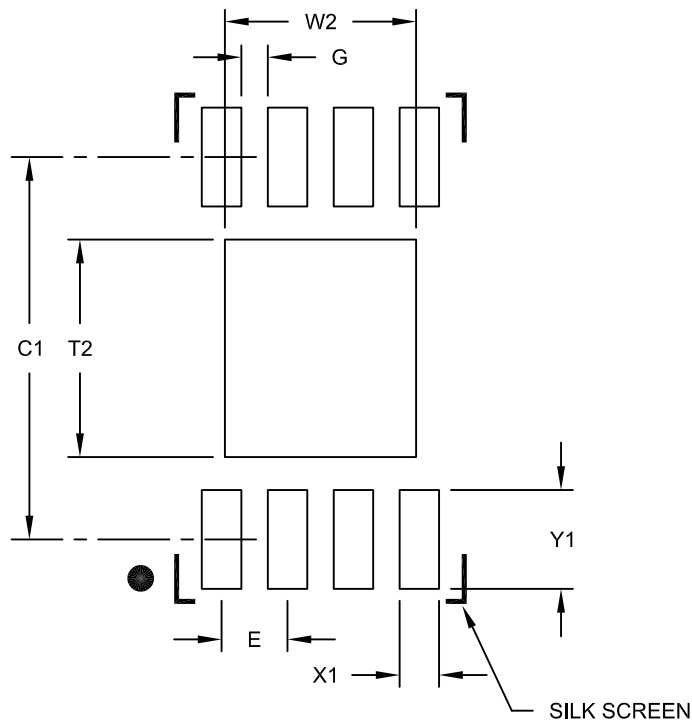
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

## 8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

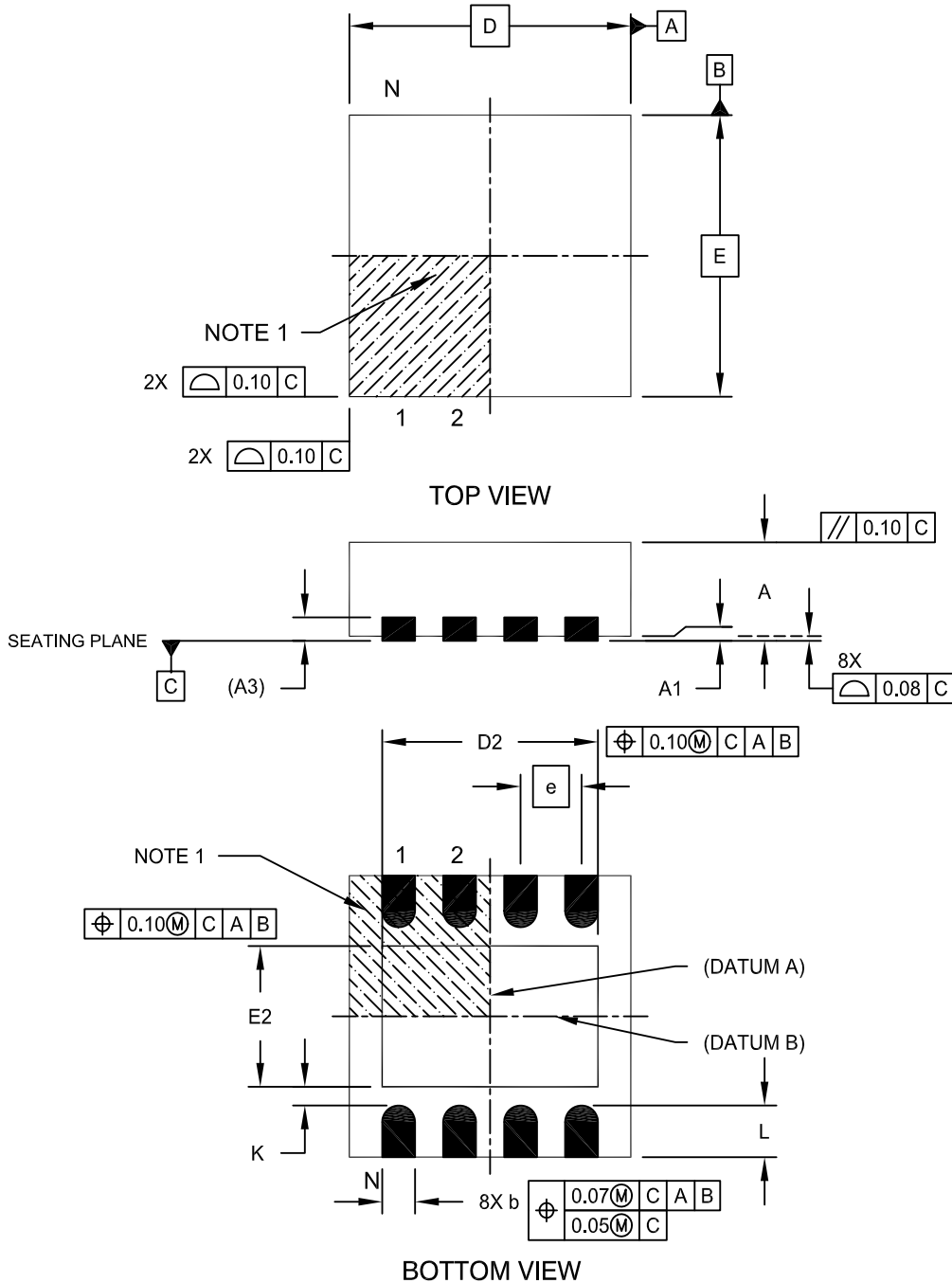
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

# MCP2003B

## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

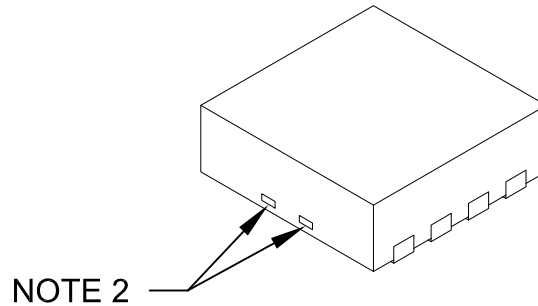
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-062C Sheet 1 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Width	E2	1.34	-	1.60
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.60	-	2.40
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.20	0.30	0.55
Contact-to-Exposed Pad	K	0.20	-	-

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

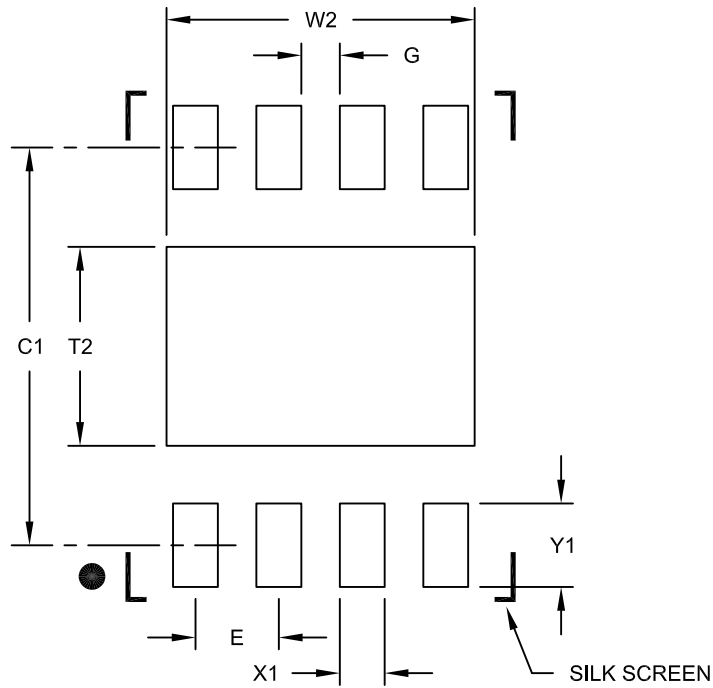
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

# MCP2003B

## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.30		

**Notes:**

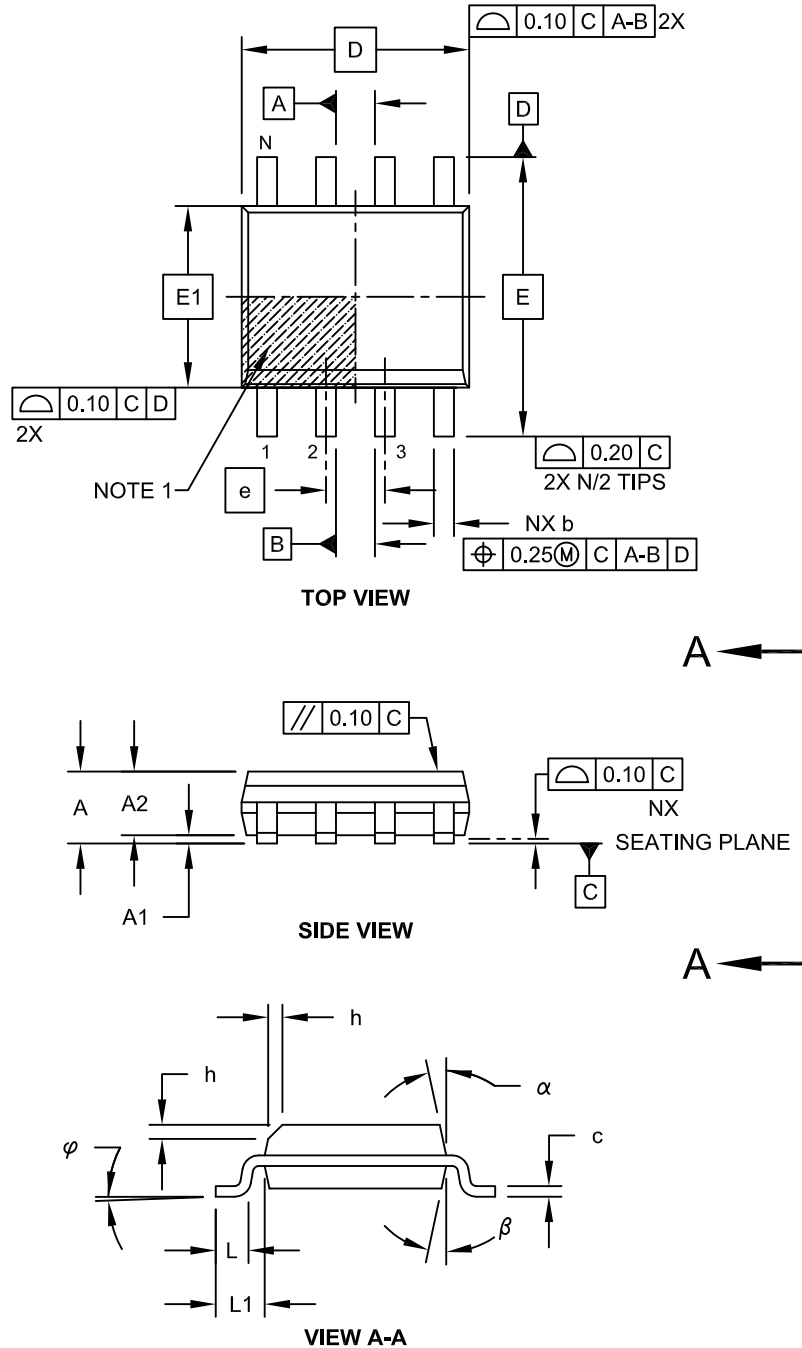
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



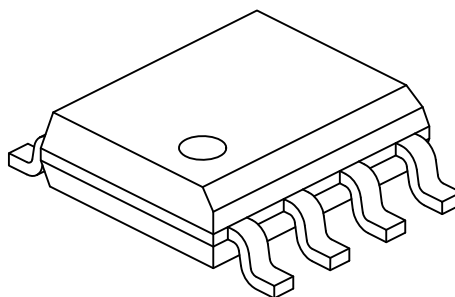
Microchip Technology Drawing No. C04-057C Sheet 1 of 2



# MCP2003B

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

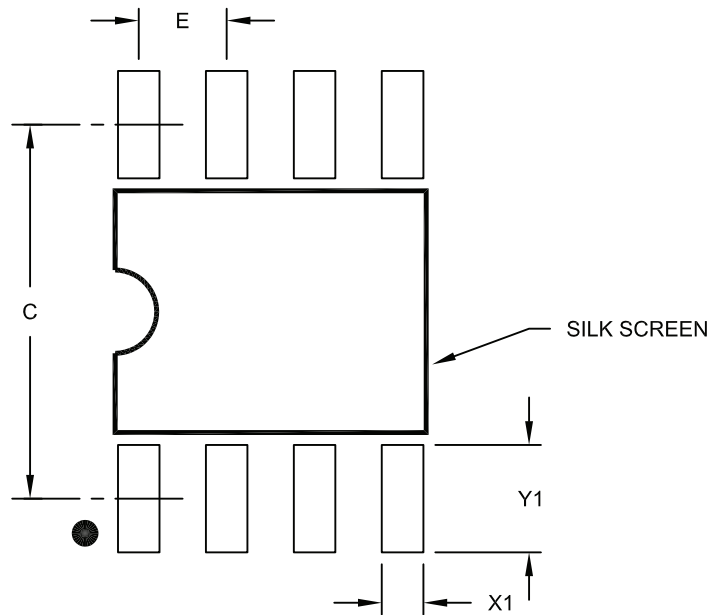
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A