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MCP2021A/2A

LIN Transceiver with Voltage Regulator

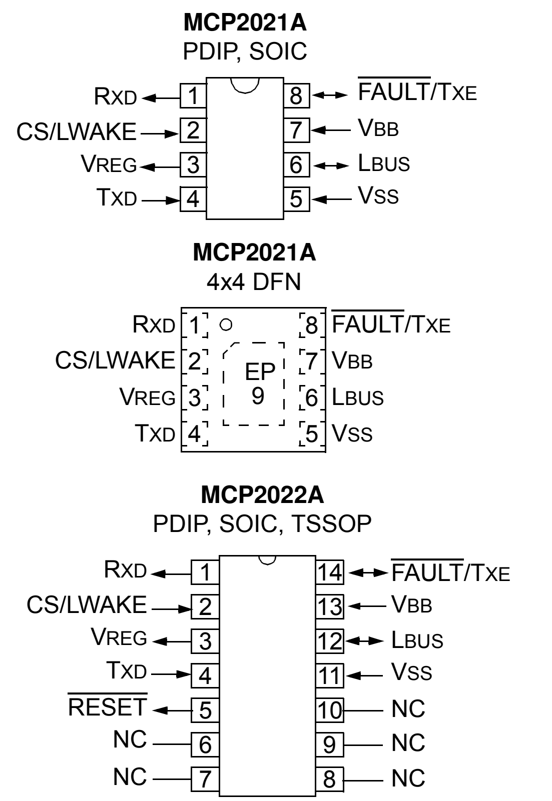
Features:

- The MCP2021A/2A are compliant with LIN Bus Specifications Version 1.3, 2.1 and with SAE J2602-2
- Support Baud Rates up to 20 kBaud
- 43V Load Dump Protected
- Maximum Continuous Input Voltage: 30V
- Wide LIN-Compliant Supply Voltage: 6.0 – 18.0V
- Extended Temperature Range: -40 to +125°C
- Interface to PIC® MCU EUSART and Standard USARTs
- Wake-Up on LIN Bus Activity or Local Wake Input
- Local Interconnect Network (LIN) Bus Pin:
  - Internal Pull-Up Termination Resistor and Diode for Slave Node
  - Protected Against VBAT Shorts
  - Protected Against Loss of Ground
  - High-Current Drive
- TXD and LIN Bus Dominant Time-Out Function
- Two Low-Power Modes:
  - Transmitter Off: 90 µA (typical)
  - Power Down: 4.5 µA (typical)
- Output Indicating Internal Reset State (POR or Sleep Wake)
- MCP2021A/2A On-Chip Voltage Regulator:
  - Output Voltage of 5.0V or 3.3V at 70 mA Capability with Tolerances of ±3% Over the Temperature Range
  - Internal Short Circuit Current Limit
  - External Components Limited to Filter Capacitor and Load Capacitor
- Automatic Thermal Shutdown
- High Electromagnetic Immunity (EMI), Low Electromagnetic Emission (EME)
- Robust ESD Performance: ±15 kV for LBUS and VBB pin (IEC61000-4-2)
- Transient Protection for LBUS and VBB Pins in Automotive Environment (ISO7637)
- Meets Stringent Automotive Design Requirements, including "OEM Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications", Version 1.2, March 2011
- Multiple Package Options, including Small 4x4 mm DFN Package

Description:

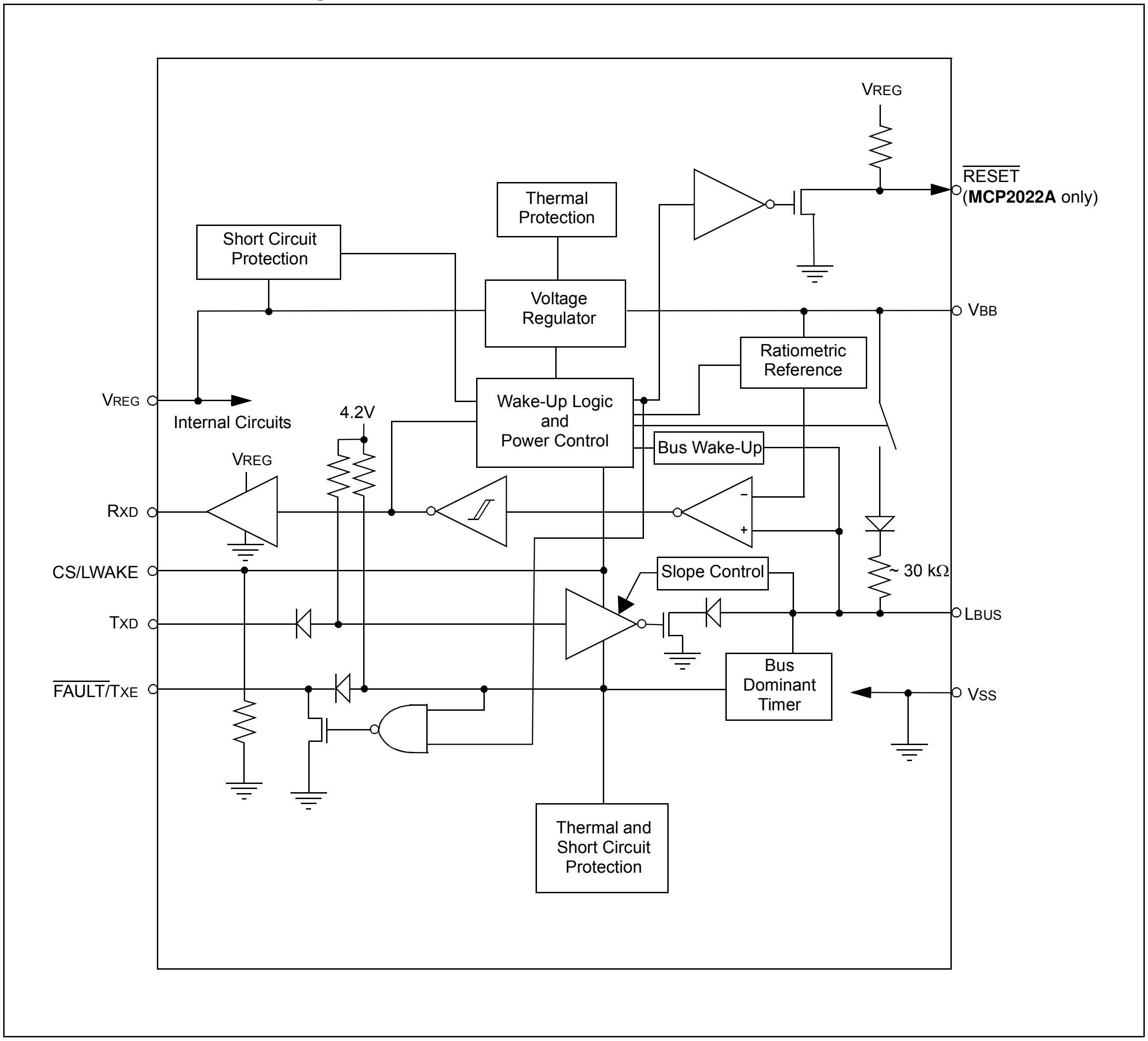
The MCP2021A/2A provide a bidirectional, half-duplex communication physical interface to meet the LIN bus specification Revision 2.1 and SAE J2602-2. The devices incorporate a voltage regulator with 5V or 3.3V at 70 mA regulated power supply output. The devices have been designed to meet the stringent quiescent current requirements of the automotive industry and will survive +43V load dump transients and double battery jumps.

Package Types



* Includes Exposed Thermal Pad (EP), see Table 1-2.

MCP2021A/2A Block Diagram



1.0 DEVICE OVERVIEW

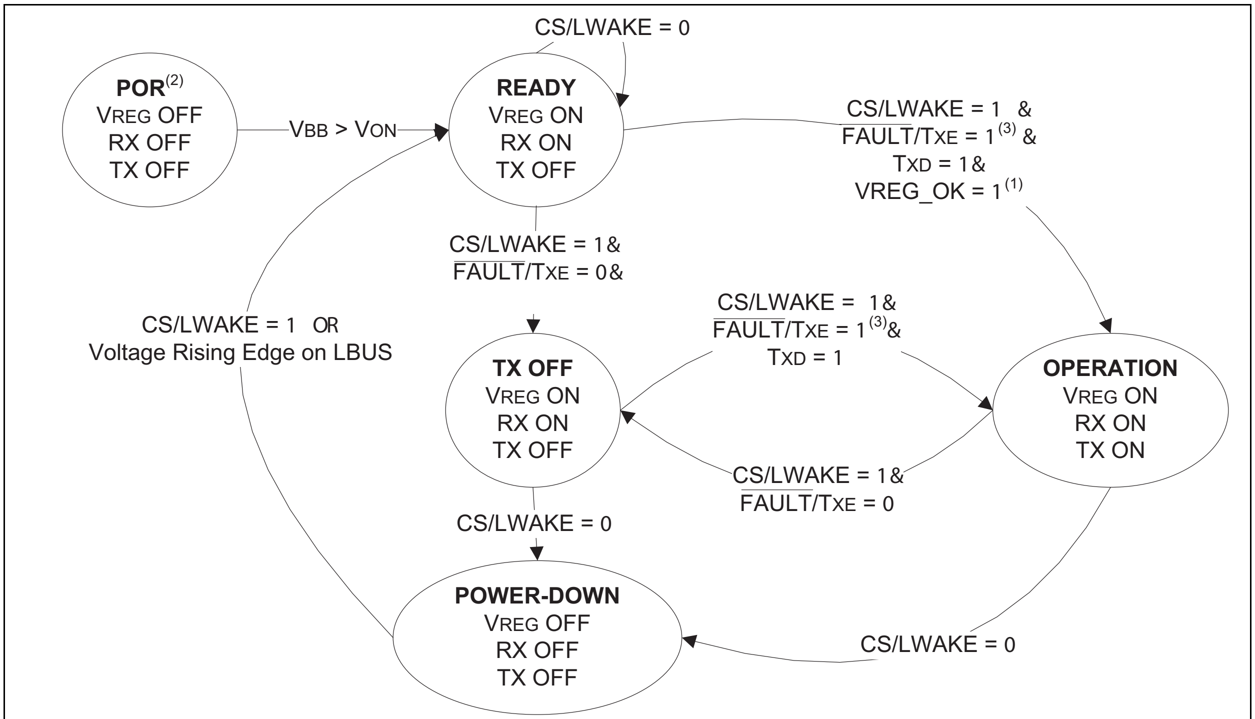
The MCP2021A/2A devices provide a physical interface between a microcontroller and a LIN half-duplex bus. They are intended for automotive and industrial applications with serial bus baud rates up to 20 kBaud. These devices will translate the CMOS/TTL logic levels to LIN logic levels and vice versa.

The MCP2021A/2A offer optimum EMI and ESD performance and can withstand high voltage on the LIN bus. The devices support two low-power modes to meet automotive industry power consumption requirements. The MCP2021A/2A also provide a +5V or 3.3V regulated power output at 70 mA.

1.1 Modes of Operation

The MCP2021A/2A work in five modes: Power-On Reset, Power-Down, Ready, Operation and Transmitter Off. For an overview of all operational modes, please refer to Table 1-1. For the operational mode transition, please refer to Figure 1-1.

FIGURE 1-1: STATE DIAGRAM



Note 1: VREG_OK: Regulator Output Voltage > 0.8VREG_NOM.

2: If the voltage on pin V_{BB} falls below V_{OFF}, the device will enter Power-On Reset mode from all other modes, which is not shown in the figure.

3: FAULT/TXE = 1 represents input high and no fault conditions. FAULT/TXE = 0 represents input low or a fault condition. Refer to Table 1-5.

1.1.1 POWER-ON RESET MODE

Upon application of V_{BB} or whenever the voltage on V_{BB} is below the threshold of regulator turn-off voltage V_{OFF} (typically 4.50V), the device enters Power-On Reset (POR) mode. During this mode, the device maintains the digital section in a Reset mode and waits until the voltage on the V_{BB} pin rises above the threshold of regulator turn-on voltage V_{ON} (typically 5.75V) to enter Ready mode. In Power-On Reset mode, the LIN physical layer and voltage regulator are disabled and the $\overline{\text{RESET}}$ output (**MCP2022A** only) is forced to low.

1.1.2 READY MODE

The device enters Ready mode from POR mode after the voltage on V_{BB} rises above the threshold of regulator turn-on voltage V_{ON} or from Power-Down mode when a remote or local wake-up event happens.

Upon entering Ready mode, the voltage regulator and the receiver section of the transceiver are powered up. The transmitter remains in an off state. The device is ready to receive data but not to transmit. In order to minimize the power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and it is thus slower. However, the 70 mA drive capability is unchanged.

The device stays in Ready mode until the output of the voltage regulator has stabilized and the CS/LWAKE pin is high (‘1’).

1.1.3 OPERATION MODE

If V_{REG} is $\overline{\text{OK}}$ (V_{REG} > 0.8 V_{REG_NORM}) and the CS/LWAKE, $\overline{\text{FAULT}}$/TXE and TXD pins are high, the part enters Operation mode from either Ready or Transmitter Off mode.

In this mode, all internal modules are operational. The internal pull-up resistor between LBUS and V_{BB} is connected only in this mode.

The device goes into Power-Down mode at the falling edge on CS/LWAKE or into Transmitter Off mode at the falling edge on $\overline{\text{FAULT}}$/TXE while CS/LWAKE stays high.

1.1.4 TRANSMITTER OFF MODE

In Transmitter Off mode, the receiver is enabled but the LBUS transmitter is off. It is a lower power mode.

In order to minimize power consumption, the regulator operates in a reduced-power mode. It has a lower GBW product and it is thus slower. However, the 70 mA drive capability is unchanged.

The transmitter may be re-enabled whenever the $\overline{\text{FAULT}}$/TXE signal returns high, by removing the internal fault condition and by driving FAULT/TXE high. The transmitter will not be enabled even if the $\overline{\text{FAULT}}$/TXE pin is brought high externally, when the internal fault is still present. However, externally forcing the $\overline{\text{FAULT}}$/TXE high while the internal fault is still present should be avoided, since this will induce high current and power dissipation in the $\overline{\text{FAULT}}$/TXE pin.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption of the bus during times of uncertain operation.

1.1.5 POWER-DOWN MODE

In Power-Down mode, the transceiver and the voltage regulator are both off. Only the bus wake-up section and the CS/LWAKE pin wake-up circuits are in operation. This is the lowest power mode.

If any bus activity (e.g., a Break character) occurs during Power-Down mode, the device will immediately enter Ready mode and enable the voltage regulator. Then, once the regulator output has stabilized (approximately 0.3 ms to 1.2 ms), it goes into Operation mode. Refer to **Section 1.1.6 “Remote Wake-Up”**.

The part will also enter Ready mode from Power-Down mode, followed by the Operation mode, if the CS/LWAKE pin becomes active high (‘1’).

1.1.6 REMOTE WAKE-UP

The Remote Wake-Up sub-module observes the LBUS in order to detect bus activity. In Power-Down mode, normal LIN recessive/dominant threshold is disabled and the LIN bus wake-up voltage threshold $V_{WK(LBUS)}$ is used to detect bus activities. Bus activity is detected when the voltage on the LBUS falls below the LIN bus wake-up voltage threshold $V_{WK(LBUS)}$ (approximately 3.5V) for at least t_{BDB} (a typical duration of 80 µs) followed by a rising edge. Such a condition causes the device to leave Power-Down mode.

TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Receiver	Internal Wake Module	Voltage Regulator	Operation	Comments
POR	OFF	OFF	OFF	OFF	Proceed to Ready mode after $V_{BB} > V_{ON}$	
Ready	OFF	ON	OFF	ON	If CS/LWAKE is high, then proceed to Operation or Transmitter Off mode.	Bus Off state
Operation	ON	ON	OFF	ON	If CS/LWAKE is low, then proceed to Power-Down mode. If $\overline{FAULT}$/TXE is low, then proceed to Transmitter Off mode.	Normal Operation mode
Power-Down	OFF	OFF	ON Activity Detect	OFF	On LIN bus rising edge or CS/LWAKE high level, go to Ready mode.	Lowest power mode
Transmitter Off	OFF	ON	OFF	ON	If CS/LWAKE is low, then proceed to Power-Down mode. If $\overline{FAULT}$/TXE is high, then proceed to Operation mode.	Bus Off state, lower power mode

1.2 Pin Descriptions

The descriptions of the pins are listed in Table 1-2.

TABLE 1-2: PIN FUNCTION TABLE

Pin Name	Pin Number			Pin Type	Description
	8-lead PDIP, SOIC	4x4 DFN	14-lead PDIP, SOIC, TSSOP		
RXD	1	1	1	Output	Receive Data Output
CS/LWAKE	2	2	2	TTL Input, HV-tolerant	Chip Select and Local Wake-up Input
VREG	3	3	3	Output	Voltage Regulator Output
TXD	4	4	4	Input, HV-tolerant	Transmit Data Input
RESET	—	—	5	Output	Reset Output
NC	—	—	6–10	—	No Connection
VSS	5	5	11	Power	Ground
LBUS	6	6	12	I/O, HV	LIN Bus
VBB	7	7	13	Power	Battery
FAULT/TXE	8	8	14	I/O, HV-tolerant	Fault Detect Output/Transmitter Enable Input
EP	—	9	—	—	Exposed Thermal Pad

1.2.1 RECEIVE DATA OUTPUT (RXD)

Receive Data Output pin. The RXD pin is a standard CMOS output pin and it follows the state of the LBUS pin.

1.2.2 CHIP SELECT AND LOCAL WAKE-UP INPUT (CS/LWAKE)

Chip Select and Local Wake-up Input pin (TTL level, high-voltage tolerant). This pin controls the device state transition. Refer to Figure 1-1.

If CS/LWAKE = 1, the device can work in Operation mode (FAULT/TXE = 1) or in Transmitter Off mode (FAULT/TXE = 0). If CS/LWAKE = 0, the device can work in Power-Down mode or in Ready mode.

An internal pull-down resistor will keep the CS/LWAKE pin low to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-On Reset and I/O initialization sequence. When CS/LWAKE is '1', a weak pull-down (~600 kΩ) is used to reduce current. When CS/LWAKE is '0', a stronger pull-down (~300 kΩ) is used to maintain the logic level.

This pin may also be used as a local wake-up input (see Figure 1-1). The microcontroller will set the I/O pin to control the CS/LWAKE. An external switch or another source can then wake up both the transceiver and the microcontroller.

Note: CS/LWAKE should NOT be tied directly to the VREG pin as this could force the MCP2021A/2A into Operation mode before the microcontroller is initialized.

1.2.3 POWER OUTPUT (VREG)

Positive Supply Voltage Regulator Output pin. An on-chip LDO gives +5.0 or +3.3V at 70 mA regulated voltage on this pin.

1.2.4 TRANSMIT DATA INPUT (TXD)

Transmit Data Input pin (TTL level, HV-compliant, adaptive pull-up). The transmitter reads the data stream on the TXD pin and sends it to the LIN bus. The LBUS pin is low (dominant) when TXD is low and high (recessive) when TXD is high.

TXD is internally pulled up to approximately 4.2V. When TXD is '0', a weak pull-up (~900 kΩ) is used to reduce current. When TXD is '1', a stronger pull-up (~300 kΩ) is used to maintain the logic level. A series reverse-blocking diode allows applying TXD input voltages greater than the internally generated 4.2V and renders the TXD pin HV-compliant up to 30V (see MCP2021A/2A Block Diagram).

1.2.5 RESET (MCP2022A ONLY)

RESET output pin. This pin is open-drain with ~90 kΩ pull-up to VREG. It indicates the internal voltage has reached a valid, stable level. As long as the internal voltage is valid (above 0.8 VREG), this pin will remain high ('1'); otherwise, the RESET pin switches to low ('0').

1.2.6 NO CONNECTION (NC)

No internal connection.

1.2.7 GROUND (VSS)

Ground pin.

1.2.8 LIN BUS (LBUS)

LIN Bus pin. LBUS is a bidirectional LIN bus interface pin and is controlled by the signal TXD. It has an open collector output with a current limitation. To reduce electromagnetic emission, the slopes during signal changes are controlled and the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus and generates the output signal RXD that follows the state of the LBUS. A 1st degree 160 kHz low-pass input filter optimizes electromagnetic immunity.

1.2.9 BATTERY POSITIVE SUPPLY VOLTAGE (VBB)

Battery Positive Supply Voltage pin. An external diode is connected in series to prevent the device from being reversely powered (refer to Figure 1-7).

1.2.10 FAULT DETECT OUTPUT/TRANSMITTER ENABLE INPUT ($\overline{\text{FAULT}}$/TXE)

Fault Detect Output/Transmitter Enable Input pin. The output section is HV-tolerant open-drain (up to 30V). The input section is identical to the TXD section (TTL level, HV-compliant, adaptive pull-up). The internal pull-up resistor may be too weak for some applications. We recommend adding a 10 kΩ external pull-up resistor to ensure a logic high level. Its state is defined as shown in Table 1-5. The device is placed in Transmitter Off mode whenever this pin is low (‘0’), either from an internal fault condition or by external drive.

If CS/LWAKE is high (‘1’), the $\overline{\text{FAULT}}$/TXE signals a mismatch between the TXD input and the LBUS level. This can be used to detect a bus contention. Since the bus exhibits a propagation delay, the sampling of the internal compare is debounced to eliminate false faults.

After the device wakes up, the $\overline{\text{FAULT}}$/TXE indicates what wakes the device if CS/LWAKE remains low (‘0’) (refer to Table 1-5).

The $\overline{\text{FAULT}}$/TXE pin sampled at a rate faster than every 10 µs.

TABLE 1-3: $\overline{\text{FAULT}}$/TXE TRUTH TABLE

TXD In	RXD Out	LINBUS I/O	Thermal Override	$\overline{\text{FAULT}}$/TXE External Input	$\overline{\text{FAULT}}$/TXE Driven Output	Definition
CS = 1						
L	H	VBB	OFF	H	L	**FAULT**, TXD driven low, LBUS shorted to VBB **(Note 1)** or LBUS/TXD permanent dominant detected and Transmit time-out shutdown.
H	H	VBB	OFF	H	H	**OK**
L	L	GND	OFF	H	H	**OK**
H	L	GND	OFF	H	H	**OK**, data is being received from LBUS
x	x	VBB	ON	H	L	**FAULT**, Transceiver in thermal shutdown
x	x	VBB	x	L	x	**NO FAULT**, the CPU is commanding the transceiver to turn off the transmitter driver
CS = 0						
x	x	x	x	x	L	**Wake-up from LIN bus activity**
x	x	x	x	x	H	**Wake-up from POR**

Legend: x = Don’t care

Note 1: The $\overline{\text{FAULT}}$/TXE is valid after approximately 25 µs after the TXD falling edge. This is to eliminate false fault reporting during bus propagation delays.

1.3 Fail-Safe Features

1.3.1 GENERAL FAIL-SAFE FEATURES

- An internal pull-down resistor on CS/LWAKE pin disables the transmitter if the pin is floating.
- An internal pull-up resistor on the TXD pin places TXD in high and the LBUS in recessive if the TXD pin is floating.
- High-impedance and low-leakage current on LBUS during loss of power or ground.
- The current limit on LBUS protects the transceiver from being damaged if the pin is shorted to V_{BB}.

1.3.2 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator.

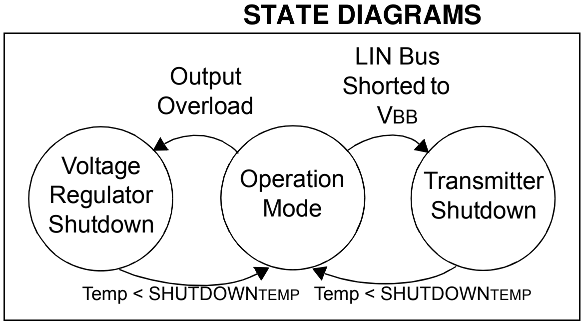
There are three causes for a thermal overload. A thermal shutdown can be triggered by any one, or a combination of, the following thermal overload conditions:

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

The recovery time from the thermal shutdown is equal to adequate cooling time.

Driving the TXD and checking the RXD pin make it possible to determine whether there is a bus contention (TXD = high, RXD = low) or a thermal overload condition (TXD = low, RXD = high).

FIGURE 1-2: THERMAL SHUTDOWN STATE DIAGRAMS



1.3.3 TXD/LBUS TIME-OUT TIMER

The LIN bus can be driven to a dominant level either from the TXD pin or externally. An internal timer deactivates the LBUS transmitter if a dominant status (low) on the LIN bus lasts longer than Bus Dominant Time-out Time, $t_{TO(LIN)}$ (approximately 20 milliseconds). At the same time, the RXD output is put in recessive (high), $\overline{FAULT}$/TXE is also driven to low and the internal LIN pull-up resistor is disconnected. The timer is reset on any recessive LBUS status or POR mode. The recessive status on LBUS can be caused either by the bus being externally pulled up or by the TXD pin being returned high.

1.4 Internal Voltage Regulator

The MCP2021A/2A have a positive regulator capable of supplying +5.00 or +3.30 V_{DC} ±3% at up to 70 mA of load current over the entire operating temperature range of -40°C to +125°C. The regulator uses a LDO design, is short-circuit-protected and will turn the regulator output off if its output falls below the shutdown voltage threshold, V_{SD}.

With a load current of 70 mA, the minimum input to output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 µA with a full 70 mA load current when the input to output voltage differential is greater than +3.00V.

Regarding the correlation between V_{BB}, V_{REG} and I_{DD}, please refer to Figures 1-4 and 1-5. When the input voltage (V_{BB}) drops below the differential needed to provide stable regulation, the voltage regulator output, V_{REG}, will track the input down to approximately V_{OFF}, at which point the regulator will turn off the output. This will allow PIC® microcontrollers with internal POR circuits to generate a clean arming of the POR trip point. The MCP2021A/2A will then monitor V_{BB} and turn on the regulator when V_{BB} is above the threshold of regulator turn-on voltage, V_{ON}.

In Power-Down mode, the V_{BB} monitor is turned off.

Under specific ambient temperature and battery voltage range, the voltage regulator can output as high as 150 mA current. For current load capability of the voltage regulator, refer to Figures 2-8 and 2-9.

Note:	The regulator has an overload current limit of approximately 250 mA. The regulator output voltage, V_{REG}, is monitored. If output voltage V_{REG} is lower than V_{SD}, the voltage regulator will turn off. After a recovery time of about 3 ms, the V_{REG} will be checked again. If there is no short circuit ($V_{REG} > V_{SD}$), then the voltage regulator remains on.

The regulator requires an external output bypass capacitor for stability. See Figure 2-1 for correct capacity and ESR for stable operation.

Note: A ceramic capacitor of at least 10 µF or a tantalum capacitor of at least 2.2 µF is recommended for stability.

In worst-case scenarios, the ceramic capacitor may derate by 50%, based on tolerance, voltage and temperature. Therefore, in order to ensure stability, ceramic capacitors smaller than 10 µF may require a small series resistance to meet the ESR requirements, as shown in Table 1-4.

TABLE 1-4: RECOMMENDED SERIES RESISTANCE FOR CERAMIC CAPACITORS

Resistance	Capacitor
1Ω	1 µF
0.47Ω	2.2 µF
0.22Ω	4.7 µF
0.1Ω	6.8 µF

FIGURE 1-3: VOLTAGE REGULATOR BLOCK DIAGRAM

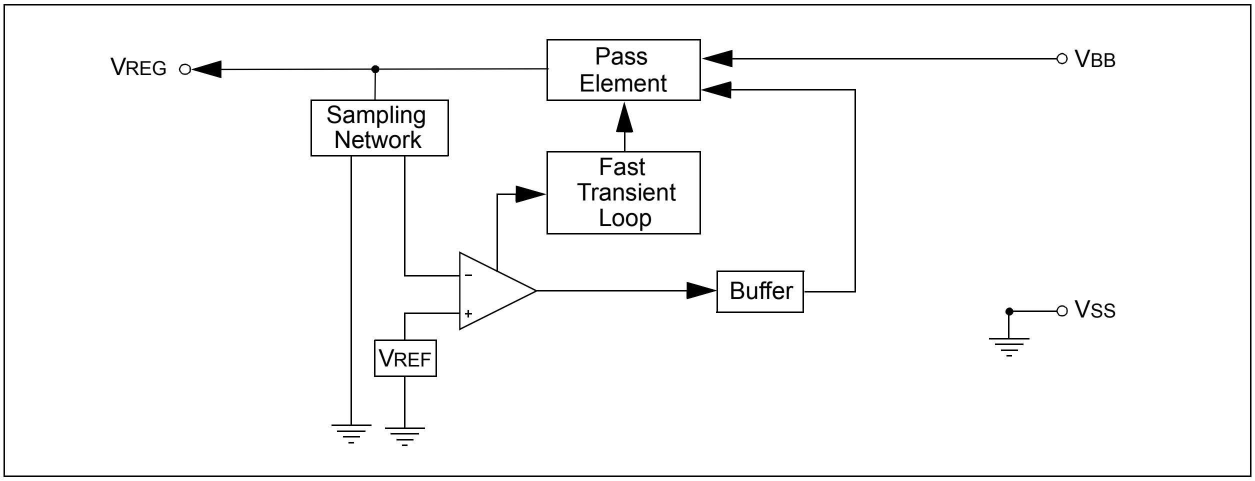
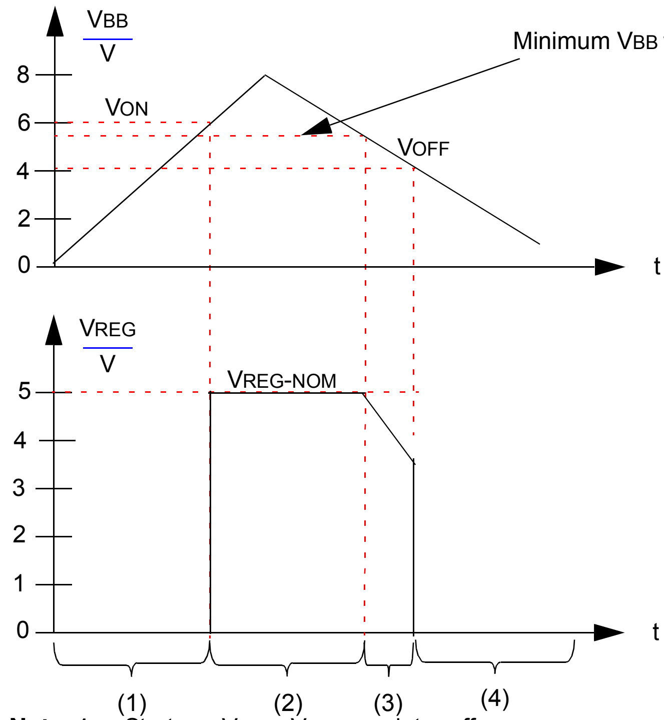
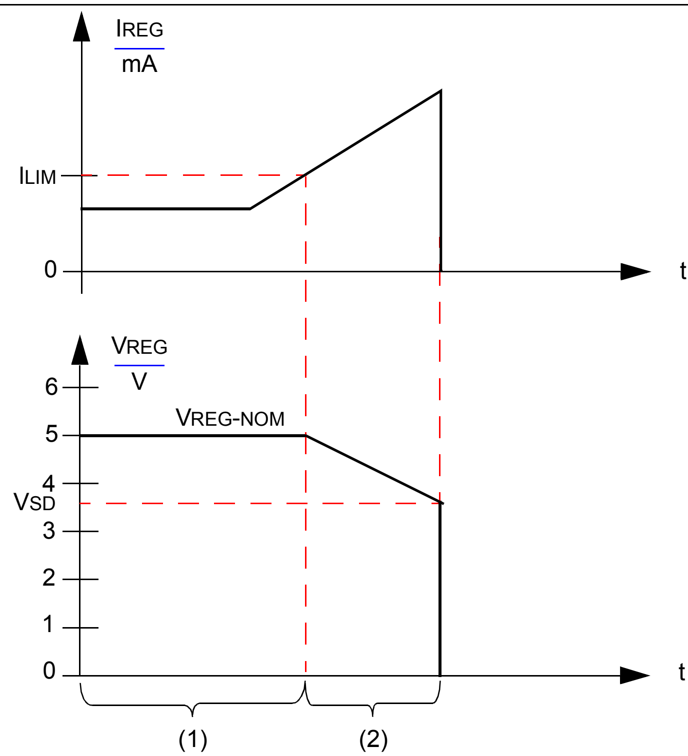


FIGURE 1-4: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET



Note 1: Start-up, VBB < VON, regulator off.
2: VBB > VON, regulator on.
3: VBB ≤ Minimum VBB to maintain regulation.
4: VBB < VOFF, regulator will turn off.

FIGURE 1-5: VOLTAGE REGULATOR OUTPUT ON OVERCURRENT PROTECTION



Note 1: IREG less than ILIM, regulator on.
2: After IREG exceeds ILIM, the voltage regulator output will be reduced until VSD is reached.

1.5 Optional External Protection

1.5.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see Figure 1-7).

1.5.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between VBB and ground, with a transient protection resistor (RTP) in series with the battery supply and the VBB pin, protects the device from power transients and ESD events greater than 43V (see Figure 1-7). The maximum value for the RTP protection resistor depends upon two parameters: the minimum voltage the part will start at and the impacts of this RTP resistor on the VBB value, thus on the bus recessive level and slopes.

This leads to a set of three equations to fulfill.

Equation 1-1 provides a maximum RTP value according to the minimum battery voltage the user wants.

Equation 1-2 provides a maximum RTP value according to the maximum error on the recessive level, thus VBB, since the part uses VBB as the reference value for the recessive level.

Equation 1-3 provides a maximum RTP value according to the maximum relative variation the user can accept on the slope when IREG varies.

Since both Equations 1-1 and 1-2 must be fulfilled, the maximum allowed value for RTP is thus the smaller of the two values found when solving Equations 1-1 and 1-2.

Usually Equation 1-1 gives the higher constraint (smaller value) for RTP, as shown in the following example where V_{BATmin} is 8V.

However, the user needs to check that the value found with Equation 1-1 fulfills Equations 1-2 and 1-3.

While this protection is optional, it should be considered as good engineering practice.

EQUATION 1-1:

$$R_{TP} \leq \frac{V_{BATmin} - 5.5V}{250\ mA}$$

$$5.5V = V_{OFF} + 1.0V$$

Where:

250 mA = Peak current at power-on when VBB = 5.5V

Assume V_{BATmin} = 8V. Equation 1-1 shows 10Ω.

EQUATION 1-2:

$$R_{TP} \leq \frac{\Delta V_{RECESSIVE}}{I_{REGMAX}}$$

Where:

ΔVRECESSIVE = Maximum variation tolerated on the recessive level

Assume ΔVRECESSIVE = 1V and IREGMAX = 50 mA. Equation 1-2 shows 20Ω.

EQUATION 1-3:

$$R_{TP} \leq \frac{\Delta Slope \times (V_{BATmin} - 1V)}{I_{REGMAX}}$$

Where:

ΔSlope = Maximum variation tolerated on the slope level

IREGMAX = Maximum current the current will provide to the load

V_{BATmin} > VOFF + 1.0V

Assume ΔSlope = 15%, VBATMIN = 8V and IREGMAX = 50 mA. Equation 1-2 shows 20Ω.

1.5.3 CBAT CAPACITOR

Selecting CBAT = 10 x CREG is recommended. However, this leads to a high value capacitor. Lower values for CBAT capacitor can be used with respect to some rules. In any case, the voltage at the VBB pin should remain above VOFF when the device is turned on.

The current peak at start-up (due to the fast charge of the CREG and CBAT capacitors) may induce a significant drop on the VBB pin. This drop is proportional to the impedance of the VBAT connection (see Figure 1-7).

The VBAT connection is mainly inductive and resistive. Therefore, it can be modeled as a resistor (RTOT) in series with an inductor (L). RTOT and L can be measured.

The following formula gives an indication of the minimum value of CBAT using RTOT and L:

EQUATION 1-4:

$$\frac{C_{BAT}}{C_{REG}} = \sqrt{\frac{100L^2 + R_{TOT}^2}{1 + L^2 + \frac{R_{TOT}^2}{100}}}$$

Where:

L = Inductor (measured in mH)

RTOT = RLINE + RTP (measured in Ω)

Equation 1-4 allows lower CBAT/CREG values than the 10x ratio we recommend.

Assume that we have a good quality VBAT connection with RTOT = 0.1Ω and L = 0.1 mH.

Solving the equation gives CBAT/CREG = 1.

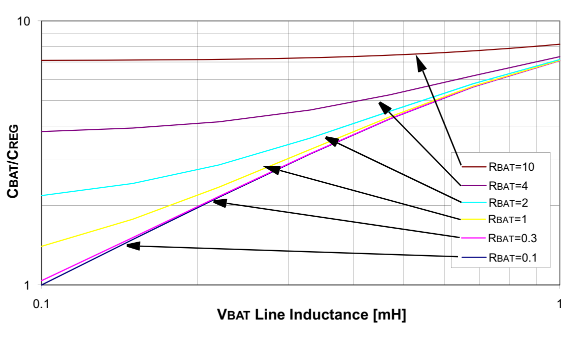
If we increase RTOT up to 1Ω, the result becomes CBAT/CREG = 1.4. However, if the connection is highly resistive or highly inductive (poor connection), the CBAT/CREG ratio greatly increases.

TABLE 1-5: CBAT/CREG RATIO BY VBAT CONNECTION TYPE

Connection Type	RTOT	L	CBAT/CREG Ratio
Good	0.1Ω	0.1 mH	1
Typical	1Ω	0.1 mH	1.4
Highly inductive	0.1Ω	1 mH	7
Highly resistive	10Ω	0.1 mH	7

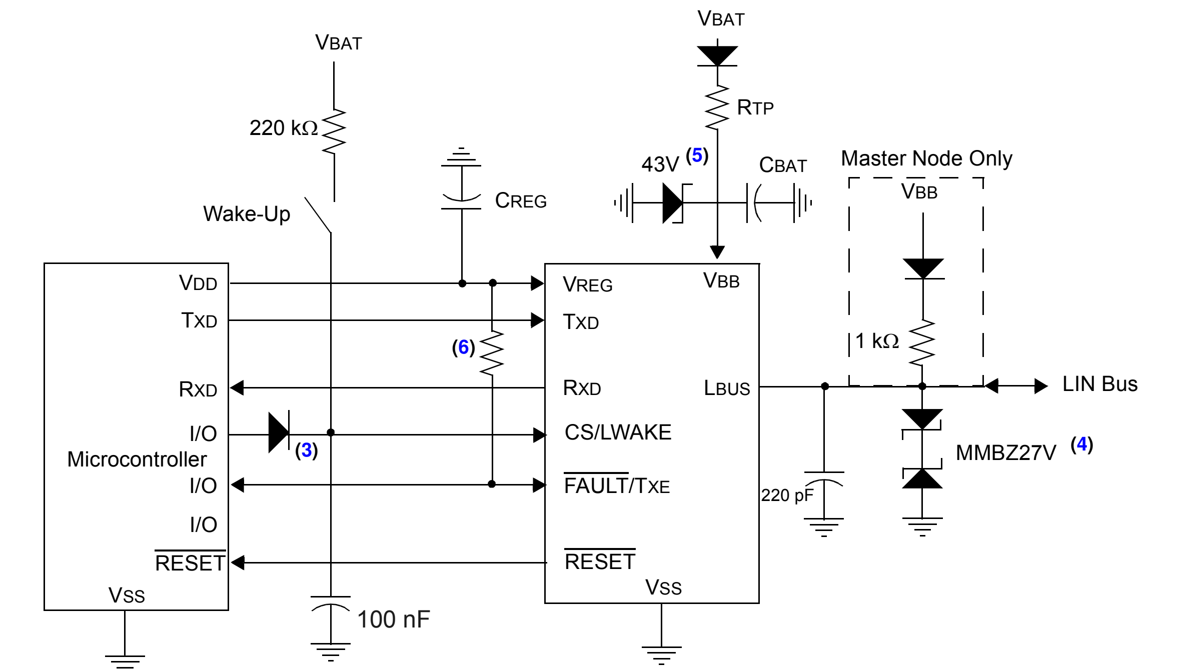
Figure 1-6 shows the minimum recommended CBAT/CREG ratio as a function of the impedance of the VBAT connection.

FIGURE 1-6: MINIMUM RECOMMENDED CBAT/CREG RATIO



1.6 Typical Applications

FIGURE 1-7: TYPICAL APPLICATION CIRCUIT



Note 1: CREG, the load capacitor, should be ceramic or tantalum rated for extended temperatures, 1.0 – 22 µF. See Figure 2-1 to select the correct ESR.

2: CBAT is the filter capacitor for the external voltage supply. Typically 10 x CREG, with no ESR restriction. See Figure 1-6 to select the minimum recommended value for CBAT. The RTP value is added to the line resistance.

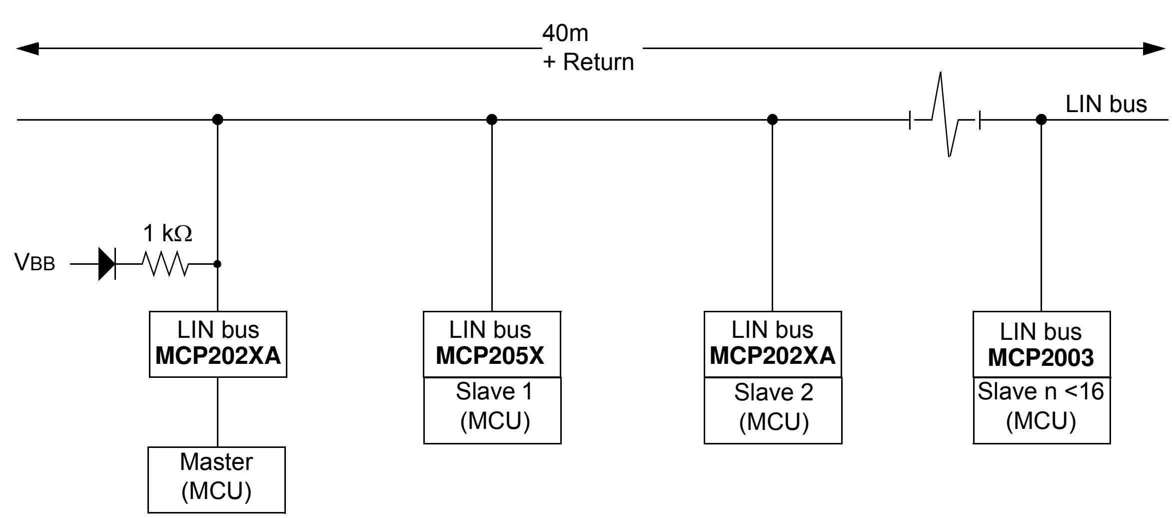
3: This diode is only needed if CS/LWAKE is connected to the VBAT supply.

4: ESD protection diode.

5: This component is for additional load dump protection.

6: An external 10 kΩ resistor is recommended for some applications.

FIGURE 1-8: TYPICAL LIN NETWORK CONFIGURATION



1.7 ICSP™ Considerations

The following should be considered when the MCP2021A/2A are connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller can be supplied from the programmer or from the MCP2021A/2A.
- The voltage on the V_{REG} pin should not exceed the maximum value of V_{REG} in DC Specifications.

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V_{IN} DC Voltage on R_{XD} and $\overline{RESET}$ .... -0.3V to V_{REG} + 0.3
V_{IN} DC Voltage on T_{XD}, CS/LWAKE, $\overline{FAULT}/T_{XE}$ .... -0.3 to +40V
V_{BB} Battery Voltage, continuous, non-operating (**Note 1**) .... -0.3 to +40V
V_{BB} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) (**Note 2**) .... -0.3 to +43V
V_{BB} Battery Voltage, transient ISO 7637 Test 1 .... -100V
V_{BB} Battery Voltage, transient ISO 7637 Test 2a .... +75V
V_{BB} Battery Voltage, transient ISO 7637 Test 3a .... -150V
V_{BB} Battery Voltage, transient ISO 7637 Test 3b .... +100V
V_{LBUS} Bus Voltage, continuous .... -18 to +30V
V_{LBUS} Bus Voltage, transient (**Note 3**) .... -27 to +43V
I_{LBUS} Bus Short Circuit Current Limit .... 200 mA
ESD protection on LIN, V_{BB} (IEC 61000-4-2) (**Note 4**) .... ±15 kV
ESD protection on LIN, V_{BB} (Human Body Model) (**Note 5**) .... ±8 kV
ESD protection on all other pins (Human Body Model) (**Note 5**) .... ±4 kV
ESD protection on all pins (Charge Device Model) (**Note 6**) .... ±1500V
ESD protection on all pins (Machine Model) (**Note 7**) .... ±200V
Maximum Junction Temperature .... 150°C
Storage Temperature .... -65 to +150°C

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: LIN 2.x compliant specification.
2: SAE J2602-2 compliant specification.
3: ISO 7637/1 load dump compliant (t < 500 ms).
4: According to IEC 61000-4-2, 330Ω, 150 pF and Transceiver EMC Test Specifications [2] to [4].
5: According to AEC-Q100-002/JESD22-A114.
6: According to AEC-Q100-011B.
7: According to AEC-Q100-003/JESD22-A115.

2.2 Nomenclature Used in This Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

LIN 2.1 Name	Term used in the following tables	Definition
V_{BAT}	*not used*	ECU operating voltage
V_{SUP}	V_{BB}	Supply voltage at device pin
V_{BUS_LIM}	I_{SC}	Current limit of driver
V_{BUSREC}	$V_{IH(LBUS)}$	Recessive state
V_{BUSDOM}	$V_{IL(LBUS)}$	Dominant state

2.3 DC Specifications

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C, C_{REG} = 10 µF.					
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Power						
V_{BB} Quiescent Operating Current	I_{BBQ}	—	—	200	µA	I_{OUT} = 0 mA L_{BUS} recessive V_{REG} = 5.0V
		—	—	200	µA	I_{OUT} = 0 mA L_{BUS} recessive V_{REG} = 3.3V
V_{BB} Ready Current	I_{BBRD}	—	—	100	µA	I_{OUT} = 0 mA L_{BUS} recessive V_{REG} = 5.0V
		—	—	100	µA	I_{OUT} = 0 mA L_{BUS} recessive V_{REG} = 3.3V
V_{BB} Transmitter-Off Current	I_{BBTO}	—	—	100	µA	With voltage regulator on, transmitter off, receiver on, $\overline{FAULT}/T_{XE} = V_{IL}$, CS = V_{IH}, V_{REG} = 5.0V
		—	—	100	µA	With voltage regulator on, transmitter off, receiver on, $\overline{FAULT}/T_{XE} = V_{IL}$, CS = V_{IH}, V_{REG} = 3.3V
V_{BB} Power-Down Current	I_{BBPD}	—	4.5	8	µA	With voltage regulator off, receiver on and transmitter off, $\overline{FAULT}/T_{XE} = V_{IH}$, $T_{XD} = V_{IH}$, CS = V_{IL}
V_{BB} Current with V_{SS} Floating	$I_{BBNOGND}$	-1	—	1	mA	V_{BB} = 12V, GND to V_{BB}, V_{LIN} = 0 – 18V
Microcontroller Interface						
High-Level Input Voltage (T_{XD}, $\overline{FAULT}/T_{XE}$)	V_{IH}	2.0	—	V_{REG} +0.3	V	
Low-Level Input Voltage (T_{XD}, $\overline{FAULT}/T_{XE}$)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (T_{XD}, $\overline{FAULT}/T_{XE}$)	I_{IH}	-2.5	—	0.4	µA	Input voltage = 4.0V ~800 kΩ internal adaptive pull-up
Low-Level Input Current (T_{XD}, $\overline{FAULT}/T_{XE}$)	I_{IL}	-10	—	—	µA	Input voltage = 0.5V ~800 kΩ internal adaptive pull-up
High-Level Input Voltage (CS/LWAKE)	V_{IH}	2.0	—	V_{BB}	V	Through a current-limiting resistor
Low-Level Input Voltage (CS/LWAKE)	V_{IL}	-0.3	—	0.8	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0W, TX = 0, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled. $V_{WK(LBUS)}$ is used to detect bus activities.

2.3 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C, C_{REG} = 10 µF.					
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
High-Level Input Current (CS/LWAKE)	I_{IH}	—	—	8.0	µA	Input voltage = $0.8V_{REG}$ ~1.3 MΩ internal pull-down to V_{SS}
Low-Level Input Current (CS/LWAKE)	I_{IL}	—	—	5.0	µA	Input voltage = $0.2V_{REG}$ ~1.3 MΩ internal pull-down to V_{SS}
Low-Level Output Voltage (R_{XD})	V_{OLRXD}	—	—	$0.2V_{REG}$	V	I_{OL} = 2 mA
High-Level Output Voltage (R_{XD})	V_{OHRXD}	$0.8V_{REG}$	—	—	V	I_{OH} = 2 mA
Low-Level Output Voltage ($\overline{FAULT}/T_{XE}$)	V_{OLOD}	—	—	1.0	V	I_{OL} = 4 mA
Low-Level Output Voltage ($\overline{RESET}$)	V_{OLRST}	—	—	1.0	V	I_{OL} = 4 mA
Bus Interface						
High-Level Input Voltage	$V_{IH(LBUS)}$	0.6 V_{BB}	—	—	V	Recessive state
Low-Level Input Voltage	$V_{IL(LBUS)}$	-8	—	0.4 V_{BB}	V	Dominant state
Input Hysteresis	V_{HYS}	—	—	0.175 V_{BB}	V	$V_{IH(LBUS)} – V_{IL(LBUS)}$
Low-Level Output Current	$I_{OL(LBUS)}$	40	—	200	mA	Output voltage = 0.1 V_{BB}, V_{BB} = 12V
Pull-Up Current on Input	$I_{PU(LBUS)}$	-180	—	-72	µA	~30 kΩ internal pull-up @ $V_{IH(LBUS)}$ = 0.7 V_{BB}, V_{BB} = 12V
Short Circuit Current Limit	I_{SC}	50	—	200	mA	**Note 1**
High-Level Output Voltage	$V_{OH(LBUS)}$	0.8 V_{BB}	—	V_{BB}	V	
Driver Dominant Voltage	V_{LOSUP}	—	—	1.1	V	V_{BB} = 7.3V R_{LOAD} = 1000Ω
	V_{HISUP}	—	—	1.2	V	V_{BB} = 18V R_{LOAD} = 1000Ω
Input Leakage Current (at the receiver during dominant bus level)	$I_{BUS\_PAS\_DOM}$	-1	—	—	mA	Driver off V_{BUS} = 0V V_{BB} = 12V
Input Leakage Current (at the receiver during recessive bus level)	$I_{BUS\_PAS\_REC}$	-20	—	20	µA	Driver off 8V < V_{BB} < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{BB}$
Leakage Current (disconnected from ground)	$I_{BUS\_NO\_GND}$	-10	—	+10	µA	GND_{DEVICE} = V_{BB} 0V < V_{BUS} < 18V V_{BB} = 12V
Leakage Current (disconnected from V_{BB})	$I_{BUS\_NO\_PWR}$	-10	—	+10	µA	V_{BB} = GND 0 < V_{BUS} < 18V
Receiver Center Voltage	V_{BUS_CNT}	0.475 V_{BB}	0.5 V_{BB}	0.525 V_{BB}	V	$V_{BUS\_CNT} = (V_{IL(LBUS)} + V_{IH(LBUS)})/2$
Slave Termination	R_{SLAVE}	20	30	47	kΩ	**Note 2**

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0W, TX = 0, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled. $V_{WK(LBUS)}$ is used to detect bus activities.

2.3 DC Specifications (Continued)

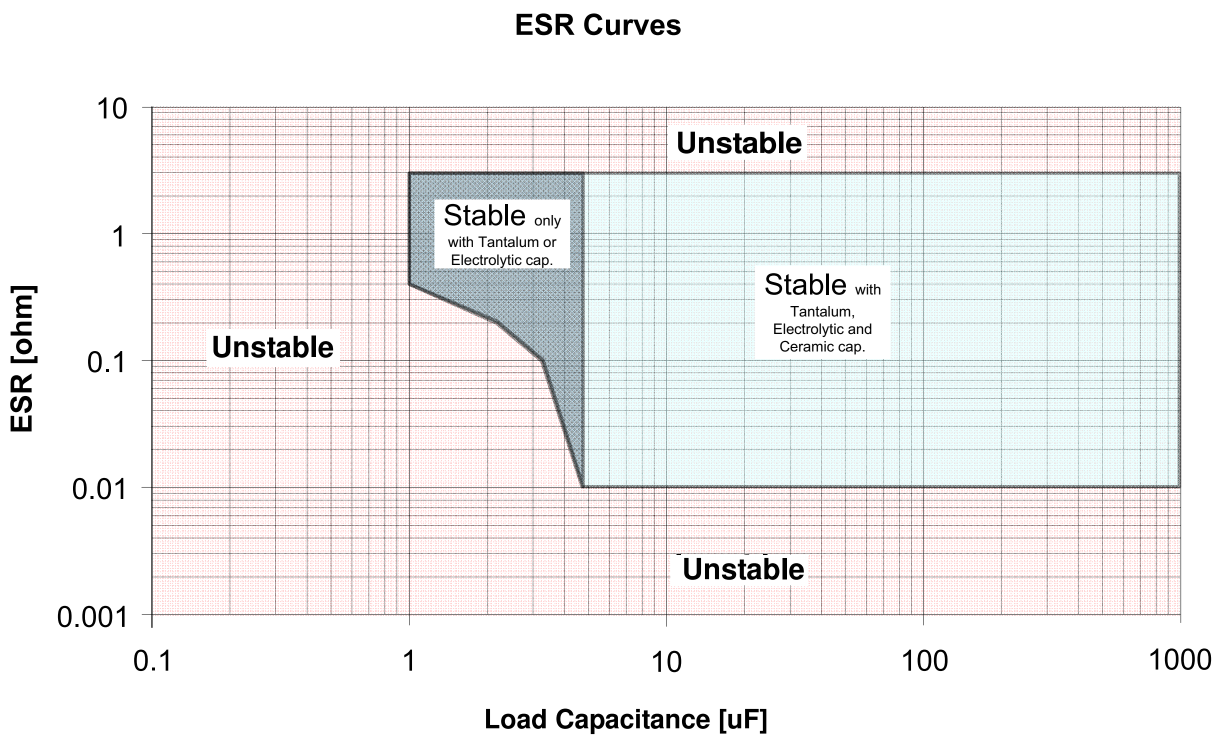
DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C, C_{REG} = 10 µF.					
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Capacitance of Slave Node	C_{SLAVE}	—	—	50	pF	Note 2
Wake-Up Voltage Threshold on LIN Bus	$V_{WK(LBUS)}$	—	—	3.4	V	Wake-up from Power-Down mode (Note 3)
Voltage Regulator – 5.0V						
Output Voltage Range	V_{REG}	4.85	5.00	5.15	V	0 mA < I_{OUT} < 70 mA
Line Regulation	ΔV_{OUT1}	—	10	50	mV	I_{OUT} = 1 mA 6.0V < V_{BB} < 18V
Load Regulation	ΔV_{OUT2}	—	10	50	mV	5 mA < I_{OUT} < 70 mA 6.0V < V_{BB} < 12V
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @ 10 – 20 kHz I_{LOAD} = 20 mA
Output Noise Voltage	eN	—	—	100	µV_{RMS}	10 Hz – 40 MHz C_{FILTER} = 10 µf C_{BP} = 0.1 µf I_{LOAD} = 20 mA
Shutdown Voltage Threshold	V_{SD}	3.5	—	4.0	V	See Figure 1-5 (Note 2)
Input Voltage to Turn-Off Output	V_{OFF}	3.9	—	4.5	V	
Input Voltage to Turn-On Output	V_{ON}	5.25	—	6.0	V	
Voltage Regulator – 3.3V						
Output Voltage	V_{REG}	3.20	3.30	3.40	V	0 mA < I_{OUT} < 70 mA
Line Regulation	ΔV_{OUT1}	—	10	50	mV	I_{OUT} = 1 mA 6.0V < V_{BB} < 18V
Load Regulation	ΔV_{OUT2}	—	10	50	mV	5 mA < I_{OUT} < 70 mA 6.0V < V_{BB} < 12V
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 V_{PP} @ 10 – 20 kHz I_{LOAD} = 20 mA
Output Noise Voltage	eN	—	—	100	µV_{RMS}/√Hz	10 Hz – 40 MHz C_{FILTER} = 10 µf C_{BP} = 0.1 µf I_{LOAD} = 20 mA
Shutdown Voltage Threshold	V_{SD}	2.5	—	2.7	V	See Figure 1-5 (Note 2)
Input Voltage to Turn-Off Output	V_{OFF}	3.9	—	4.5	V	
Input Voltage to Turn-On Output	V_{ON}	5.25	—	6	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0W, TX = 0, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: In Power-Down mode, normal LIN recessive/dominant threshold is disabled. $V_{WK(LBUS)}$ is used to detect bus activities.

FIGURE 2-1: ESR CURVES FOR LOAD CAPACITOR SELECTION



Note 1: The graph shows the minimum required capacitance after derating due to tolerance, temperature and voltage.

2.4 AC Specifications

AC Characteristics	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C.					
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Bus Interface – Constant Slope Time Parameters						
Slope Rising and Falling Edges	t_{SLOPE}	3.5	—	22.5	µs	7.3V ≤ V_{BB} ≤ 18V
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	5.0	µs	$t_{TRANSPD}$ = max. ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	µs	t_{RECPD} = max. (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver Rising Edge w.r.t. Falling Edge	t_{RECSYM}	-2.0	—	2.0	µs	t_{RECSYM} = max. (t_{RECPDF} – t_{RECPDR}) R_{RXD} = 2.4 kΩ to V_{CC} C_{RXD} = 20 pF
Symmetry of Propagation Delay of Transmitter Rising Edge w.r.t. Falling Edge	$t_{TRANSSYM}$	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max. ($t_{TRANSPDF}$ – $t_{TRANSPDR}$)
Bus Dominant Time-Out Time	$t_{TO(LIN)}$	—	25	—	ms	
Time to Sample $\overline{FAULT}$/T_{XE} for Bus Conflict Reporting	t_{FAULT}	—	—	32.5	µs	t_{FAULT} = max. ($t_{TRANSPD}$ + t_{SLOPE} + t_{RECPD})
Duty Cycle 1 @ 20.0 kbps		0.396	—	—	%t_{BIT}	C_{BUS}; R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.744 x V_{BB}, $TH_{DOM(MAX)}$ = 0.581 x V_{BB}, V_{BB} = 7.0V – 18V; t_{BIT} = 50 µs. D1 = $t_{BUS\_REC(MIN)}$/2 x t_{BIT}
Duty Cycle 2 @ 20.0 kbps		—	—	0.581	%t_{BIT}	C_{BUS}; R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.284 x V_{BB}, $TH_{DOM(MAX)}$ = 0.422 x V_{BB}, V_{BB} = 7.6V – 18V; t_{BIT} = 50 µs. D2 = $t_{BUS\_REC(MAX)}$/2 x t_{BIT}
Duty Cycle 3 @ 10.4 kbps		0.417	—	—	%t_{BIT}	C_{BUS}; R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.778 x V_{BB}, $TH_{DOM(MAX)}$ = 0.616 x V_{BB}, V_{BB} = 7.0V – 18V; t_{BIT} = 96 µs. D3 = $t_{BUS\_REC(MIN)}$/2 x t_{BIT}

Note 1: Time depends on external capacitance and load. Test condition: C_{REG} = 4.7 µF, no resistor load.
2: Characterized, not 100% tested.

2.4 AC Specifications (Continued)

AC Characteristics	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C.					
Parameter	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Duty Cycle 4 @ 10.4 kbps		—	—	0.590	%t_{BIT}	C_{BUS}; R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω $TH_{REC(MAX)}$ = 0.251 x V_{BB}, $TH_{DOM(MAX)}$ = 0.389 x V_{BB}, V_{BB} = 7.6V – 18V; t_{BIT} = 96 µs. D4 = $t_{BUS\_REC(MAX)}$/2 x t_{BIT}
Voltage Regulator						
Bus Activity Debounce time	t_{BDB}	30	80	250	µs	
Bus Activity to Voltage Regulator Enabled	$t_{BACTIVE}$	35	—	200	µs	
Voltage Regulator Enabled to Ready	t_{VEVR}	300	—	1200	µs	Note 1
Chip Select to Ready Mode	t_{CSR}	—	—	230	µs	
Chip Select to Power-Down	t_{CSPD}	—	—	330	µs	Note 2
Short Circuit to Shutdown	$t_{SHUTDOWN}$	20	—	100	µs	
$\overline{RESET}$ Timing						
V_{REG} OK Detect to $\overline{RESET}$ Inactive	t_{RPU}	—	—	60	µs	
V_{REG} Not OK Detect to $\overline{RESET}$ Active	t_{RPD}	—	—	60	µs	

Note 1: Time depends on external capacitance and load. Test condition: C_{REG} = 4.7 µF, no resistor load.

2: Characterized, not 100% tested.

2.5 Thermal Specifications

Parameter	Sym	Min	Typ	Max	Units	Test Conditions
Specified Temperature Range	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Recovery Temperature	$\theta_{RECOVERY}$	—	+140	—	°C	
Shutdown Temperature	$\theta_{SHUTDOWN}$	—	+150	—	°C	
Short Circuit Recovery Time	t_{THERM}	—	1.5	5.0	ms	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-DFN	θ_{JA}	—	48	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	90.8	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The maximum power dissipation is a function of T_{JMAX}, θ_{JA}, and ambient temperature, T_A. The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} – T_A) \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP2021A/2A will go into thermal shutdown.

2.6 Typical Performance Curves

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C.

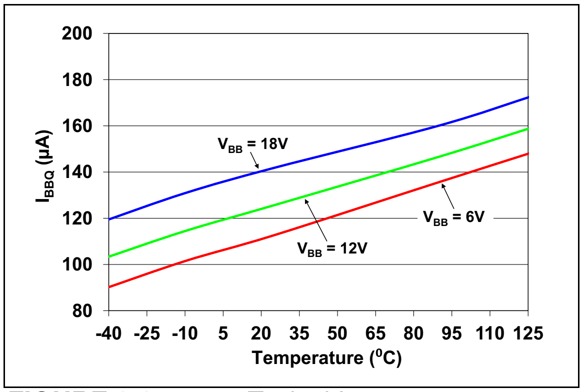


FIGURE 2-2: *Typical I_{BBQ} vs. Temperature – 5.0V.*

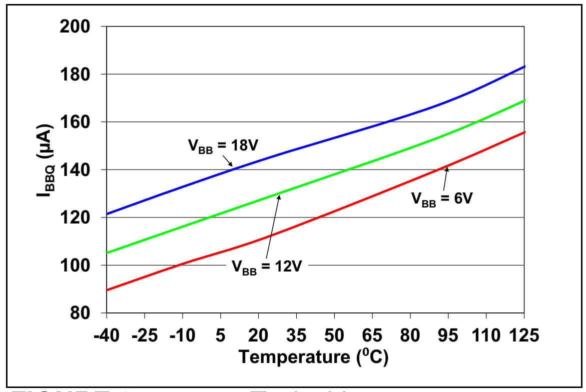


FIGURE 2-5: *Typical I_{BBQ} vs. Temperature – 3.3V.*

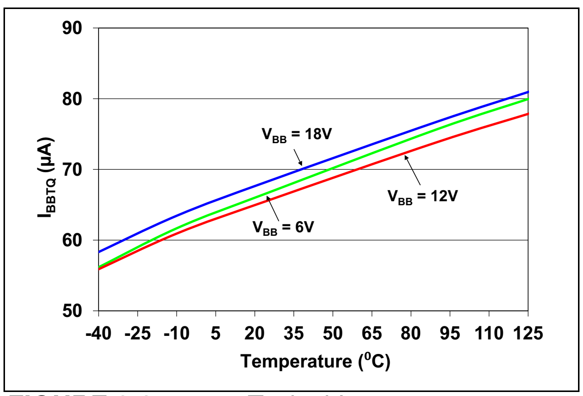


FIGURE 2-3: *Typical I_{BBTO} vs. Temperature – 5.0V.*

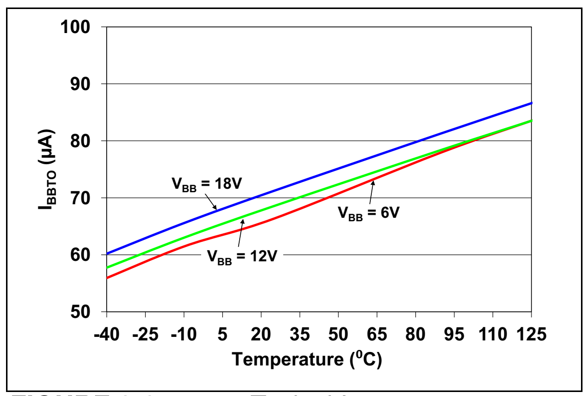


FIGURE 2-6: *Typical I_{BBTO} vs. Temperature – 3.3V.*

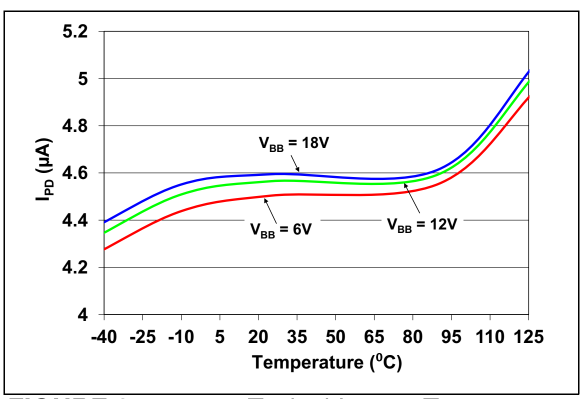


FIGURE 2-4: *Typical I_{PD} vs. Temperature – 5.0V.*

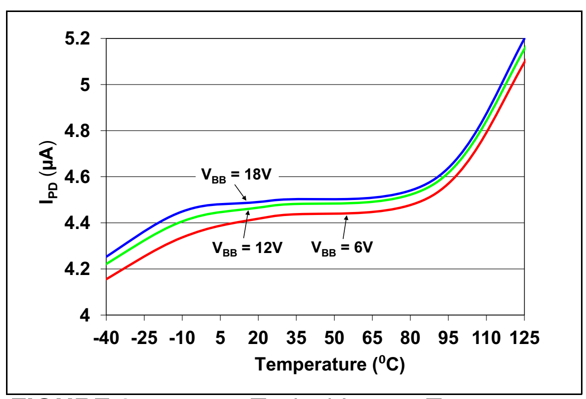


FIGURE 2-7: *Typical I_{PD} vs. Temperature – 3.3V.*

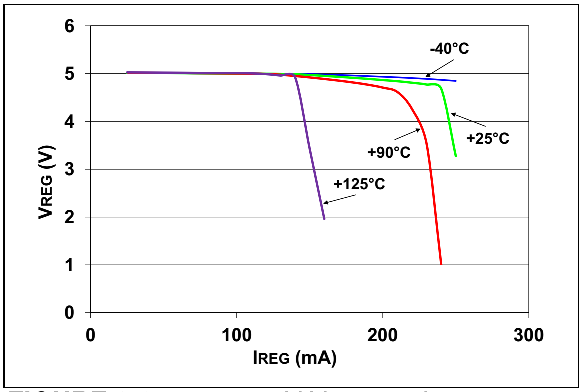


FIGURE 2-8: *5.0V VREG vs. IREG at VBB = 12V.*

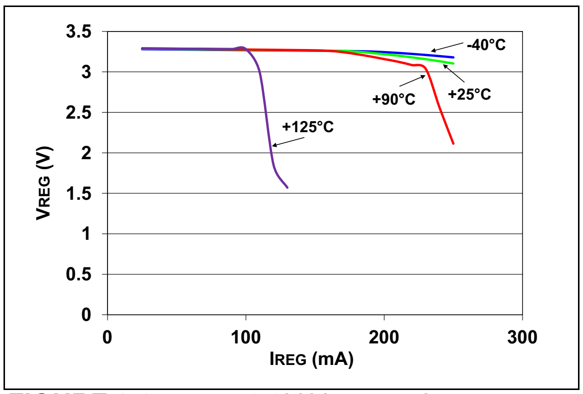


FIGURE 2-9: *3.3V VREG vs. IREG at VBB = 12V.*

2.7 Timing Diagrams and Specifications

FIGURE 2-10: BUS TIMING DIAGRAM

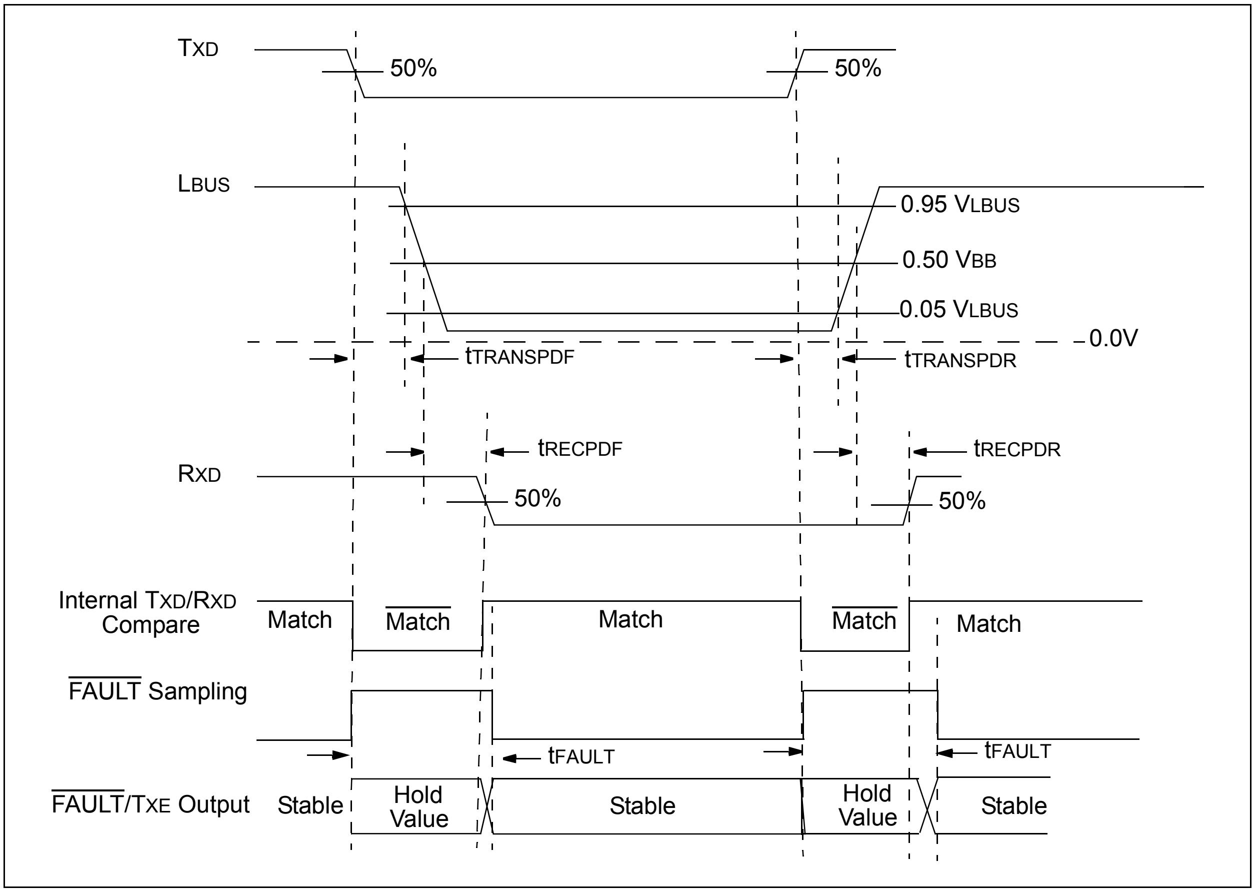


FIGURE 2-11: REGULATOR CS/LWAKE TIMING DIAGRAM

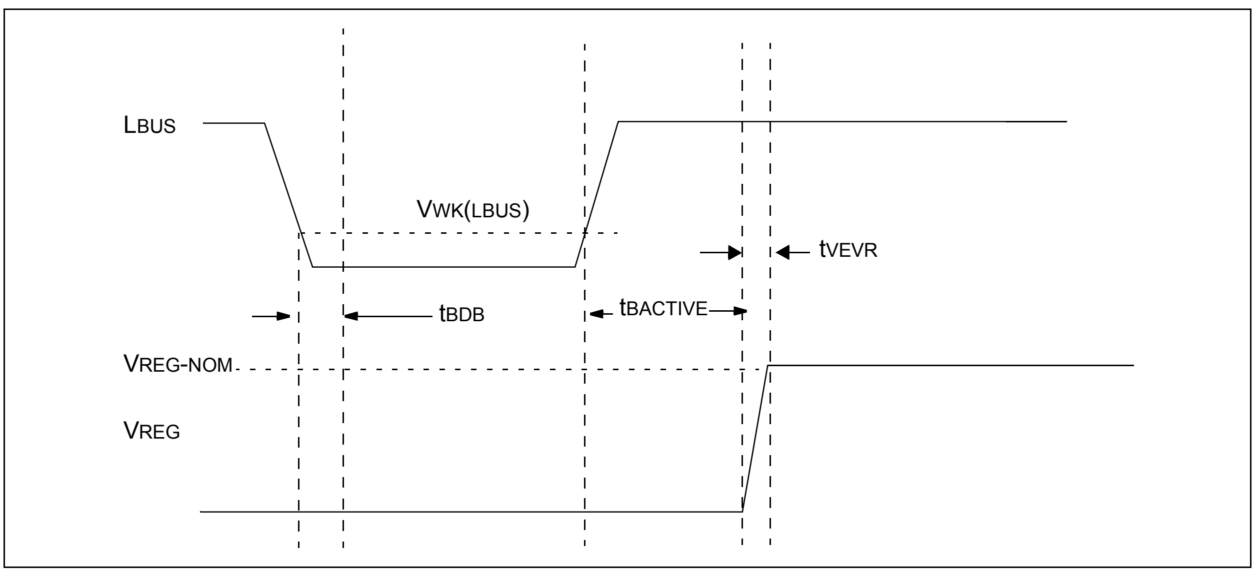


FIGURE 2-12: CS/LWAKE, REGULATOR AND $\overline{\text{RESET}}$ TIMING DIAGRAM