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MCP2030

Three-Channel Analog Front-End Device

Device Features:

- Three input pins for analog input signals
- High input detection sensitivity (3 mV_{PP}, typical)
- High modulation depth sensitivity (as low as 8%)
- Three output selections:
  - Demodulated data
  - Carrier clock
  - RSSI
- Input carrier frequency: 125 kHz, typical
- Input data rate: 10 Kbps, maximum
- 8 internal Configuration registers
- Bidirectional transponder communication (LF talk back)
- Programmable antenna tuning capacitance (up to 63 pF, 1 pF/step)
- Programmable output enable filter
- Low standby current: 4 μA (with 3 channels enabled), typical
- Low operating current: 13 μA (with 3 channels enabled), typical
- Serial Peripheral Interface (SPI™) with external devices
- Supports Battery Back-Up mode and batteryless operation with external circuits
- Industrial and Extended Temperature Range: -40°C to +85°C (industrial)

Typical Applications:

- Automotive industry applications:
  - Passive Keyless Entry (PKE) transponder
  - Remote door locks and gate openers
  - Engine immobilizer
  - LF initiator sensor for tire pressure monitoring systems
- Security Industry applications:
  - Long range access control transponder
  - Parking lot entry transponder
  - Hands-free apartment door access
  - Asset control and management

Description:

The MCP2030 is a stand-alone Analog Front-End (AFE) device for Low-Frequency (LF) sensing and bidirectional communication applications. The device has eight internal Configuration registers which are readable and programmable, except the read-only STATUS register, by an external device.

The device has three low-frequency input channels. Each input channel can be individually enabled or disabled. The device can detect an input signal with amplitude as low as ~1 mV_{PP} and can demodulate an amplitude-modulated input signal with as low as 8% modulation depth. The device can also transmit data by clamping and unclamping the input LC antenna voltage.

The device can output demodulated data, carrier clock or RSSI current depending on the register setting. The demodulated data and carrier clock outputs are available on the LFDATA pin, while the RSSI output is available on the RSSI pin. The RSSI current output is linearly proportional to the input signal strength.

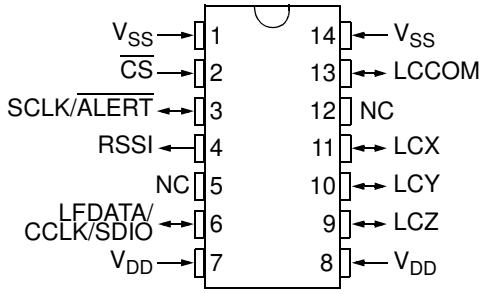
The device has programmable internal tuning capacitors for each input channel. The user can program these capacitors up to 63 pF, 1 pF per step. These internal tuning capacitors can be used effectively for fine-tuning of the external LC resonant circuit.

The device is optimized for very low current consumption and has various battery-saving low-power modes (Sleep, Standby, Active). The device can also be operated in Battery Back-up and Batteryless modes using a few external components.

This device is available in 14-pin PDIP, SOIC, and TSSOP packages. This device is also used as the AFE in the PIC16F639.

Package Types:

MCP2030
PDIP, SOIC, TSSOP



NOTES:

1.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

Ambient temperature under bias.....-40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V
Voltage on all other pins with respect to V_{SS} .....-0.3V to (V_{DD} + 0.3V)
Maximum current out of V_{SS} pin .....300 mA
Maximum current into V_{DD} pin .....250 mA
Maximum LC Input Voltage (LCX, LCY, LCZ) loaded, with device.....10.0 V_{PP}
Maximum LC Input Voltage (LCX, LCY, LCZ) unloaded, without device.....700.0 V_{PP}
Maximum Input Current (rms) into device per LC Channel.....10 mA
Human Body ESD rating.....2000 (min.) V
Machine Model ESD rating .....200 (min.) V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Electrical Specifications: Standard Operating Conditions (unless otherwise stated)
Operating temperature -40°C ≤ T_A ≤ +85°C
LC Signal Input Sinusoidal 300 mV_{PP}
Carrier Frequency 125 kHz
LCCOM connected to V_{SS}

Parameters	Sym.	Min.	Typ†	Max.	Units	Conditions
Supply Voltage	V_{DD}	2.0	3.0	3.6	V	
V_{DD} Start Voltage to ensure internal Power-on Reset signal	V_{POR}	—	—	1.8	V	
Modulation Transistor-on Resistance	R_M	—	50	100	Ω	V_{DD} = 3.0V
Active Current (detecting signal) 1 LC Input Channel Receiving Signal 3 LC Input Channel Receiving Signals	I_{ACT}	 — —	 10 13	 — 18	 µA µA	$\overline{CS}$ = V_{DD} Input = Continuous Wave (CW); Amplitude = 300 mV_{PP}. All channels enabled.
Standby Current (wait to detect signal) 1 LC Input Channel Enabled 2 LC Input Channels Enabled 3 LC Input Channels Enabled	I_{STDBY}	 — — —	 2 3 4	 5 6 7	 µA µA µA	$\overline{CS}$ = V_{DD}; $\overline{ALERT}$ = V_{DD}
Sleep Current	I_{SLEEP}	—	0.2	1	µA	$\overline{CS}$ = V_{DD}; $\overline{ALERT}$ = V_{DD}
Analog Input Leakage Current LCX, LCY, LCZ LCCOM	I_{AIL}	 — —	 — —	 ± 1 ± 1	 µA µA	V_{DD} = 3.6V, V_{SS} ≤ V_{IN} ≤ 1V with respect to ground. Internal tuning capacitors are switched off, tested in Sleep mode.
Digital Input Low Voltage	V_{IL}	V_{SS}	—	0.3 V_{DD}	V	SCLK, SDI, $\overline{CS}$
Digital Input High Voltage	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	SCLK, SDI, $\overline{CS}$
Digital Input Leakage Current **(Note 1)** SDI SCLK, $\overline{CS}$	I_{IL}	 — —	 — —	 ± 1 ± 1	 µA µA	V_{DD} = 3.6V V_{SS} ≤ V_{PIN} ≤ V_{DD} V_{PIN} ≤ V_{DD}
Digital Output Low Voltage $\overline{ALERT}$, LFDATA/SDIO	V_{OL}	—	—	V_{SS} + 0.4	V	Analog Front-End section I_{OL} = 1.0 mA, V_{DD} = 2.0V
Digital Output High Voltage $\overline{ALERT}$, LFDATA/SDIO	V_{OH}	V_{DD} - 0.5	—	—	V	I_{OH} = -400 µA, V_{DD} = 2.0V
Digital Input Pull-Up Resistor $\overline{CS}$, SCLK	R_{PU}	50	200	350	kΩ	V_{DD} = 3.6V

* These parameters are characterized but not tested.
† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
Note 1: Negative current is defined as current sourced by the pin.

AC Characteristics

Electrical Specifications: Standard Operating Conditions (unless otherwise stated)
Supply Voltage $2.0V \le V_{DD} \le 3.6V$
Operating temperature $-40°C \le T_A \le +85°C$
LCCOM connected to V_{SS}
LC Signal Input Sinusoidal 300 mV_{PP}
Carrier Frequency 125 kHz
LCCOM connected to V_{SS}

Parameters	Sym.	Min.	Typ†	Max.	Units	Conditions
Input Sensitivity	V_{SENSE}	1	3.0	6	mV_{PP}	V_{DD} = 3.0V Output enable filter disabled AGCSIG = 0; MODMIN = 00 (33% modulation depth setting) Input = Continuous Wave (CW) Output = Logic level transition from low-to-high at sensitivity level for CW input.
Coil de-Q'ing Voltage - RF Limiter (R_{FLM}) must be active	V_{DE_Q}	3	—	5	V	V_{DD} = 3.0V, Force I_{IN} = 5 µA (worst case)
RF Limiter Turn-on Resistance (LCX, LCY, LCZ)	R_{FLM}	—	300	700	Ω	V_{DD} = 2.0V, V_{IN} = 8 V_{DC}
Sensitivity Reduction	S_{ADJ}	— —	0 -30	— —	dB dB	V_{DD} = 3.0V No sensitivity reduction selected Max. reduction selected Monotonic increment in attenuation value from setting = 0000 to 1111 by design
Minimum Modulation Depth 60% setting 33% setting 14% setting 8%	V_{IN_MOD}	 — — —	 60 33 14 8	 84 49 26	 % % % %	V_{DD} = 3.0V See **Section 5.21 "Minimum Modulation Depth Requirement for Input Signal"**. See Modulation Depth Definition in Figure 5-5.
Carrier frequency	$F_{CARRIER}$	—	125	—	kHz	
Input modulation frequency	F_{MOD}	—	—	10	kHz	Input data rate with NRZ data format. V_{DD} = 3.0V Minimum modulation depth setting = 33% Input conditions: Amplitude = 300 mV_{PP} Modulation depth = 100%
LCX Tuning Capacitor	C_{TUNX}	— 44	0 59	— 82	pF pF	V_{DD} = 3.0V, Config. Reg. 1, bits <6:1> Setting = 000000 63 pF ±30% Config. Reg. 1, bits <6:1> Setting = 111111 63 steps, approx. 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
LCY Tuning Capacitor	C_{TUNY}	— 44	0 59	— 82	pF pF	V_{DD} = 3.0V, Config. Reg. 2, bits <6:1> Setting = 000000 63 pF ±30% Config. Reg. 2, bits <6:1> Setting = 111111 63 steps, approx. 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
LCZ Tuning Capacitor	C_{TUNZ}	— 44	0 59	— 82	pF pF	V_{DD} = 3.0V, Config. Reg. 3, bits<6:1> Setting = 000000 63 pF ±30% Config. Reg. 3, bits<6:1> Setting = 111111 63 steps, approx. 1 pF/step Monotonic increment in capacitor value from setting = 000000 to 111111 by design
Q of Internal Tuning Capacitors	Q_C	50 *	—	—		
Demodulator Charge Time (delay time of demodulated output to rise)	T_{DR}	—	50	—	µs	V_{DD} = 3.0V Minimum modulation depth setting = 33% Input conditions: Amplitude = 300 mV_{PP} Modulation depth = 100%

* Parameter is characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required output enable filter high time must account for input path analog delays (= T_{OEH} - T_{DR} + T_{DF}).

2: Required output enable filter low time must account for input path analog delays (= T_{OEL} + T_{DR} - T_{DF}).

AC Characteristics (Continued)

Electrical Specifications: Standard Operating Conditions (unless otherwise stated)
Supply Voltage $2.0V \le V_{DD} \le 3.6V$
Operating temperature $-40°C \le T_A \le +85°C$
LCCOM connected to V_{SS}
LC Signal Input Sinusoidal 300 mV_{PP}
Carrier Frequency 125 kHz
LCCOM connected to V_{SS}

Parameters	Sym.	Min.	Typ†	Max.	Units	Conditions
Demodulator Discharge Time (delay time of demodulated output to fall)	T_{DF}	—	50	—	µs	V_{DD} = 3.0V MOD depth setting = 33% Input conditions: Amplitude = 300 mV_{PP} Modulation depth = 100%
Rise time of LFDATA	TR_{LFDATA}	—	0.5	—	µs	V_{DD} = 3.0V. Time is measured from 10% to 90% of amplitude
Fall time of LFDATA	TF_{LFDATA}	—	0.5	—	µs	V_{DD} = 3.0V Time is measured from 10% to 90% of amplitude
AGC stabilization time (T_{AGC} + T_{PAGC})	T_{STAB}	4	—	—	ms	
AGC initialization time	T_{AGC}	—	3.5	—	ms	
High time after AGC initialization time	T_{PAGC}	—	62.5	—	µs	
Gap time after AGC stabilization time	T_{GAP}	200	—	—	µs	
Time element of pulse	T_E	100	—	—	µs	Minimum pulse width
Time from exiting Sleep or POR to being ready to receive signal	T_{RDY}	—	—	50*	ms	
Minimum time AGC level must be held after receiving AGC Preserve command	T_{PRES}	5*	—	—	ms	AGC level must not change more than 10% during T_{PRES}.
Internal RC oscillator frequency	F_{OSC}	27	32	35.5	kHz	Internal clock trimmed at 32 kHz during test
Inactivity timer time-out	T_{INACT}	13.5	16	17.75	ms	512 cycles of RC oscillator @ F_{OSC}
Alarm timer time-out	T_{ALARM}	27	32	35.5	ms	1024 cycles of RC oscillator @ F_{OSC}
LC Pin Input Resistance for LCX, LCY, LCZ pins	R_{IN}	—	800*	—	kΩ	LCCOM grounded, V_{DD} = 3V, $F_{CARRIER}$ = 125 kHz.
LC Pin Input Parasitic Capacitance for LCX, LCY, LCZ pins	C_{IN}	—	24*	—	pF	LCCOM grounded, V_{DD} = 3V, $F_{CARRIER}$ = 125 kHz.
Minimum output enable filter high time **OEH (Bits Config0<8:7>)** 01 = 1 ms 10 = 2 ms 11 = 4 ms 00 = Filter Disabled	T_{OEH}	 32 (~1 ms) 64 (~2 ms) 128 (~4 ms) —	 — — — —	 — — — —	 clock count	RC oscillator = F_{OSC} (see F_{OSC} specification for variations). Viewed from the pin input: **(Note 1)**
Minimum output enable filter low time **OEL (Bits Config0<6:5>)** 00 = 1 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms	T_{OEL}	 32 (~1 ms) 32 (~1 ms) 64 (~2 ms) 128 (~4 ms)	 — — — —	 — — — —	 clock count	RC oscillator = F_{OSC} Viewed from the pin input: **(Note 2)**
Maximum output enable filter period **OEH OEL T_{OEH} T_{OEL}** 01 00 = 1 ms 1 ms (Filter 1) 01 01 = 1 ms 1 ms (Filter 1) 01 10 = 1 ms 2 ms (Filter 2) 01 11 = 1 ms 4 ms (Filter 3) 10 00 = 2 ms 1 ms (Filter 4) 10 01 = 2 ms 1 ms (Filter 4) 10 10 = 2 ms 2 ms (Filter 5) 10 11 = 2 ms 4 ms (Filter 6) 11 00 = 4 ms 1 ms (Filter 7) 11 01 = 4 ms 1 ms (Filter 7) 11 10 = 4 ms 2 ms (Filter 8) 11 11 = 4 ms 4 ms (Filter 9) 00 XX = Filter Disabled	T_{OET}	 — — — — — — — — — — — — —	 — — — — — — — — — — — — —	 96 (~3 ms) 96 (~3 ms) 128 (~4 ms) 192 (~6 ms) 128 (~4 ms) 128 (~4 ms) 160 (~5 ms) 250 (~8 ms) 192 (~6 ms) 192 (~6 ms) 256 (~8 ms) 320 (~10 ms) —	 clock count	RC oscillator = F_{OSC} LFDATA output appears as long as input signal level is greater than V_{SENSE}.

* Parameter is characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Required output enable filter high time must account for input path analog delays (= T_{OEH} - T_{DR} + T_{DF}).

2: Required output enable filter low time must account for input path analog delays (= T_{OEL} + T_{DR} - T_{DF}).

AC Characteristics (Continued)

Electrical Specifications: Standard Operating Conditions (unless otherwise stated)
Supply Voltage $2.0V \le V_{DD} \le 3.6V$
Operating temperature $-40°C \le T_A \le +85°C$
LCCOM connected to V_{SS}
LC Signal Input Sinusoidal 300 mV_{PP}
Carrier Frequency 125 kHz
LCCOM connected to V_{SS}

Parameters	Sym.	Min.	Typ†	Max.	Units	Conditions
RSSI current output	I_{RSSI}	— 6 —	0.65 12 100	2 20.3 —	µA µA µA	V_{IN} = 37 mV_{PP} V_{IN} = 370 mV_{PP} V_{DD} = 3.0V, V_{IN} = 0 to 4 V_{PP} Linearly increases with input signal amplitude. Tested at V_{IN} = 37 mV_{PP}, 100 mV_{PP}, and 370 mV_{PP} at +25ºC.
RSSI current linearity	ILR_{RSSI}	-15	—	15	%	Tested at room temperature only (see Equation 5-1 and Figure 5-7 for test method).

* Parameter is characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.
Note 1: Required output enable filter high time must account for input path analog delays (= T_{OEH} - T_{DR} + T_{DF}).
2: Required output enable filter low time must account for input path analog delays (= T_{OEL} + T_{DR} - T_{DF}).

SPI Timing

Electrical Specifications: Standard Operating Conditions (unless otherwise stated)
Supply Voltage $2.0V \le V_{DD} \le 3.6V$
Operating temperature $-40°C \le T_A \le +85°C$
LC Signal Input Sinusoidal 300 mV_{PP}
Carrier Frequency 125 kHz
LCCOM connected to V_{SS}

Parameters	Sym.	Min.	Typ†	Max.	Units	Conditions
SCLK Frequency	F_{SCLK}	—	—	3	MHz	
$\overline{CS}$ fall to first SCLK edge setup time	T_{CSSC}	100	—	—	ns	
SDI setup time	T_{SU}	30	—	—	ns	
SDI hold time	T_{HD}	50	—	—	ns	
SCLK high time	T_{HI}	150	—	—	ns	
SCLK low time	T_{LO}	150	—	—	ns	
SDO setup time	T_{DO}	—	—	150	ns	
SCLK last edge to $\overline{CS}$ rise setup time	T_{SCCS}	100	—	—	ns	
$\overline{CS}$ high time	T_{CSH}	500	—	—	ns	
$\overline{CS}$ rise to SCLK edge setup time	T_{CS1}	50	—	—	ns	
SCLK edge to $\overline{CS}$ fall setup time	T_{CS0}	50	—	—	ns	SCLK edge when $\overline{CS}$ is high
Rise time of SPI data (SPI Read command)	TR_{SPI}	—	10	—	ns	V_{DD} = 3.0V. Time is measured from 10% to 90% of amplitude
Fall time of SPI data (SPI Read command)	TF_{SPI}	—	10	—	ns	V_{DD} = 3.0V. Time is measured from 90% to 10% of amplitude

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

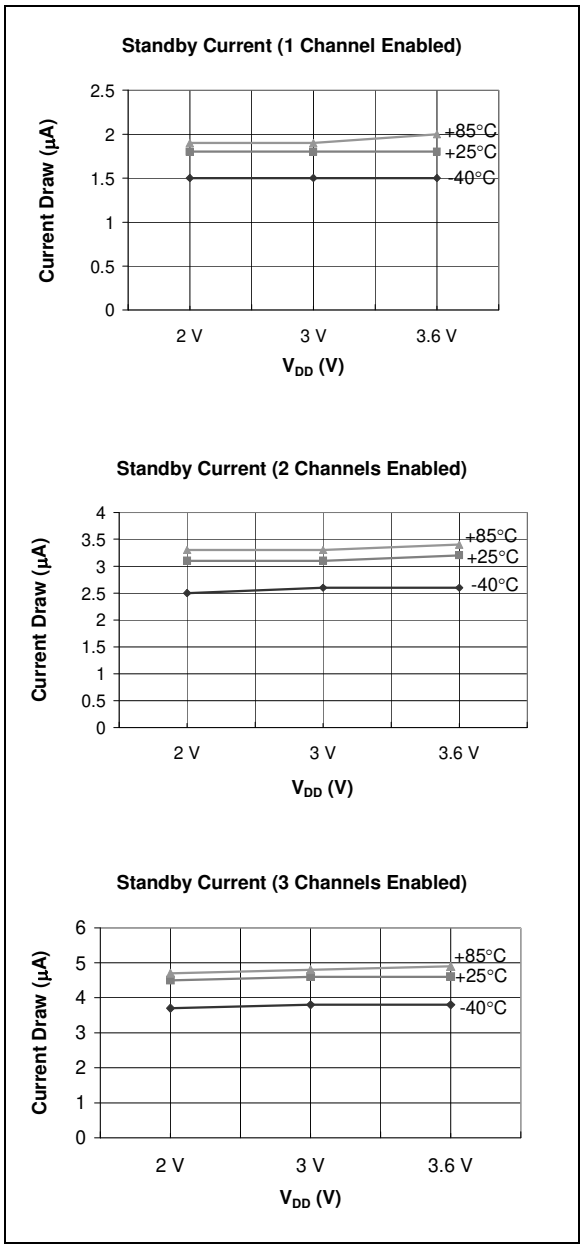


FIGURE 2-1: *Typical Standby Current.*

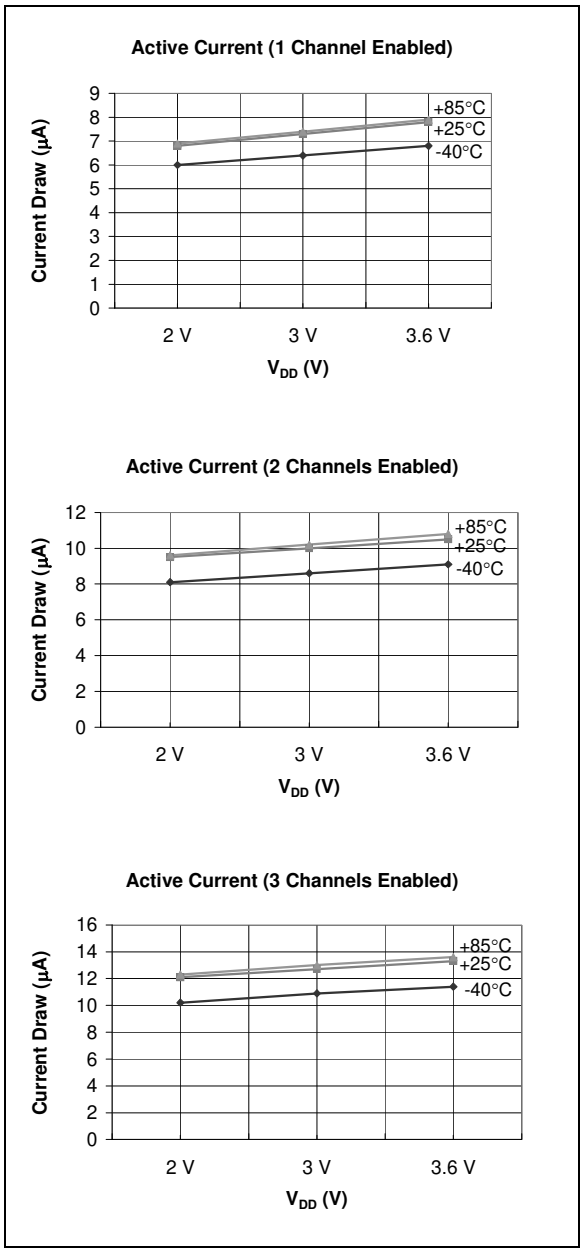


FIGURE 2-2: *Typical Active Current.*

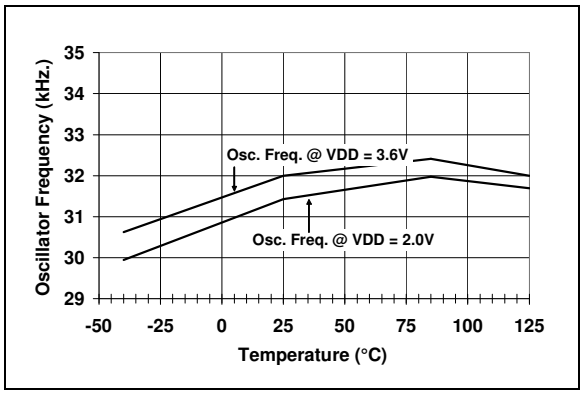


FIGURE 2-3: *Oscillator Frequency vs. Temperature, V_{DD} = 3.6V and 2.0V.*

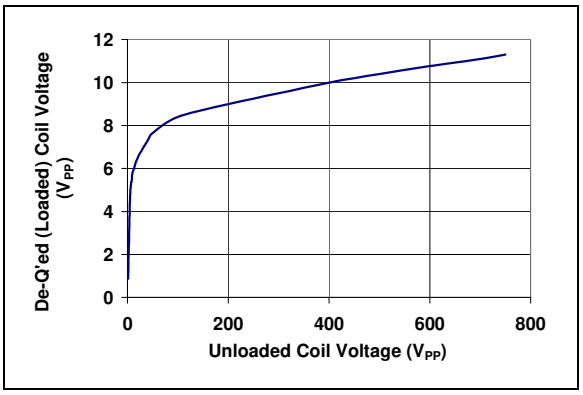


FIGURE 2-6: *De-Q'ed Voltage vs. Unloaded Coil Voltage.*

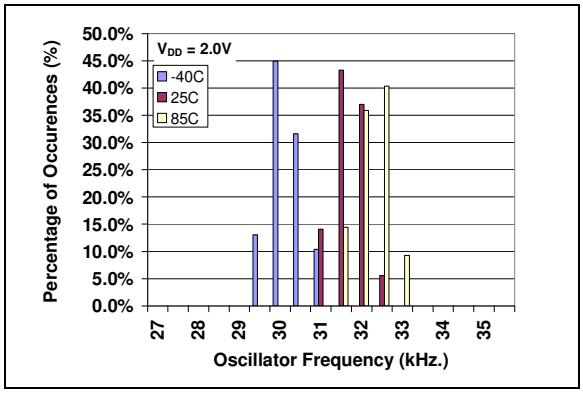


FIGURE 2-4: *Oscillator Frequency Histograms vs. Temperature, V_{DD} = 2V.*

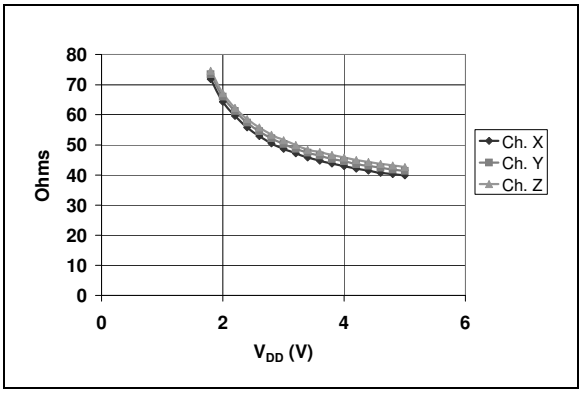


FIGURE 2-7: *Modulation Transistor-on Resistance (+25°C).*

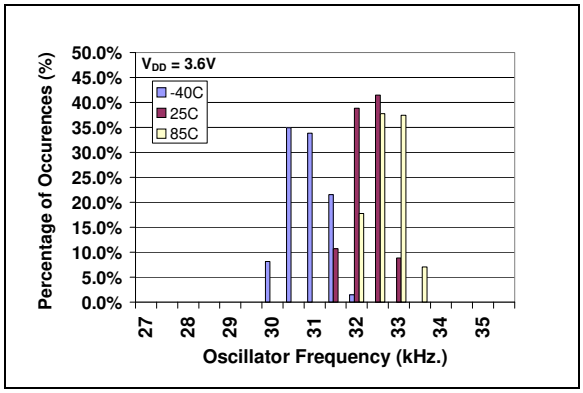


FIGURE 2-5: *Oscillator Frequency Histograms vs. Temperature at V_{DD} = 3V.*

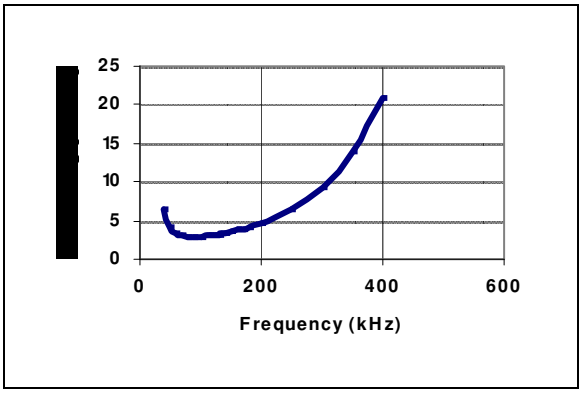


FIGURE 2-8: *Channel Sensitivity vs. Bandwidth.*

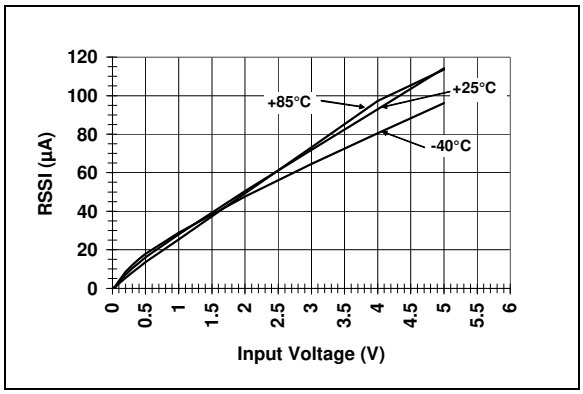


FIGURE 2-9: *Typical RSSI Output Current vs. Input Signal Strength.*

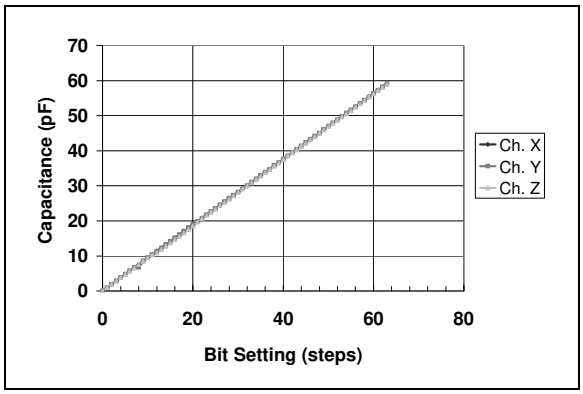


FIGURE 2-11: *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting (V_{DD} = 3V,Temperature = -40°C.*

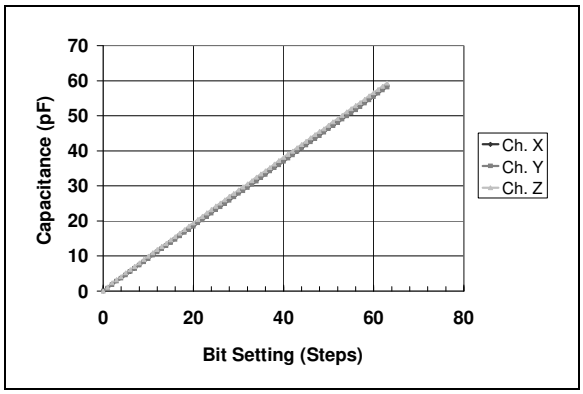


FIGURE 2-10: *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting (V_{DD} = 3V, Temperature = +25°C.*

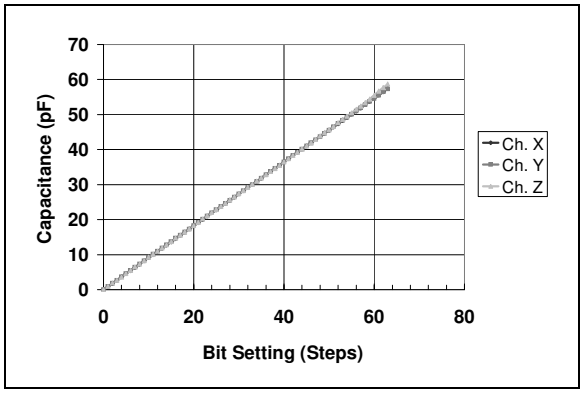
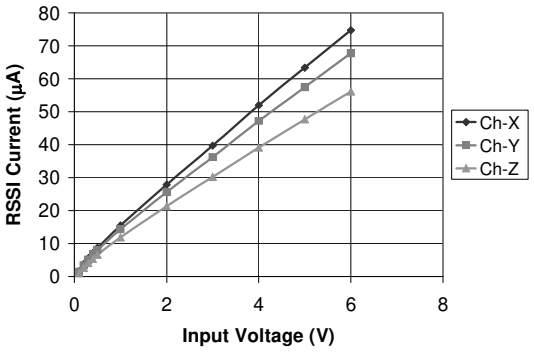
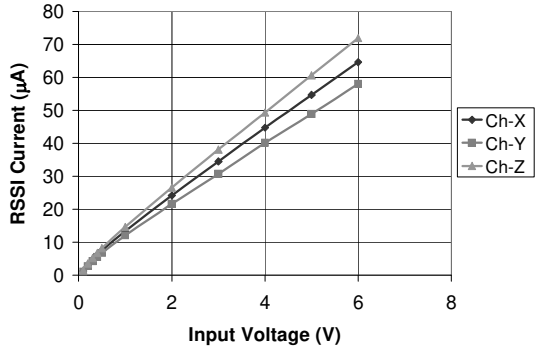


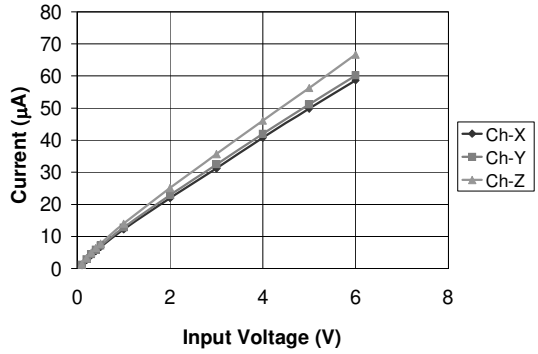
FIGURE 2-12: *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting (V_{DD} = 3V,Temperature = +85°C.*



Device (a)



Device (b)



Device (c)

Note: Equal amplitude is applied to each channel.

FIGURE 2-13: *Examples of RSSI Output Current Variations Between Channel to Channel and Device to Device at Room Temperature.*

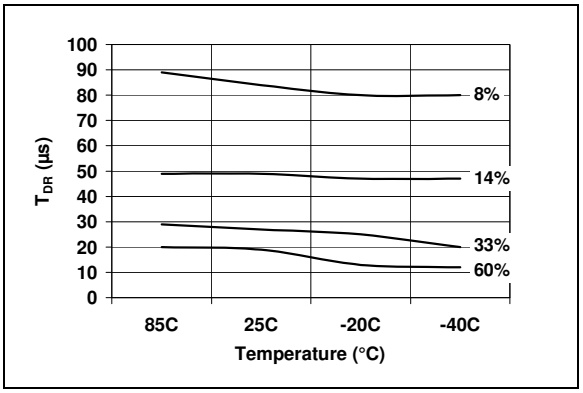


FIGURE 2-14: *Example of Typical T_{DR} Changes over Temperature. Input Signal Condition: Amplitude = 300 mV_{PP}, Modulation Depth = 100 %.*

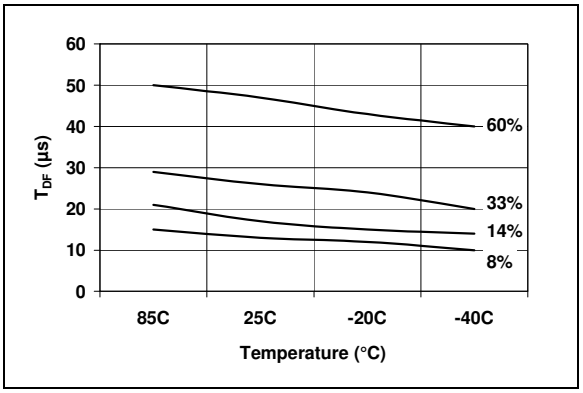


FIGURE 2-15: *Example of Typical T_{DF} Changes over Temperature. Input Signal Condition: Amplitude = 300 mV_{PP}, Modulation Depth = 100 %.*

2.1 Performance Plots

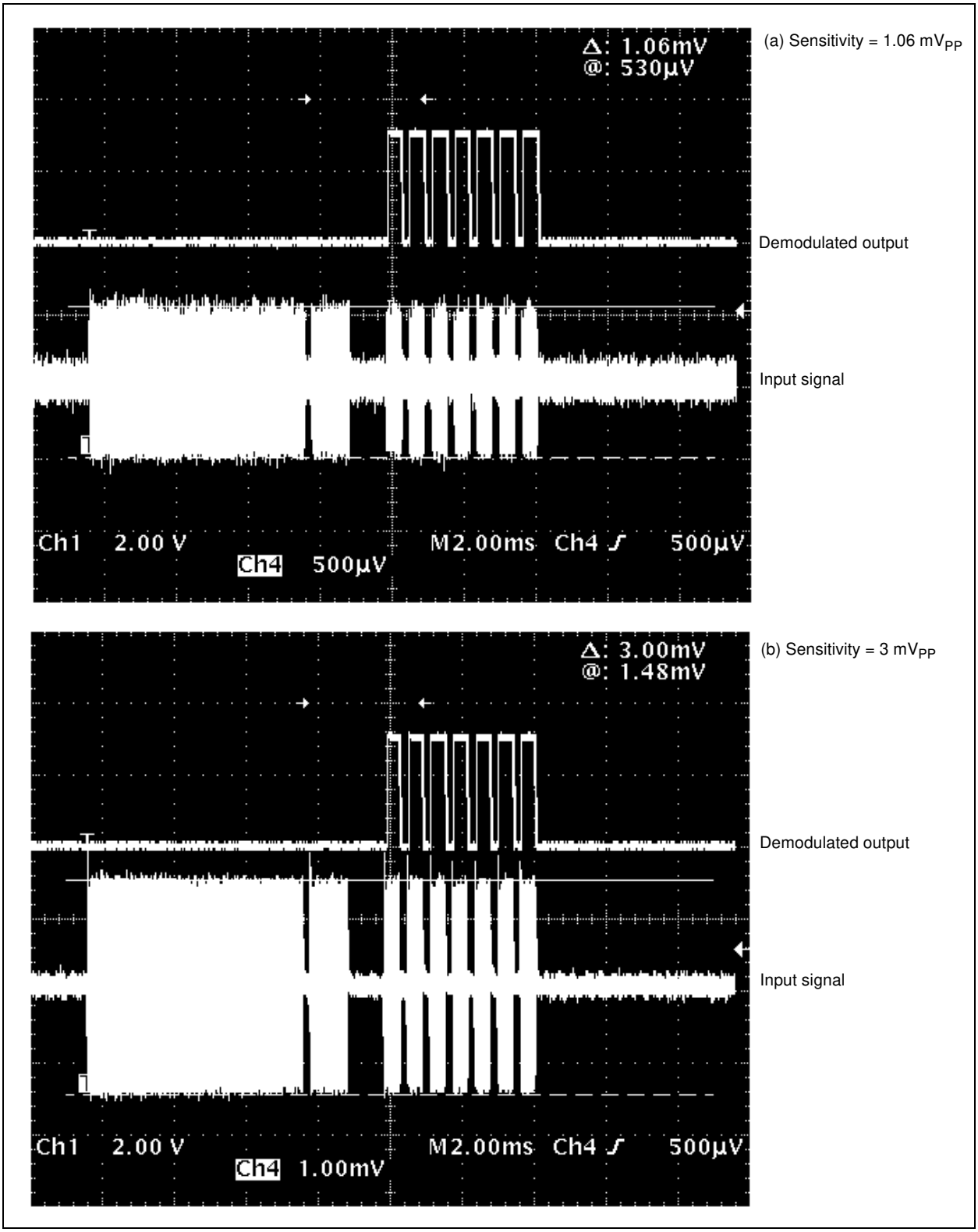
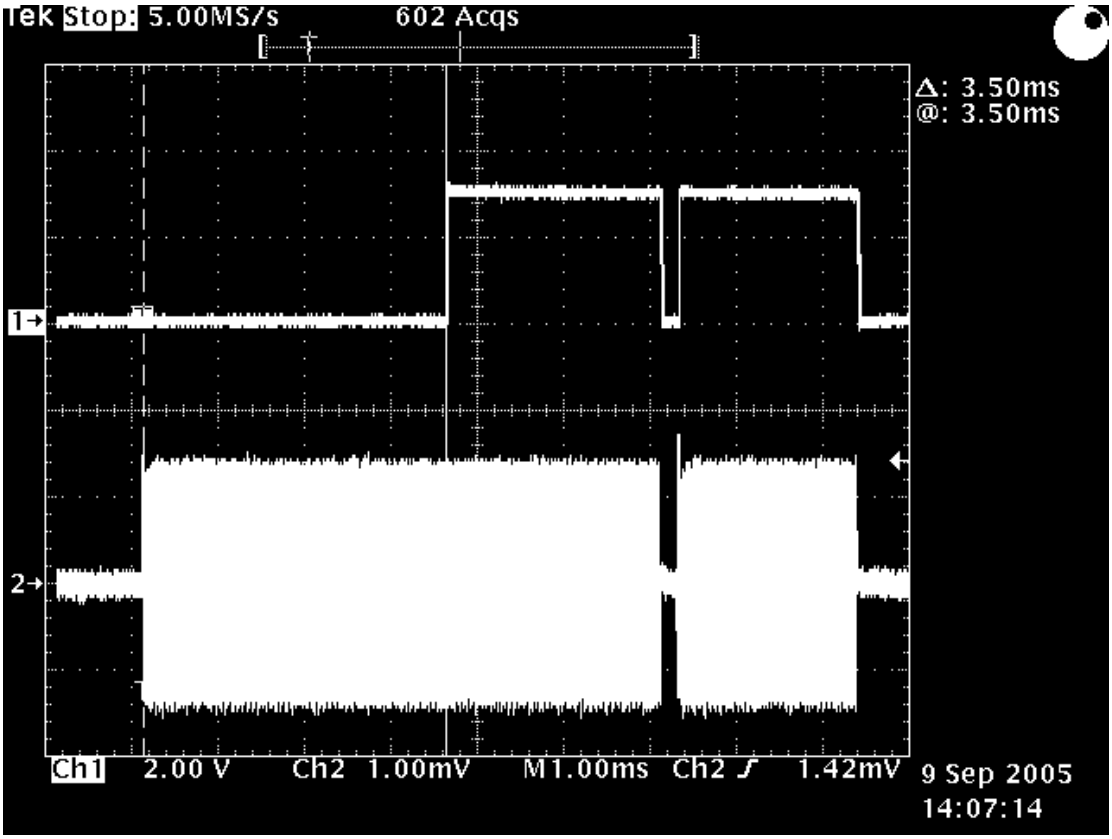
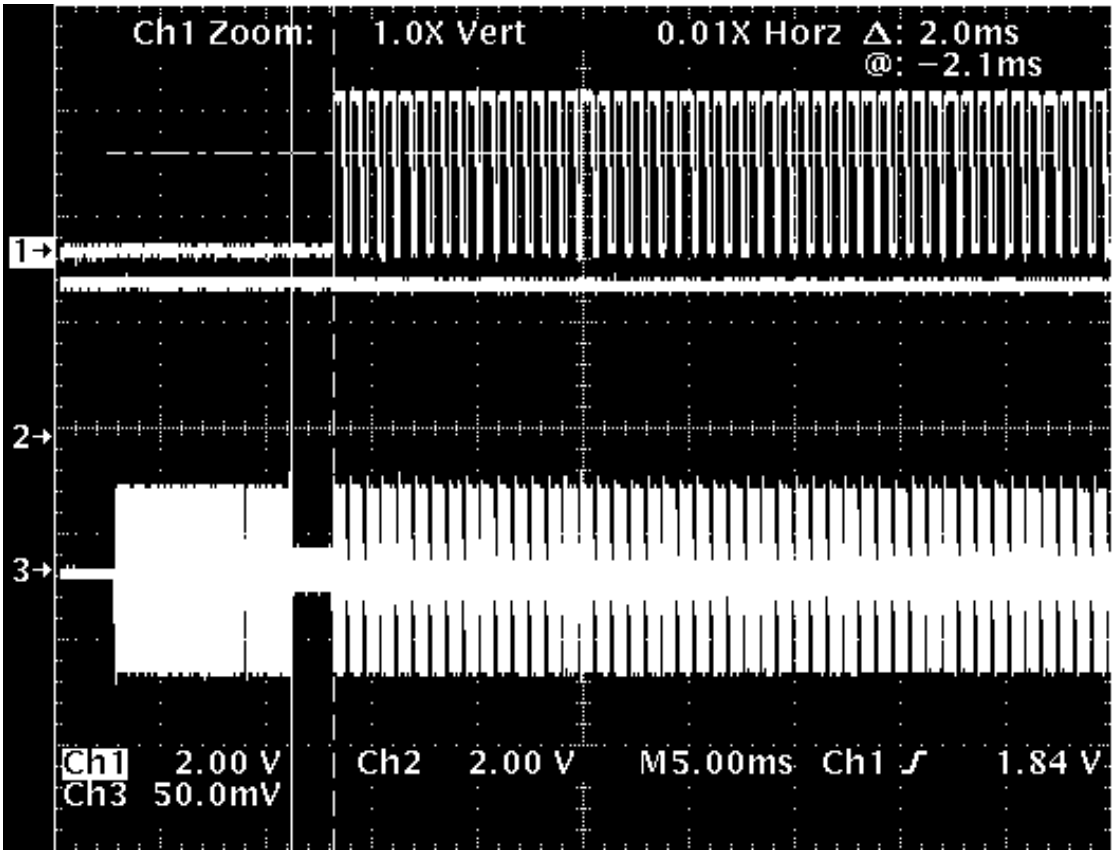


FIGURE 2-16: *Input Sensitivity Example.*



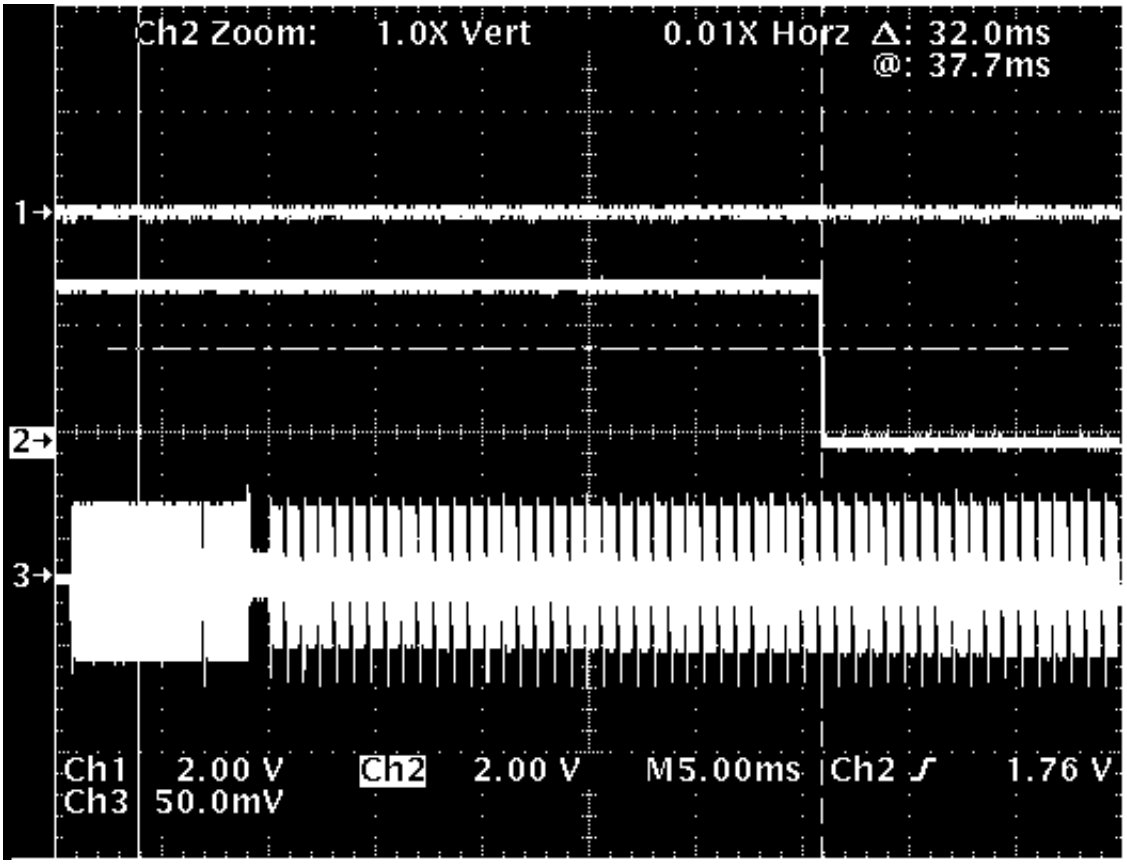
Note: Ch2 is the input and Ch1 is the output (demodulated data appears after AGC Initialization time (T_{AGC})). Output Enable Filter is disabled.

FIGURE 2-17: *Typical AGC Initialization Time at Room Temperature (V_{DD} = 3V).*



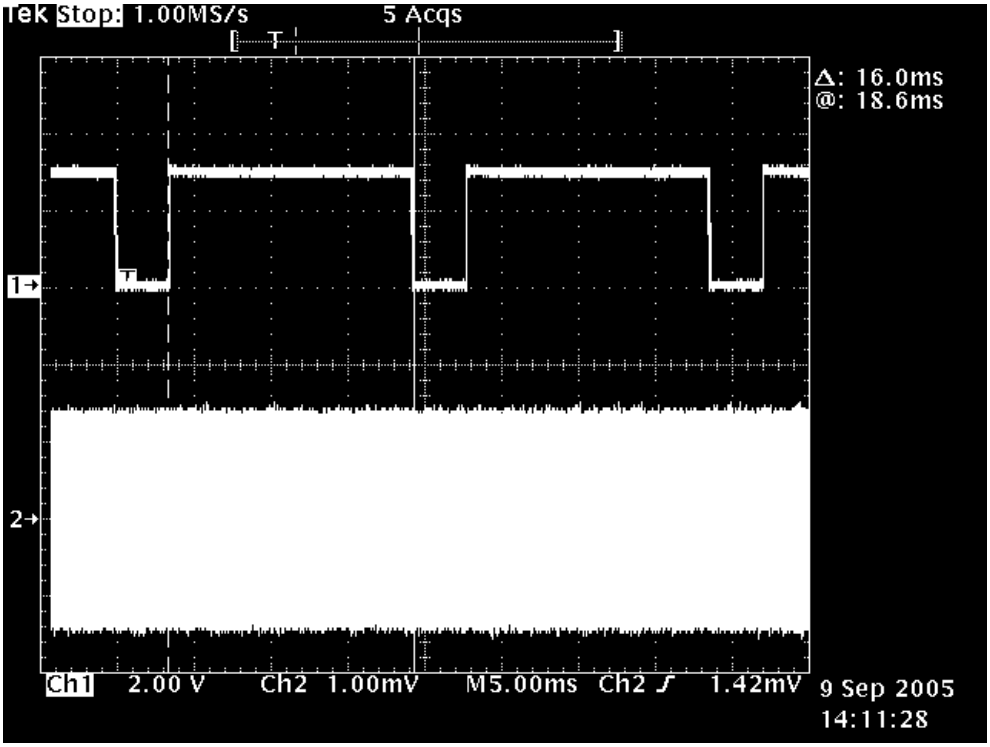
Note: Ch3 is the input with correct Output Enable Filter timing.
Ch1 is the demodulated LFDATA output.
Ch2 is the $\overline{\text{ALERT}}$ pin output. It shows that the $\overline{\text{ALERT}}$ output pin maintains logic high if the input signal meets the programmed filter timing requirement.

FIGURE 2-18: *$\overline{\text{ALERT}}$ Output Example: With No Parity Error and no 32 ms Alarm Timer Time-out.*



Note: The 32 ms Alarm Timer is enabled only if the Output Enable Filter is enabled.
Ch3 is the input signal with incorrect Output Enable Filter timing.
Ch1 is the demodulated LFDATA output. No output since the input filter is not matched.
Ch2 is the $\overline{\text{ALERT}}$ output.
The output shows that the logic level changes after 32 ms from the AGC initialization time (T_{AGC}) if the input signal does not meet the programmed filter timing requirement.

FIGURE 2-19: *$\overline{\text{ALERT}}$ Output Example: With 32 ms Alarm Timer Timed out.*



(a) Output (Ch 1): Device repeats Soft Reset after 16 ms inactivity timer has timed out

(b) Input (Ch 2): Input has no modulation

Note: Ch 2 is the input without modulation (i.e., noise)
Ch 1 is the output at the LFDATA pin due to the 16 ms Soft Inactivity Timer timed out. Note the 3.5 ms AGC initialization time after the Soft Reset.
The cases shown above apply when the Output Filter is disabled.

FIGURE 2-20: *Examples of Soft Inactivity Timer Timed out: This output is available only if the Output Enable Filter is disabled.*

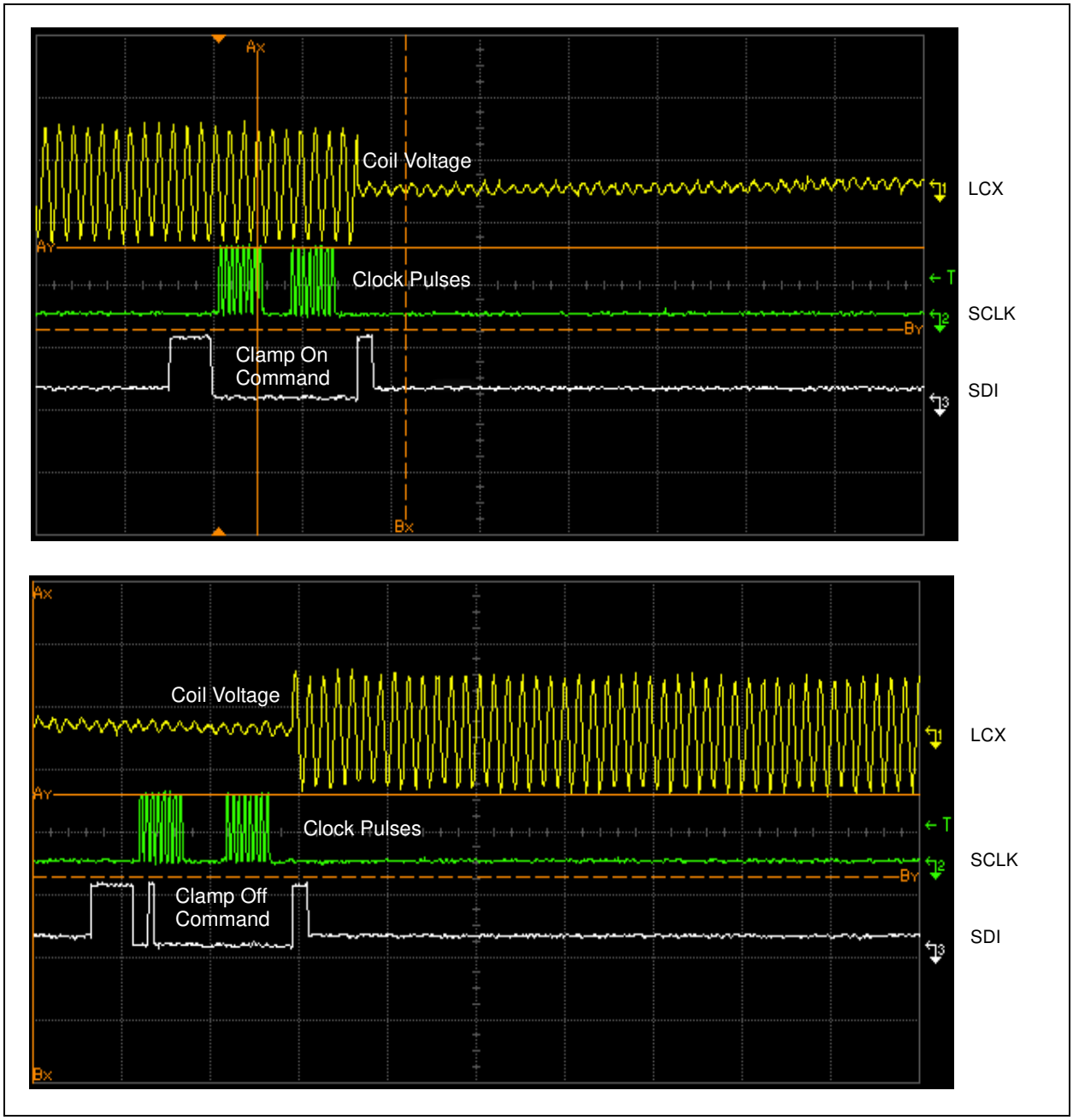


FIGURE 2-21: *Examples of Clamp-On and Clamp-Off Commands and Changes in Coil Voltage.*

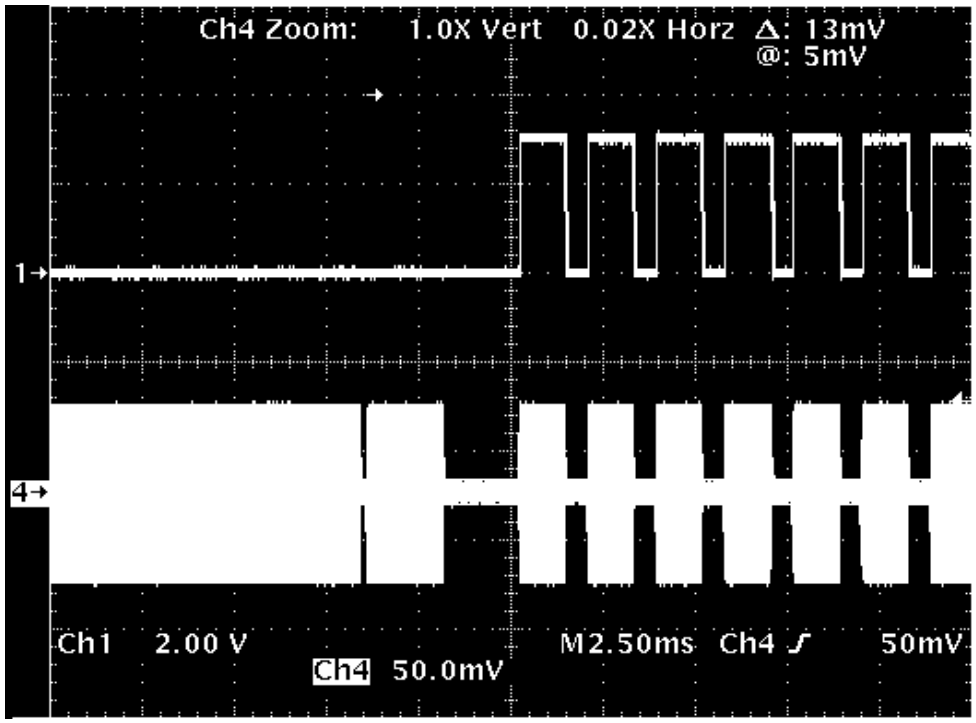
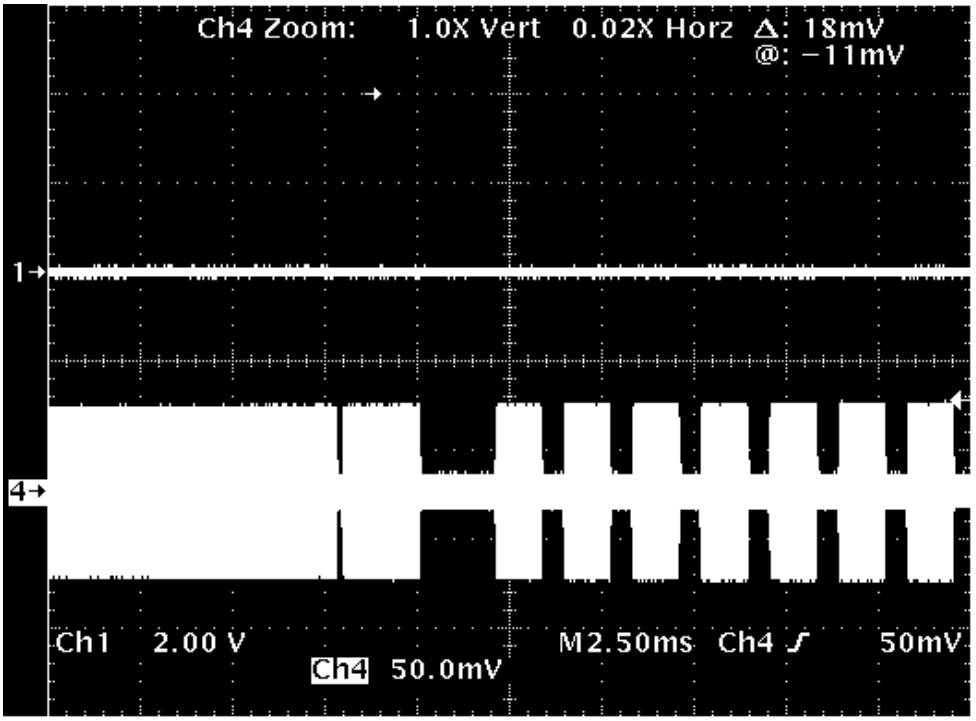


FIGURE 2-22: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 77%, Minimum Modulation Depth (MODMIN) Setting = 60%.*



Note: There is no demodulated output since the modulation depth of the input signal is lower than the minimum modulation depth setting. The device will have demodulated output if the Minimum Modulation Depth option is set to 8%, 14%, or 33%.

FIGURE 2-23: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 56%, Minimum Modulation Depth (MODMIN) Setting = 60%.*

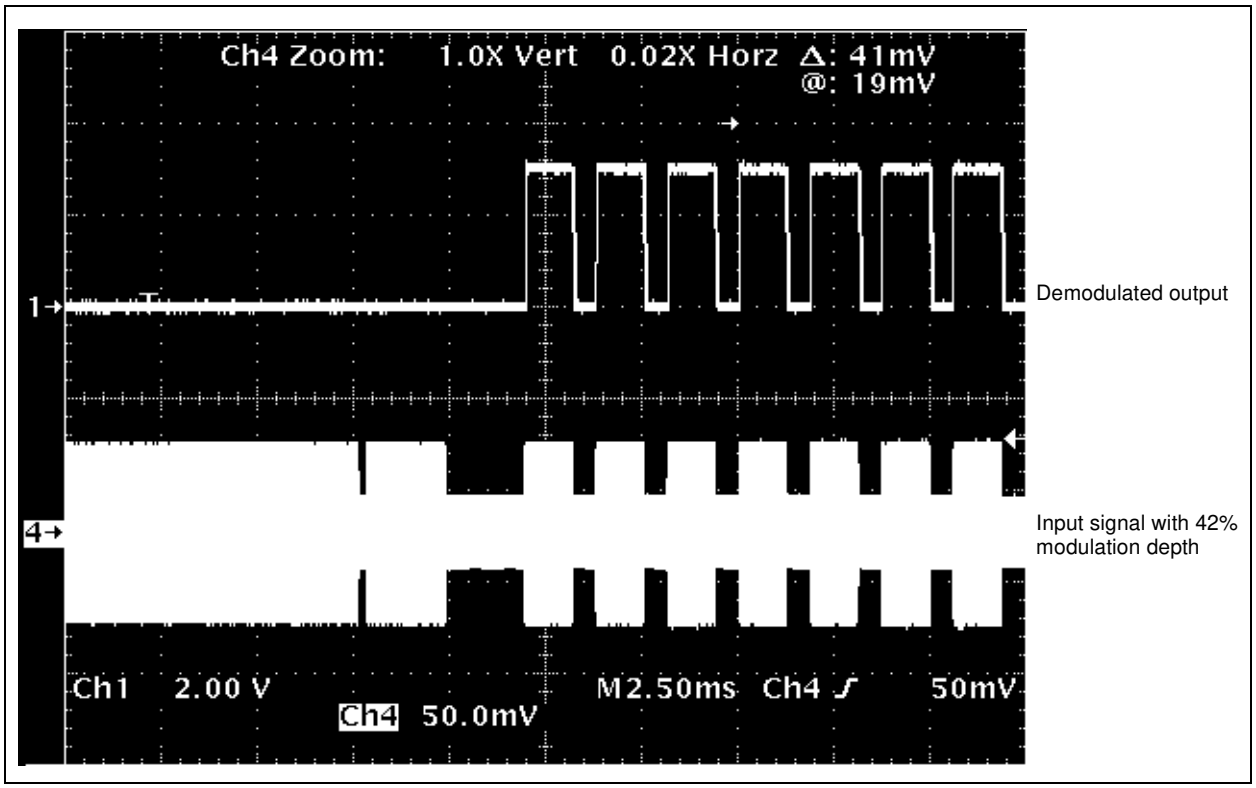


FIGURE 2-24: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 42%, Minimum Modulation Depth (MODMIN) Setting = 33%.*

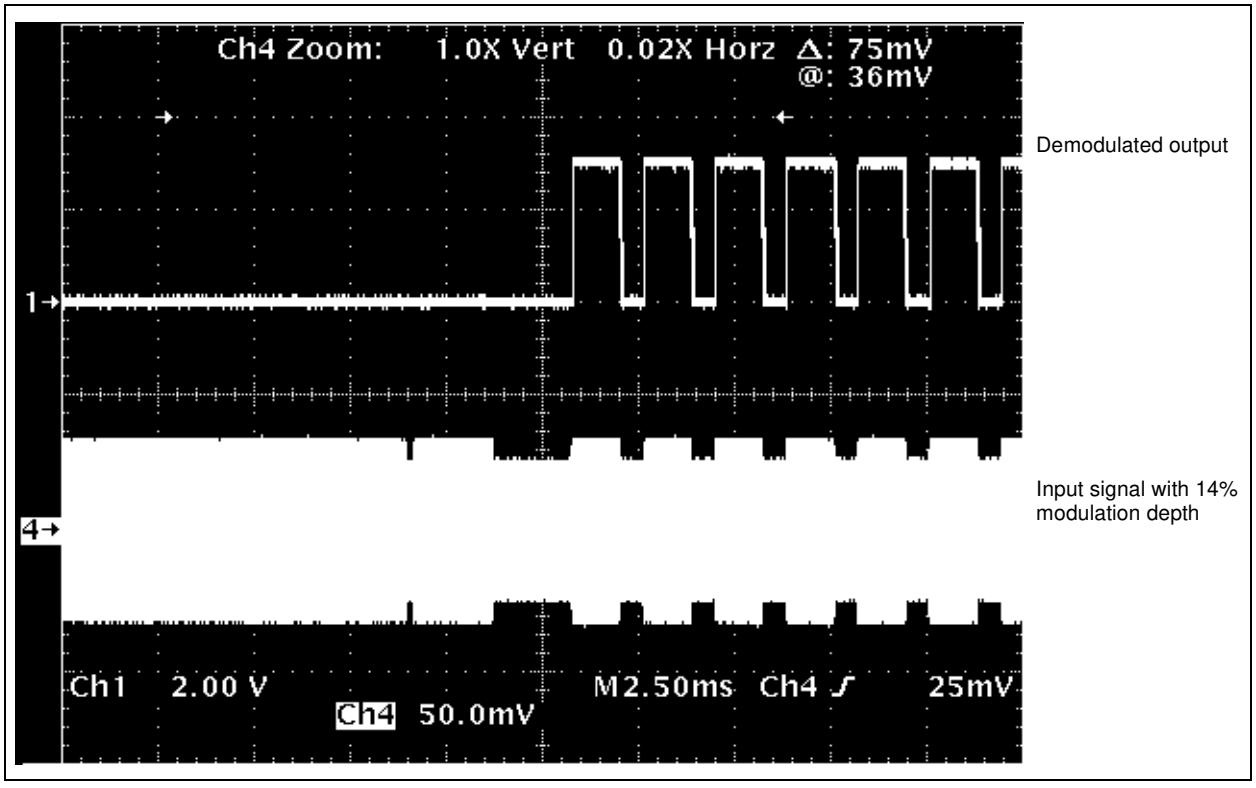
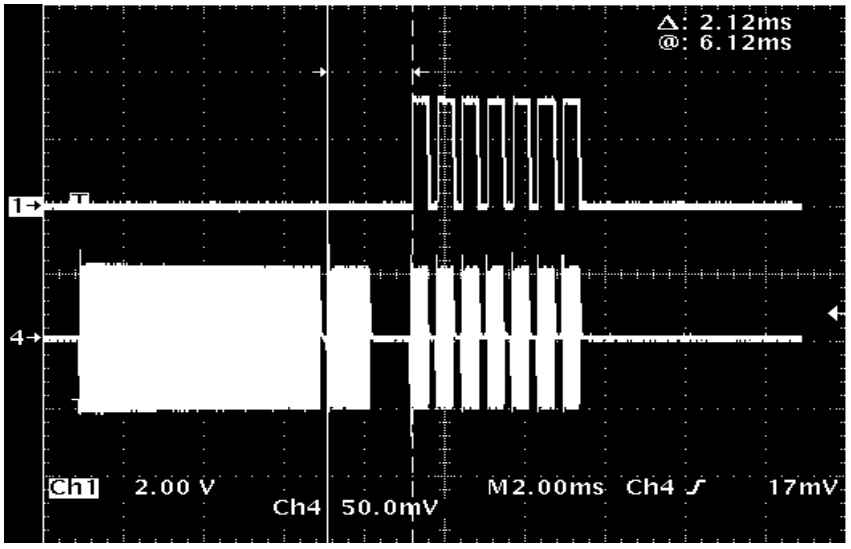
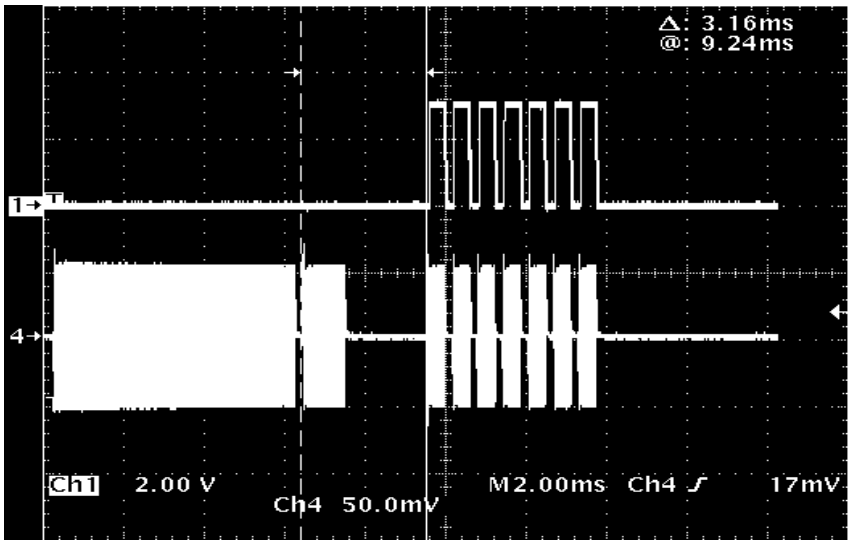


FIGURE 2-25: *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 14%, Minimum Modulation Depth (MODMIN) Setting = 14%.*



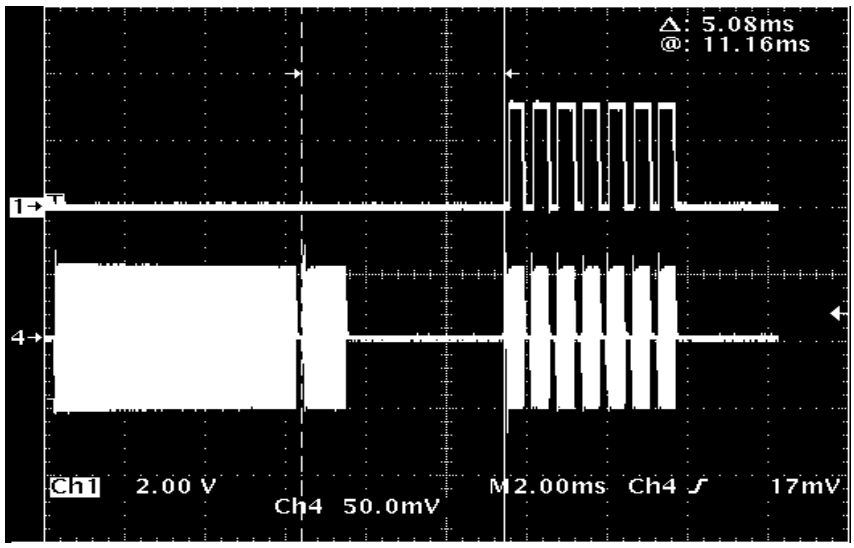
Filter 1

Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 1 ms T_{OEL} = 1 ms T_{OET} = 3 ms	01 or 01	00 01



Filter 2

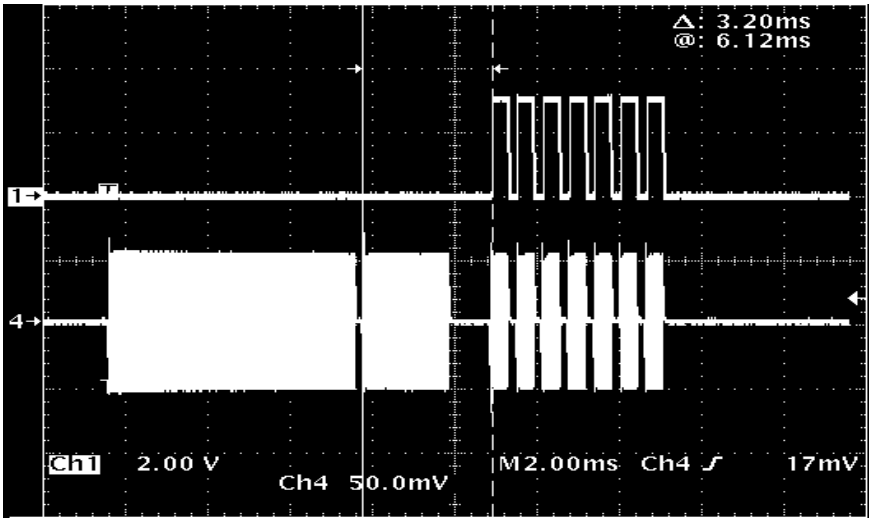
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 1 ms T_{OEL} = 2 ms T_{OET} = 4 ms	01	10



Filter 3

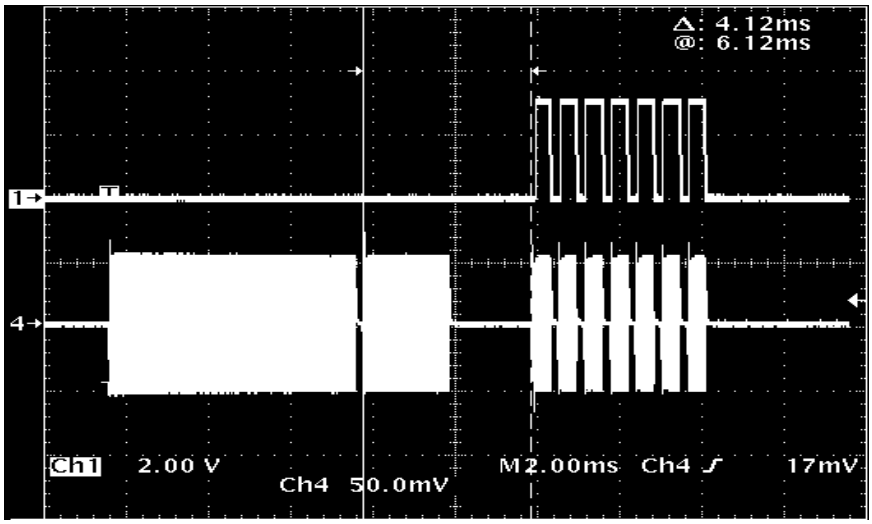
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 1 ms T_{OEL} = 4 ms T_{OET} = 6 ms	01	11

FIGURE 2-26: *Examples of Output Enable Filters 1 through 3 (Wake-up Filters) and Demodulated Outputs.*



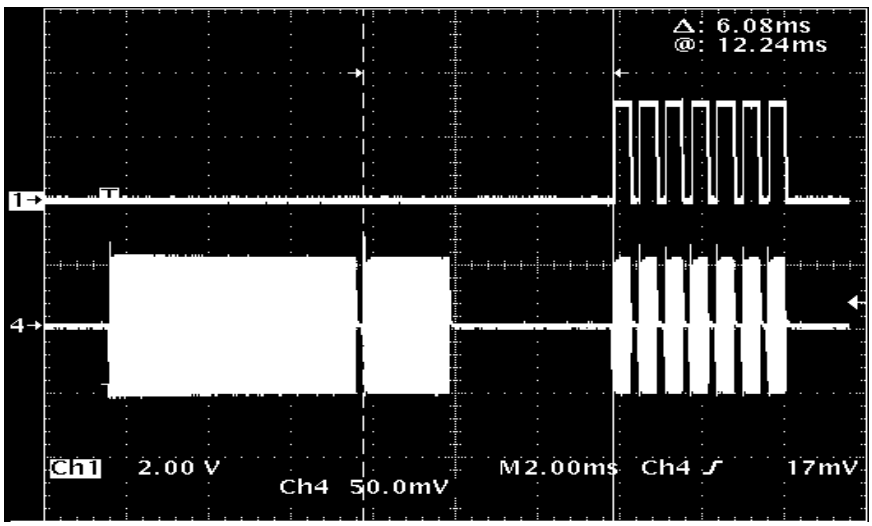
Filter 4

Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 2 ms T_{OEL} = 1 ms T_{OET} = 4 ms	10 or 10	00 01



Filter 5

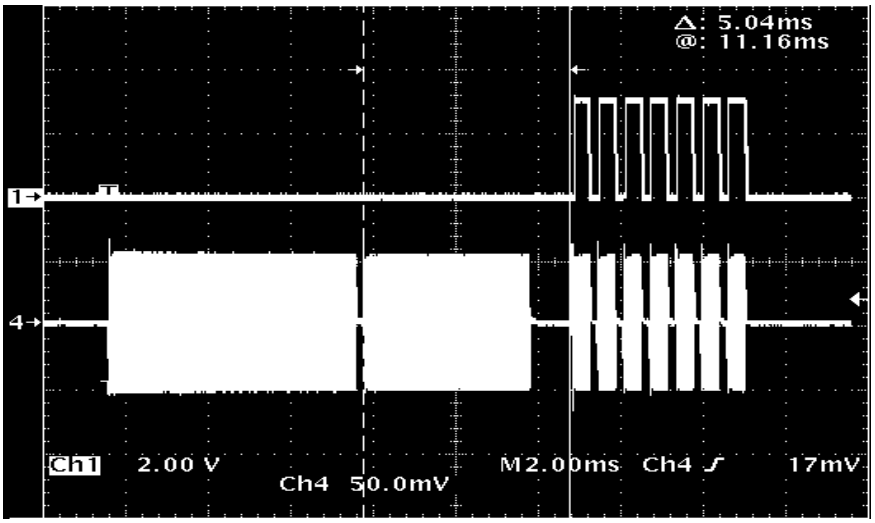
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 2 ms T_{OEL} = 2 ms T_{OET} = 5 ms	10	10



Filter 6

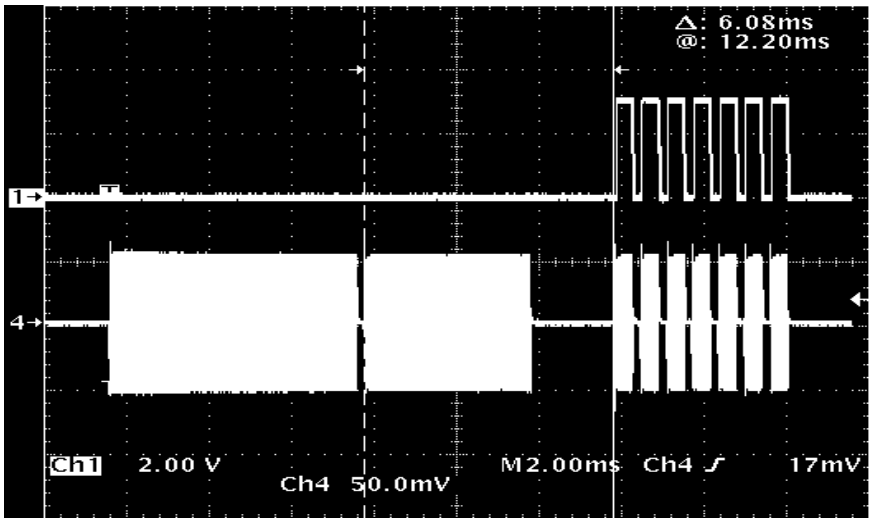
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 2 ms T_{OEL} = 4 ms T_{OET} = 8 ms	10	11

FIGURE 2-27: *Examples of Output Enable Filters 4 through 6 (Wake-up Filters) and Demodulated Outputs.*



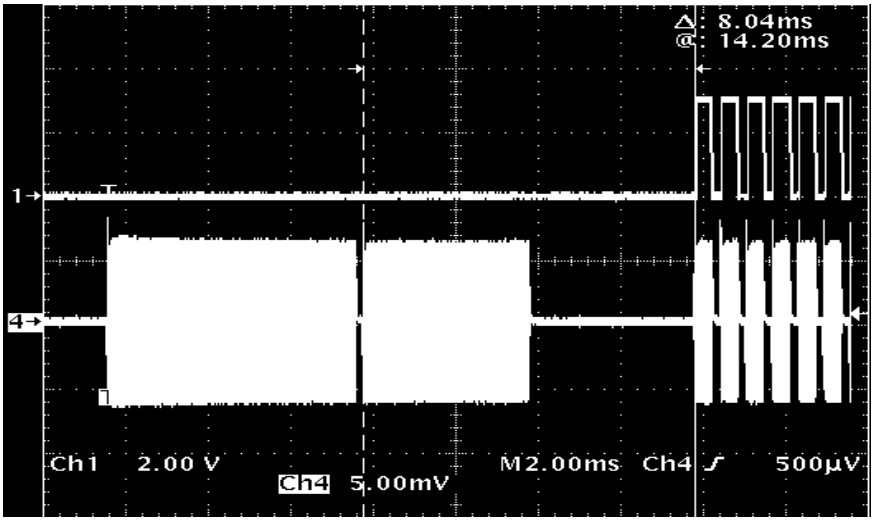
Filter 7

Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 4 ms T_{OEL} = 1 ms T_{OET} = 6 ms	11 or 11	00 01



Filter 8

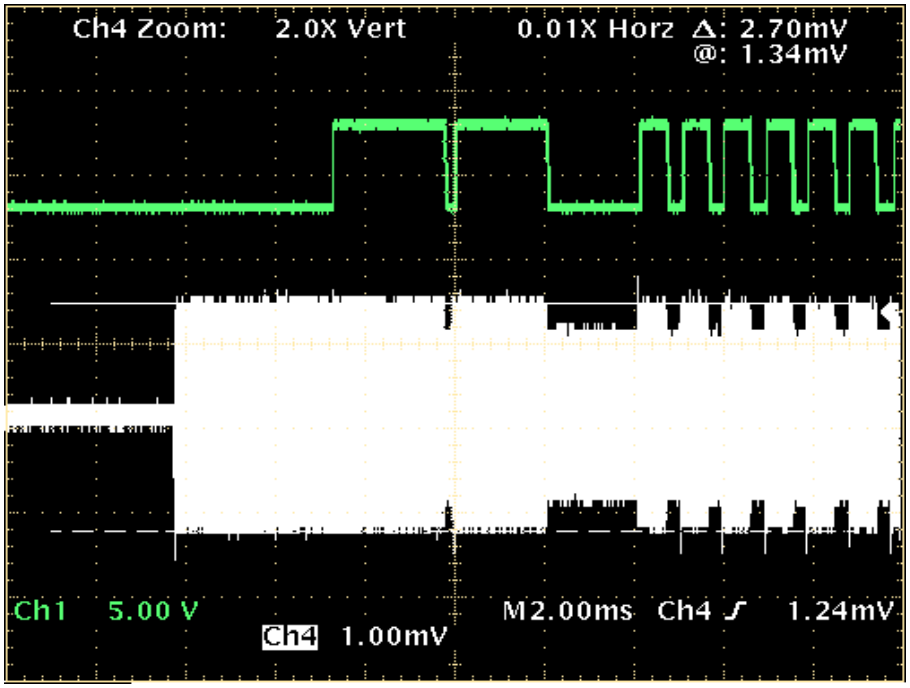
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 4 ms T_{OEL} = 2 ms T_{OET} = 8 ms	11	10



Filter 9

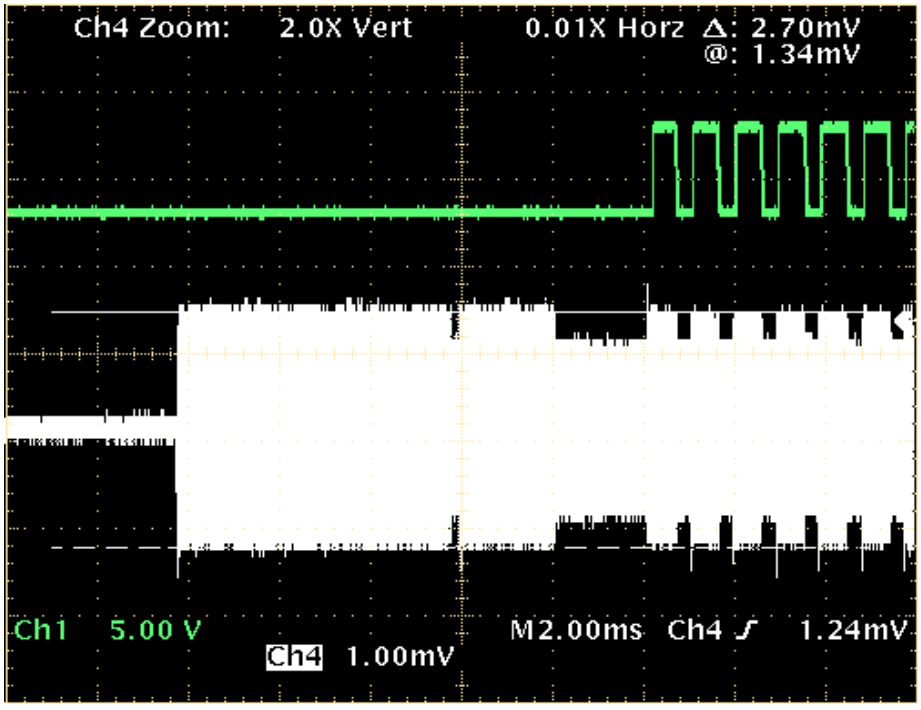
Output Enable Filter Timing of Input Signal	Configuration Bit Settings	
	OEH	OEL
T_{OEH} = 4 ms T_{OEL} = 4 ms T_{OET} = 10 ms	11	11

FIGURE 2-28: *Examples of Output Enable Filters 7 through 9 (Wake-up Filters) and Demodulated Outputs.*



Note: Demodulated output is available immediately after AGC initialization.

FIGURE 2-29: *Input Signal and Demodulated Output When the Output Enable Filter is Disabled.*



Note: Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 5-1). If the criteria is met, the output is available after the low timing (T_{OEL}) of the Enable Filter.

FIGURE 2-30: *Input Signal and Demodulator Output When Output Enable Filter is Enabled and Input Meets Filter Timing Requirements.*

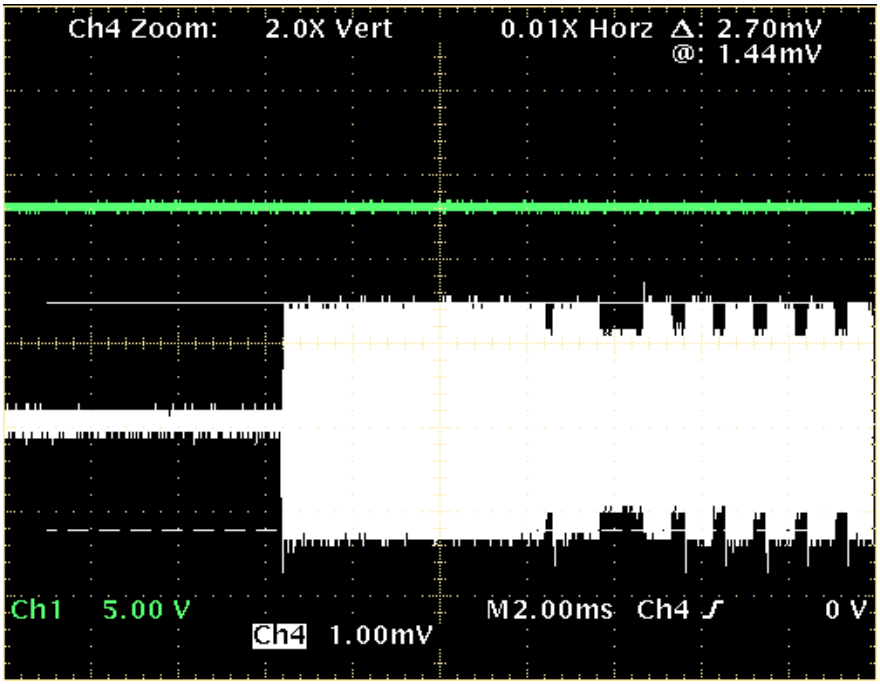
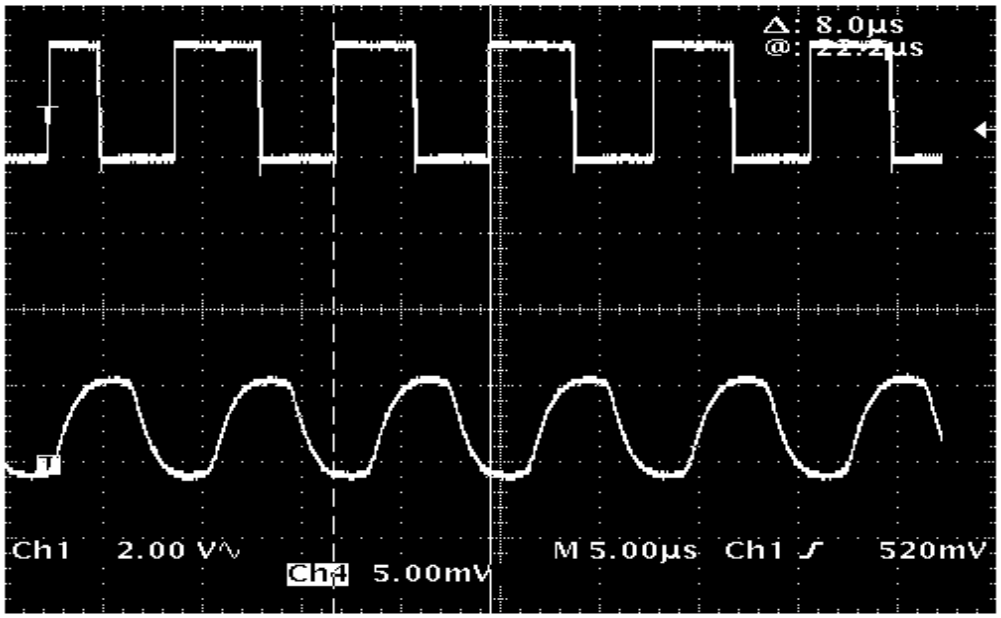
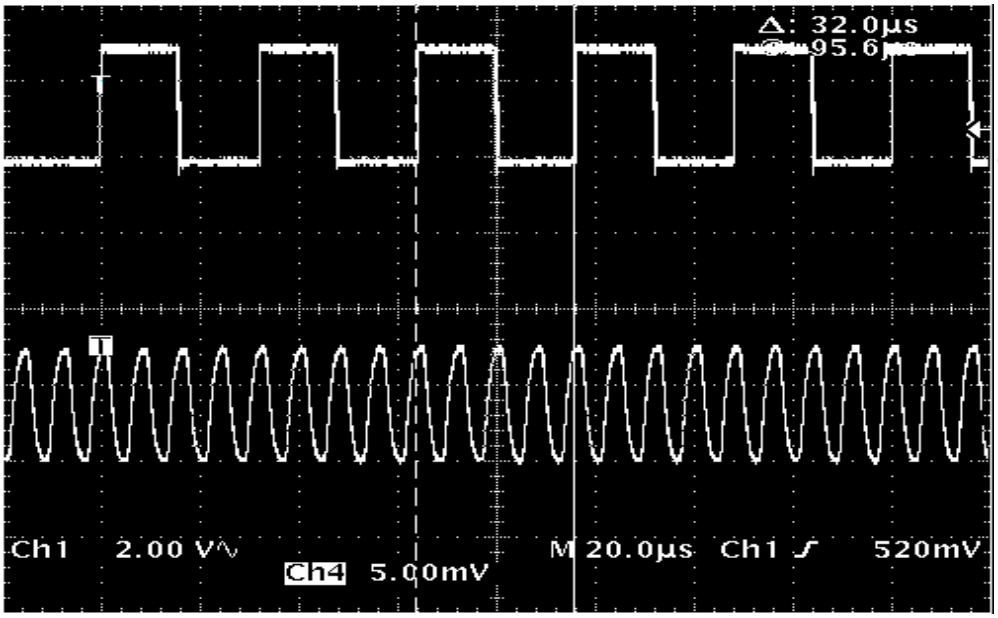


FIGURE 2-31: *No Demodulator Output When Output Enable Filter is Enabled But Input Does Not Meet Filter Timing Requirements.*



(a) Carrier Clock Output with Carrier/1 Option



(b) Carrier Clock Output with Carrier/4 Option

FIGURE 2-32: *Carrier Clock Output Examples.*

3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN FUNCTION TABLES

Pin No.	Symbol	I/O/P	Function
1	V_{SS}	P	Ground Pin.
2	$\overline{CS}$	I	Chip Select Digital Input Pin.
3	SCLK/$\overline{ALERT}$	I/O	Clock input for the modified 3-wire SPI interface. $\overline{ALERT}$ output: This pin goes low if there is a parity error in the Configuration register or the 32 ms alarm timer is timed out.
4	RSSI	O	Received Signal Strength Indicator (RSSI) current output.
5	NC	N/A	No Connect.
6	LFDATA/CCLK/SDIO	I/O	Demodulated data output. Carrier clock output. Serial input or output data for the modified 3-wire SPI interface.
7	V_{DD}	P	Positive Supply Voltage Pin.
8	V_{DD}	P	Positive Supply Voltage Pin.
9	LCZ	I	Input pin for external LC antennas.
10	LCY	I	Input pin for external LC antennas.
11	LCX	I	Input pin for external LC antennas.
12	NC	N/A	No Connect.
13	LCCOM	I	Common reference input for the external LC antennas.
14	V_{SS}	P	Ground Pin.

Type Identification: I = Input; O = Output; P = Power

3.1 Supply Voltage (V_{DD}, V_{SS})

The V_{DD} pin is the power supply pin for the analog and digital circuitry within the MCP2030. This pin requires an appropriate bypass capacitor of 0.1 µF. The voltage on this pin should be maintained in the 2.0V-3.6V range for specified operation.

The V_{SS} pin is the ground pin and the current return path for both analog and digital circuitry of the MCP2030. If an analog ground plane is available, it is recommended that this device be tied to the analog ground plane of the PCB.

3.2 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin needs to stay high when the device is receiving input signals. Leaving the $\overline{CS}$ pin low will place the device in the SPI Programming mode.

The $\overline{CS}$ pin is an open collector output. This pin has an internal pull-up resistor to ensure that no spurious SPI communication occurs between power-up and pin configuration of the MCU.

3.3 SPI Clock Input (SCLK/$\overline{ALERT}$)

This pin becomes the SPI clock input (SCLK) when $\overline{CS}$ is low, and becomes the $\overline{ALERT}$ output when $\overline{CS}$ is high.

The $\overline{ALERT}$ pin is an open collector output. This pin has an internal pull-up resistor to ensure that no spurious SPI communication occurs between power-up and pin configuration of the MCU.

3.4 Received Signal Strength Indicator (RSSI)

This pin becomes the Received Signal Strength Indicator (RSSI) output current sink when the RSSI output option is selected.