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# MCP2035

## Analog Front-End Device for BodyCom Applications

### Device Features:

- Single Analog Input Pin for Signal Detection
- High Input Detection Sensitivity (3 $mV_{PP}$, typical)
- High Modulation Depth Sensitivity (as low as 8%)
- Three Output Type Selections:
  - Demodulated Data
  - Carrier Clock
  - Received Signal Strength Indicator (RSSI)
- Input Carrier Frequency: 125 kHz, typical
- Input Data Rate: 10 Kbps, maximum
- 8 Internal Configuration Registers
- Bidirectional Transponder Communication via the same input pin (LF talk-back)
- Programmable Antenna Tuning Capacitance (up to 63 pF, 1 pF/step)
- Programmable Output Enable Filter
- Low Standby Current: 2 µA, typical
- Low Operating Current: 10 µA, typical
- Serial Peripheral Interface (SPI) with external devices
- Industrial and Extended Temperature Range: -40°C to +85°C (Industrial)

### Typical Applications:

- BodyCom Applications
- Security Industry Applications
- Automotive Industry Applications

### Description:

The MCP2035 is a single-channel, stand-alone Analog Front-End (AFE) device for low-frequency (LF) signal detection and low-power short range transponder applications, such as BodyCom communications.

The device can detect an input signal with amplitude as low as ~1 $mV_{PP}$, and can demodulate an amplitude-modulated input signal with as low as 8% modulation depth. The device can also transmit data (LF talk-back) by clamping and unclamping the input LC antenna voltage.

The device can output demodulated data, carrier clock or RSSI current, depending on the output-type selection configuration register bit settings. The demodulated data and carrier clock outputs are available on the LFDATA pin, while the RSSI output is available on the RSSI pin. The RSSI current output is linearly proportional to the input signal strength.

The device has programmable internal tuning capacitors for the input channel. The user can program the input tuning capacitors up to 63 pF, 1 pF per step. The internal tuning capacitors can be used effectively for fine-tuning of the external LC resonant circuit.

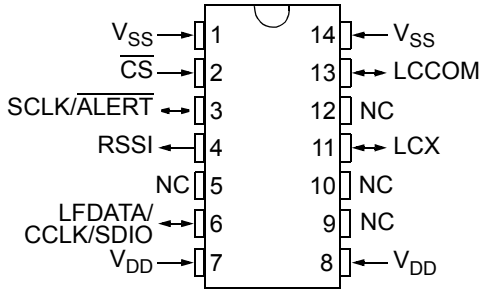
The device has eight volatile internal configuration registers for dynamic configurations of the device operation on-the-fly. All registers are readable and programmable using the serial SPI commands, except the read-only STATUS register.

The device is optimized for very low current consumption and has various battery-saving low-power modes (Sleep, Standby, Active).

This device is available in a 14-pin TSSOP package.

### Package Type:

**MCP2035**
TSSOP



**NOTES:**

## 1.0 ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +6.5V

Voltage on all other pins with respect to $V_{SS}$ ..... -0.3V to ($V_{DD}$ + 0.3V)

Maximum current out of $V_{SS}$ pin ..... 300 mA

Maximum current into $V_{DD}$ pin ..... 250 mA

Maximum LC Input Voltage (LCX) loaded, with device ..... 10.0 $V_{PP}$

Maximum LC Input Voltage (LCX) unloaded, without device ..... 700.0 $V_{PP}$

Maximum Input Current (rms) into device (LCX Input Channel) ..... 10 mA

Human Body ESD rating ..... 2000 (minimum) V

Machine Model ESD rating ..... 200 (minimum) V

**† Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

**Electrical Specifications:** Standard Operating Conditions (unless otherwise stated), Operating temperature: -40°C ≤ $T_A$ ≤ +85°C, LCX Input Signal: Sinusoidal 300 $mV_{PP}$, Carrier Frequency = 125 kHz, LCCOM connected to $V_{SS}$, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

| Parameters | Sym. | Min. | Typ.(2) | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 2.0 | 3.0 | 3.6 | V | |
| $V_{DD}$ Start Voltage to ensure internal Power-on Reset signal | $V_{POR}$ | — | — | 1.8 | V | |
| Modulation Transistor-on Resistance | $R_M$ | — | 50 | 100 | Ω | $V_{DD}$ = 3.0V |
| Active Current (detecting signal) 1 LC Input Channel (LCX) is Receiving Signal | $I_{ACT}$ | — | 10 | — | µA | $\overline{CS}$ = $V_{DD}$ Input = Continuous Wave (CW) Amplitude = 300 $mV_{PP}$ LCX input channel is enabled. |
| Standby Current (wait to detect signal) | $I_{STDBY}$ | — | 2 | 5 | µA | $\overline{CS}$ = $V_{DD}$; $\overline{ALERT}$ = $V_{DD}$ LCX input channel is enabled. |
| Sleep Current | $I_{SLEEP}$ | — | 0.2 | 1 | µA | $\overline{CS}$ = $V_{DD}$; $\overline{ALERT}$ = $V_{DD}$ |
| Analog Input Leakage Current on LCX and LCCOM pins | $I_{AIL}$ | — | — | ±1 | µA | $V_{DD}$ = 3.6V, $V_{SS}$ ≤ $V_{IN}$ ≤ 1V with respect to ground. Internal tuning capacitors are switched off, tested in Sleep mode |
| Digital Input Low Voltage | $V_{IL}$ | $V_{SS}$ | — | 0.3 $V_{DD}$ | V | SCLK, SDI, $\overline{CS}$ |
| Digital Input High Voltage | $V_{IH}$ | 0.8 $V_{DD}$ | — | $V_{DD}$ | V | SCLK, SDI, $\overline{CS}$ |

**Note 1:** These parameters are characterized but not tested.

**2:** Data in “Typ.” column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**3:** Negative current is defined as current sourced by the pin.

## DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Standard Operating Conditions (unless otherwise stated), Operating temperature: -40°C ≤ $T_A$ ≤ +85°C, LCX Input Signal: Sinusoidal 300 $mV_{PP}$, Carrier Frequency = 125 kHz, LCCOM connected to $V_{SS}$, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

| Parameters | Sym. | Min. | Typ.(2) | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Digital Input Leakage Current SDI, SCLK, $\overline{CS}$ **(Note 3)** | $I_{IL}$ | — | — | ±1 | µA | $V_{DD}$ = 3.6V<br>$V_{SS} \le V_{PIN} \le V_{DD}$<br>$V_{PIN} \le V_{DD}$ |
| Digital Output Low Voltage $\overline{ALERT}$, LFDATA/SDIO | $V_{OL}$ | — | — | $V_{SS}$ + 0.4 | V | Analog Front-End section<br>$I_{OL}$ = 1.0 mA, $V_{DD}$ = 2.0V |
| Digital Output High Voltage $\overline{ALERT}$, LFDATA/SDIO | $V_{OH}$ | $V_{DD}$ - 0.5 | — | — | V | $I_{OH}$ = -400 µA, $V_{DD}$ = 2.0V |
| Digital Input Pull-Up Resistor $\overline{CS}$, SCLK | $R_{PU}$ | 50 | 200 | 350 | kΩ | $V_{DD}$ = 3.6V |

**Note 1:** These parameters are characterized but not tested.

**2:** Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**3:** Negative current is defined as current sourced by the pin.

## AC CHARACTERISTICS

**Electrical Specifications:** Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ $V_{DD}$ ≤ 3.6V, Operating temperature: -40°C ≤ $T_A$ ≤ +85°C, LCCOM connected to $V_{SS}$, LCX Input Signal: Sinusoidal 300 $mV_{PP}$, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

| Parameters | Sym. | Min. | Typ(2) | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Sensitivity | $V_{SENSE}$ | 1 | 3.0 | 6 | $mV_{PP}$ | $V_{DD}$ = 3.0V<br>Output enable filter disabled<br>AGCSIG = 0;<br>MODMIN = 00<br>(33% modulation depth setting)<br>Input = Continuous Wave (CW)<br>Output = Logic level transition from low-to-high at sensitivity level for CW input. |
| Coil de-Q'ing Voltage - RF Limiter ($R_{FLM}$) must be active | $V_{DE\_Q}$ | 3 | — | 5 | V | $V_{DD}$ = 3.0V, Force $I_{IN}$ = 5 µA<br>(worst case) |
| RF Limiter Turn-on Resistance at LCX pin | $R_{FLM}$ | — | 300 | 700 | Ω | $V_{DD}$ = 2.0V, $V_{IN}$ = 8 $V_{DC}$ |
| Sensitivity Reduction | $S_{ADJ}$ | — | 0 | — | dB | $V_{DD}$ = 3.0V<br>No sensitivity reduction selected<br>Maximum reduction selected<br>Monotonic increment in attenuation value from setting = 0000 to 1111 by design |
| | | — | -30 | — | dB | |
| Minimum Modulation Depth | | | | | | |
| 60% setting | $V_{IN\_MOD}$ | — | 60 | 84 | % | $V_{DD}$ = 3.0V<br>See **Section 5.20 "Minimum Modulation Depth Requirement for Input Signal"**.<br>See Modulation Depth Definition in Figure 5-5. |
| 33% setting | | — | 33 | 49 | % | |
| 14% setting | | — | 14 | 26 | % | |
| 8% | | | 8 | | % | |
| Carrier frequency | $F_{CARRIER}$ | — | 125 | — | kHz | |
| Input modulation frequency | $F_{MOD}$ | — | — | 10 | kHz | Input data rate with NRZ data format.<br>$V_{DD}$ = 3.0V<br>Minimum modulation depth setting = 33%<br>Input conditions:<br>Amplitude = 300 $mV_{PP}$<br>Modulation depth = 100% |

**Note 1:** Parameter is characterized but not tested.

**2:** Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**3:** Required output enable filter high time must account for input path analog delays (= $T_{OEH}$ - $T_{DR}$ + $T_{DF}$).

**4:** Required output enable filter low time must account for input path analog delays (= $T_{OEL}$ + $T_{DR}$ - $T_{DF}$).

## AC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ $V_{DD}$ ≤ 3.6V, Operating temperature: -40°C ≤ $T_A$ ≤ +85°C, LCCOM connected to $V_{SS}$, LCX Input Signal: Sinusoidal 300 $mV_{PP}$, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

| Parameters | Sym. | Min. | Typ(2) | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| LCX Tuning Capacitor | $C_{TUNX}$ | — | 0 | — | pF | $V_{DD}$ = 3.0V,<br>Config. Reg. 1,<br>bits <6:1> Setting = 000000 |
| | | 44 | 59 | 82 | pF | 63 pF ±30%<br>Config. Reg. 1, bits <6:1> Setting = 111111<br>63 steps, approx. 1 pF/step<br>Monotonic increment in capacitor value from setting = 000000 to 111111 by design |
| Q of Internal Input Tuning Capacitors | Q_C | 50(1) | — | — | | |
| Demodulator Charge Time (delay time of demodulated output to rise) | $T_{DR}$ | — | 50 | — | µs | $V_{DD}$ = 3.0V<br>Minimum modulation depth setting = 33%<br>Input conditions:<br>Amplitude = 300 $mV_{PP}$<br>Modulation depth = 100% |
| Demodulator Discharge Time (delay time of demodulated output to fall) | $T_{DF}$ | — | 50 | — | µs | $V_{DD}$ = 3.0V<br>MOD depth setting = 33%<br>Input conditions:<br>Amplitude = 300 $mV_{PP}$<br>Modulation depth = 100% |
| Rise time of LFDATA | $TR_{LFDATA}$ | — | 0.5 | — | µs | $V_{DD}$ = 3.0V. Time is measured from 10% to 90% of amplitude |
| Fall time of LFDATA | $TF_{LFDATA}$ | — | 0.5 | — | µs | $V_{DD}$ = 3.0V<br>Time is measured from 10% to 90% of amplitude |
| Automatic Gain Control (AGC) stabilization time ($T_{AGC}$ + $T_{PAGC}$) | $T_{STAB}$ | 4 | — | — | ms | |
| AGC initialization time | $T_{AGC}$ | — | 3.5 | — | ms | |
| High time after AGC initialization time | $T_{PAGC}$ | — | 62.5 | — | µs | |

**Note 1:** Parameter is characterized but not tested.

**2:** Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**3:** Required output enable filter high time must account for input path analog delays (= $T_{OEH}$ - $T_{DR}$ + $T_{DF}$).

**4:** Required output enable filter low time must account for input path analog delays (= $T_{OEL}$ + $T_{DR}$ - $T_{DF}$).

## AC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ $V_{DD}$ ≤ 3.6V, Operating temperature: -40°C ≤ $T_A$ ≤ +85°C, LCCOM connected to $V_{SS}$, LCX Input Signal: Sinusoidal 300 $mV_{PP}$, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

| Parameters | Sym. | Min. | Typ(2) | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Gap time after AGC stabilization time | $T_{GAP}$ | 200 | — | — | µs | |
| Time element of pulse | $T_E$ | 100 | — | — | µs | Minimum pulse width |
| Time from exiting Sleep or POR to being ready to receive signal | $T_{RDY}$ | — | — | 50(1) | ms | |
| Minimum time AGC level must be held after receiving AGC Preserve command | $T_{PRES}$ | 5(1) | — | — | ms | AGC level must not change more than 10% during $T_{PRES}$ |
| Internal RC oscillator frequency | $F_{OSC}$ | 27 | 32 | 35.5 | kHz | Internal clock trimmed at 32 kHz during test |
| Inactivity Timer time-out | $T_{INACT}$ | 13.5 | 16 | 17.75 | ms | 512 cycles of RC oscillator @ $F_{OSC}$ |
| Alarm Timer time-out | $T_{ALARM}$ | 27 | 32 | 35.5 | ms | 1024 cycles of RC oscillator @ $F_{OSC}$ |
| **Input Resistance (LCX)** | $R_{IN}$ | — | 800(1) | — | kΩ | LCCOM grounded, $V_{DD}$ = 3V, $F_{CARRIER}$ = 125 kHz |
| **Input Parasitic Capacitance (LCX)** | $C_{IN}$ | — | 24(1) | — | pF | LCCOM grounded, $V_{DD}$ = 3V, $F_{CARRIER}$ = 125 kHz |
| Minimum output enable filter high time **OEH (Bits Config0<8:7>)** | | | | | | |
| 01 = 1 ms | $T_{OEH}$ | 32 (~1 ms) | — | — | clock count | RC oscillator = $F_{OSC}$ (see $F_{OSC}$ specification for variations). Viewed from the pin input: **(Note 3)** |
| 10 = 2 ms | | 64 (~2 ms) | — | — | | |
| 11 = 4 ms | | 128 (~4 ms) | — | — | | |
| 00 = Filter Disabled | | — | — | — | | |
| Minimum output enable filter low time **OEL (Bits Config0<6:5>)** | | | | | | |
| 00 = 1 ms | $T_{OEL}$ | 32 (~1 ms) | — | — | clock count | RC oscillator = $F_{OSC}$ Viewed from the pin input: **(Note 4)** |
| 01 = 1 ms | | 32 (~1 ms) | — | — | | |
| 10 = 2 ms | | 64 (~2 ms) | — | — | | |
| 11 = 4 ms | | 128 (~4 ms) | — | — | | |

**Note 1:** Parameter is characterized but not tested.

**2:** Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**3:** Required output enable filter high time must account for input path analog delays (= $T_{OEH}$ - $T_{DR}$ + $T_{DF}$).

**4:** Required output enable filter low time must account for input path analog delays (= $T_{OEL}$ + $T_{DR}$ - $T_{DF}$).

## AC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Standard Operating Conditions (unless otherwise stated), Supply Voltage: 2.0V ≤ $V_{DD}$ ≤ 3.6V, Operating temperature: -40°C ≤ $T_A$ ≤ +85°C, LCCOM connected to $V_{SS}$, LCX Input Signal: Sinusoidal 300 $mV_{PP}$, Carrier Frequency = 125 kHz, **Bits <3:1>** of Configuration Register 0: LCXEN = 0, LCZEN = LCYEN = 1.

| Parameters | Sym. | Min. | Typ(2) | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Maximum output enable filter period<br>**OEH OEL $T_{OEH}$ $T_{OEL}$** | | | | | | |
| 01 00 = 1 ms 1 ms (Filter 1) | $T_{OET}$ | — | — | 96 (~3 ms) | clock count | RC oscillator = $F_{OSC}$ |
| 01 01 = 1 ms 1 ms (Filter 1) | | — | — | 96 (~3 ms) | | |
| 01 10 = 1 ms 2 ms (Filter 2) | | — | — | 128 (~4 ms) | | |
| 01 11 = 1 ms 4 ms (Filter 3 | | — | — | 192 (~6 ms) | | |
| 10 00 = 2 ms 1 ms (Filter 4) | | — | — | 128 (~4 ms) | | |
| 10 01 = 2 ms 1 ms (Filter 4) | | — | — | 128 (~4 ms) | | |
| 10 10 = 2 ms 2 ms (Filter 5) | | — | — | 160 (~5 ms) | | |
| 10 11 = 2 ms 4 ms (Filter 6) | | — | — | 250 (~8 ms) | | |
| 11 00 = 4 ms 1 ms (Filter 7) | | — | — | 192 (~6 ms) | | |
| 11 01 = 4 ms 1 ms (Filter 7) | | — | — | 192 (~6 ms) | | |
| 11 10 = 4 ms 2 ms (Filter 8) | | — | — | 256 (~8 ms) | | |
| 11 11 = 4 ms 4 ms (Filter 9) | | — | — | 320 (~10 ms) | | |
| 00 XX = Filter Disabled | | — | — | — | | LFDATA output appears as long as input signal level is greater than $V_{SENSE}$. |
| RSSI current output | $I_{RSSI}$ | — | 0.65 | 2 | µA | $V_{IN}$ = 37 $mV_{PP}$ |
| | | 6 | 12 | 20.3 | µA | $V_{IN}$ = 370 $mV_{PP}$ |
| | | — | 100 | — | µA | $V_{DD}$ = 3.0V, $V_{IN}$ = 0 to 4 $V_{PP}$<br>Linearly increases with input signal amplitude.<br>Tested at $V_{IN}$ = 37 $mV_{PP}$, 100 $mV_{PP}$, and 370 $mV_{PP}$ at +25ºC. |
| RSSI current linearity | $ILR_{RSSI}$ | -15 | — | 15 | % | Tested at room temperature only (see Equation 5-1 and Figure 5-7 for test method). |

**Note 1:** Parameter is characterized but not tested.

**2:** Data in "Typ." column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**3:** Required output enable filter high time must account for input path analog delays (= $T_{OEH}$ - $T_{DR}$ + $T_{DF}$).

**4:** Required output enable filter low time must account for input path analog delays (= $T_{OEL}$ + $T_{DR}$ - $T_{DF}$).

## SPI TIMING

**Electrical Specifications:** Standard Operating Conditions (unless otherwise stated),
Supply Voltage: 2.0V ≤ $V_{DD}$ ≤ 3.6V, Operating temperature: -40°C ≤ $T_A$ ≤ +85°C,
LCX Input Signal: Sinusoidal 300 $mV_{PP}$, Carrier Frequency: 125 kHz, LCCOM connected to $V_{SS}$

| Parameters | Sym | Min | Typ(1) | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| SCLK Frequency | $F_{SCLK}$ | — | — | 3 | MHz | |
| $\overline{CS}$ fall to first SCLK edge setup time | $T_{CSSC}$ | 100 | — | — | ns | |
| SDI setup time | $T_{SU}$ | 30 | — | — | ns | |
| SDI hold time | $T_{HD}$ | 50 | — | — | ns | |
| SCLK high time | $T_{HI}$ | 150 | — | — | ns | |
| SCLK low time | $T_{LO}$ | 150 | — | — | ns | |
| SDO setup time | $T_{DO}$ | — | — | 150 | ns | |
| SCLK last edge to $\overline{CS}$ rise setup time | $T_{SCCS}$ | 100 | — | — | ns | |
| $\overline{CS}$ high time | $T_{CSH}$ | 500 | — | — | ns | |
| $\overline{CS}$ rise to SCLK edge setup time | $T_{CS1}$ | 50 | — | — | ns | |
| SCLK edge to $\overline{CS}$ fall setup time | $T_{CS0}$ | 50 | — | — | ns | SCLK edge when $\overline{CS}$ is high |
| Rise time of SPI data (SPI Read command) | $TR_{SPI}$ | — | 10 | — | ns | $V_{DD}$ = 3.0V; time is measured from 10% to 90% of amplitude |
| Fall time of SPI data (SPI Read command) | $TF_{SPI}$ | — | 10 | — | ns | $V_{DD}$ = 3.0V; time is measured from 90% to 10% of amplitude |

**Note 1:** Data in “Typ.” column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, $V_{DD}$ = 2.0V to 3.6V, $V_{SS}$ = GND.

| Parameters | Symbol | Min | Typical | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 14L-TSSOP | $\theta_{JA}$ | — | 100 | — | °C/W | |

**NOTES:**

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $V_{DD}$ = 3V, Carrier Frequency = 125 kHz, LCCOM = connected to $V_{SS}$, $T_A$ = +25°C.

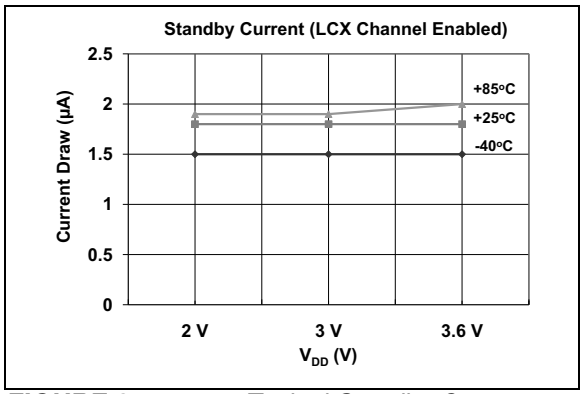



***FIGURE 2-1:*** *Typical Standby Current.*

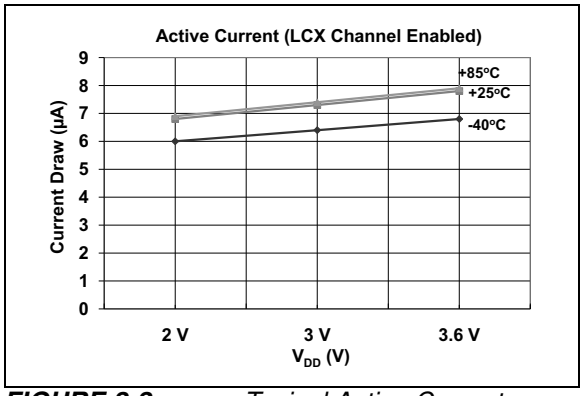



***FIGURE 2-2:*** *Typical Active Current.*

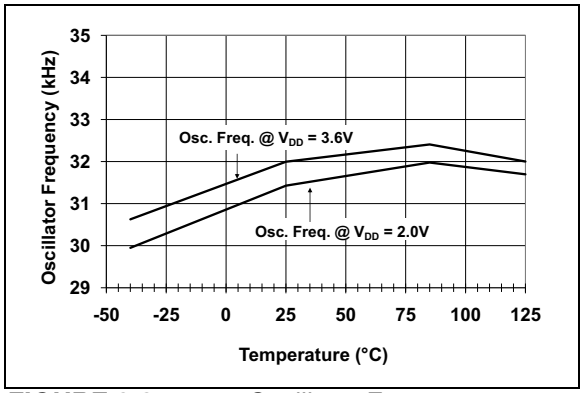



***FIGURE 2-3:*** *Oscillator Frequency vs. Temperature, $V_{DD}$ = 3.6V and 2.0V.*

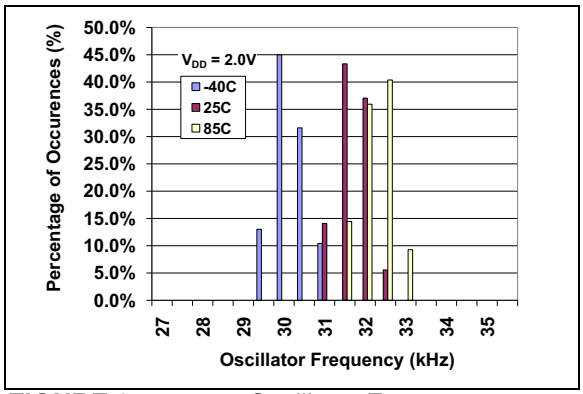



***FIGURE 2-4:*** *Oscillator Frequency Histograms vs. Temperature, $V_{DD}$ = 2V.*

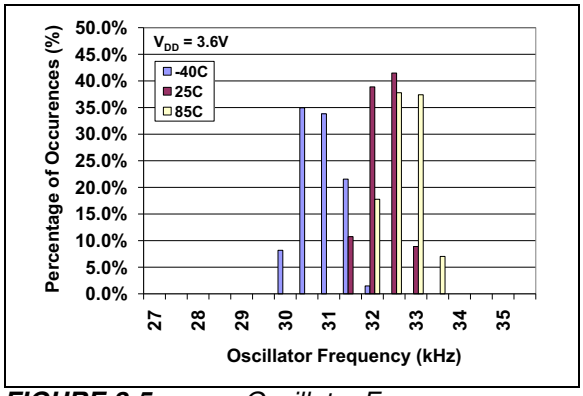



***FIGURE 2-5:*** *Oscillator Frequency Histograms vs. Temperature at $V_{DD}$ = 3V.*

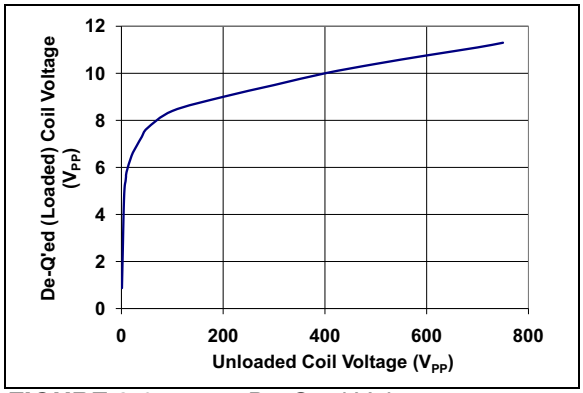



***FIGURE 2-6:*** *De-Q'ed Voltage vs. Unloaded Coil Voltage.*

**Note:** Unless otherwise indicated, $V_{DD}$ = 3V, Carrier Frequency = 125 kHz, LCCOM = connected to $V_{SS}$.

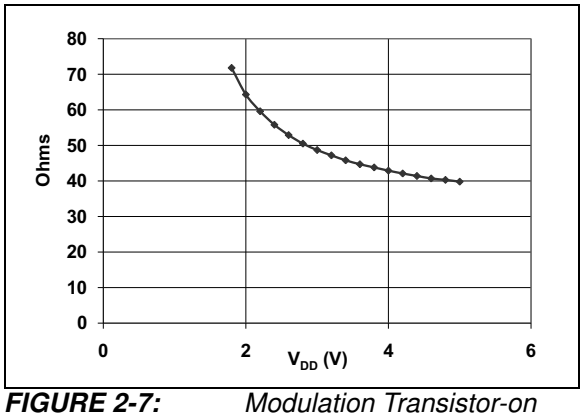



***FIGURE 2-7:*** *Modulation Transistor-on Resistance (+25°C).*

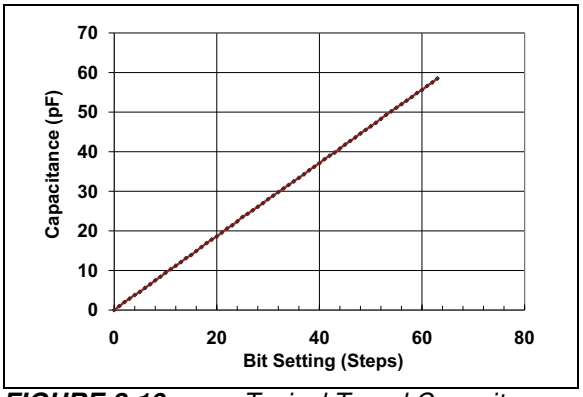



***FIGURE 2-10:*** *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting ($V_{DD}$ = 3V, Temperature = +25°C).*

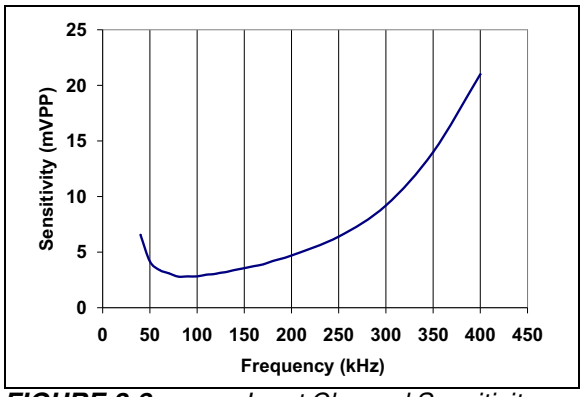



***FIGURE 2-8:*** *Input Channel Sensitivity vs. Bandwidth.*

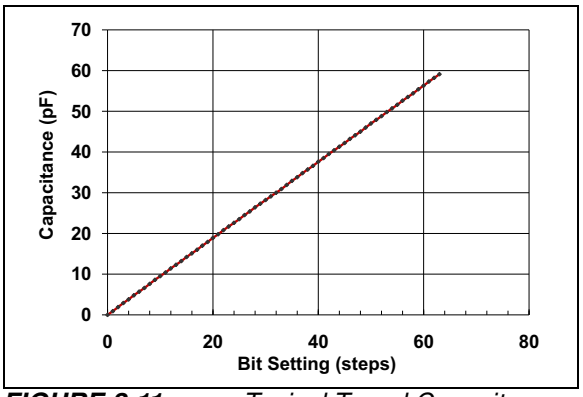



***FIGURE 2-11:*** *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting ($V_{DD}$ = 3V, Temperature = -40°C).*

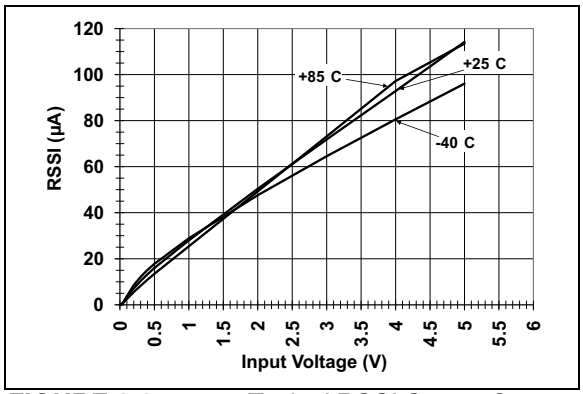



***FIGURE 2-9:*** *Typical RSSI Output Current vs. Input Signal Strength.*

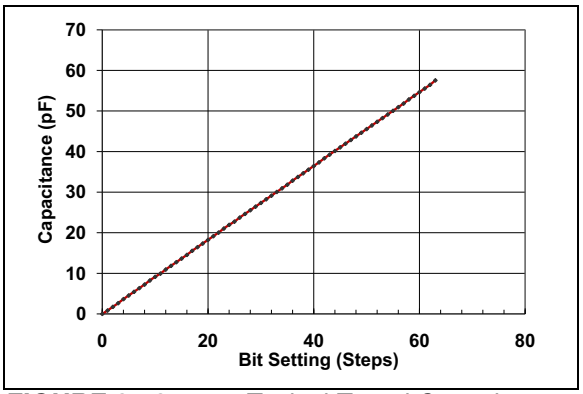
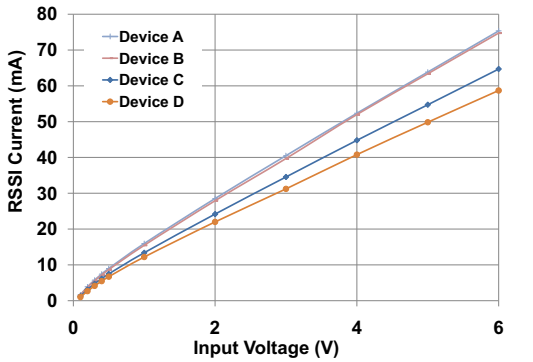



***FIGURE 2-12:*** *Typical Tuned Capacitance Value vs. Configuration Register Bit Setting ($V_{DD}$ = 3V, Temperature = +85°C).*

**Note:** Unless otherwise indicated, $V_{DD}$ = 3V, Carrier Frequency = 125 kHz, LCCOM = connected to $V_{SS}$.




**Note:** Equal amplitude is applied to each device.

***FIGURE 2-13:*** *Examples of RSSI Output Current Variations Between Device to Device at Room Temperature.*

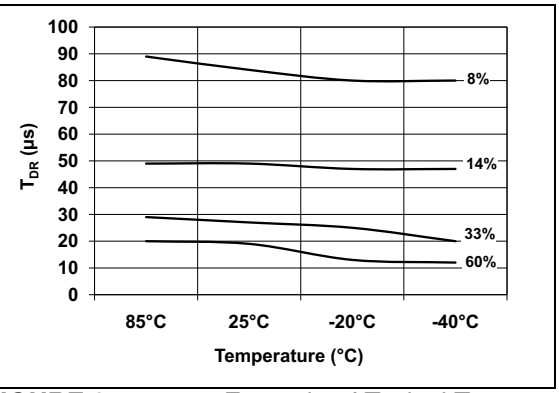



***FIGURE 2-14:*** *Example of Typical $T_{DR}$ Changes over Temperature.*
*Input Signal Condition: Amplitude = 300 $mV_{PP}$, Modulation Depth = 100 %.*

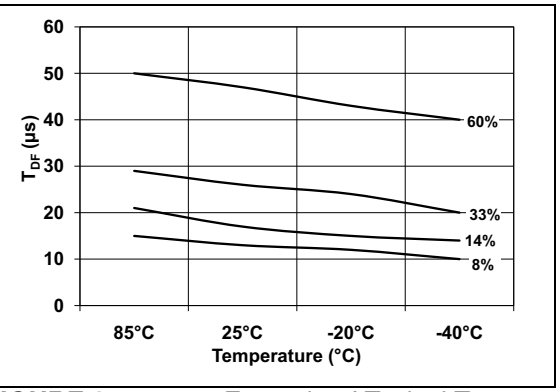



***FIGURE 2-15:*** *Example of Typical $T_{DF}$ Changes over Temperature.*
*Input Signal Condition: Amplitude = 300 $mV_{PP}$, Modulation Depth = 100 %.*

## 2.1 Performance Plots

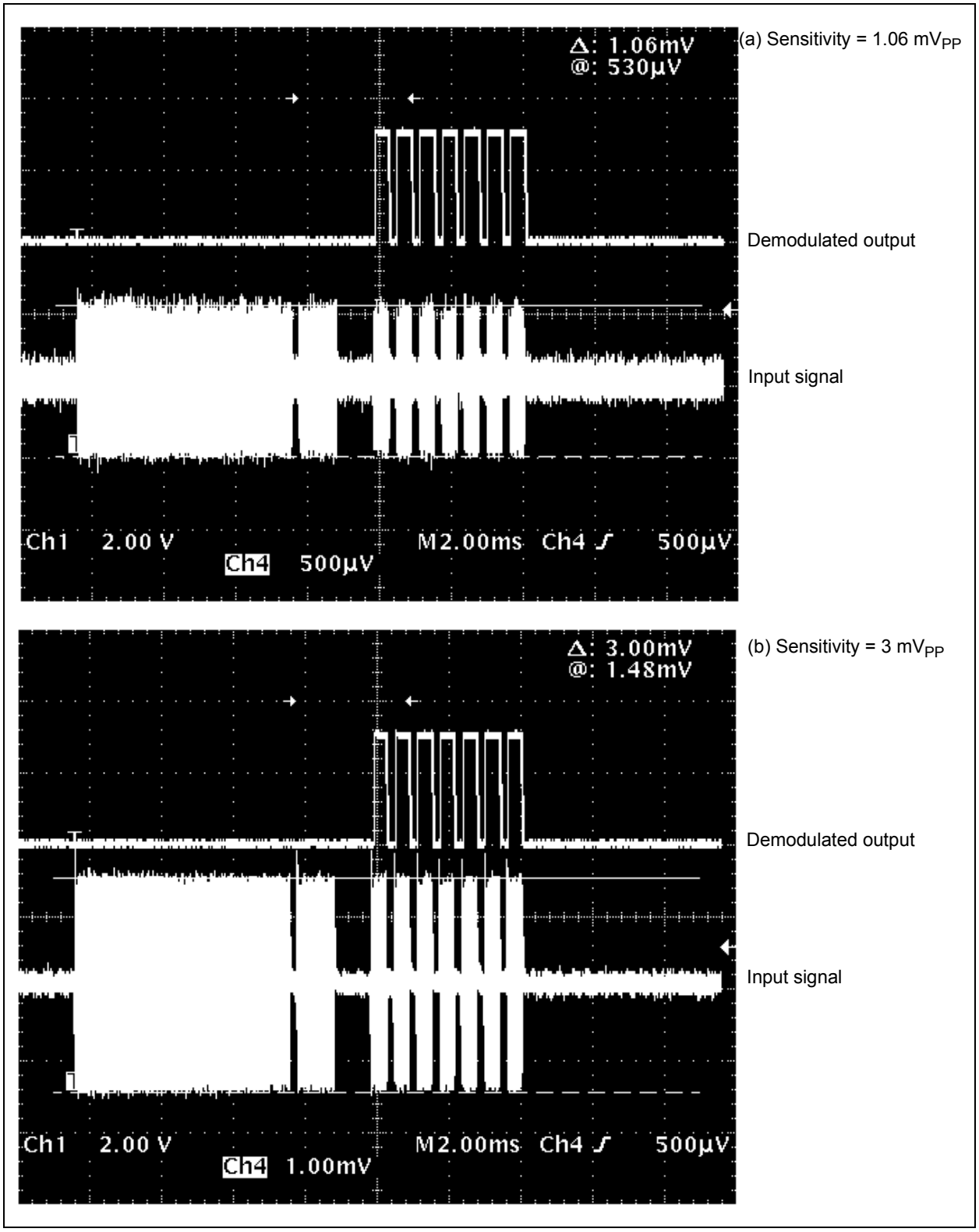
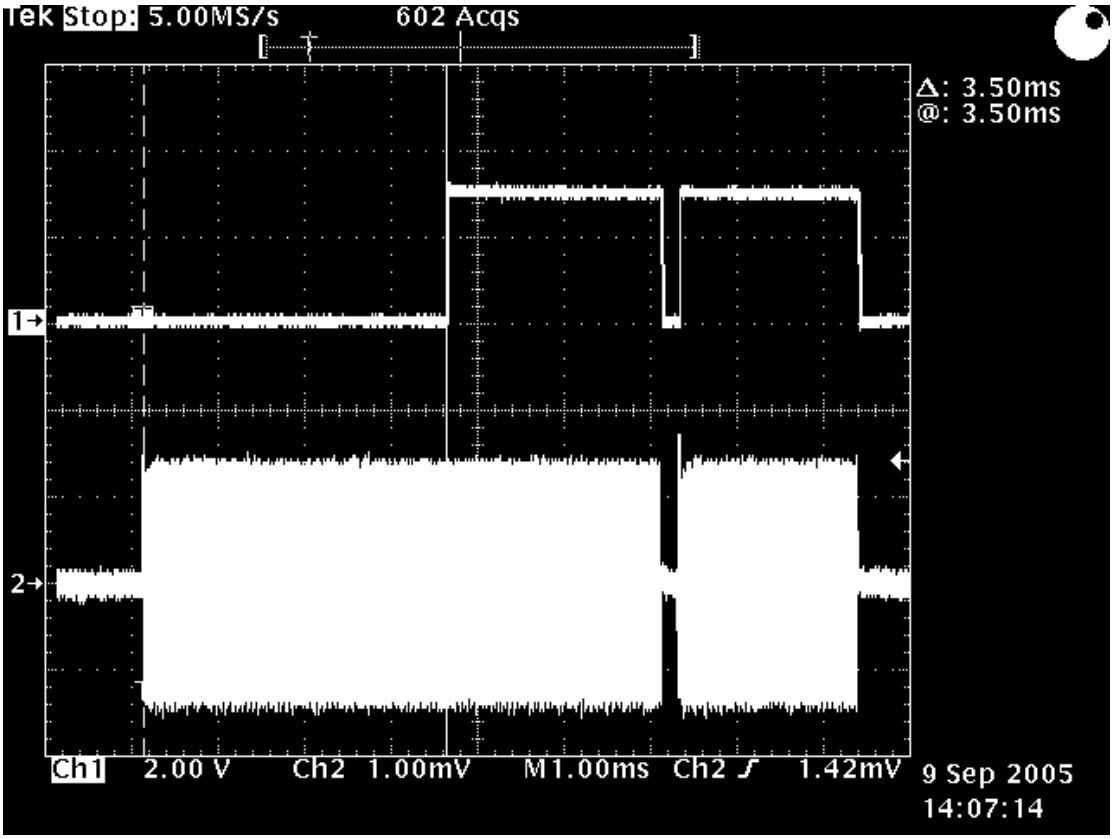
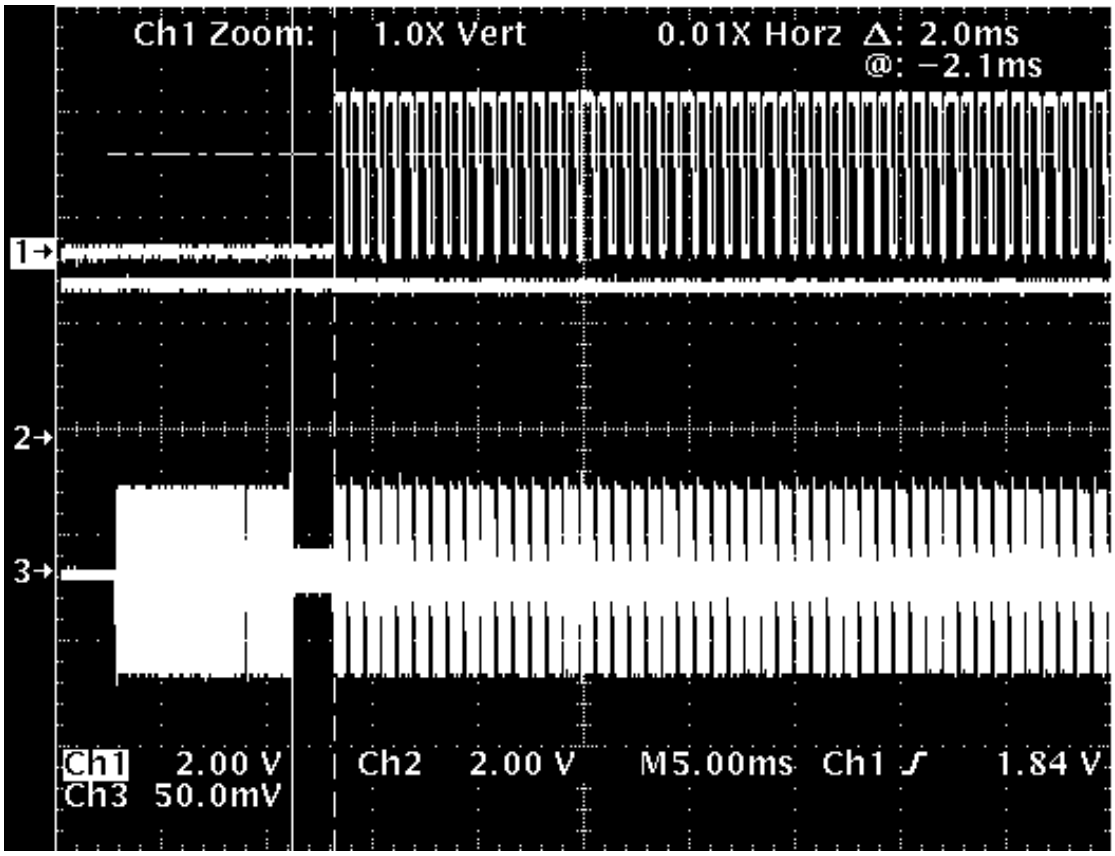



***FIGURE 2-16:*** *Input Sensitivity Example.*



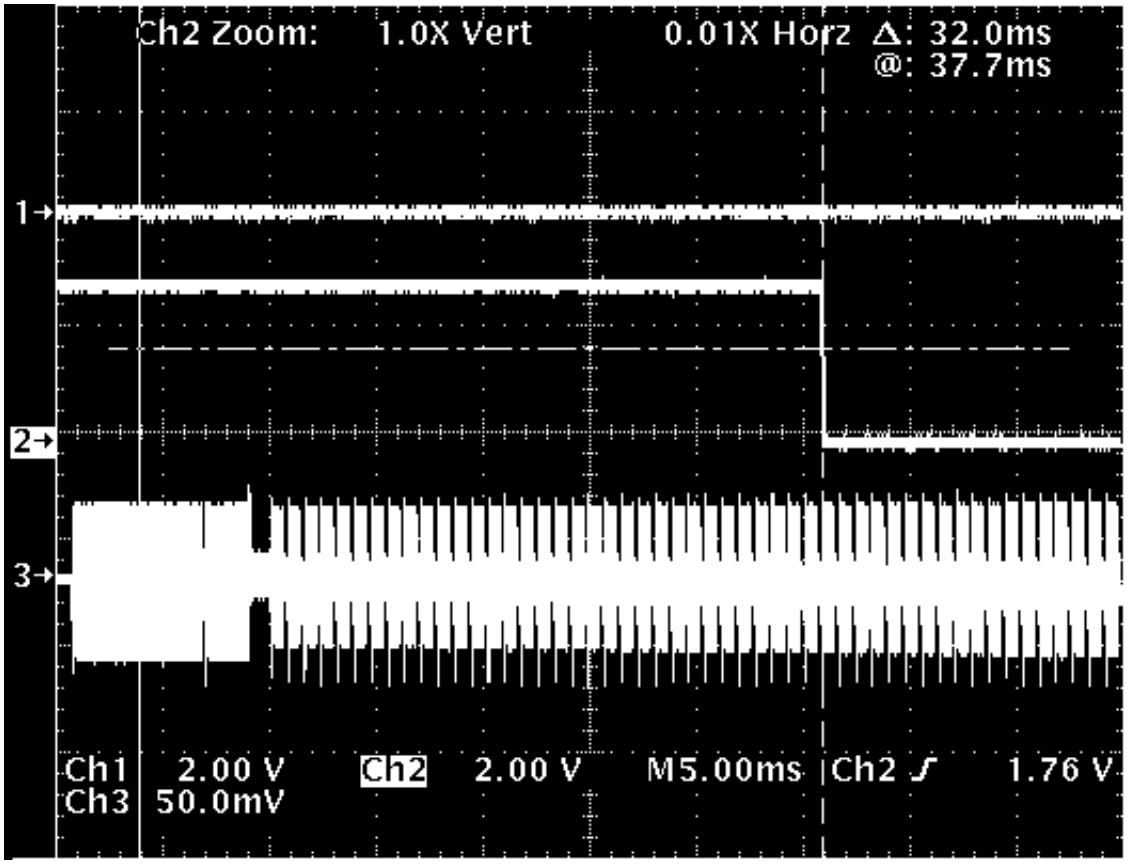

**Note:** Ch2 is the input and Ch1 is the output (demodulated data appears after AGC Initialization time ($T_{AGC}$)). Output Enable Filter is disabled.

***FIGURE 2-17:*** *Typical AGC Initialization Time at Room Temperature ($V_{DD}$ = 3V).*



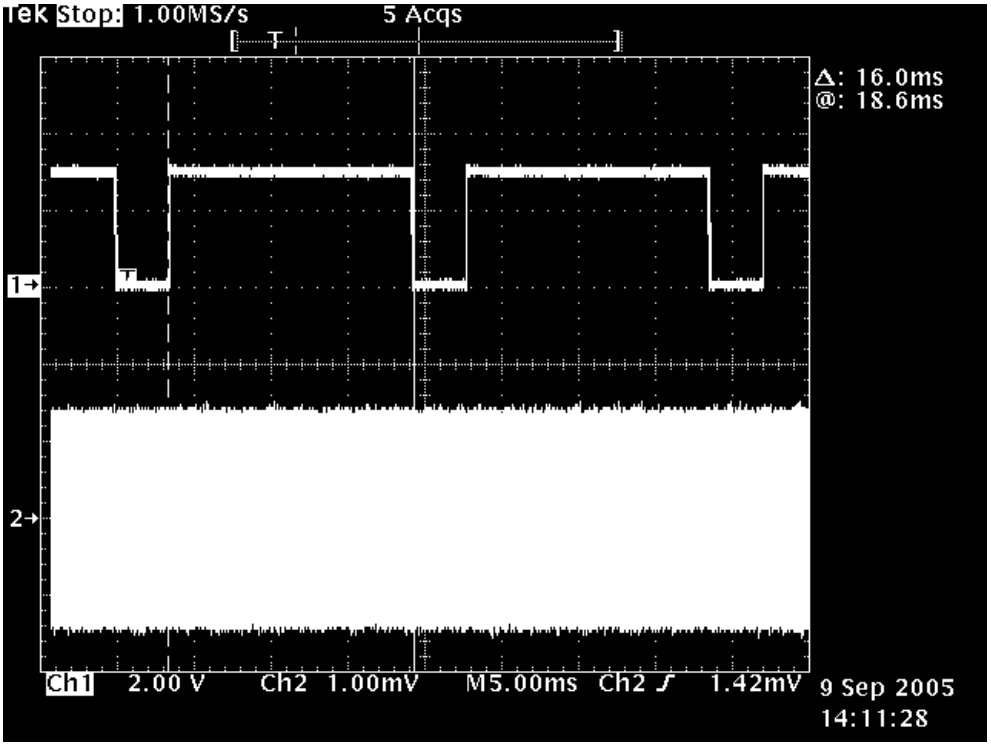

**Note:** Ch3 is the input with correct Output Enable Filter timing.
Ch1 is the demodulated LFDATA output.
Ch2 is the $\overline{\text{ALERT}}$ pin output. It shows that the $\overline{\text{ALERT}}$ output pin maintains logic high if the input signal meets the programmed filter timing requirement.

***FIGURE 2-18:*** *$\overline{\text{ALERT}}$ Output Example: With No Parity Error and no 32 ms Alarm Timer Time-out.*




**Note:** The 32 ms Alarm Timer is enabled only if the Output Enable Filter is enabled.
Ch3 is the input signal with incorrect Output Enable Filter timing.
Ch1 is the demodulated LFDATA output. No output since the input filter is not matched.
Ch2 is the $\overline{\text{ALERT}}$ output.
The output shows that the logic level changes after 32 ms from the AGC initialization time ($T_{AGC}$) if the input signal does not meet the programmed filter timing requirement.

***FIGURE 2-19:*** *$\overline{\text{ALERT}}$ Output Example: With 32 ms Alarm Timer Timed Out.*




(a) Output (Ch1): Device repeats Soft Reset after 16 ms, Inactivity Timer has timed out

(b) Input (Ch2): Input has no modulation

**Note:** Ch2 is the input without modulation (i.e., noise).
Ch1 is the output at the LFDATA pin due to the 16 ms Soft Inactivity Timer time out. Note the 3.5 ms AGC initialization time after the Soft Reset.
The cases shown above apply when the Output Filter is disabled.

***FIGURE 2-20:*** *Examples of Soft Inactivity Timer Time Out: This output is available only if the Output Enable Filter is disabled.*

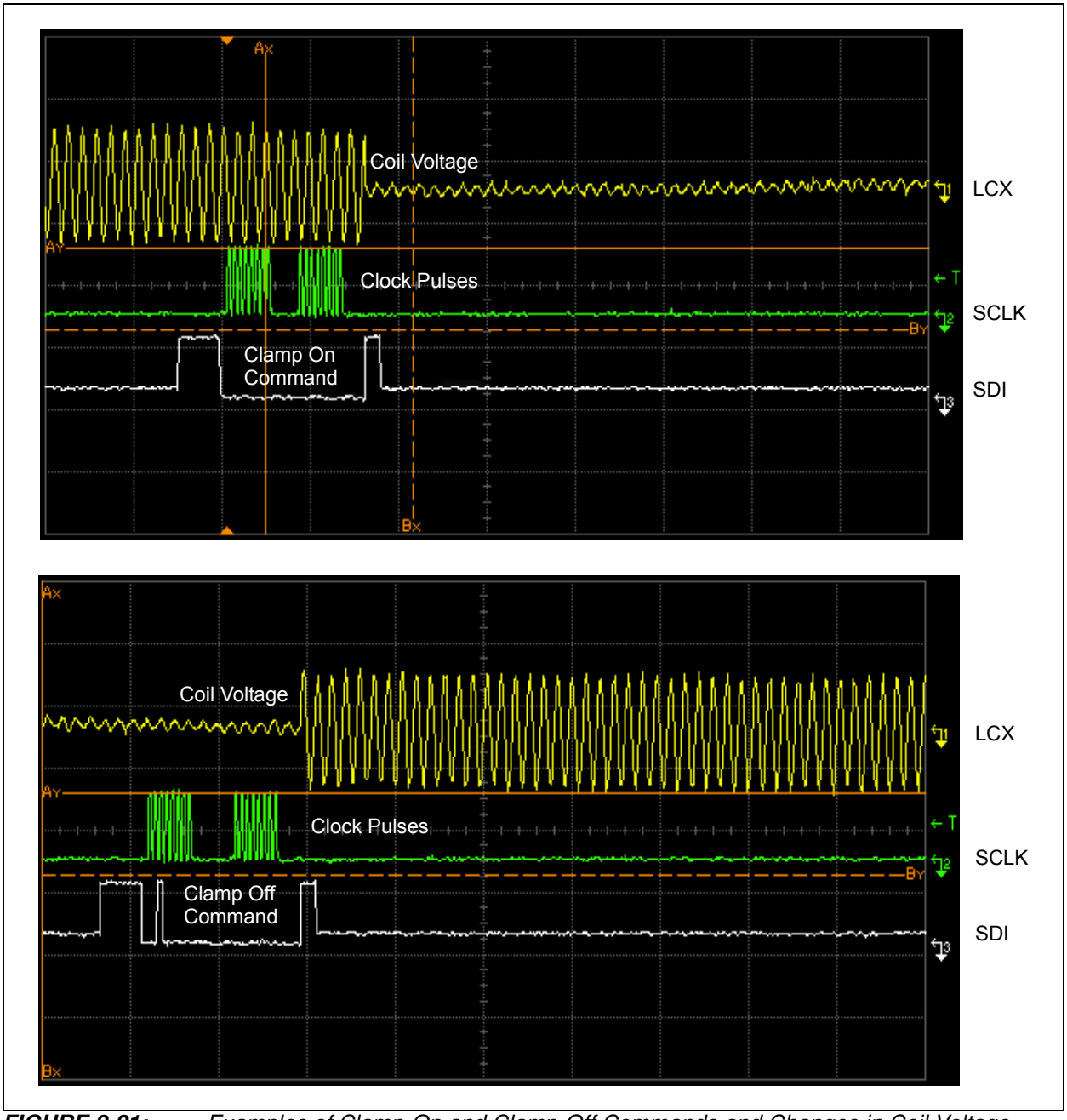



***FIGURE 2-21:*** *Examples of Clamp-On and Clamp-Off Commands and Changes in Coil Voltage.*

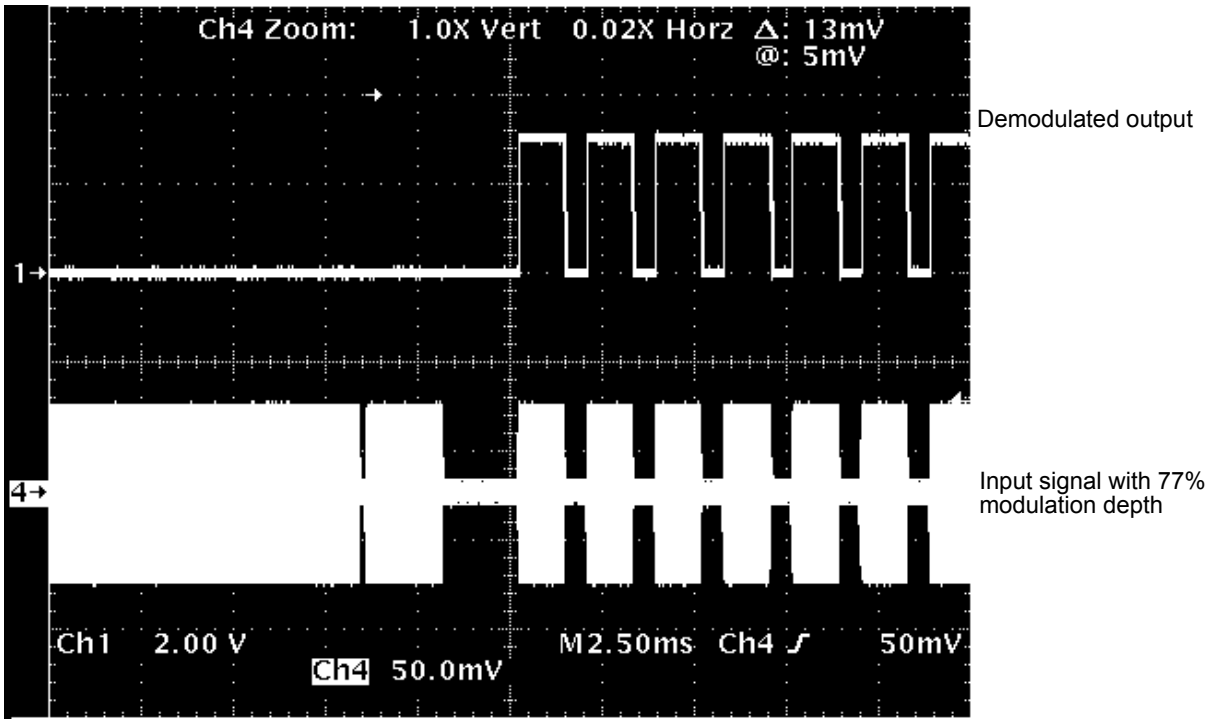
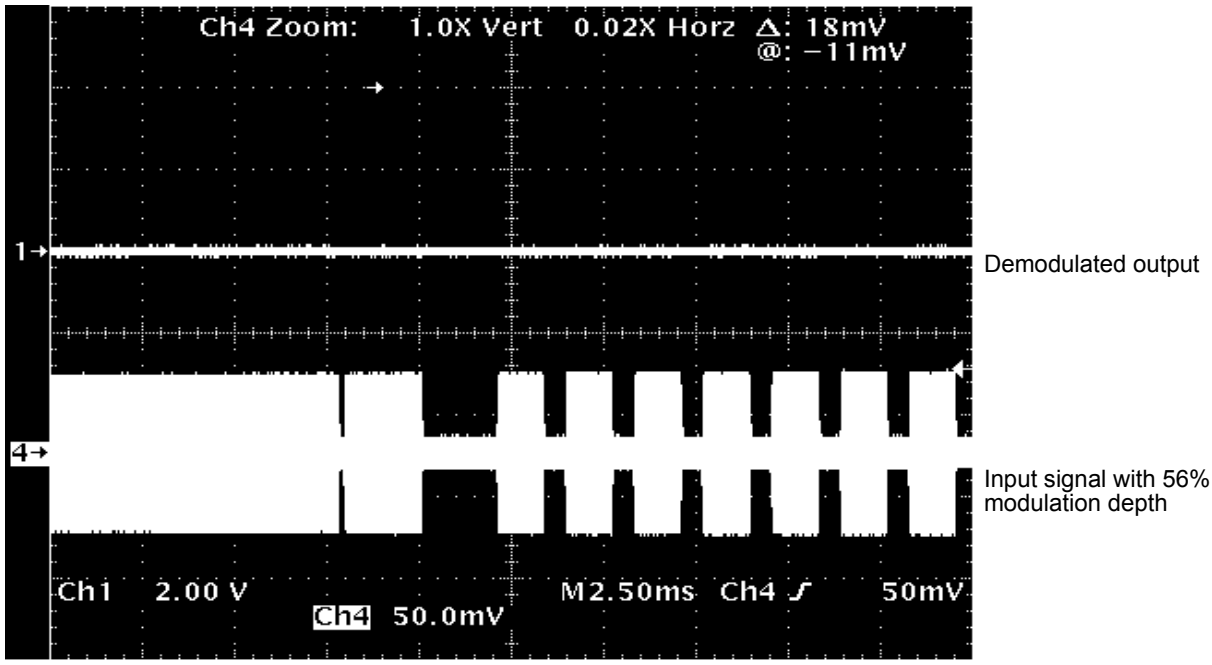



***FIGURE 2-22:*** *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 77%, Minimum Modulation Depth (MODMIN) Setting = 60%.*




**Note:** There is no demodulated output since the modulation depth of the input signal is lower than the minimum modulation depth setting. The device will have demodulated output if the Minimum Modulation Depth option is set to 8%, 14%, or 33%.

***FIGURE 2-23:*** *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 56%, Minimum Modulation Depth (MODMIN) Setting = 60%.*

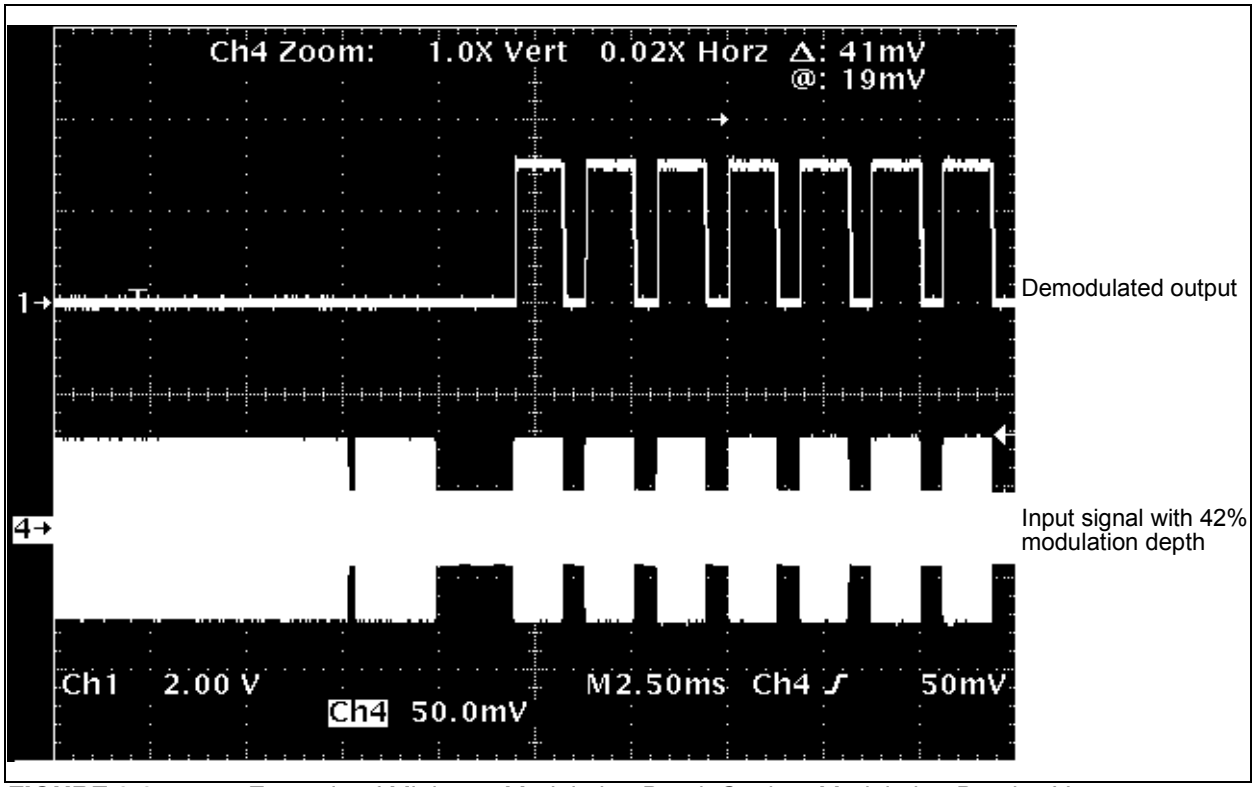



***FIGURE 2-24:*** *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 42%, Minimum Modulation Depth (MODMIN) Setting = 33%.*

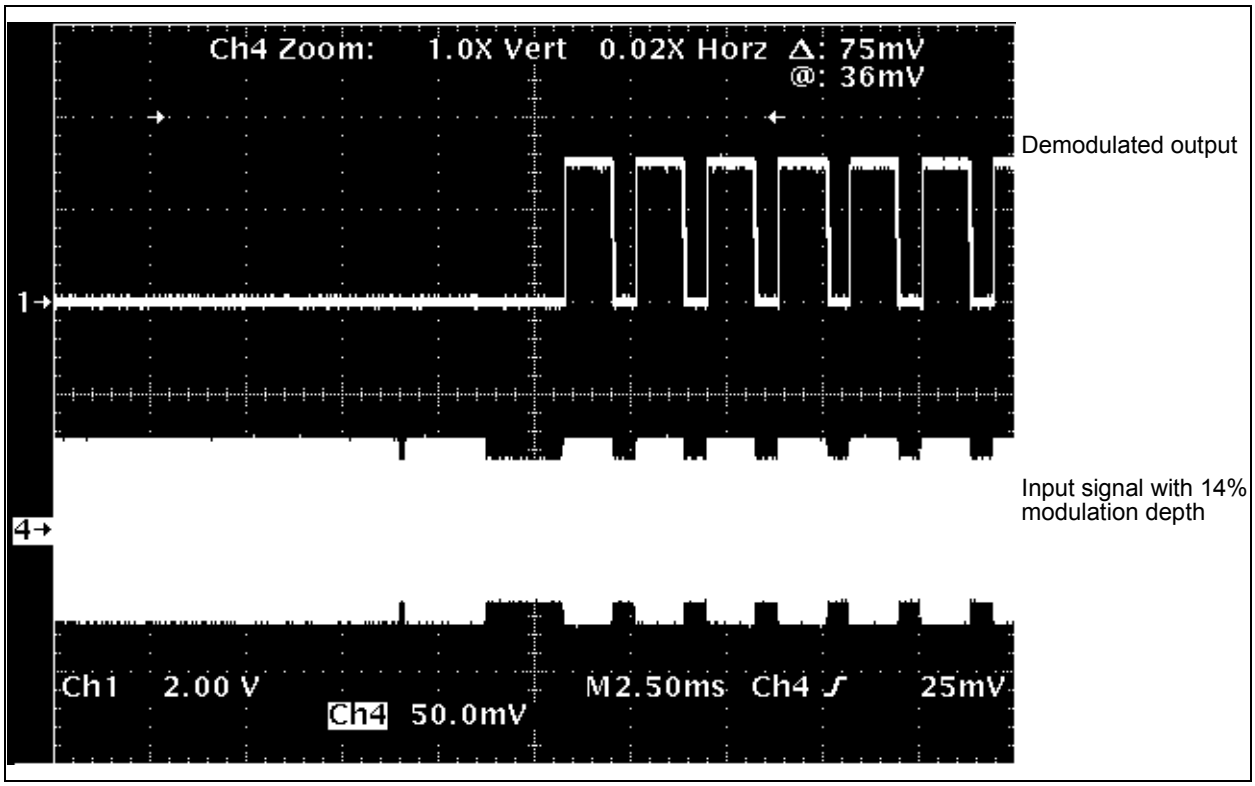
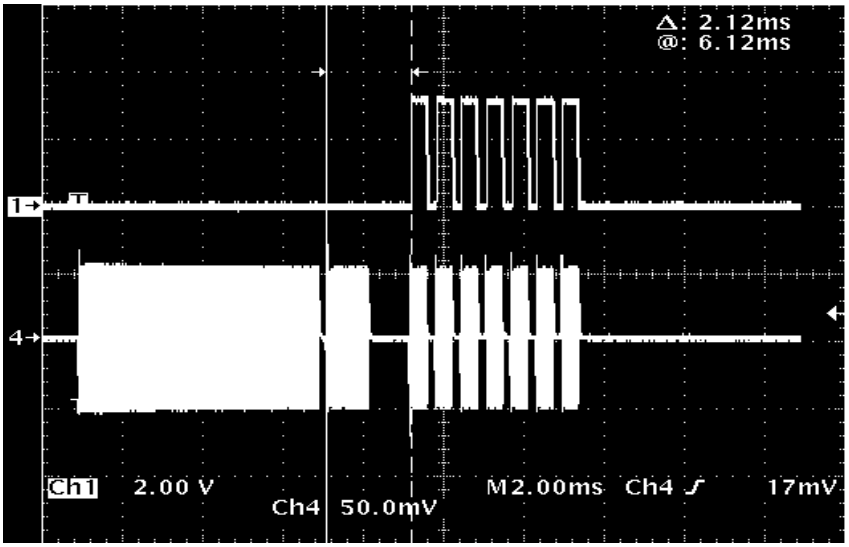
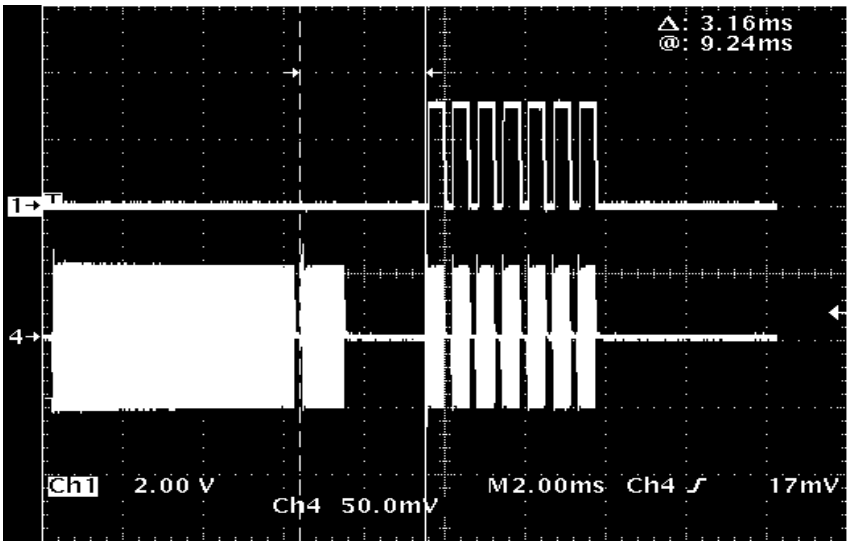



***FIGURE 2-25:*** *Example of Minimum Modulation Depth Setting: Modulation Depth of Input Signal = 14%, Minimum Modulation Depth (MODMIN) Setting = 14%.*



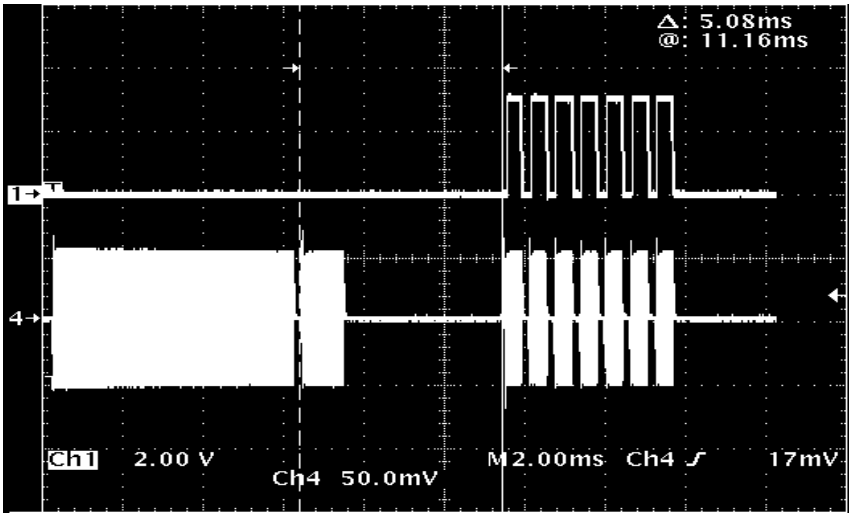

**Filter 1**

| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 1 ms<br>$T_{OEL}$ = 1 ms<br>$T_{OET}$ = 3 ms | 01<br>or<br>01 | 00<br><br>01 |




**Filter 2**

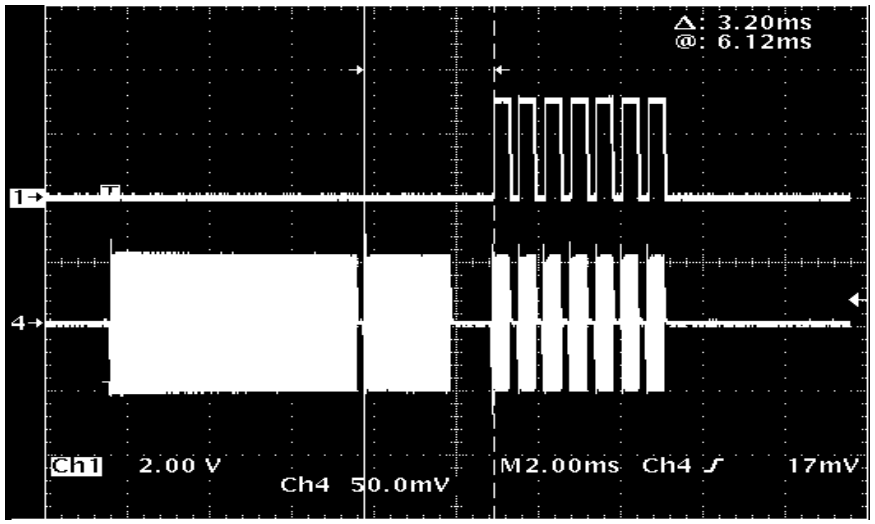
| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 1 ms<br>$T_{OEL}$ = 2 ms<br>$T_{OET}$ = 4 ms | 01 | 10 |




**Filter 3**

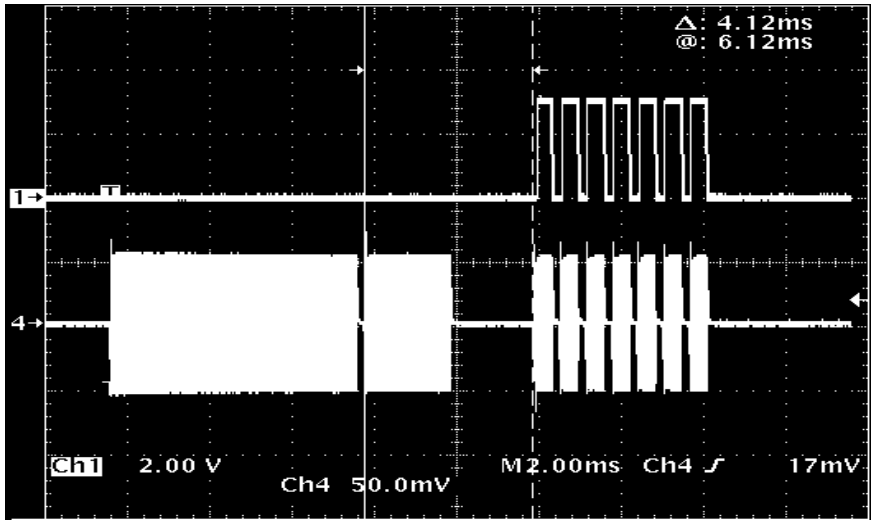
| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 1 ms<br>$T_{OEL}$ = 4 ms<br>$T_{OET}$ = 6 ms | 01 | 11 |

***FIGURE 2-26:*** *Examples of Output Enable Filters 1 through 3 (Wake-up Filters) and Demodulated Outputs.*



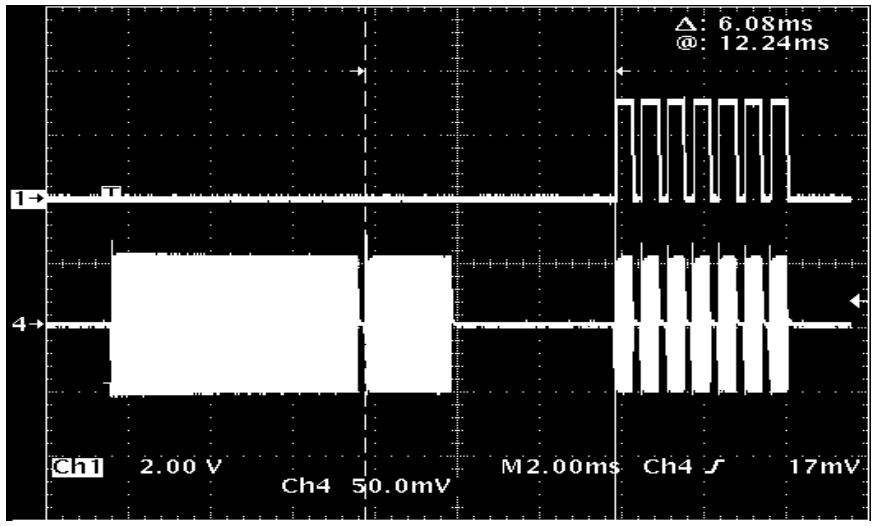

**Filter 4**

| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 2 ms<br>$T_{OEL}$ = 1 ms<br>$T_{OET}$ = 4 ms | 10<br>or<br>10 | 00<br><br>01 |




**Filter 5**

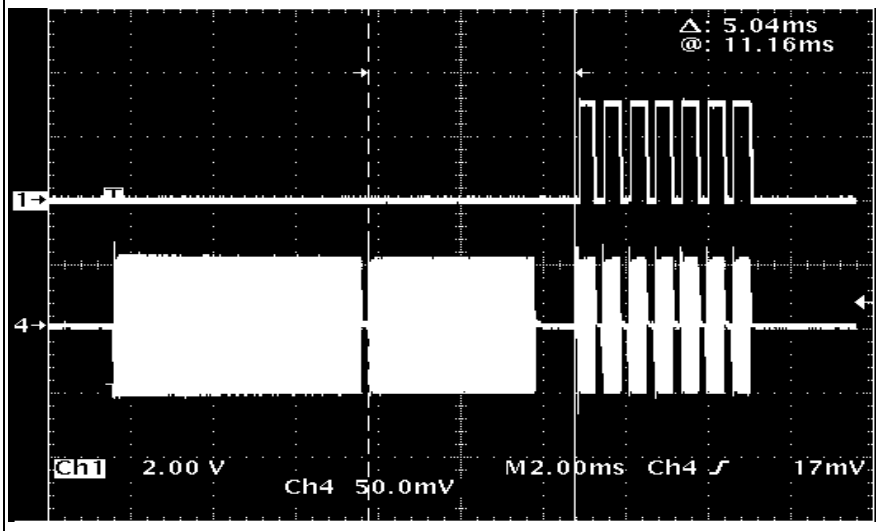
| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 2 ms<br>$T_{OEL}$ = 2 ms<br>$T_{OET}$ = 5 ms | 10 | 10 |




**Filter 6**

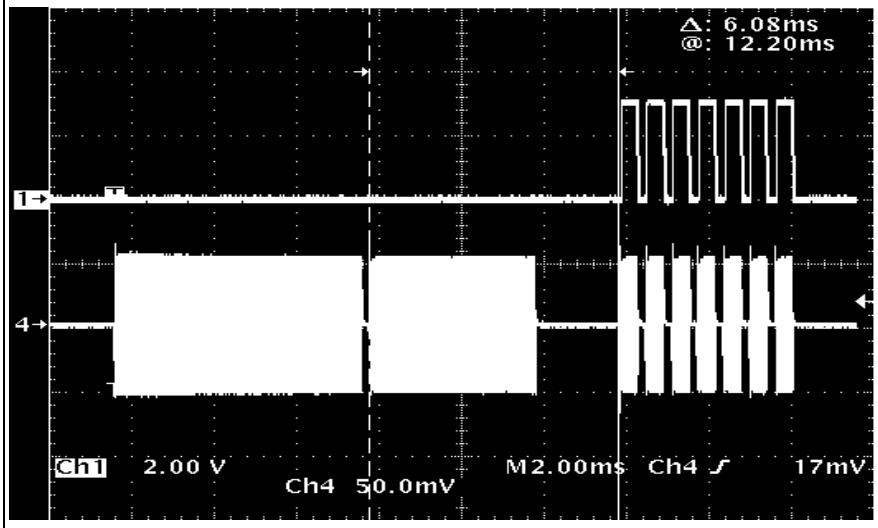
| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 2 ms<br>$T_{OEL}$ = 4 ms<br>$T_{OET}$ = 8 ms | 10 | 11 |

***FIGURE 2-27:*** *Examples of Output Enable Filters 4 through 6 (Wake-up Filters) and Demodulated Outputs.*



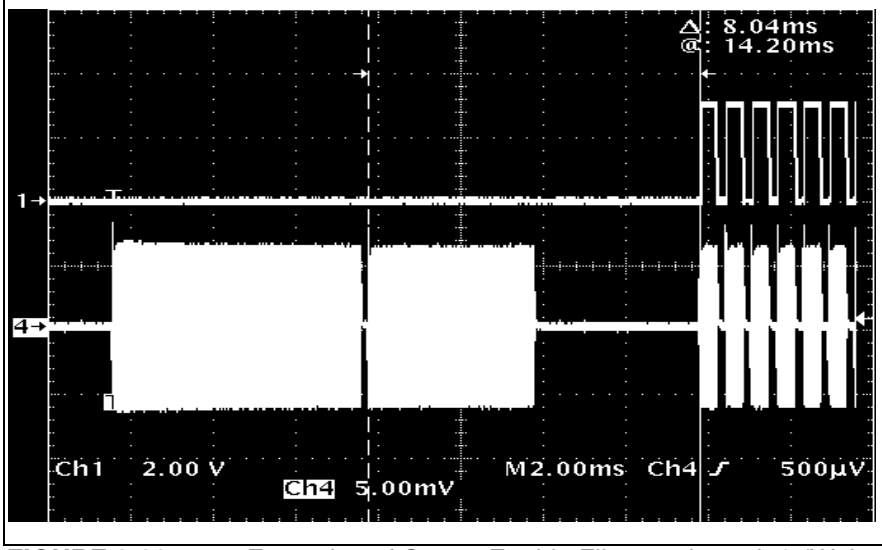

**Filter 7**

| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 4 ms<br>$T_{OEL}$ = 1 ms<br>$T_{OET}$ = 6 ms | 11<br>or<br>11 | 00<br><br>01 |




**Filter 8**

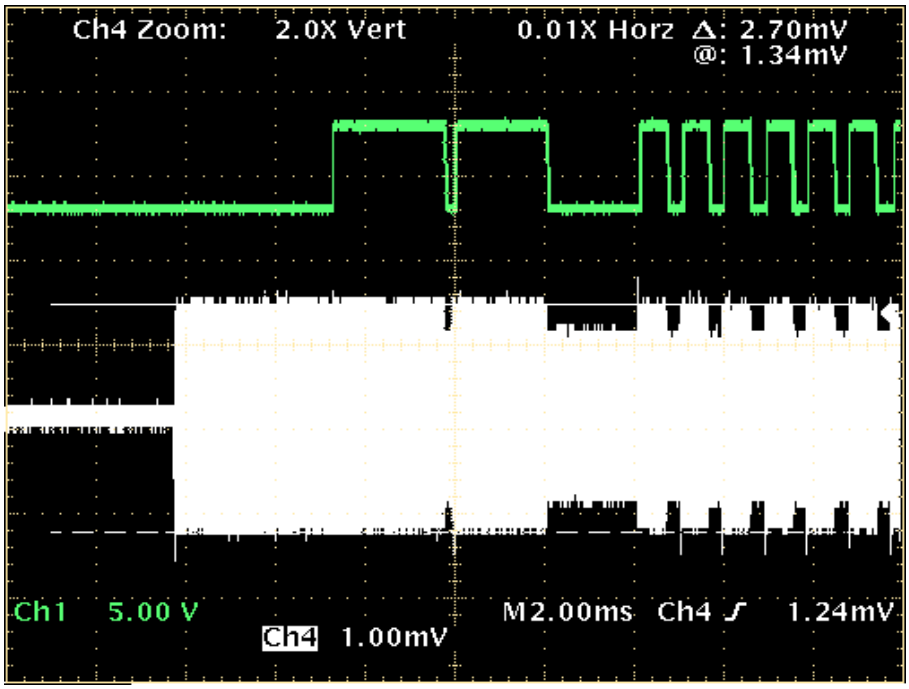
| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 4 ms<br>$T_{OEL}$ = 2 ms<br>$T_{OET}$ = 8 ms | 11 | 10 |




**Filter 9**

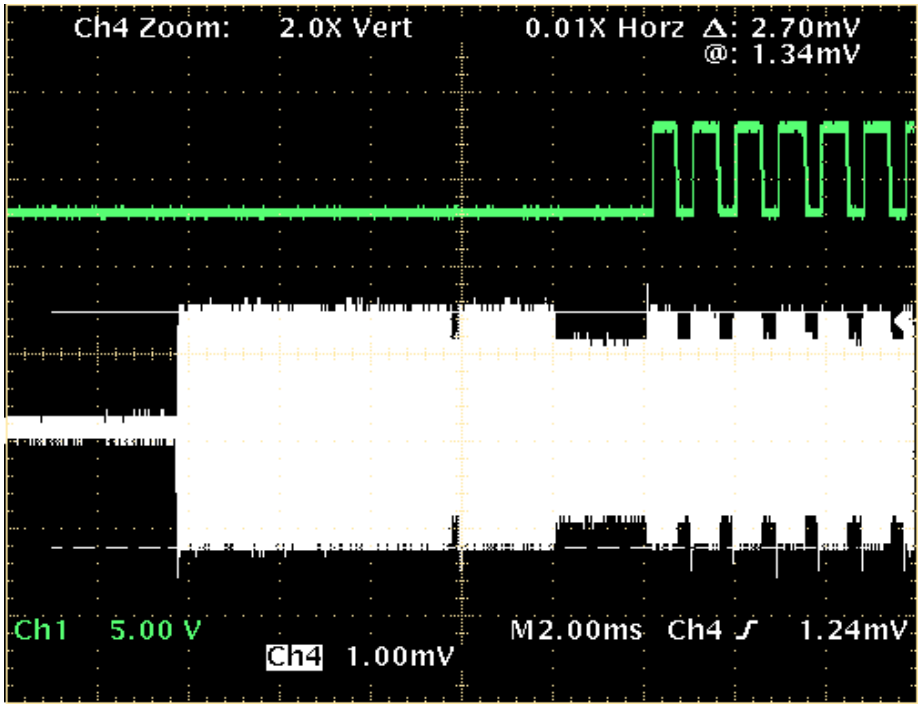
| Output Enable Filter Timing of Input Signal | Configuration Bit Settings | |
|---|---|---|
| | OEH | OEL |
| $T_{OEH}$ = 4 ms<br>$T_{OEL}$ = 4 ms<br>$T_{OET}$ = 10 ms | 11 | 11 |

***FIGURE 2-28:*** *Examples of Output Enable Filters 7 through 9 (Wake-up Filters) and Demodulated Outputs.*




**Note:** Demodulated output is available immediately after AGC initialization.

***FIGURE 2-29:*** *Input Signal and Demodulated Output When the Output Enable Filter is Disabled.*




**Note:** Demodulated output is available only if the incoming signal meets the enable filter timing criteria that is defined in the Configuration Register 0 (Register 5-1). If the criteria is met, the output is available after the low timing ($T_{OEL}$) of the Enable Filter.

***FIGURE 2-30:*** *Input Signal and Demodulator Output When Output Enable Filter is Enabled and Input Meets Filter Timing Requirements.*