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MCP23016

16-Bit I²C™ I/O Expander

Features

- 16-bit remote bidirectional I/O port
  - 16 I/O pins default to 16 inputs
- Fast I²C™ bus clock frequency (0 - 400 kbits/s)
- Three hardware address pins allow use of up to eight devices
- High-current drive capability per I/O: ±25 mA
- Open-drain interrupt output on input change
- Interrupt port capture register
- Internal Power-On Reset (POR)
- Polarity inversion register to configure the polarity of the input port data
- Compatible with most microcontrollers
- Available temperature range:
  - Industrial (I): -40°C to +85°C

CMOS Technology

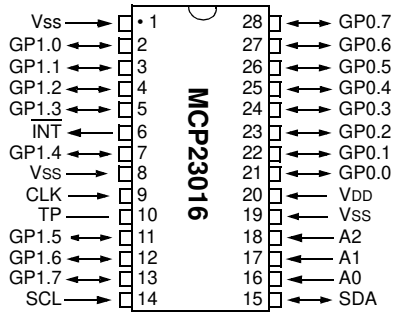
- Operating Supply Voltage: 2.0V to 5.5V
- Low standby current

Packages

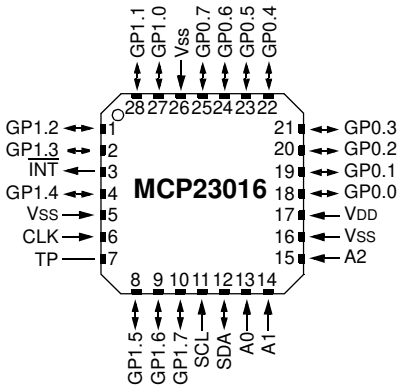
- 28-pin PDIP, 300 mil; 28-pin SOIC, 300 mil
- 28-pin SSOP, 209 mil; 28-pin QFN, 6x6 mm

Package Types

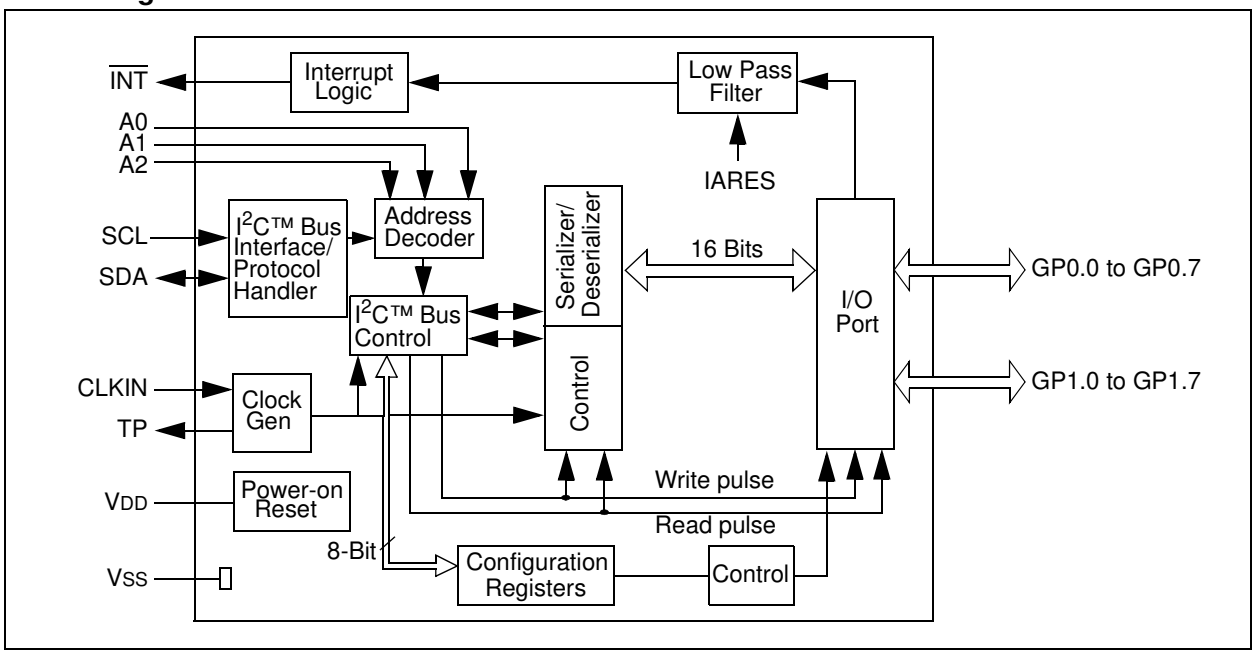
PDIP, SOIC, SSOP



QFN



Block Diagram



NOTES:

1.0 DEVICE OVERVIEW

The MCP23016 device provides 16-bit, general purpose, parallel I/O expansion for I^2C bus applications.

This device includes high-current drive capability, low supply current and individual I/O configuration. I/O expanders provide a simple solution when additional I/Os are needed for ACPI, power switches, sensors, push buttons, LEDs and so on.

The MCP23016 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the read register can be inverted with the polarity inversion register (see **Section 1.7.3, "Input Polarity Registers"**). All registers can be read by the system master.

The open-drain interrupt output is activated when any input state differs from its corresponding input port register state. This is used to indicate to the system master that an input state has changed. The interrupt capture register captures port value at this time. The Power-on Reset sets the registers to their default values and initializes the device state machine.

Three device inputs (A0 - A2) determine the I^2C address and allow up to eight I/O expander devices to share the same I^2C bus.

1.1 Pin Descriptions

TABLE 1-1: PINOUT DESCRIPTION

Pin Name	PDIP, SOIC, SSOP Pin No.	QFN Pin No.	I/O/P Type	Buffer Type	Description
CLK	9	6	I	ST	Clock source input
TP	10	7	O	—	Test Pin (This pin must be left floating)
GP1.0	2	27	I/O	TTL	D0 digital input/output for GP1
GP1.1	3	28	I/O	TTL	D1 digital input/output for GP1
GP1.2	4	1	I/O	TTL	D2 digital input/output for GP1
GP1.3	5	2	I/O	TTL	D3 digital input/output for GP1
GP1.4	7	4	I/O	TTL	D4 digital input/output for GP1
GP1.5	11	8	I/O	ST	D5 digital input/output for GP1
GP1.6	12	9	I/O	ST	D6 digital input/output for GP1
GP1.7	13	10	I/O	ST	D7 digital input/output for GP1
GP0.0	21	18	I/O	TTL	D0 digital input/output for GP0
GP0.1	22	19	I/O	TTL	D1 digital input/output for GP0
GP0.2	23	20	I/O	TTL	D2 digital input/output for GP0
GP0.3	24	21	I/O	TTL	D3 digital input/output for GP0
GP0.4	25	22	I/O	TTL	D4 digital input/output for GP0
GP0.5	26	23	I/O	TTL	D5 digital input/output for GP0
GP0.6	27	24	I/O	TTL	D6 digital input/output for GP0
GP0.7	28	25	I/O	TTL	D7 digital input/output for GP0
SCL	14	11	I	ST	Serial clock input
SDA	15	12	I/O	ST	Serial data I/O
$\overline{INT}$	6	3	O	OD	Interrupt output
A0	16	13	I	ST	Address input 1
A1	17	14	I	ST	Address input 2
A2	18	15	I	ST	Address input 3
V_{SS}	1, 8, 19	5, 16, 26	P	—	Ground reference for logic and I/O pins
V_{DD}	20	17	P	—	Positive supply for logic and I/O pins

1.2 Power-on Reset (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level to deactivate the POR circuit (i.e., release RESET). A maximum rise time for VDD is specified in the electrical specifications.

When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature) must be met to ensure proper operation.

1.3 Power-up Timer (PWRT)

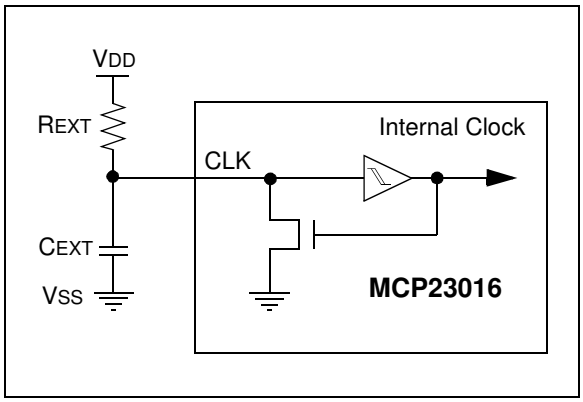
The Power-up Timer provides a 72 ms nominal time-out on power-up, keeping the device in RESET and allowing VDD to rise to an acceptable level.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See Table 2-4 for details (TPWRT, parameter 3).

1.4 Clock Generator

The MCP23016 uses an external RC circuit to determine the internal clock speed. The user must connect R and C to the MCP23016, as shown in Figure 1-1.

FIGURE 1-1: CLOCK CONFIGURATION



A 1 MHz (typ.) internal clock is needed for the device to function properly. The internal clock can be measured on the TP pin. Recommended REXT and CEXT values are shown in Table 1-2.

Note:	Set IARES = 1 to measure the clock output on TP.

TABLE 1-2: RECOMMENDED VALUES

REXT	CEXT
3.9 kΩ	33 pF

1.5 I²C Bus Interface/ Protocol Handler

This block manages the functionality of the I²C bus interface and protocol handling. The MCP23016 supports the following commands:

TABLE 1-3: COMMAND BYTE TO REGISTER RELATIONSHIP

Command Byte	Result
0h	Access to GP0
1h	Access to GP1
2h	Access to OLAT0
3h	Access to OLAT1
4h	Access to IPOL0
5h	Access to IPOL1
6h	Access to IODIR0
7h	Access to IODIR1
8h	Access to INTCAP0 (Read-Only)
9h	Access to INTCAP1 (Read-Only)
Ah	Access to IOCON0
Bh	Access to IOCON1

1.6 Address Decoder

The last three LSb of the 7-bit address are user-defined (see Table 1-4). Three hardware pins (<A2:A0>) define these bits.

TABLE 1-4: DEVICE ADDRESS

0	1	0	0	A2	A1	A0

1.7 Register Block

The register block contains the Configuration and Port registers, as shown in Table 1-5.

TABLE 1-5: REGISTER SUMMARY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
Port Registers									
GP0	GP0.7	GP0.6	GP0.5	GP0.4	GP0.3	GP0.2	GP0.1	GP0.0	0000 0000
GP1	GP1.7	GP1.6	GP1.5	GP1.4	GP1.3	GP1.2	GP1.1	GP0.0	0000 0000
OLAT0	OL0.7	OL0.6	OL0.5	OL0.4	OL0.3	OL0.2	OL0.1	OL0.0	0000 0000
OLAT1	OL1.7	OL1.6	OL1.5	OL1.4	OL1.3	OL1.2	OL1.1	OL1.0	0000 0000
Configuration Registers									
IPOL0	IGP0.7	IGP0.6	IGP0.5	IGP0.4	IGP0.3	IGP0.2	IGP0.1	IGP0.0	0000 0000
IPOL1	IGP1.7	IGP1.6	IGP1.5	IGP1.4	IGP1.3	IGP1.2	IGP1.1	IGP1.0	0000 0000
IODIR0	IOD0.7	IOD0.6	IOD0.5	IOD0.4	IOD0.3	IOD0.2	IOD0.1	IOD0.0	1111 1111
IODIR1	IOD1.7	IOD1.6	IOD1.5	IOD1.4	IOD1.3	IOD1.2	IOD1.1	IOD1.0	1111 1111
INTCAP0	ICP0.7	ICP0.6	ICP0.5	ICP0.4	ICP0.3	ICP0.2	ICP0.1	ICP0.0	xxxx xxxx
INTCAP1	ICP1.7	ICP1.6	ICP1.5	ICP1.4	ICP1.3	ICP1.2	ICP1.1	ICP1.0	xxxx xxxx
IOCON0	—	—	—	—	—	—	—	IARES	---- ---0
IOCON1	—	—	—	—	—	—	—	IARES	---- ---0

Legend: ‘1’ bit is set, ‘0’ bit is cleared, x = unknown, — = unimplemented.

1.7.1 DATA PORT REGISTERS

Two registers provide access to the two GPIO ports:

- GP0 (provides access to data port GP0)
- GP1 (provides access to data port GP1)

A read from this register provides status on pins of these ports. A write to these registers will modify the output latch registers (OLAT0, OLAT1) and data output.

REGISTER 1-1: GP0 - GENERAL PURPOSE I/O PORT REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP0.7	GP0.6	GP0.5	GP0.4	GP0.3	GP0.2	GP0.1	GP0.0
bit 7							bit 0

bit 7-0 **GP0.0:GP0.7**: Reflects the logic level on the pins.
1 = Logic '1'
0 = Logic '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 1-2: GP1 - GENERAL PURPOSE I/O PORT REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP1.7	GP1.6	GP1.5	GP1.4	GP1.3	GP1.2	GP1.1	GP1.0
bit 7							bit 0

bit 7-0 **GP1.0:GP1.7**: Reflects the logic level on the pins.
1 = Logic '1'
0 = Logic '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.7.2 OUTPUT LATCH REGISTERS

Two registers provide access to the two port output latches:

- OLAT0 (provides access to the output latch for port GP0)
- OLAT1 (provides access to the output latch for port GP1)

A read from these registers results in a read of the latch that controls the output and not the actual port. A write to these registers updates the output latch that controls the output.

REGISTER 1-3: OLAT0 - OUTPUT LATCH REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL0.7	OL0.6	OL0.5	OL0.4	OL0.3	OL0.2	OL0.1	OL0.0
bit 7							bit 0

bit 7-0 **OL0.0:O0.7**: Reflects the logic level on the output latch.
1 = Logic '1'
0 = Logic '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 1-4: OLAT1 - OUTPUT LATCH REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL1.7	OL1.6	OL1.5	OL1.4	OL1.3	OL1.2	OL1.1	OL1.0
bit 7							bit 0

bit 7-0 **OL1.0:O1.7**: Reflects the logic level on the output latch.
1 = Logic '1'
0 = Logic '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.7.3 INPUT POLARITY REGISTERS

These registers allow the user to configure the polarity of the input port data (GP0 and GP1). If a bit in this register is set, the corresponding input port (GPn) data bit polarity will be inverted.

- IPOL0 (controls the polarity of GP0)
- IPOL1 (controls the polarity of GP1)

REGISTER 1-5: IPOL0 - INPUT POLARITY PORT REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IGP0.7	IGP0.6	IGP0.5	IGP0.4	IGP0.3	IGP0.2	IGP0.1	IGP0.0
bit 7							bit 0

bit 7-0 **IGP0.0:IGP0.7**: Controls the polarity inversion for the input pins
1 = Corresponding GP0 bit is inverted
0 = Corresponding GP0 bit is not inverted

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 1-6: IPOL1 - INPUT POLARITY PORT REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IGP1.7	IGP1.6	IGP1.6	IGP1.4	IGP1.3	IGP1.2	IGP1.1	IGP1.0
bit 7							bit 0

bit 7-0 **IGP1.0:IGP1.7**: Controls the polarity inversion for the input pins
1 = Corresponding GP1 bit is inverted
0 = Corresponding GP1 bit is not inverted

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.7.4 I/O DIRECTION REGISTERS

Two registers control the direction of data I/O:

- IODIR0 (controls GP0)
- IODIR1 (controls GP1)

When a bit in these registers is set, the corresponding pin becomes an input. Otherwise, it becomes an output. At Power-on Reset, the device ports are configured as inputs.

REGISTER 1-7: IODIR0 - I/O DIRECTION REGISTER 0

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IOD0.7	IOD0.6	IOD0.5	IOD0.4	IOD0.3	IOD0.2	IOD0.1	IOD0.0
bit 7							bit 0

bit 7-0 **IOD0.0:IO0.7:** Controls the direction of data I/O
1 = Input
0 = Output

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 1-8: IODIR1 - I/O DIRECTION REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IOD1.7	IOD1.6	IOD1.5	IOD1.4	IOD1.3	IOD1.2	IOD1.1	IOD1.0
bit 7							bit 0

bit 7-0 **IOD1.0:IO1.7:** Controls the direction of data I/O
1 = Input
0 = Output

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.7.5 INTERRUPT CAPTURE REGISTERS

Two registers contain the value of the port that generated the interrupt:

- INTCAP0 contains the value of GP0 at time of GP0 change interrupt
- INTCAP1 contains the value of GP1 at time of GP1 change interrupt

These registers are 'read-only' registers (A write to these registers is ignored).

REGISTER 1-9: INTCAP0 - INTERRUPT CAPTURED VALUE FOR PORT REGISTER 0

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP0.7	ICP0.6	ICP0.5	ICP0.4	ICP0.3	ICP0.2	ICP0.1	ICP0.0
bit 7							bit 0

bit 7-0 **ICP0.0:ICP0.7:** Reflects the logic level on the GP0 pins at the time of interrupt due to pin change
1 = Logic '1'
0 = Logic '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 1-10: INTCAP1 - INTERRUPT CAPTURED VALUE FOR PORT REGISTER 1

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP1.7	ICP1.6	ICP1.5	ICP1.4	ICP1.3	ICP1.2	ICP1.1	ICP1.0
bit 7							bit 0

bit 7-0 **ICP1.0:ICP1.7:** Reflects the logic level on the GP1 pins at the time of interrupt due to pin change
1 = Logic '1'
0 = Logic '0'

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1.7.6 I/O EXPANDER CONTROL REGISTER

- IOCON0 controls the functionality of the MCP23016.

The IARES (Interrupt Activity Resolution) bit controls the sampling frequency of the GP port pins. The higher the sampling frequency, the higher the device current requirements. If this bit is '0' (default), the maximum time to detect the activity on the port is 32 ms (max.), which results in lower standby current. If this bit is '1', the maximum time to detect activity on the port is 200 µsec. (max.) and results in higher standby current.

REGISTER 1-11: IOCON0 - I/0 EXPANDER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IARES
bit 7							bit 0

bit 1-7 **Unimplemented bit:** Read as '0'

bit 0 **IARES:** Interrupt Activity Resolution
1 = Fast sample rate
0 = Normal sample rate

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

IOCON1 is a shadow register for IOCON0. Access to IOCON1 results in access to IOCON0.

1.8 Serializer/Deserializer

The Serializer/Deserializer block converts and transfers data between the I^2C bus and GPIO.

1.9 Interrupt Logic

The MCP23016 asserts the open-drain interrupt output ($\overline{INT}$) low when one of the port pins changes state. Only those pins that are configured as an input can cause an interrupt. Pins defined as an output have no effect on $\overline{INT}$. The interrupt will remain active until a read from either the port (GPn) on which the interrupt occurred or the INTCAPn register is performed. If the input returns to its previous state before a read operation, it will reset the interrupt and the $\overline{INT}$ pin output will tri-state. Each 8-bit port is read separately, so reading GP0 or INTCAP0 will not clear the interrupt generated by GP1 or INTCAP1, and vice versa.

Input change activity on each port will generate an interrupt and the value of the particular port will be captured and copied into INTCAP0/INTCAP1. The INTCAPn registers are only updated when an interrupt occurs on $\overline{INT}$. These values will stay unchanged until the user clears the interrupt by reading the port or the INTCAPn register.

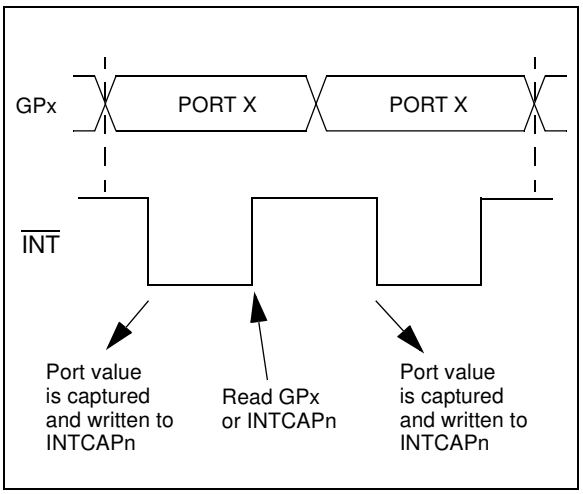
If the input port value changes back to normal before a user-read, the $\overline{INT}$ output will be reset. However, the INTCAP0/INTCAP1 will still contain the value of the port at the interrupt change. If the port value changes again, it will re-activate the interrupt and the new value will be captured.

The first interrupt on change event following an interrupt RESET will result in a capture event. Any further change event that occurs before the interrupt is reset will not result in a capture event.

1.9.1 INTERRUPT EVENT DETECTION

The IARES bit controls the resolution for detecting an interrupt-on-change event. If this bit is '0' (default), the maximum time for detecting a change of event is high, which results in lower standby current. If this bit is '1', it takes less time for scanning the activity on the port and results in higher standby current.

FIGURE 1-2: READING PORTX AFTER INTERRUPT EVENT



1.9.2 WRITING THE REGISTERS

To write to a MCP23016 register, the Master I^2C device needs to follow the requirements, as illustrated in Figure 1-3. First, the device is selected by sending the slave address and setting the R/$\overline{W}$ bit to logic '0'. The command byte is sent after the address and determines which register will be written. Table 1-3 shows the relationship of the command byte and register.

The MCP23016 has twelve 8-bit registers. They are configured to operate as six 16-bit register pairs, supporting the device's 16-bit port. These pairs are formed based on their functions (e.g., GP0 and GP1 are grouped together). The I^2C commands apply to one register pair to provide faster access. The first data byte following a command byte is written into the register pointed to by the command byte, while the second data is written into another register in the same pair. For example, if the first byte is sent to OLAT1 (command byte 03h), the next data byte will be written into the second register of that pair, OLAT0. If the first byte is written to OLAT0 (command byte 02h), the second byte will be written to OLAT1.

There is no limitation on the number of data bytes in one write transmission. Figure 1-4 shows the case of multiple byte writes in one write operation. In this case, the multiple writes are made to the same data pair.

Note:	The bus must remain free until after the ninth clock pulse for a minimum of 12 µs (see Table 2-5 and Figure 2-4).

FIGURE 1-3: WRITE TO CONFIGURATION REGISTERS (CASE 1)

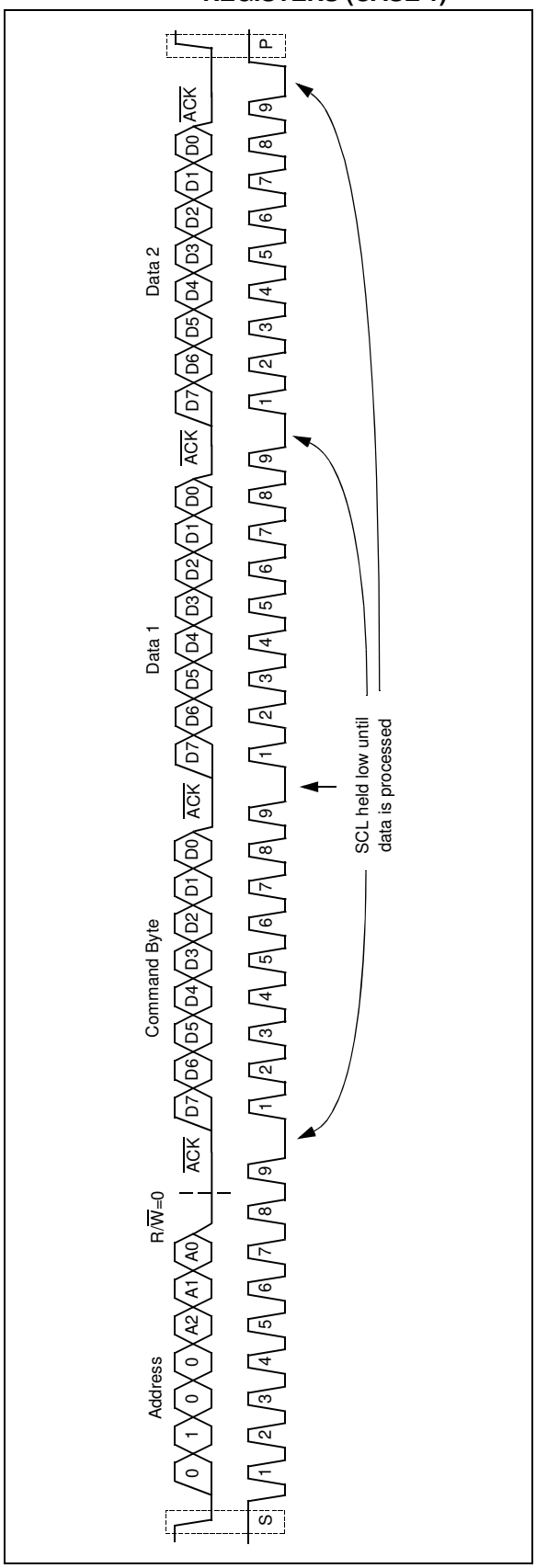


FIGURE 1-4: WRITE TO CONFIGURATION REGISTERS (CASE 2)

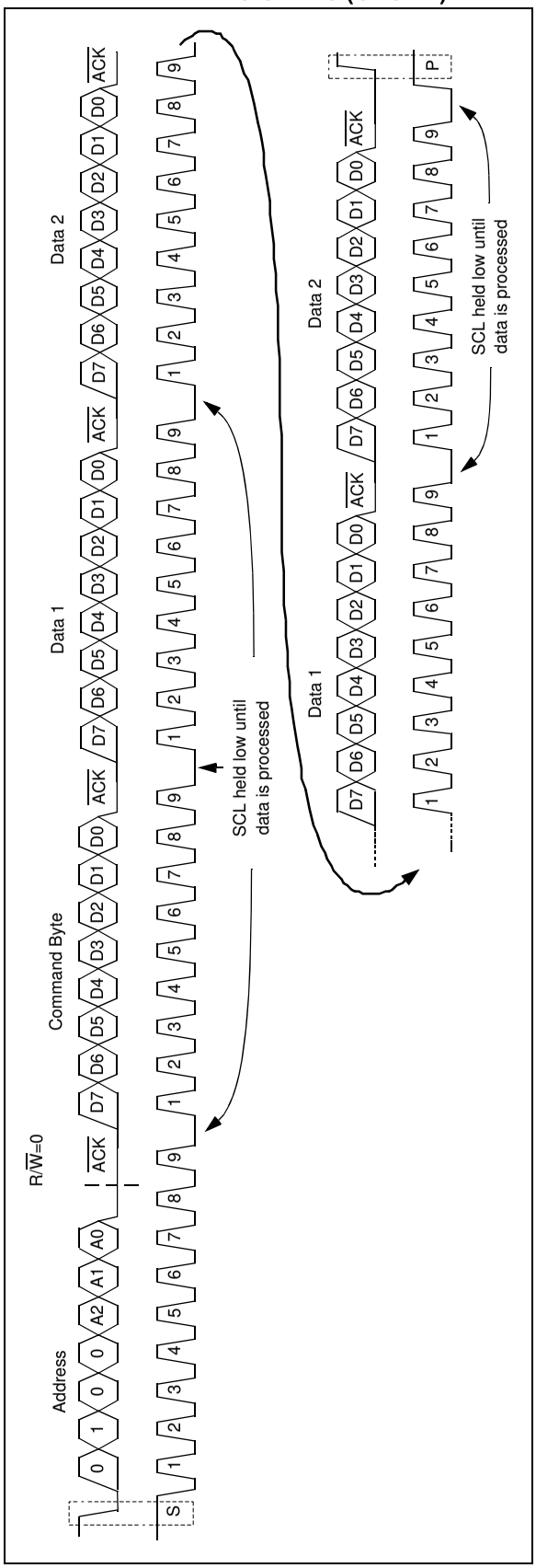
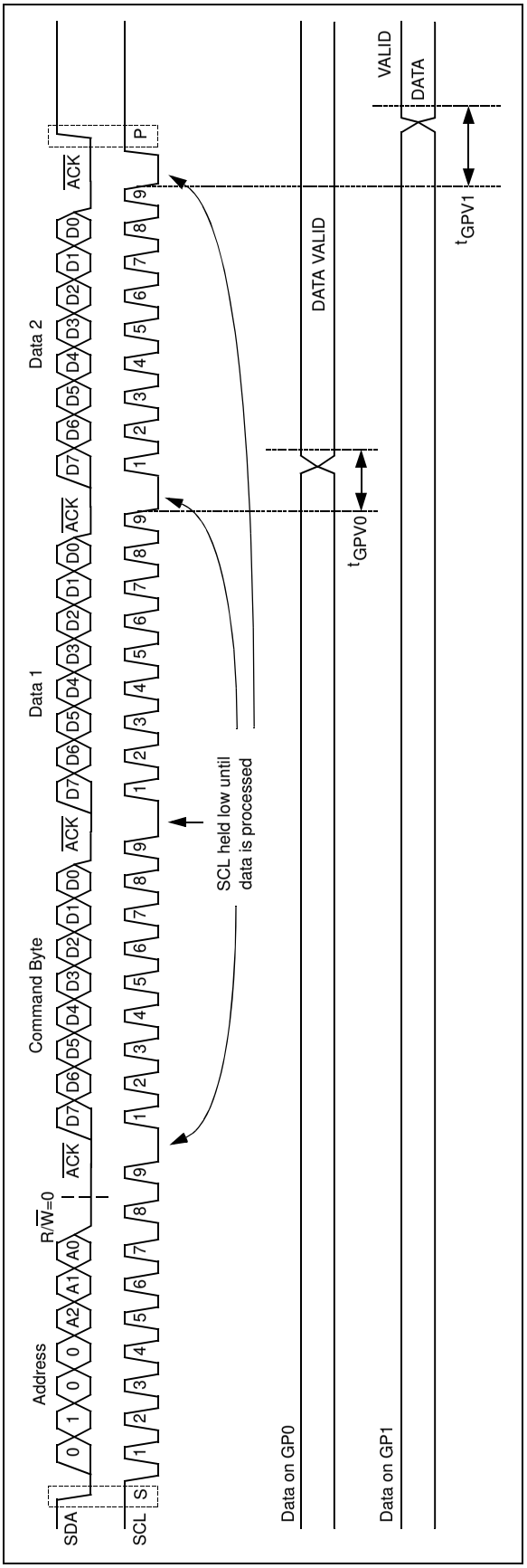


FIGURE 1-5: WRITE TO OUTPUT PORTS



1.9.3 READING THE REGISTERS

To read a MCP23016 register, the Master needs to follow the requirements shown in Figure 1-6. First, the device is selected by sending the slave address and setting the R/$\overline{W}$ bit to logic '0'. The command byte is sent after the address and determines which register will be read. A restart condition is generated and the device address is sent again with the R/$\overline{W}$ bit set to logic '1'. The data register defined by the command byte will be sent first, followed by the other register in the register pair. The logic for register selection is the same as explained in Write mode (**Section 1.9.2, "Writing the Registers"**).

The falling edge of the ninth clock initiates the register read action. The SCL clock will be held low while the data is read from the register and is transferred to the I^2C bus control block by the Serializer/Deserializer block.

The MCP23016 holds the clock low after the falling edge of the ninth clock pulse. The configuration registers (or port control registers) are read and the value is stored. Finally, the clock is released to enable the next transmission.

There is no limitation on the number of data bytes in one read transmission. Figure 1-8 shows the case of multiple byte read in one read operation. In this case, the multiple writes are made to the same data pair.

Note:	The bus must remain free until after the ninth clock pulse for a minimum of 12 µs (see Table 2-5 and Figure 2-4).

FIGURE 1-6: READ FROM CONFIGURATION REGISTER

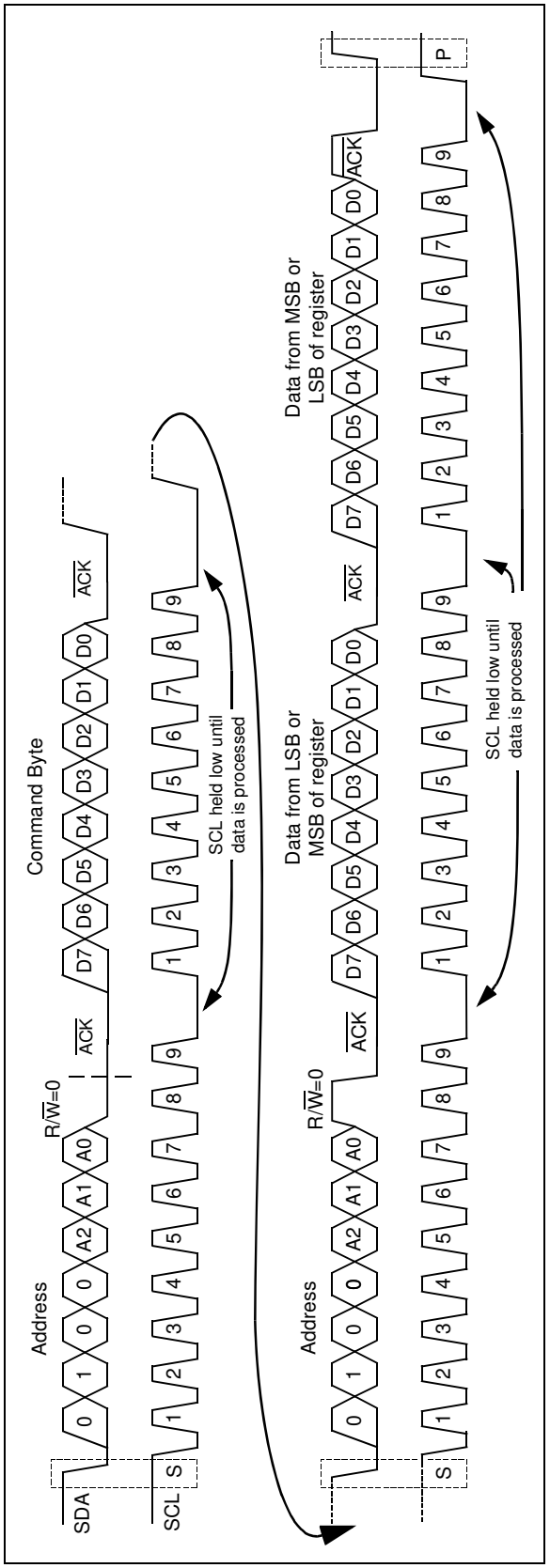


FIGURE 1-7: READ FROM INPUT PORTS (CASE 1)

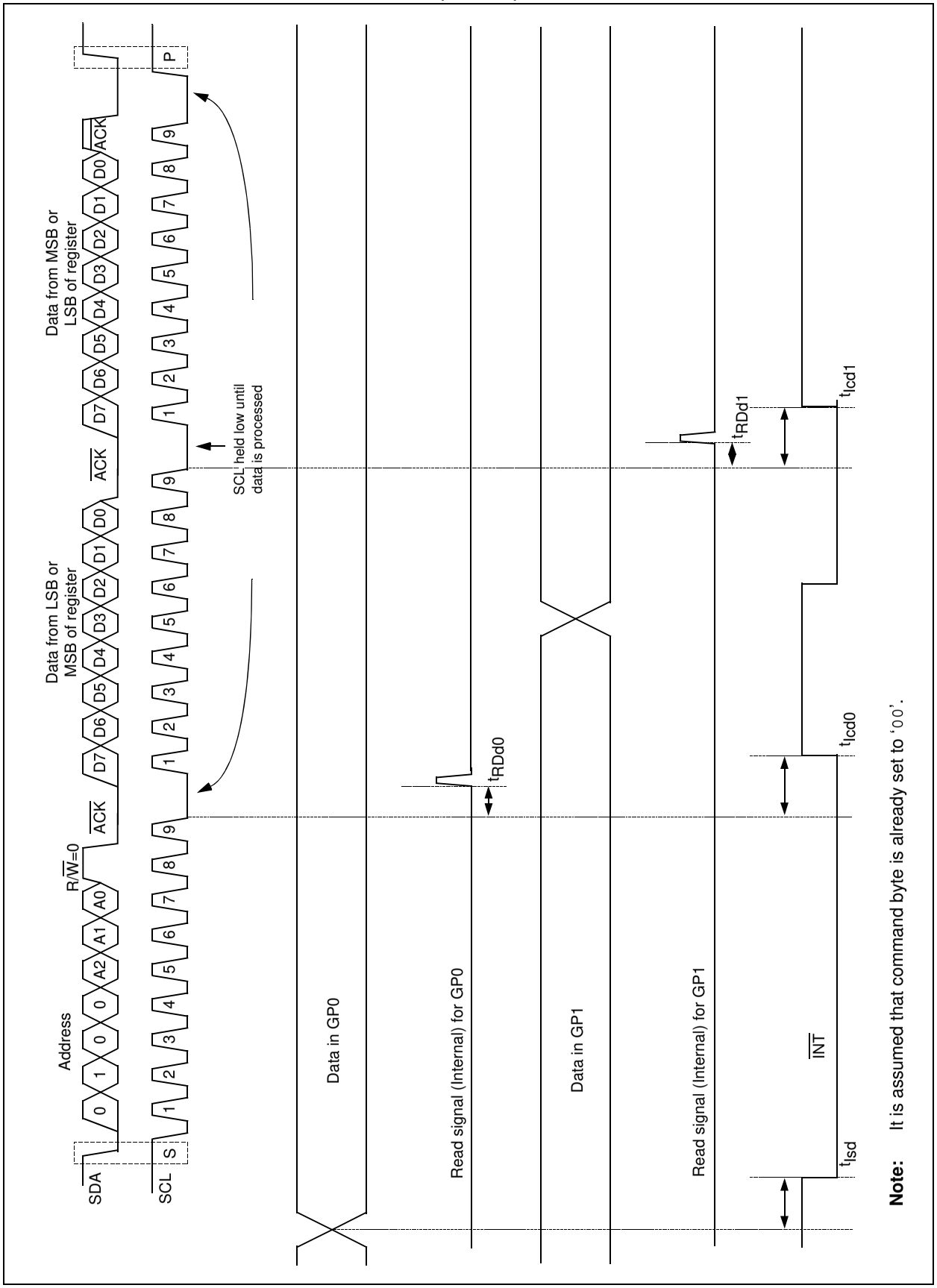
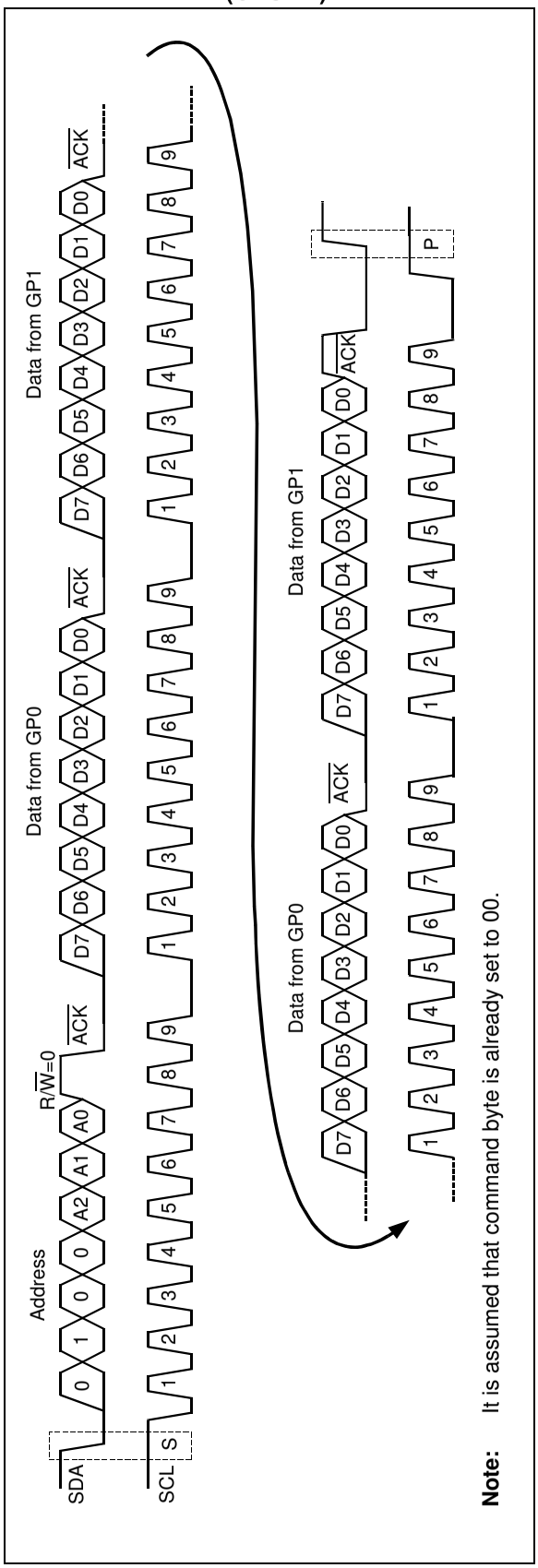


FIGURE 1-8: READ FROM INPUT PORTS (CASE 2)



Note: It is assumed that command byte is already set to 00.

NOTES:

2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -55 to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to V_{SS} ..... -0.3V to (V_{DD} + 0.3V)

Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.5V

Total power dissipation **(Note 1)** ..... 1.0 W

Maximum current out of V_{SS} pin ..... 300 mA

Maximum current into V_{DD} pin ..... 250 mA

Input clamp current, I_{IK} (V_I < 0, or V_I > V_{DD}) ..... ± 20 mA

Output clamp current, I_{OK} (V_O < 0, or V_O > V_{DD}) ..... ± 20 mA

Maximum output current sunk by any I/O pin ..... 25 mA

Maximum output current sourced by any I/O pin ..... 25 mA

Maximum current sunk by combined PORTS ..... 200 mA

Maximum current sourced by combined PORTS ..... 200 mA

Note 1: Power dissipation is calculated as follows:
$Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OI} \times I_{OL})$

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.1 DC Characteristics

TABLE 2-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature: -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D001	Supply Voltage	VDD	2.0	—	5.5	V	
D002	Standby Current	IDD	—	0.4		mA	IARES = 1
D003	Standby Current	IPD	—	25		µA	IARES = 0
	Input Low Voltage						
	I/O ports	VIL					
D004	TTL buffer		Vss	—	0.15 VDD	V	For entire VDD range
D004A			Vss	—	0.8V		4.5V ≤ VDD ≤ 5.5V
D005	Schmitt Trigger buffer		Vss	—	0.2 VDD	V	
	Input High Voltage						
	I/O ports	VIH		—			
D006	TTL buffer		2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D006A			0.25 VDD + 0.8V	—	VDD	V	For entire VDD range
D007	Schmitt Trigger buffer		0.8 VDD	—	VDD	V	For entire VDD range
	Input Leakage Current						
D008	I/O ports	IIL	—	—	±1.0	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
D009	CLK		—	—	±5.0	µA	Vss ≤ VPIN ≤ VDD
	Output Low Voltage						
D010	I/O Ports	VOL	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V
	Output High Voltage						
D010	I/O Ports	VOH	VDD-0.7	—	—	V	IOH = 3.0 mA, VDD = 4.5V
D011	VDD start voltage to ensure internal POR signal	VPOR	—	Vss	—	V	
D012	VDD rise rate to ensure internal POR signal	SVDD	0.05	-	—	V/ms	**Note 1**
	DC Trip Point	VTPOR	1.5	1.7	1.9	V	DC Slow Ramp
D012	VDD rise rate to ensure internal POR signal with PWRT enabled	SVDD	0.05	—	—	V/ms	**Note 1**
	DC Current Draw	IPOR	—	5.0	—	µA	At 5.0V (1 µ/Volt typical)

Note 1: These parameters are characterized but not tested.

2: Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

3: Standby current is measured with all I/O in hi-impedance state and tied to VDD and VSS.

4: For RC CLK, current through REXT is not included. The current through the resistor can be estimated by the formula
Ir = VDD/2 REXT (mA) with REXT in kohm.

5: Negative current is defined as coming out of the pin.

FIGURE 2-1: RESPONSE TIME

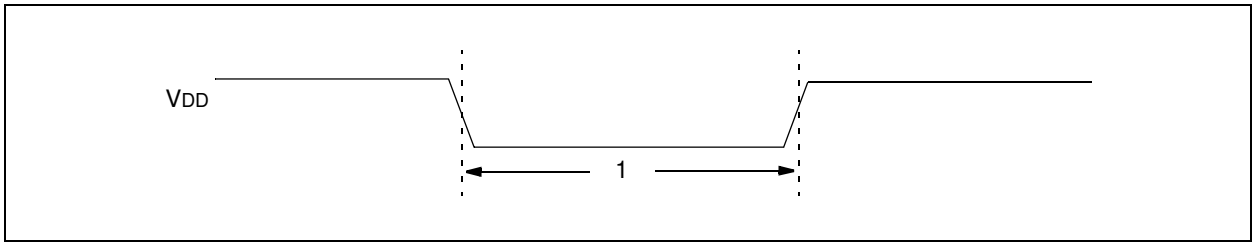


TABLE 2-2: RESPONSE TIME

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
1		Response Time	100	—	—	ns	Minimum time where a VDD transition from 5.0V to 0.0V to 5.0V will cause a RESET. All times less than 100 ns will be filtered.

FIGURE 2-2: TEST POINT CLOCK TIMING

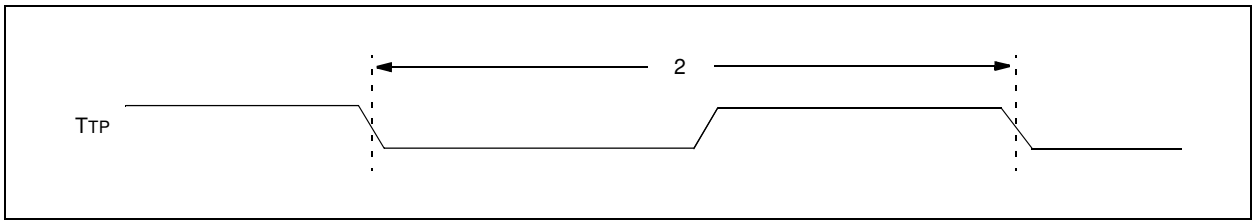


TABLE 2-3: TEST POINT CLOCK TIMING

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
	FTP	TP pin Frequency	—	1.0	—	MHz	Measured at TP pin, IARES = '1'.
2	TTP	TP pin CLK Period	—	1.0	—	µs	Measured at TP pin, IARES = '1'.

† Data in "Typ" column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 2-4: POWER-UP TIMER REQUIREMENTS

Parameter No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
3	TPWRT	Power-up Timer Period	—	72	—	ms	

† Data in "Typ" column is at 5V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 2-3: I²C BUS START/STOP BITS TIMING

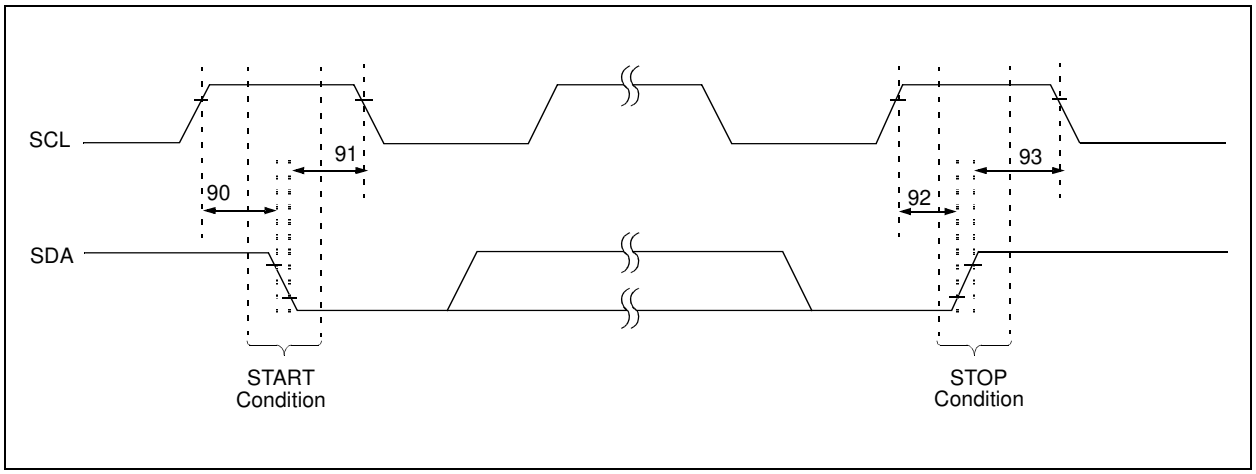


TABLE 2-5: I²C BUS START/STOP BITS REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode	4700	—	—	ns	Only relevant for Repeated START condition **(Note 1)**
			400 kHz mode	600	—	—		
91	THD:STA	START condition Hold time	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated **(Note 1)**
			400 kHz mode	600	—	—		
92	TSU:STO	STOP condition Setup time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	STOP condition Hold time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

Note 1: These parameters are characterized but not tested.

FIGURE 2-4: I²C BUS DATA TIMING

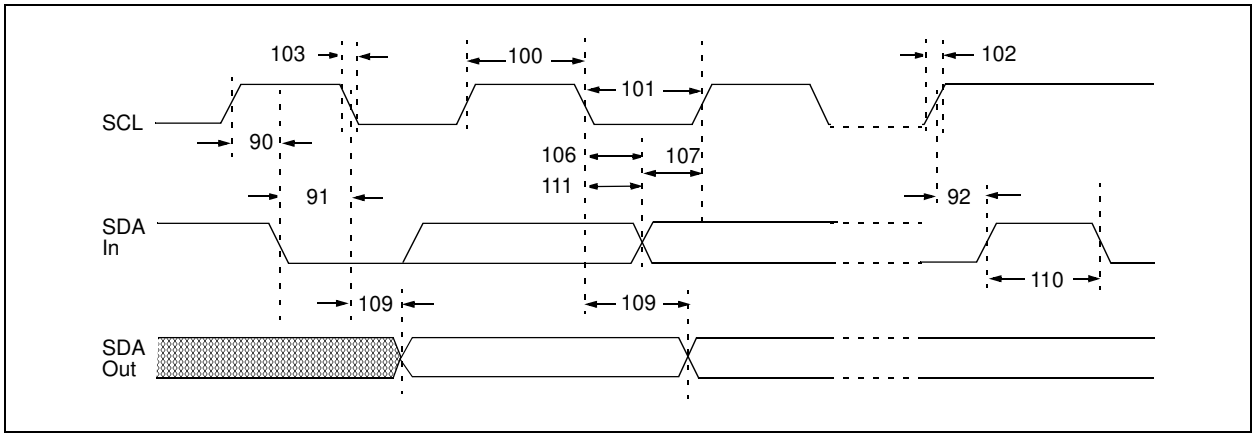


TABLE 2-5: I²C BUS DATA REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock High Time	100 kHz mode	4.0	—	µs	**(Note 1)**
			400 kHz mode	0.6	—	µs	
101	TLOW	Clock Low Time	100 kHz mode	4.7	—	µs	**(Note 1)**
			400 kHz mode	1.3	—	µs	
102	TR	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	**(Note 1)**
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10 - 400 pF
103	TF	SDA and SCL Fall Time	100 kHz mode	—	300	ns	**(Note 1)**
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10 - 400 pF
90	TSU:STA	START Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for repeated START condition **(Note 1)**
			400 kHz mode	0.6	—	µs	
91	THD:STA	START Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated **(Note 1)**
			400 kHz mode	0.6	—	µs	
106	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	**(Note 1)**
			400 kHz mode	0	0.9	µs	
107	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**(Note 1) (Note 3)**
			400 kHz mode	100	—	ns	
92	TSU:STO	STOP Condition Setup Time	100 kHz mode	4.7	—	µs	**(Note 1)**
			400 kHz mode	0.6	—	µs	
109	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	**(Note 1) (Note 2)**
			400 kHz mode	—	—	ns	
110	TBUF	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start **(Note 1)**
			400 kHz mode	1.3	—	µs	
	CB	Bus Capacitive Loading		—	400	pF	
111	TWAIT	Clock wait time after ninth pulse	100 kHz mode	12 µs	—	µs	Time the bus must remain free after the ninth clock pulse before a new transmission can start.
			400 kHz mode	12 µs	—	µs	

Note 1: These parameters are characterized but not tested.

2: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement TSU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line TR max.+TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

TABLE 2-7: GP0 AND GP1 TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ.	Max	Units	Conditions
	t_{GPV0}	GP0 output data valid time	—	40	—	µs	TP = 1 MHz
	t_{GPV1}	GP1 output data valid time	—	50	—	µs	
	t_{RDd0}	GP0 data read delay time	—	40	—	µs	
	t_{RDd1}	GP1 data read delay time	—	50	—	µs	
	t_{ISD0}	GP0 Interrupt set delay time	—	—	200	µs	IARES = 1, TP = 1 MHz
			—	—	32	ms	IARES = 0, TP = 1 MHz
	t_{ISD1}	GP1 Interrupt set delay time	—	—	200	µs	IARES = 1, TP = 1 MHz
			—	—	32	ms	IARES = 0, TP = 1 MHz
	t_{LCD0}	GP0 Interrupt clear delay time (for read)	—	100	—	µs	TP = 1 MHz
	t_{LCD1}	GP1 Interrupt clear delay time (for read)	—	100	—	µs	

Note 1: These parameters are characterized but not tested.