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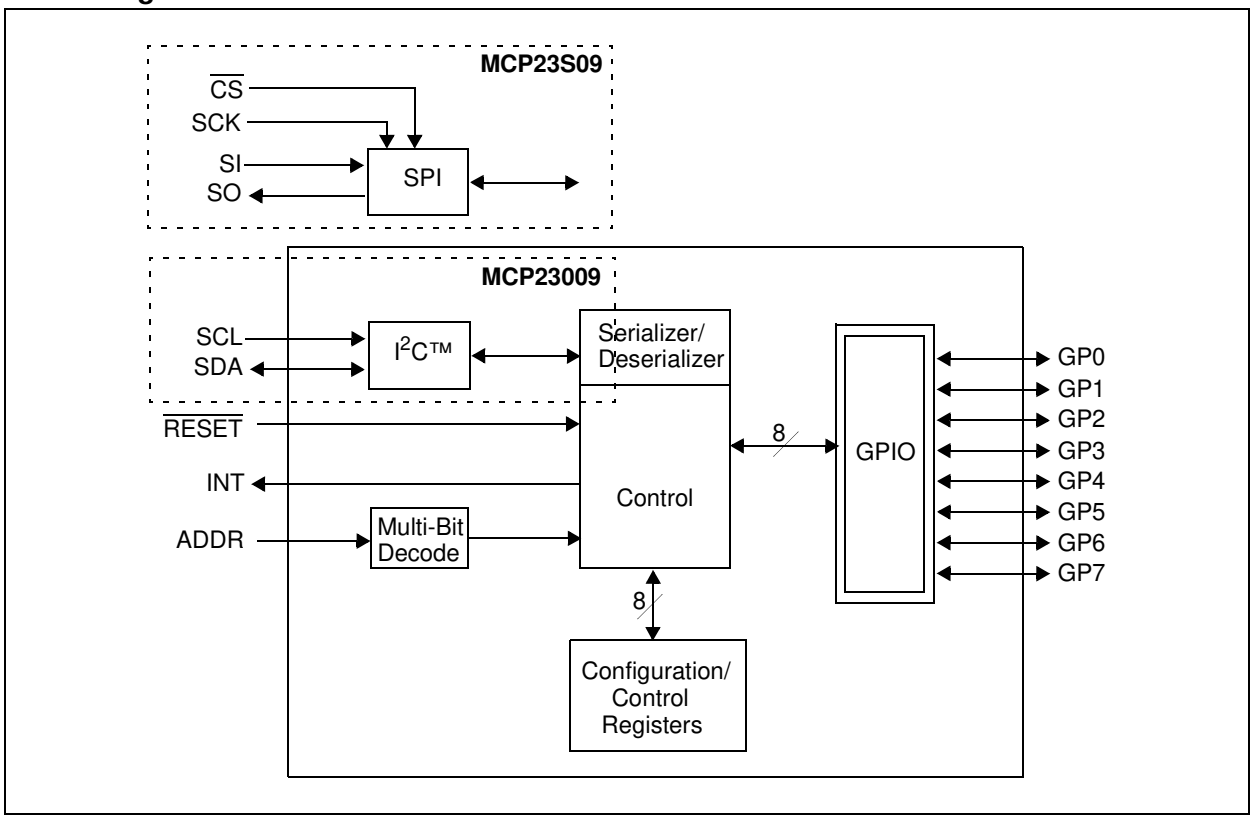
MCP23009/MCP23S09

8-Bit I/O Expander with Open-Drain Outputs

Features:

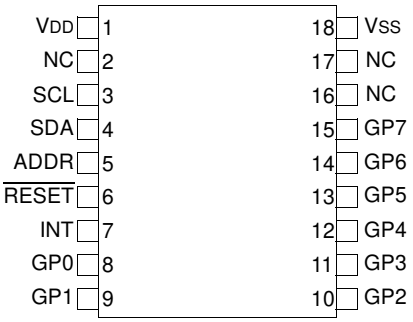
- 8-Bit Remote Bidirectional I/O Port:
  - I/O Pins Default to Input
- Open-Drain Outputs:
  - 5.5V Tolerant
  - 25 mA Sink Capable (per Pin)
  - 200 mA Total
- High-Speed I²C™ Interface (**MCP23009**):
  - 100 kHz
  - 400 kHz
  - 3.4 MHz
- High-Speed SPI Interface (**MCP23S09**):
  - 10 MHz
- Single Hardware Address Pin (**MCP23009**):
  - Voltage input to allow up to eight devices on the bus
- Configurable Interrupt Output Pins:
  - Configurable as active-high, active-low or open-drain
- Configurable Interrupt Source:
  - Interrupt-on-Change from configured defaults or pin change
- Polarity inversion register to configure the polarity of the input port data
- External Reset Input
- Low Standby Current:
  - 1 µA (-40°C ≤ TA ≤ +85°C)
  - 6 µA (+85°C ≤ TA ≤ +125°C)
- Operating Voltage:
  - 1.8V to 5.5V
- Available Packages:
  - 16-Lead QFN (3x3x0.9 mm)
  - 18-Lead PDIP (300 mil)
  - 18-Lead SOIC (7.50 mm)
  - 20-Lead SSOP (5.30 mm)

Block Diagram

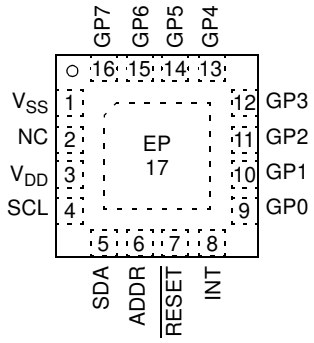


Package Types

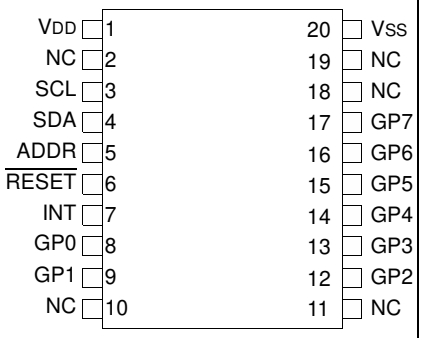
MCP23009
PDIP, SOIC



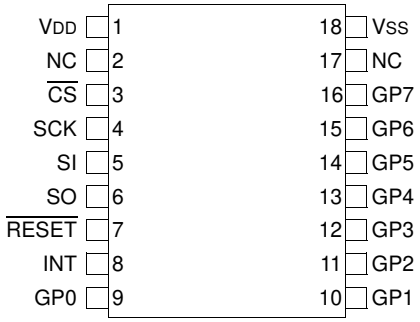
MCP23009
3 x 3 QFN*



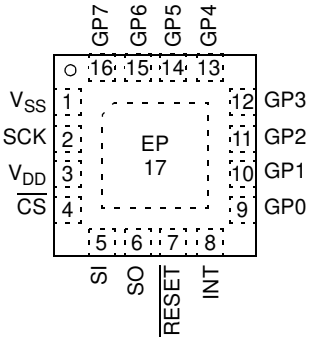
MCP23009
SSOP



MCP23S09
PDIP/SOIC



MCP23S09
3 x 3 QFN*



* Includes Exposed Thermal Pad (EP); see Tables 1-1 and 1-2.

1.0 DEVICE OVERVIEW

The MCP23X09 device provides 8-bit, general purpose parallel I/O expansion for I^2C bus or SPI applications. The two devices differ only in the serial interface.

- MCP23009 – I^2C interface
- MCP23S09 – SPI interface

The MCP23X09 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. All registers can be read by the system master.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding input port register state. This is used to indicate to the system master that an input state has changed.
2. When an input state differs from a pre-configured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the Interrupt, thereby saving the condition that caused the Interrupt.

The Power-On Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pin is used to determine the device address.

1.1 Pin Descriptions

TABLE 1-1: I²C™ PINOUT DESCRIPTION (MCP23009)

Pin Name	Pin Number			Pin Type	Standard Function
	16-lead QFN	18-lead PDIP/SOIC	20-lead SSOP		
VDD	3	1	1	P	Power
NC	2	2, 16-17	2, 10-11, 18-19	—	Not connected
SCL	4	3	3	I	Serial clock input
SDA	5	4	4	I/O	Serial data I/O
ADDR	6	5	5	I	Hardware address pin allows up to eight slave devices on the bus
$\overline{\text{RESET}}$	7	6	6	I	Hardware reset
INT	8	7	7	O	Interrupt output for port. Can be configured as active-high, active-low or open-drain.
GP0	9	8	8	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
GP1	10	9	9	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
GP2	11	10	12	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
GP3	12	11	13	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
GP4	13	12	14	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
GP5	14	13	15	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
GP6	15	14	16	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
GP7	16	15	17	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for interrupt on change and/or internal pull-up resistor.
VSS	1	18	20	P	Ground
EP	17	—	—	—	Exposed Thermal Pad (EP). Can be left floating or connected to VSS.

TABLE 1-2: SPI PINOUT DESCRIPTION (MCP23S09)

Pin Name	Pin Number		Pin Type	Standard Function
	16-lead QFN	18-lead PDIP/SOIC		
V_{DD}	3	1	P	Power (high-current capable)
NC	—	2, 17	—	Not connected
$\overline{CS}$	4	3	I	Chip select
SCK	2	4	I	Serial clock input
SI	5	5	I	Serial data input
SO	6	6	O	Serial data out
$\overline{RESET}$	7	7	I	Hardware reset (must be externally biased)
INT	8	8	O	Interrupt output for port. Can be configured as active-high, active-low or open-drain.
GP0	9	9	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
GP1	10	10	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
GP2	11	11	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
GP3	12	12	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
GP4	13	13	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
GP5	14	14	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
GP6	15	15	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
GP7	16	16	I/O	Bidirectional I/O pin (5.5V tolerant inputs; open-drain outputs). Can be enabled for Interrupt-on-Change and/or internal pull-up resistor.
V_{SS}	1	18	P	Ground (high-current capable)
EP	17	—	—	Exposed Thermal Pad (EP). Can be left floating or connected to V_{SS}.

1.2 Power-On Reset (POR)

The on-chip POR circuit holds the device in reset until VDD has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The maximum VDD rise time is specified in the electrical specification section.

When the device exits the POR condition (releases reset), the device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

1.3 Serial Interface

This block handles the functionality of the I2C (MCP23009) or SPI (MCP23S09) interface protocol. The MCP23X09 contains eleven (11) individual registers which can be addressed through the Serial Interface block (Table 1-3).

TABLE 1-3: REGISTER ADDRESSES

Address	Access to
00h	IODIR
01h	IPOL
02h	GPINTEN
03h	DEFVAL
04h	INTCON
05h	IOCON
06h	GPPU
07h	INTF
08h	INTCAP (read-only)
09h	GPIO
0Ah	OLAT

1.3.1 BYTE MODE AND SEQUENTIAL MODE

The MCP23X09 has the ability to operate in Byte mode or Sequential mode (IOCON.SEQOP). Byte mode and Sequential mode are not to be confused with I2C byte operations and sequential operations. The modes explained here relate to the device's internal address pointer and whether or not it is incremented after each byte is clocked on the serial interface.

- **Byte mode** disables automatic address pointer incrementing. When operating in Byte mode, the MCP23X09 does not increment its internal address counter after each byte during the data transfer. This gives the ability to continually access the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes or for continually writing to the output latches.
- **Sequential mode** enables automatic address pointer incrementing. When operating in Sequential mode, the MCP23X09 increments its address counter after each byte during the data transfer. The address pointer automatically rolls over to address 00h after accessing the last register.

These two modes are not to be confused with single writes/reads and continuous writes/reads, which are serial protocol sequences. For example, the device may be configured for Byte mode and the master may perform a continuous read. In this case, the MCP23X09 would not increment the address pointer and would repeatedly drive data from the same location.

1.3.2 I2C INTERFACE

1.3.2.1 I2C Write Operation

The I2C write operation includes the control byte and the register address sequence, as shown in the bottom of Figure 1-1. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23009. The operation is ended with a Stop (P) or Restart (SR) condition being generated by the master.

Data is written to the MCP23009 after every byte transfer. If a Stop or Restart condition is generated during a data transfer, the data will not be written to the MCP23009.

Both Byte mode and Sequential mode are supported by the MCP23009. If Sequential mode is enabled (default), the MCP23009 increments its address counter after each ACK during the data transfer.

1.3.2.2 I2C Read Operation

I2C read operations include the control byte sequence, as shown in the bottom of Figure 1-1. This sequence is followed by another control byte (including the Start condition and ACK) with the R/W bit equal to a logic one (R/W = 1). The MCP23009 then transmits the data contained in the addressed register. The sequence is ended with the master generating a Stop or Restart condition.

1.3.2.3 I2C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a Stop or Restart condition after the data transfer, the master clocks the next byte pointed to by the address pointer (see **Section 1.3.1 "Byte Mode and Sequential Mode"** for details regarding sequential operation control).

The sequence ends with the master sending a Stop or Restart condition.

The MCP23009 address pointer will roll over to address zero after reaching the last register address.

Refer to Figure 1-1.

1.3.3 SPI INTERFACE

The MCP23S09 operates in Mode 0,0 and Mode 1,1. The difference between the two modes is the idle state of the clock.

- Mode 0,0: The idle state of the clock is low. Input data is latched on the rising edge of the clock; output data is driven on the falling edge of the clock.
- Mode 1,1: The idle state of the clock is high. Input data is latched on the rising edge of the clock; output data is driven on the falling edge of the clock.

1.3.3.1 SPI Write Operation

The SPI write operation is started by lowering $\overline{CS}$. The write command (slave address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

1.3.3.2 SPI Read Operation

The SPI read operation is started by lowering $\overline{CS}$. The SPI read command (slave address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

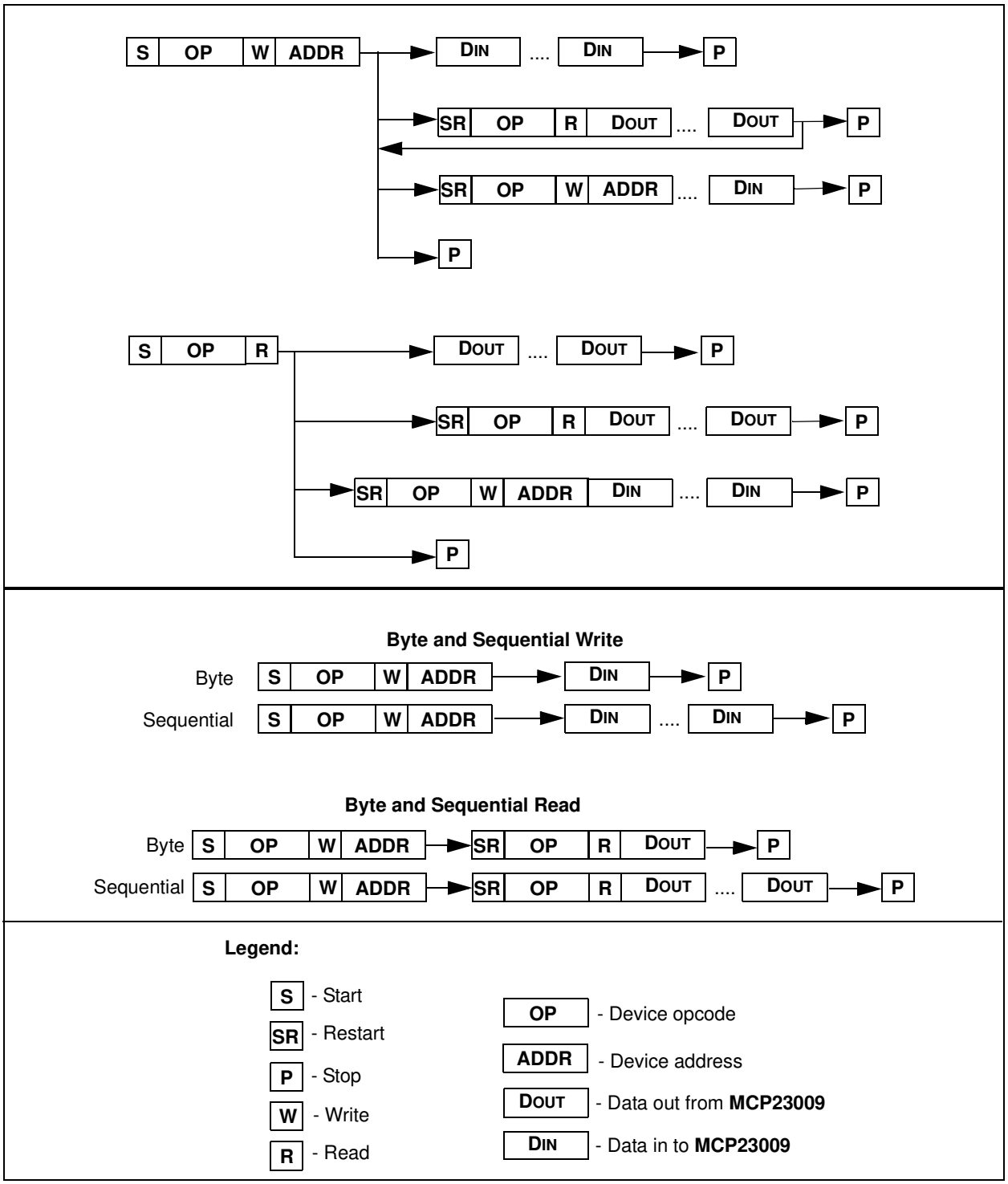
1.3.3.3 SPI Sequential Write/Read

For sequential operations, instead of deselecting the device by raising $\overline{CS}$, the master clocks the next byte pointed to by the address pointer (see **Section 1.3.1 "Byte Mode and Sequential Mode"** for details regarding sequential operation control).

The sequence ends by the raising of $\overline{CS}$.

The MCP23S09 address pointer will roll over to address zero after reaching the last register address.

FIGURE 1-1: MCP23009 I²C™ DEVICE PROTOCOL



1.4 Multi-Bit Address Decoder

The ADDR pin is used to set the slave address of the MCP23009 (I^2C only) to allow up to eight devices on the bus using only a single pin. Typically, this would require three pins.

The multi-bit Address Decoder employs a basic FLASH ADC architecture (Figure 1-4). The seven comparators generate eight unique values based on the analog input. This value is converted to a 3-bit code which corresponds to the address bits (A2, A1, A0) in the serial OPCODE.

Sequence of operation (see Figure 1-5 for timings):

1. Upon power-up (after VDD stabilizes), the module becomes active after time tADEN. Note that the analog value on the ADDR pin must be stable before this point to ensure accurate address assignment.
2. The 3-bit address is latched after tADDRLAT.
3. The module powers down after the first rising edge of the serial clock is detected (tADDIS).

Once the address bits are latched, the device will keep the slave address until a POR or Reset condition occurs.

1.4.1 CALCULATING VOLTAGE ON ADDR

When calculating the required voltage on the ADDR pin (V2), the set point should be the mid point of the LSb of the ADC.

The examples in Figures 1-2 and 1-3 show how to determine the mid-point voltage (V2) and the range of voltages based on a voltage divider circuit. The maximum tolerance is 20%, however, it is recommended to use 5% tolerance worst-case (10% total tolerance).

FIGURE 1-2: VOLTAGE DIVIDER EXAMPLE

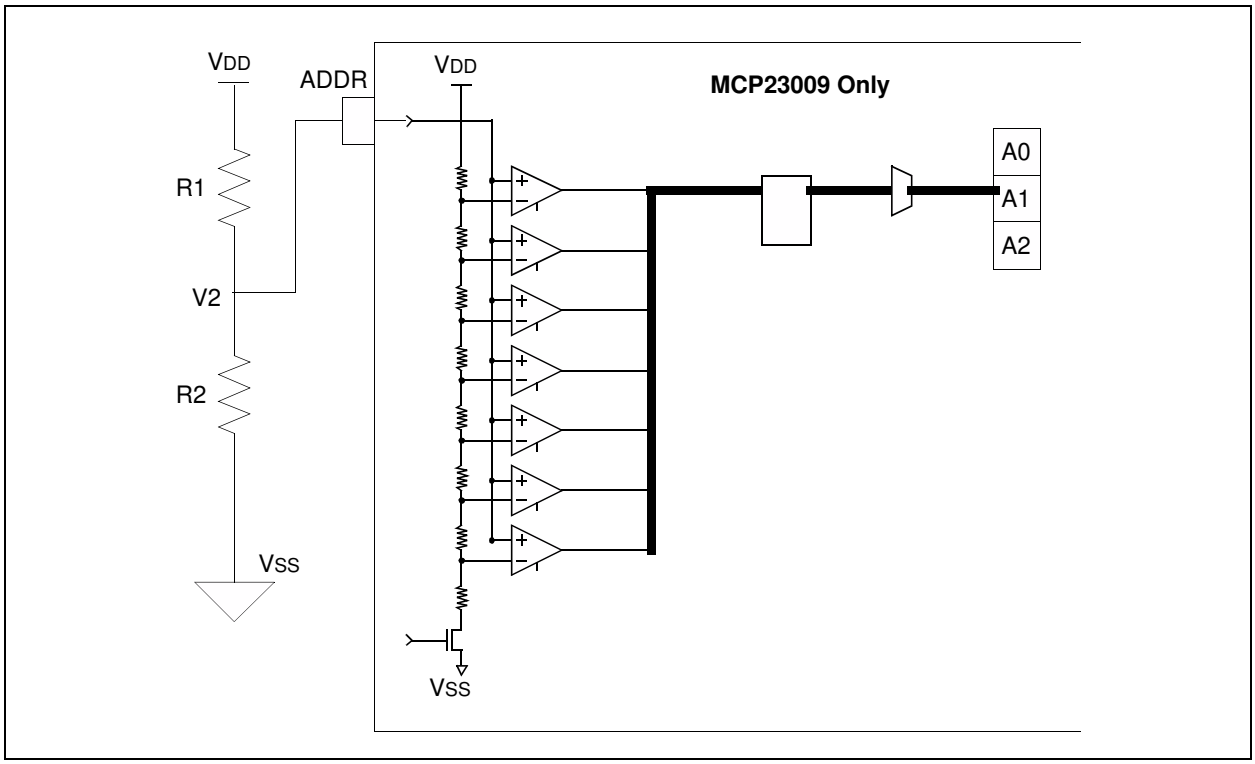


FIGURE 1-3: VOLTAGE AND CODE EXAMPLE

Assume:
n = A2, A1, A0 in opcode
ratio = R2/(R1+R2)
V2 = voltage on ADDR pin
V2(min) = V2 – (V_{DD}/8) x %tolerance
V2(max) = V2 + (V_{DD}/8) x %tolerance

			V_{DD} = 1.8		10% Tolerance (total)	
n	**R2 = 2n + 1**	**R1 = 16 – R2**	**R2/(R1 + R2)**	**V2**	**V2(min)**	**V2(max)**
0	1	15	0.0625	**0.113**	0.00	0.14
1	3	13	0.1875	**0.338**	0.32	0.36
2	5	11	0.3125	**0.563**	0.54	0.59
3	7	9	0.4375	**0.788**	0.77	0.81
4	9	7	0.5625	**1.013**	0.99	1.04
5	11	5	0.6875	**1.238**	1.22	1.26
6	13	3	0.8125	**1.463**	1.44	1.49
7	15	1	0.9375	**1.688**	1.67	1.80

			V_{DD} = 2.7		10% Tolerance (total)	
n	**R2 = 2n + 1**	**R1 = 16 – R2**	**R2/(R1 + R2)**	**V2**	**V2(min)**	**V2(max)**
0	1	15	0.0625	**0.169**	0.00	0.19
1	3	13	0.1875	**0.506**	0.48	0.53
2	5	11	0.3125	**0.844**	0.82	0.87
3	7	9	0.4375	**1.181**	1.16	1.20
4	9	7	0.5625	**1.519**	1.50	1.54
5	11	5	0.6875	**1.856**	1.83	1.88
6	13	3	0.8125	**2.194**	2.17	2.22
7	15	1	0.9375	**2.531**	2.51	2.70

			V_{DD} = 3.3		10% Tolerance (total)	
n	**R2 = 2n + 1**	**R1 = 16 – R2**	**R2/(R1 + R2)**	**V2**	**V2(min)**	**V2(max)**
0	1	15	0.0625	**0.206**	0.00	0.23
1	3	13	0.1875	**0.619**	0.60	0.64
2	5	11	0.3125	**1.031**	1.01	1.05
3	7	9	0.4375	**1.444**	1.42	1.47
4	9	7	0.5625	**1.856**	1.83	1.88
5	11	5	0.6875	**2.269**	2.25	2.29
6	13	3	0.8125	**2.681**	2.66	2.70
7	15	1	0.9375	**3.094**	3.07	3.30

			V_{DD} = 5.5		10% Tolerance (total)	
n	**R2 = 2n + 1**	**R1 = 16 – R2**	**R2/(R1 + R2)**	**V2**	**V2(min)**	**V2(max)**
0	1	15	0.0625	**0.344**	0.00	0.37
1	3	13	0.1875	**1.031**	1.01	1.05
2	5	11	0.3125	**1.719**	1.70	1.74
3	7	9	0.4375	**2.406**	2.38	2.43
4	9	7	0.5625	**3.094**	3.07	3.12
5	11	5	0.6875	**3.781**	3.76	3.80
6	13	3	0.8125	**4.469**	4.45	4.49
7	15	1	0.9375	**5.156**	5.13	5.50

FIGURE 1-4: FLASH ADC BLOCK DIAGRAM

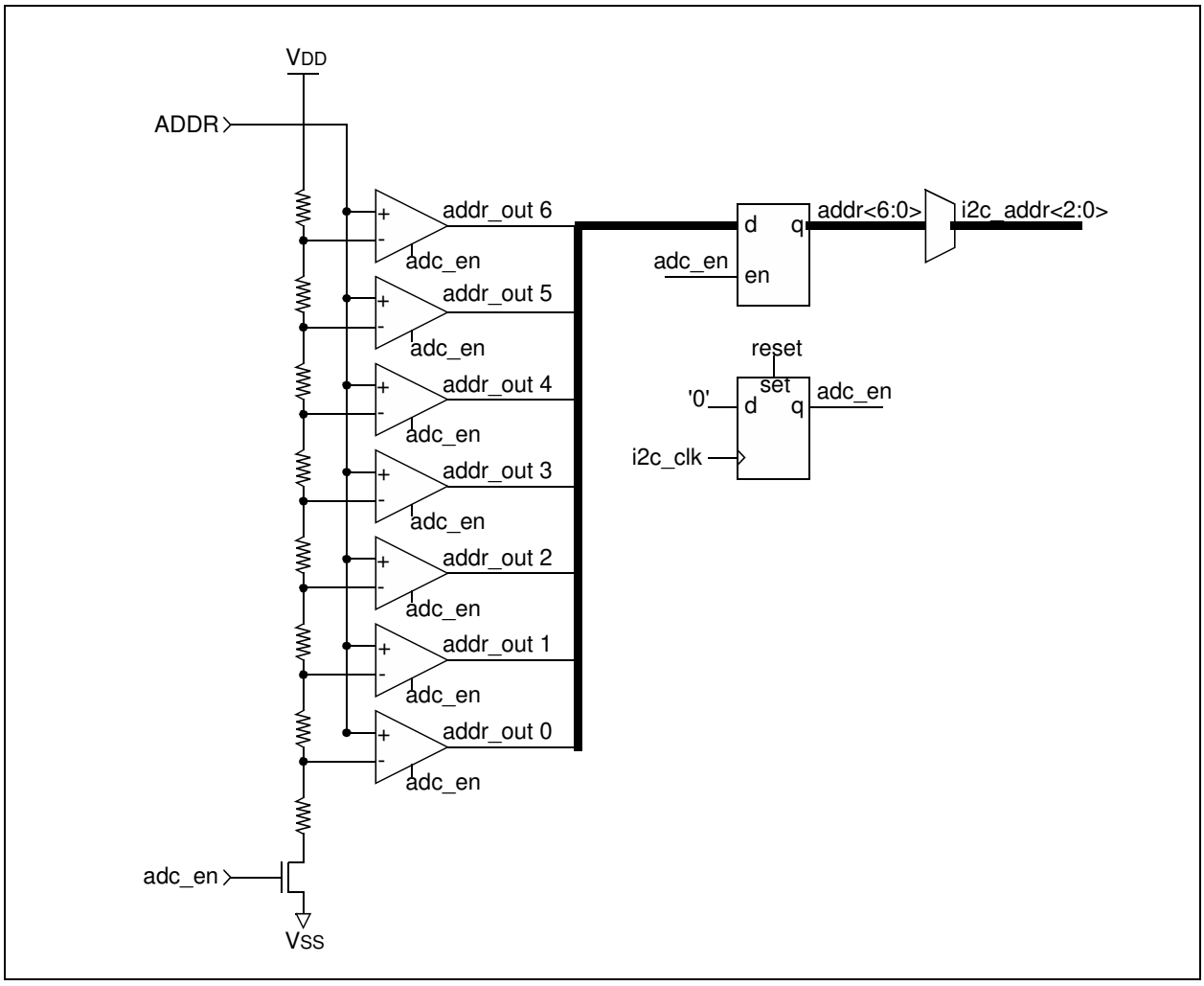
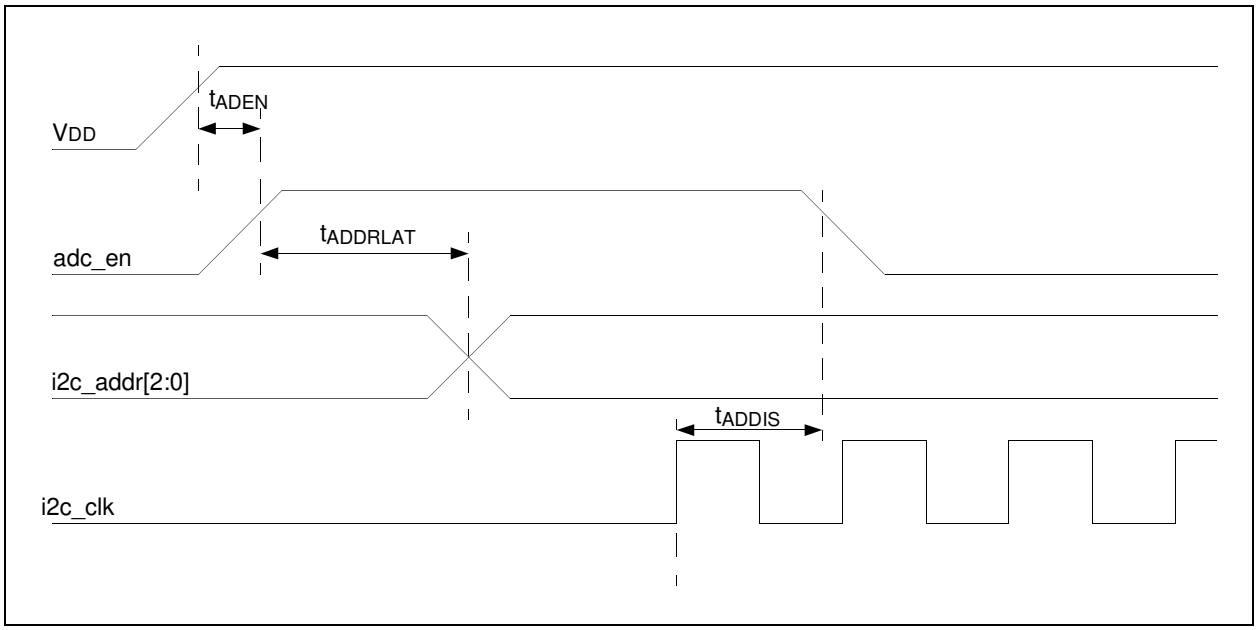


FIGURE 1-5: HARDWARE ADDRESS DECODE TIMING



1.4.2 ADDRESSING I²C DEVICES (MCP23009)

The MCP23009 is a slave I²C device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address contains four fixed bits and three user-defined hardware address bits (configured via the ADDR pin). Figure 1-6 shows the control byte format.

1.4.3 ADDRESSING SPI DEVICES (MCP23S09)

The MCP23S09 is a slave SPI device. The slave address contains seven fixed bits (no address bits), with the read/write bit filling out the control byte. Figure 1-7 shows the control byte format.

FIGURE 1-6: I²C™ CONTROL BYTE FORMAT

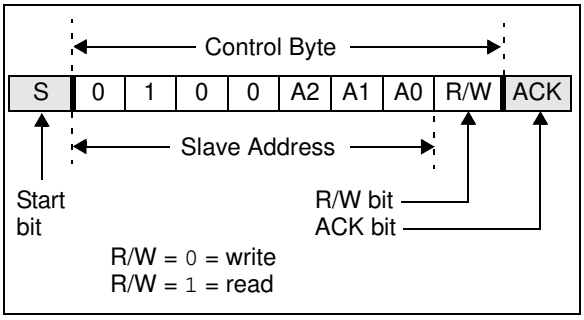


FIGURE 1-7: SPI CONTROL BYTE FORMAT

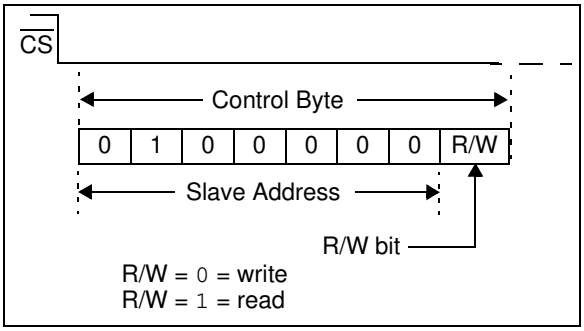


FIGURE 1-8: I²C™ ADDRESSING REGISTERS

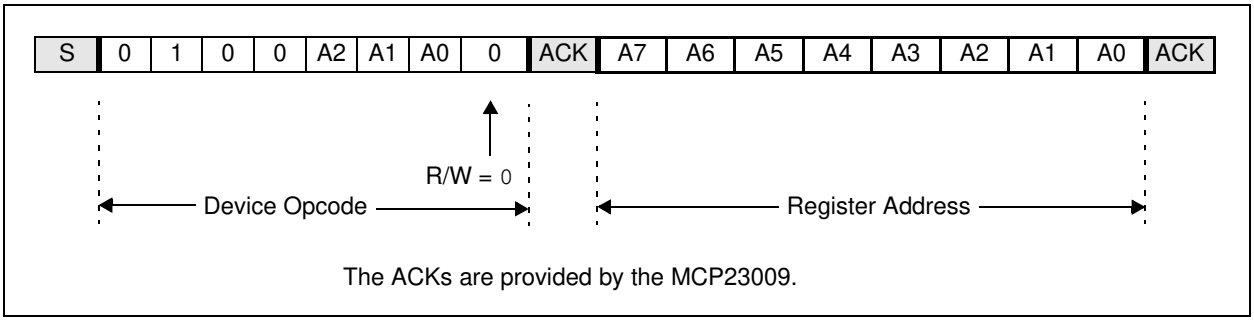
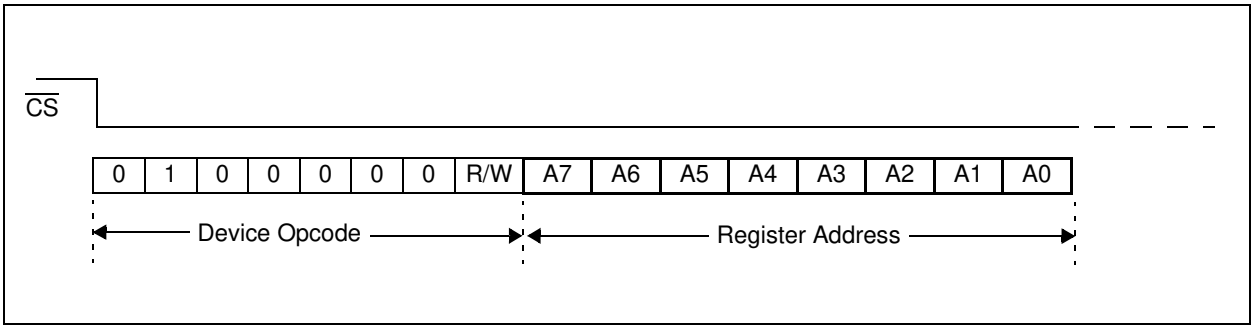


FIGURE 1-9: SPI ADDRESSING REGISTERS



1.5 GPIO Port

The GPIO module is a general purpose 8-bit wide bidirectional port.

The outputs are open-drain.

The GPIO module contains the data ports (GPIOn), internal pull-up resistors and the output latches (OLATn).

The pull-up resistors are individually configured and can be enabled when the pin is configured as an input or output.

Reading the GPIOn register reads the value on the port. Reading the OLATn register only reads the latches, not the actual value on the port.

Writing to the GPIOn register actually causes a write to the latches (OLATn). Writing to the OLATn register forces the associated output drivers to drive to the level in OLATn. Pins configured as inputs turn off the associated output driver and put it in high impedance.

1.6 Configuration and Control Registers

There are eleven (11) registers associated with the MCP23X09, as shown in Table 1-4.

TABLE 1-4: CONFIGURATION AND CONTROL REGISTERS

Register Name	Address (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR/RST Value
IODIR	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOL	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTEN	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVAL	03	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCON	04	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	05	—	—	SEQOP	—	—	ODR	INTPOL	INTCC	0000 0000
GPPU	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTF	07	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAP	08	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIO	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLAT	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

1.6.1 I/O DIRECTION REGISTER

This register controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

REGISTER 1-1: IODIR – I/O DIRECTION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **IO<7:0>:** Controls the direction of data I/O <7:0>

1 = Pin is configured as an input

0 = Pin is configured as an output

1.6.2 INPUT POLARITY REGISTER

This register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

REGISTER 1-2: IPOL – INPUT POLARITY PORT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **IP<7:0>:** Controls the polarity inversion of the input pins <7:0>

1 = GPIO register bit will reflect the opposite logic state of the input pin

0 = GPIO register bit will reflect the same logic state of the input pin

1.6.3 INTERRUPT-ON-CHANGE CONTROL REGISTER

The GPINTEN register controls the Interrupt-on-Change feature for each pin.

If a bit is set, the corresponding pin is enabled for Interrupt-on-Change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for Interrupt-on-Change.

REGISTER 1-3: GPINTEN – INTERRUPT-ON-CHANGE PINS

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **GPINT<7:0>:** General-purpose I/O interrupt-on-change pins <7:0>

1 = Enable GPIO input pin for Interrupt-on-Change event
0 = Disable GPIO input pin for Interrupt-on-Change event

Refer to the INTCON and DEFVAL registers.

1.6.4 DEFAULT COMPARE REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an Interrupt to occur.

REGISTER 1-4: DEFVAL – DEFAULT VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DEF<7:0>:** Sets the compare value for pins configured for Interrupt-on-Change from defaults <7:0>.
Refer to the INTCON register.
If the associated pin level is the opposite from the register bit, an Interrupt occurs.

Refer to the INTCON and GPINTEN registers.

1.6.5 INTERRUPT CONTROL REGISTER

The INTCON register controls how the associated pin value is compared for the Interrupt-on-Change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

REGISTER 1-5: INTCON – INTERRUPT-ON-CHANGE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IOC<7:0>:** Controls how the associated pin value is compared for Interrupt-on-Change <7:0>.

1 = Pin value is compared against the associated bit in the DEFVAL register
0 = Pin value is compared against the previous pin value

Refer to the DEFVAL and GPINTEN registers.

1.6.6 CONFIGURATION REGISTER

The Sequential Operation (SEQOP) bit controls the incrementing function of the address pointer. If the address pointer is disabled, the address pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.

The Open-Drain (ODR) control bit enables/disables the INT pin for open-drain configuration.

The Interrupt Polarity (INTPOL) bit sets the polarity of the INT pin. This bit is functional only when the ODR bit is cleared, configuring the INT pin as active push-pull.

The Interrupt Clearing Control (INTCC) bit configures how Interrupts are cleared. When set (INTCC = 1), the Interrupt is cleared when the INTCAP register is read. When cleared (INTCC = 0), the Interrupt is cleared when the GPIO register is read.

The Interrupt can only be cleared when the Interrupt condition is inactive. Refer to **Section 1.7.4 "Clearing Interrupts"** for details.

REGISTER 1-6: IOCON – I/O EXPANDER CONFIGURATION REGISTER

U-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	SEQOP	—	—	ODR	INTPOL	INTCC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**: Read as '0'

bit 6 **Unimplemented**: Read as '0'

bit 5 **SEQOP:** Sequential Operation mode bit.
1 = Sequential operation disabled, address pointer does not increment
0 = Sequential operation enabled, address pointer increments

bit 4 **Unimplemented**: Read as '0'

bit 3 **Unimplemented:** Read as '0'

bit 2 **ODR:** Configures the INT pin as an open-drain output.
1 = Open-drain output (overrides the INTPOL bit)
0 = Active driver output (INTPOL bit sets the polarity)

bit 1 **INTPOL:** Sets the polarity of the INT output pin.
1 = Active-High
0 = Active-Low

bit 0 **INTCC:** Interrupt Clearing Control
1 = Reading INTCAP register clears the Interrupt
0 = Reading GPIO register clears the Interrupt

1.6.7 PULL-UP RESISTOR CONFIGURATION REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set, the corresponding port pin is internally pulled up with an internal resistor.

REGISTER 1-7: GPPU – GPIO PULL-UP RESISTOR REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
bit 7							bit 0

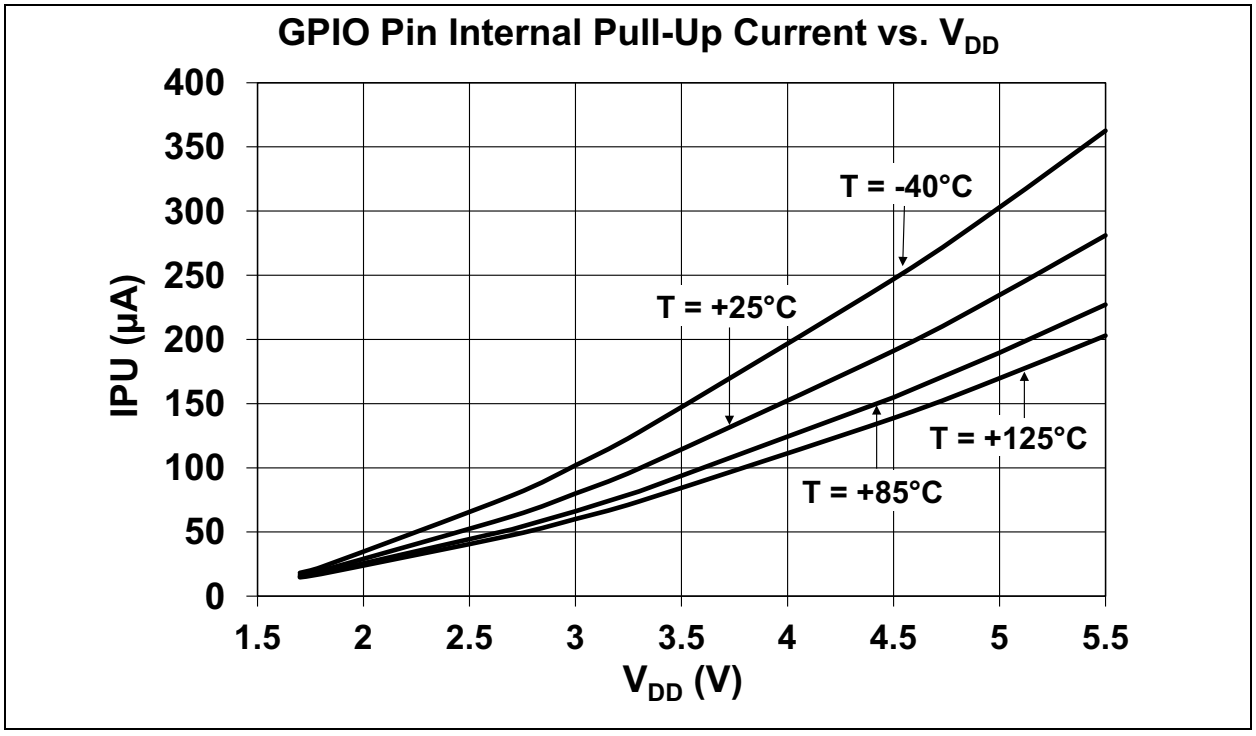
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PU<7:0>:** Controls the internal pull-up resistors on each pin (when configured as an input or output) <7:0>.

1 = Pull-Up enabled

0 = Pull-Up disabled

FIGURE 1-10: TYPICAL PERFORMANCE CURVE FOR THE INTERNAL PULL-UP RESISTORS



1.6.8 INTERRUPT FLAG REGISTER

The INTF register reflects the Interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A set bit indicates that the associated pin caused the Interrupt.

This register is read-only. Writes to this register will be ignored.

REGISTER 1-8: INTF – INTERRUPT FLAG REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **INT<7:0>:** Reflects the interrupt condition on the port. Will reflect the change only if interrupts are enabled (GPINTEN) <7:0>.

1 = Pin caused Interrupt
0 = Interrupt not pending

1.6.9 INTERRUPT CAPTURE REGISTER

The INTCAP register captures the GPIO port value at the time the Interrupt occurred. The register is read-only' and is updated only when an Interrupt occurs. The register will remain unchanged until the Interrupt is cleared via a read of INTCAP or GPIO.

REGISTER 1-9: INTCAP – INTERRUPT CAPTURED VALUE FOR PORT REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ICP<7:0>:** Reflects the logic level on the port pins at the time of Interrupt due to pin change <7:0>.

1 = Logic-High
0 = Logic-Low

1.6.10 PORT REGISTER

The GPIO register reflects the value on the port. Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

REGISTER 1-10: GPIO – GENERAL PURPOSE I/O PORT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **GP<7:0>:** Reflects the logic level on the pins <7:0>.

1 = Logic-High
0 = Logic-Low