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MCP23017/MCP23S17

16-Bit I/O Expander with Serial Interface

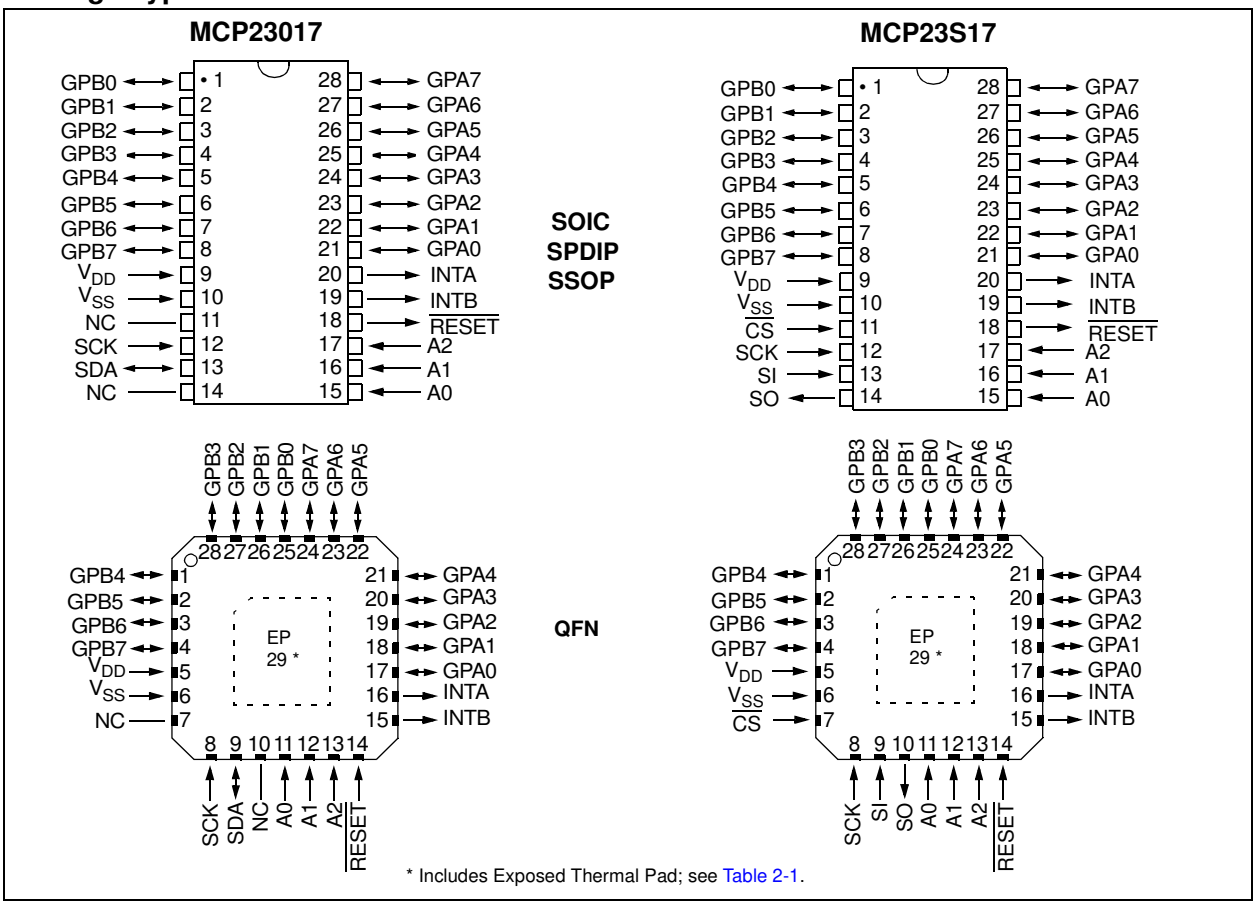
Features

- 16-Bit Remote Bidirectional I/O Port:
  - I/O pins default to input
- High-Speed I^2C Interface (**MCP23017**):
  - 100 kHz
  - 400 kHz
  - 1.7 MHz
- High-Speed SPI Interface (**MCP23S17**):
  - 10 MHz (maximum)
- Three Hardware Address Pins to Allow Up to Eight Devices On the Bus
- Configurable Interrupt Output Pins:
  - Configurable as active-high, active-low or open-drain
- INTA and INTB Can Be Configured to Operate Independently or Together
- Configurable Interrupt Source:
  - Interrupt-on-change from configured register defaults or pin changes
- Polarity Inversion Register to Configure the Polarity of the Input Port Data
- External Reset Input
- Low Standby Current: 1 µA (max.)
- Operating Voltage:
  - 1.8V to 5.5V @ -40°C to +85°C
  - 2.7V to 5.5V @ -40°C to +85°C
  - 4.5V to 5.5V @ -40°C to +125°C

Packages

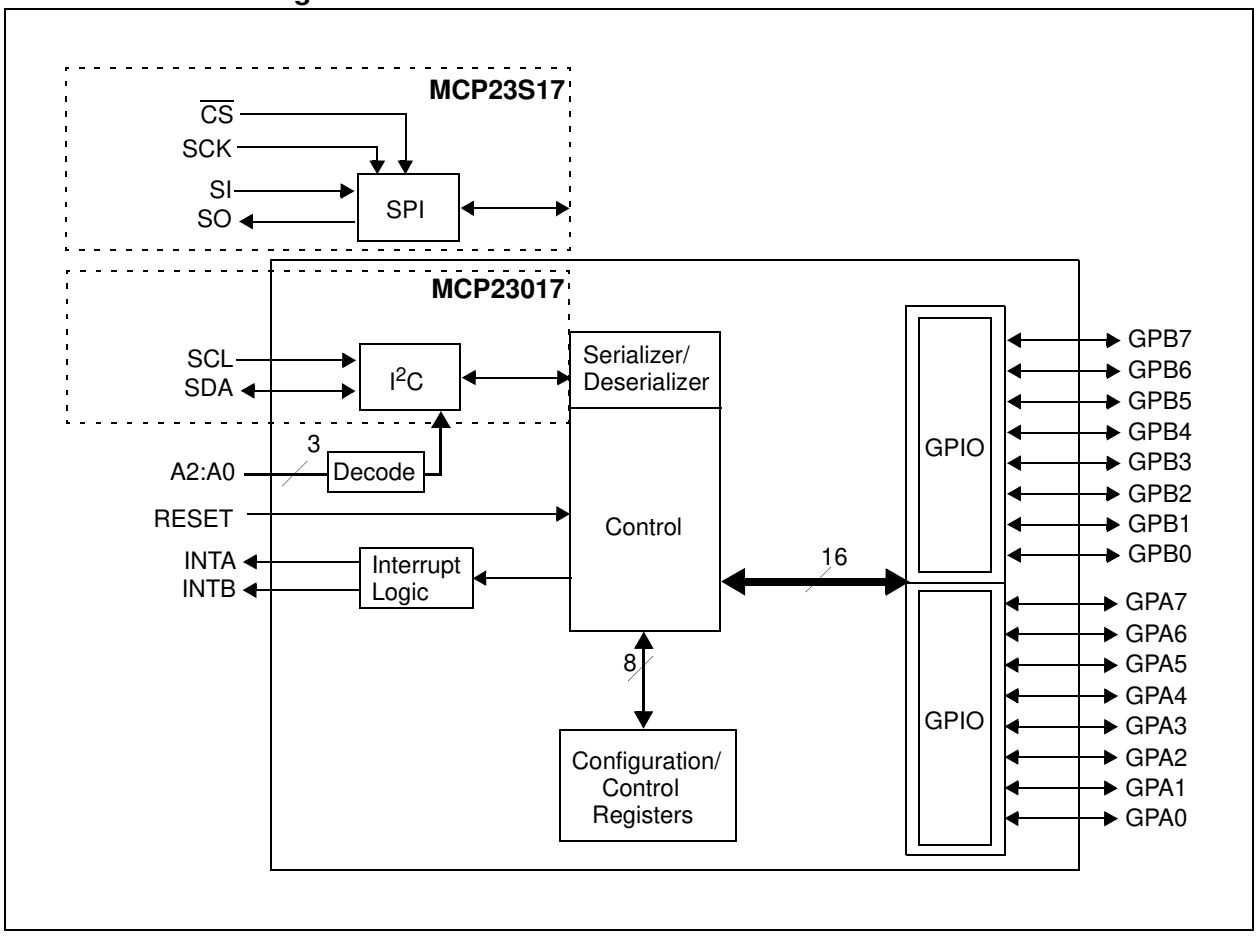
- 28-pin QFN, 6 x 6 mm Body
- 28-pin SOIC, Wide, 7.50 mm Body
- 28-pin SPDIP, 300 mil Body
- 28-pin SSOP, 5.30 mm Body

Package Types



* Includes Exposed Thermal Pad; see Table 2-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias ..... -40°C to +125°C

Storage temperature ..... -65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +5.5V

Voltage on all other pins with respect to V_{SS} (except V_{DD}) ..... -0.6V to (V_{DD} + 0.6V)

Total power dissipation ..... 700 mW

Maximum current out of V_{SS} pin ..... 150 mA

Maximum current into V_{DD} pin ..... 125 mA

Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Maximum output current sunk by any output pin ..... 25 mA

Maximum output current sourced by any output pin ..... 25 mA

ESD protection on all pins (HBM:MM) 4 kV:400V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 DC Characteristics

TABLE 1-1: DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
D001	Supply Voltage	V_{DD}	1.8	—	5.5	V	
D002	V_{DD} Start Voltage to ensure Power-on Reset	V_{POR}	—	V_{SS}	—	V	
D003	V_{DD} Rise Rate to ensure Power-on Reset	SV_{DD}	0.05	—	—	V/ms	Design guidance only. Not tested.
D004	Supply Current	I_{DD}	—	—	1	mA	SCL/SCK = 1 MHz
D005	Standby current	I_{DDS8}	—	—	1	µA	-40°C ≤ T_A ≤ +85°C
			—	—	3	µA	4.5V ≤ V_{DD} ≤ 5.5V +85°C ≤ T_A ≤+125°C **(Note 1)**
Input Low Voltage							
D030	A0, A1, A2 (TTL buffer)	V_{IL}	V_{SS}	—	0.15 V_{DD}	V	
D031	$\overline{CS}$, GPIO, SCL/SCK, SDA, $\overline{RESET}$ (Schmitt Trigger)	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
Input High Voltage							
D040	A0, A1, A2 (TTL buffer)	V_{IH}	0.25 V_{DD} + 0.8	—	V_{DD}	V	
D041	$\overline{CS}$, GPIO, SCL/SCK, SDA, $\overline{RESET}$ (Schmitt Trigger)	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	For entire V_{DD} range
Input Leakage Current							
D060	I/O port pins	I_{IL}	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
Output Leakage Current							
D065	I/O port pins	I_{LO}	—	—	±1	µA	V_{SS} ≤ V_{PIN} ≤ V_{DD}
D070	GPIO weak pull-up current	I_{PU}	40	75	115	µA	V_{DD} = 5V GP pins = V_{SS}
Output Low-Voltage							
D080	GPIO	V_{OL}	—	—	0.6	V	I_{OL} = 8.0 mA V_{DD} = 4.5V
	INT	V_{OL}	—	—	0.6	V	I_{OL} = 1.6 mA V_{DD} = 4.5V
	SO, SDA	V_{OL}	—	—	0.6	V	I_{OL} = 3.0 mA V_{DD} = 1.8V
	SDA	V_{OL}	—	—	0.8	V	I_{OL} = 3.0 mA V_{DD} = 4.5V
Output High-Voltage							
D090	GPIO, INT, SO	V_{OH}	V_{DD} – 0.7	—	—	V	I_{OH} = -3.0 mA V_{DD} = 4.5V
			V_{DD} – 0.7	—	—		I_{OH} = -400 µA V_{DD} = 1.8V
Capacitive Loading Specs on Output Pins							
D101	GPIO, SO, INT	C_{IO}	—	—	50	pF	
D102	SDA	C_B	—	—	400	pF	

Note 1: This parameter is characterized, not 100% tested.

1.2 AC Characteristics

FIGURE 1-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

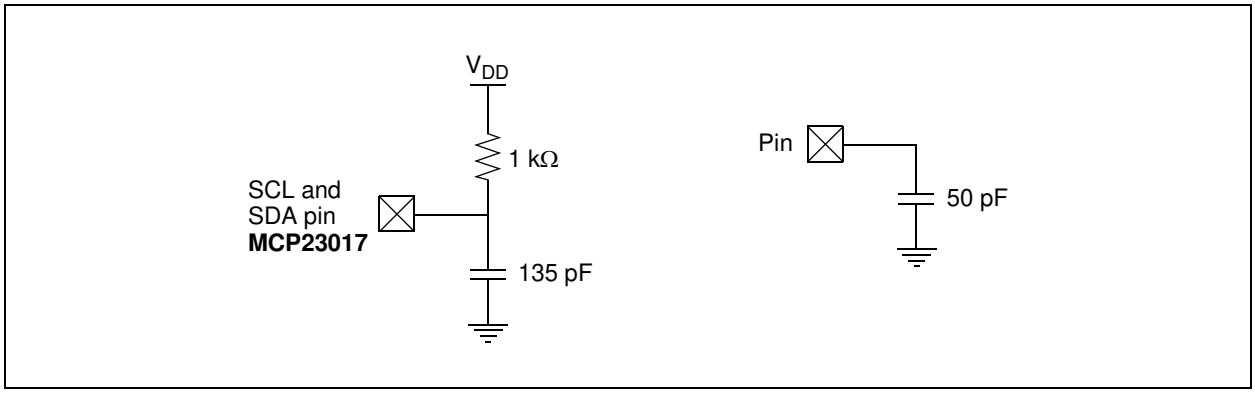


FIGURE 1-2: $\overline{\text{RESET}}$ AND DEVICE RESET TIMER TIMING

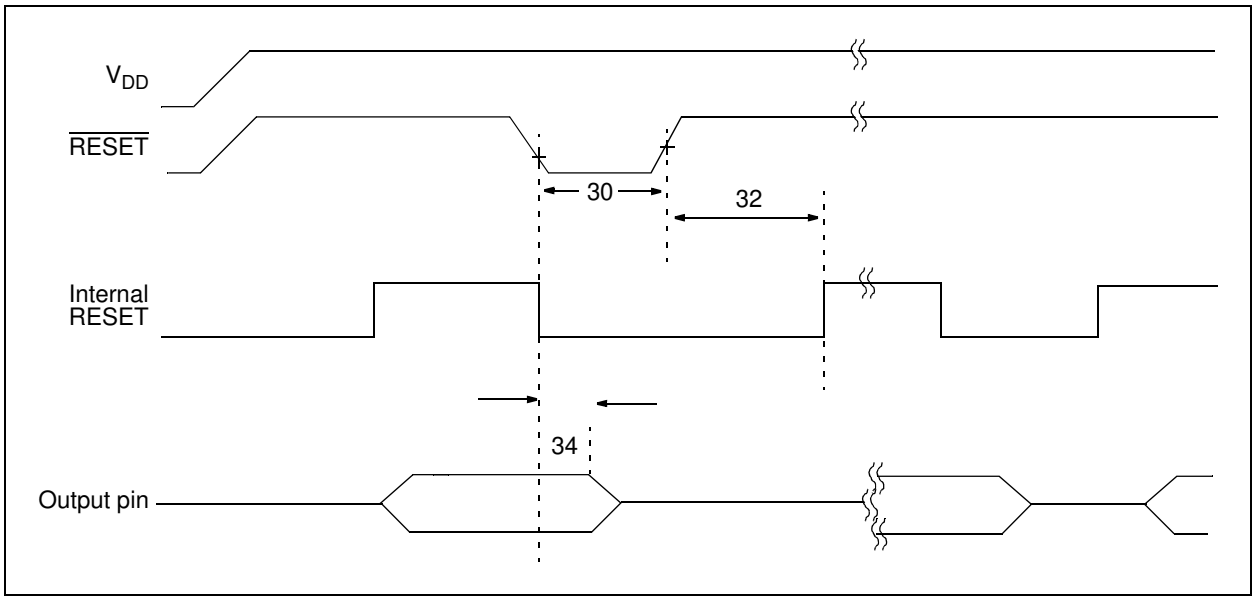


TABLE 1-2: DEVICE RESET SPECIFICATIONS

AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ. (1)**	**Max.**	**Units**	**Conditions**
30	$\overline{\text{RESET}}$ Pulse Width (Low)	T_{RSTL}	1	—	—	µs	
32	Device Active After Reset high	T_{HLD}	—	0	—	ns	V_{DD} = 5.0V
34	Output High-Impedance From $\overline{\text{RESET}}$ Low	T_{IOZ}	—	—	1	µs	

Note 1: This parameter is characterized, not 100% tested.

FIGURE 1-3: I²C BUS START/STOP BITS TIMING

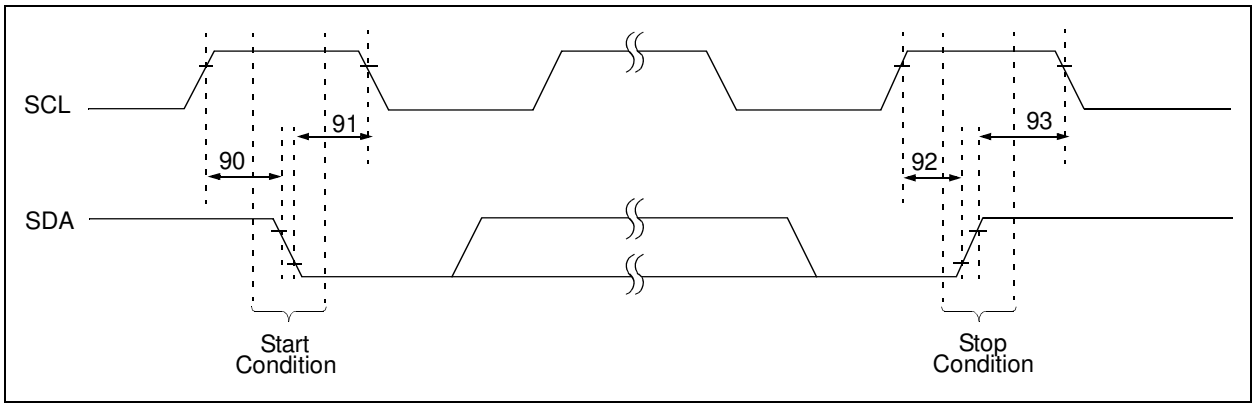


FIGURE 1-4: I²C BUS DATA TIMING

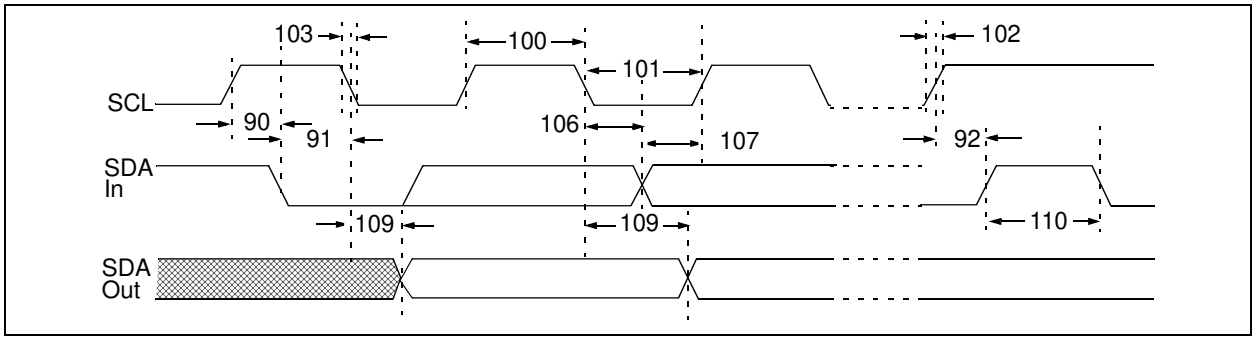


TABLE 1-3: I²C BUS DATA REQUIREMENTS

I²C Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C, R_{PU} (SCL, SDA) = 1 kΩ, C_L (SCL, SDA) = 135 pF							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
100	Clock High Time:	T_{HIGH}					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.12	—	—	µs	4.5V – 5.5V
101	Clock Low Time:	T_{LOW}					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.32	—	—	µs	4.5V – 5.5V
102	SDA and SCL Rise Time:	T_R (1)					
	100 kHz mode		—	—	1000	ns	1.8V – 5.5V
	400 kHz mode		20 + 0.1 C_B (2)	—	300	ns	2.7V – 5.5V
	1.7 MHz mode		20	—	160	ns	4.5V – 5.5V
103	SDA and SCL Fall Time:	T_F (1)					
	100 kHz mode		—	—	300	ns	1.8V – 5.5V
	400 kHz mode		20 + 0.1 C_B (2)	—	300	ns	2.7V – 5.5V
	1.7 MHz mode		20	—	80	ns	4.5V – 5.5V

Note 1: This parameter is characterized, not 100% tested.

2: C_B is specified to be from 10 to 400 pF.

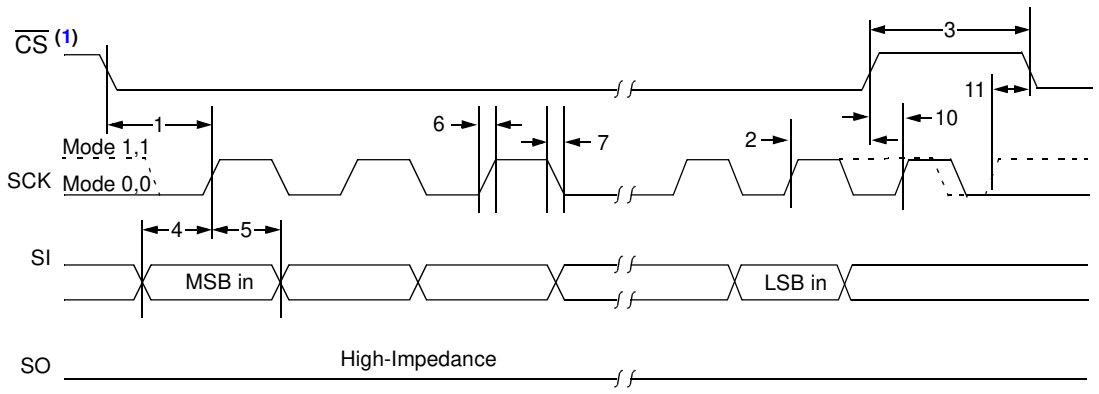
TABLE 1-3: I^2C BUS DATA REQUIREMENTS (CONTINUED)

I^2C Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C, R_{PU} (SCL, SDA) = 1 kΩ, C_L (SCL, SDA) = 135 pF							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
90	START Condition Setup Time:	$T_{SU:STA}$					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V
91	START Condition Hold Time:	$T_{HD:STA}$					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.16	—	—	µs	4.5V – 5.5V
106	Data Input Hold Time:	$T_{HD:DAT}$					
	100 kHz mode		0	—	3.45	µs	1.8V – 5.5V
	400 kHz mode		0	—	0.9	µs	2.7V – 5.5V
	1.7 MHz mode		0	—	0.15	µs	4.5V – 5.5V
107	Data Input Setup Time:	$T_{SU:DAT}$					
	100 kHz mode		250	—	—	ns	1.8V – 5.5V
	400 kHz mode		100	—	—	ns	2.7V – 5.5V
	1.7 MHz mode		0.01	—	—	µs	4.5V – 5.5V
92	Stop Condition Setup Time:	$T_{SU:STO}$					
	100 kHz mode		4.0	—	—	µs	1.8V – 5.5V
	400 kHz mode		0.6	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		0.16	—	—	µs	4.5V–5.5V
109	Output Valid From Clock:	T_{AA}					
	100 kHz mode		—	—	3.45	µs	1.8V – 5.5V
	400 kHz mode		—	—	0.9	µs	2.7V – 5.5V
	1.7 MHz mode		—	—	0.18	µs	4.5V – 5.5V
110	Bus Free Time:	T_{BUF}					
	100 kHz mode		4.7	—	—	µs	1.8V – 5.5V
	400 kHz mode		1.3	—	—	µs	2.7V – 5.5V
	1.7 MHz mode		N/A	—	N/A	µs	4.5V – 5.5V
111	Bus Capacitive Loading:	C_B					
	100 kHz and 400 kHz		—	—	400	pF	**Note 1**
	1.7 MHz		—	—	100	pF	**Note 1**
112	Input Filter Spike Suppression (SDA and SCL):	T_{SP}					
	100 kHz and 400 kHz		—	—	50	ns	
	1.7 MHz		—	—	10	ns	Spike suppression off

Note 1: This parameter is characterized, not 100% tested.

2: C_B is specified to be from 10 to 400 pF.

FIGURE 1-5: SPI INPUT TIMING



Note 1: When using SPI Mode 1,1 the $\overline{CS}$ pin needs to be toggled once before the first communication after power-up.

FIGURE 1-6: SPI OUTPUT TIMING

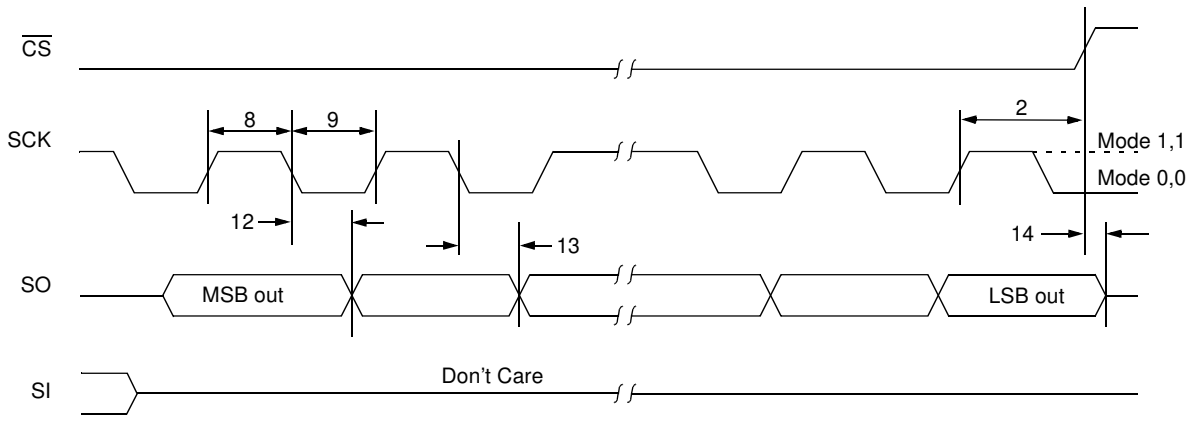


TABLE 1-4: SPI INTERFACE REQUIREMENTS

SPI Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
—	Clock Frequency	F_{CLK}	—	—	5	MHz	1.8V – 5.5V
			—	—	10	MHz	2.7V – 5.5V
			—	—	10	MHz	4.5V – 5.5V
1	$\overline{CS}$ Setup Time	T_{CSS}	50	—	—	ns	
2	$\overline{CS}$ Hold Time	T_{CSH}	100	—	—	ns	1.8V – 5.5V
			50	—	—	ns	2.7V – 5.5V
3	$\overline{CS}$ Disable Time	T_{CSD}	100	—	—	ns	1.8V – 5.5V
			50	—	—	ns	2.7V – 5.5V
4	Data Setup Time	T_{SU}	20	—	—	ns	1.8V – 5.5V
			10	—	—	ns	2.7V – 5.5V

Note 1: This parameter is characterized, not 100% tested.

TABLE 1-4: SPI INTERFACE REQUIREMENTS (CONTINUED)

SPI Interface AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
5	Data Hold Time	T_{HD}	20	—	—	ns	1.8V – 5.5V
			10	—	—	ns	2.7V – 5.5V
6	CLK Rise Time	T_R	—	—	2	µs	**Note 1**
7	CLK Fall Time	T_F	—	—	2	µs	**Note 1**
8	Clock High Time	T_{HI}	90	—	—	ns	1.8V – 5.5V
			45	—	—	ns	2.7V – 5.5V
9	Clock Low Time	T_{LO}	90	—	—	ns	1.8V – 5.5V
			45	—	—	ns	2.7V – 5.5V
10	Clock Delay Time	T_{CLD}	50	—	—	ns	
11	Clock Enable Time	T_{CLE}	50	—	—	ns	
12	Output Valid from Clock Low	T_V	—	—	90	ns	1.8V – 5.5V
			—	—	45	ns	2.7V – 5.5V
13	Output Hold Time	T_{HO}	0	—	—	ns	
14	Output Disable Time	T_{DIS}	—	—	100	ns	

Note 1: This parameter is characterized, not 100% tested.

FIGURE 1-7: GPIO AND INT TIMING

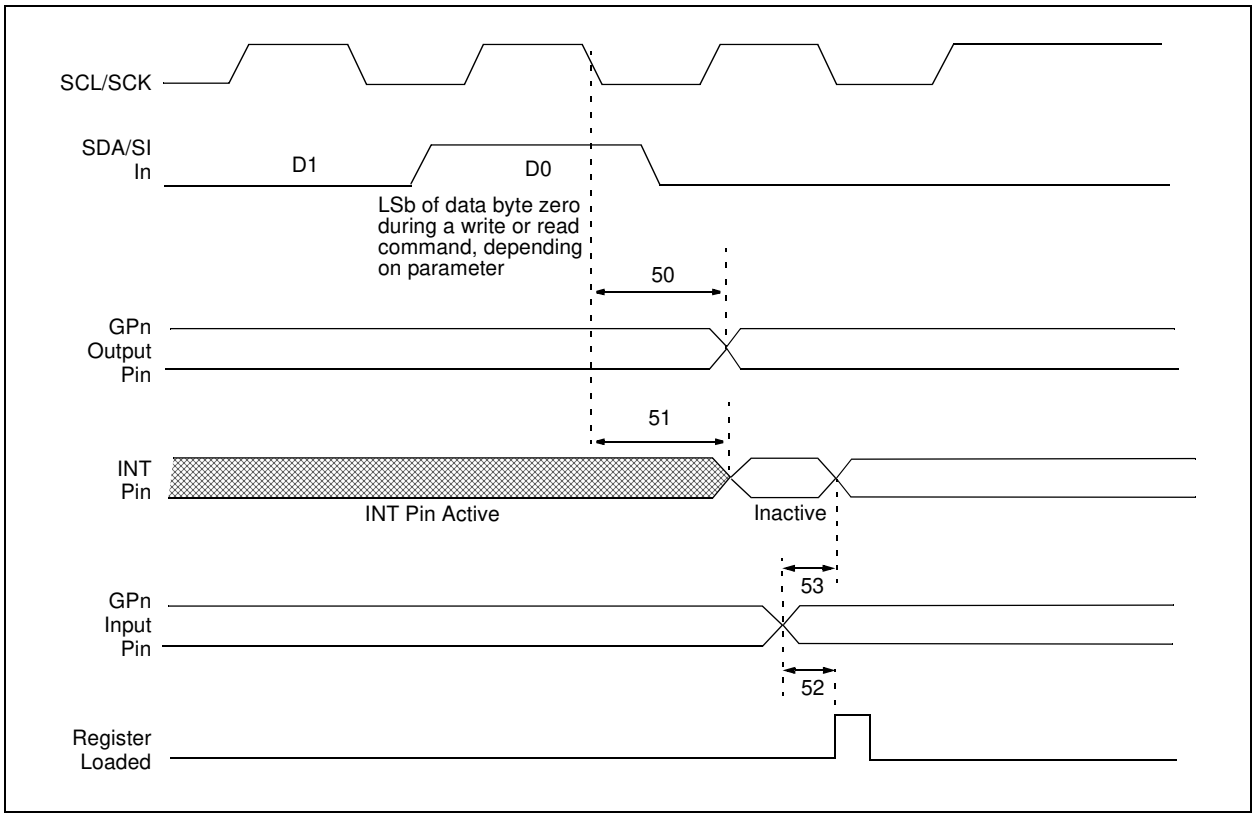


TABLE 1-5: GP AND INT PINS REQUIREMENTS

GP and INT Pins AC Characteristics: Unless otherwise noted, 1.8V ≤ V_{DD} ≤ 5.5V at -40°C ≤ T_A ≤ +125°C							
Param. No.	**Characteristic**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
50	Serial Data to Output Valid	T_{GPOV}	—	—	500	ns	
51	Interrupt Pin Disable Time	T_{INTD}	—	—	600	ns	
52	GP Input Change to Register Valid	T_{GPIV}	—	—	450	ns	
53	IOC Event to INT Active	T_{GPINT}	—	—	600	ns	
	Glitch Filter on GP Pins	T_{GLITCH}	—	—	150	ns	**Note 1**

Note 1: This parameter is characterized, not 100% tested.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PINOUT DESCRIPTION

Pin Name	QFN	SOIC SPDIP SSOP	Pin Type	Function
GPB0	25	1	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB1	26	2	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB2	27	3	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB3	28	4	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB4	1	5	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB5	2	6	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB6	3	7	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPB7	4	8	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
V_{DD}	5	9	P	Power
V_{SS}	6	10	P	Ground
NC/$\overline{CS}$	7	11	I	NC (**MCP23017**)/Chip Select (**MCP23S17**)
SCK	8	12	I	Serial clock input
SDA/SI	9	13	I/O	Serial data I/O (**MCP23017**)/Serial data input (**MCP23S17**)
NC/SO	10	14	O	NC (**MCP23017**)/Serial data out (**MCP23S17**)
A0	11	15	I	Hardware address pin. Must be externally biased.
A1	12	16	I	Hardware address pin. Must be externally biased.
A2	13	17	I	Hardware address pin. Must be externally biased.
$\overline{RESET}$	14	18	I	Hardware reset. Must be externally biased.
INTB	15	19	O	Interrupt output for PORTB. Can be configured as active-high, active-low or open-drain.
INTA	16	20	O	Interrupt output for PORTA. Can be configured as active-high, active-low or open-drain.
GPA0	17	21	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA1	18	22	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA2	19	23	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA3	20	24	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA4	21	25	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA5	22	26	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA6	23	27	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
GPA7	24	28	I/O	Bidirectional I/O pin. Can be enabled for interrupt-on-change and/or internal weak pull-up resistor.
EP	29	—	—	Exposed Thermal Pad. Either connect to V_{SS}, or leave unconnected.

3.0 DEVICE OVERVIEW

The MCP23017/MCP23S17 (MCP23X17) device family provides 16-bit, general purpose parallel I/O expansion for I^2C bus or SPI applications. The two devices differ only in the serial interface:

- MCP23017 – I^2C interface
- MCP23S17 – SPI interface

The MCP23X17 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits (IODIRA/B). The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The 16-bit I/O port functionally consists of two 8-bit ports (PORTA and PORTB). The MCP23X17 can be configured to operate in the 8-bit or 16-bit modes via IOCON.BANK.

There are two interrupt pins, INTA and INTB, that can be associated with their respective ports, or can be logically OR'ed together so that both pins will activate if either port causes an interrupt.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding Input Port register state. This is used to indicate to the system master that an input state has changed.
2. When an input state differs from a preconfigured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pins are used to determine the device address.

3.1 Power-on Reset (POR)

The on-chip POR circuit holds the device in reset until V_{DD} has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The maximum V_{DD} rise time is specified in **Section 1.0 "Electrical Characteristics"**.

When the device exits the POR condition (releases reset), device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

3.2 Serial Interface

This block handles the functionality of the I^2C (**MCP23017**) or SPI (**MCP23S17**) interface protocol. The MCP23X17 contains 22 individual registers (11 register pairs) that can be addressed through the Serial Interface block, as shown in Table 3-1.

TABLE 3-1: REGISTER ADDRESSES

Address IOCON.BANK = 1	Address IOCON.BANK = 0	Access to:
00h	00h	IODIRA
10h	01h	IODIRB
01h	02h	IPOLA
11h	03h	IPOLB
02h	04h	GPINTENA
12h	05h	GPINTENB
03h	06h	DEFVALA
13h	07h	DEFVALB
04h	08h	INTCONA
14h	09h	INTCONB
05h	0Ah	IOCON
15h	0Bh	IOCON
06h	0Ch	GPPUA
16h	0Dh	GPPUB
07h	0Eh	INTFA
17h	0Fh	INTFB
08h	10h	INTCAPA
18h	11h	INTCAPB
09h	12h	GPIOA
19h	13h	GPIOB
0Ah	14h	OLATA
1Ah	15h	OLATB

3.2.1 BYTE MODE AND SEQUENTIAL MODE

The MCP23X17 family has the ability to operate in Byte mode or Sequential mode (IOCON.SEQOP).

Byte mode disables automatic Address Pointer incrementing. When operating in Byte mode, the MCP23X17 family does not increment its internal address counter after each byte during the data transfer. This gives the ability to continually access the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes or for continually writing to the output latches.

A special mode **(Byte mode with IOCON.BANK = 0)** causes the address pointer to toggle between associated A/B register pairs. For example, if the BANK bit is cleared and the Address Pointer is initially set to address 12h (GPIOA) or 13h (GPIOB), the pointer will toggle between GPIOA and GPIOB. Note that the Address Pointer can initially point to either address in the register pair.

Sequential mode enables automatic address pointer incrementing. When operating in Sequential mode, the MCP23X17 family increments its address counter after each byte during the data transfer. The Address Pointer automatically rolls over to address 00h after accessing the last register.

These two modes are not to be confused with single writes/reads and continuous writes/reads that are serial protocol sequences. For example, the device may be configured for Byte mode and the master may perform a continuous read. In this case, the MCP23X17 would not increment the Address Pointer and would repeatedly drive data from the same location.

3.2.2 I^2C INTERFACE

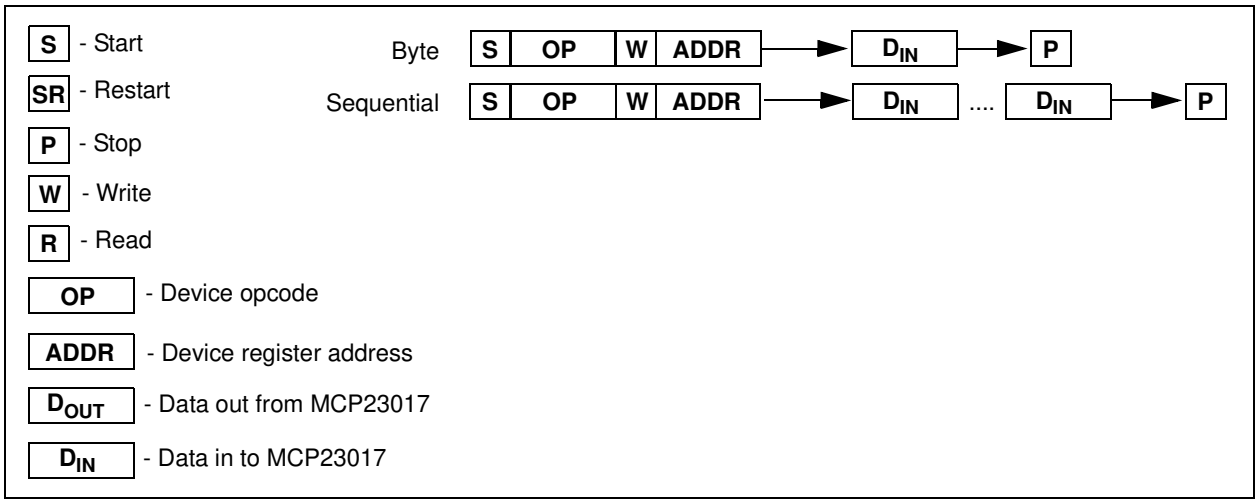
3.2.2.1 I^2C Write Operation

The I^2C write operation includes the control byte and register address sequence, as shown in Figure 3-1. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23017. The operation is ended with a Stop (P) or Restart (SR) condition being generated by the master.

Data is written to the MCP23017 after every byte transfer. If a Stop or Restart condition is generated during a data transfer, the data will not be written to the MCP23017.

Both “byte writes” and “sequential writes” are supported by the MCP23017. If Sequential mode is enabled (IOCON, SEQOP = 0) (default), the MCP23017 increments its address counter after each ACK during the data transfer.

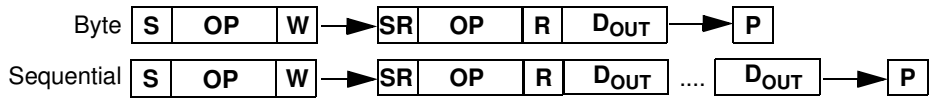
FIGURE 3-1: BYTE AND SEQUENTIAL WRITE



3.2.2.2 I²C Read Operation

I²C Read operations include the control byte sequence, as shown in Figure 3-2. This sequence is followed by another control byte (including the Start condition and ACK) with the R/W bit set (R/W = 1). The MCP23017 then transmits the data contained in the addressed register. The sequence is ended with the master generating a Stop or Restart condition.

FIGURE 3-2: BYTE AND SEQUENTIAL READ



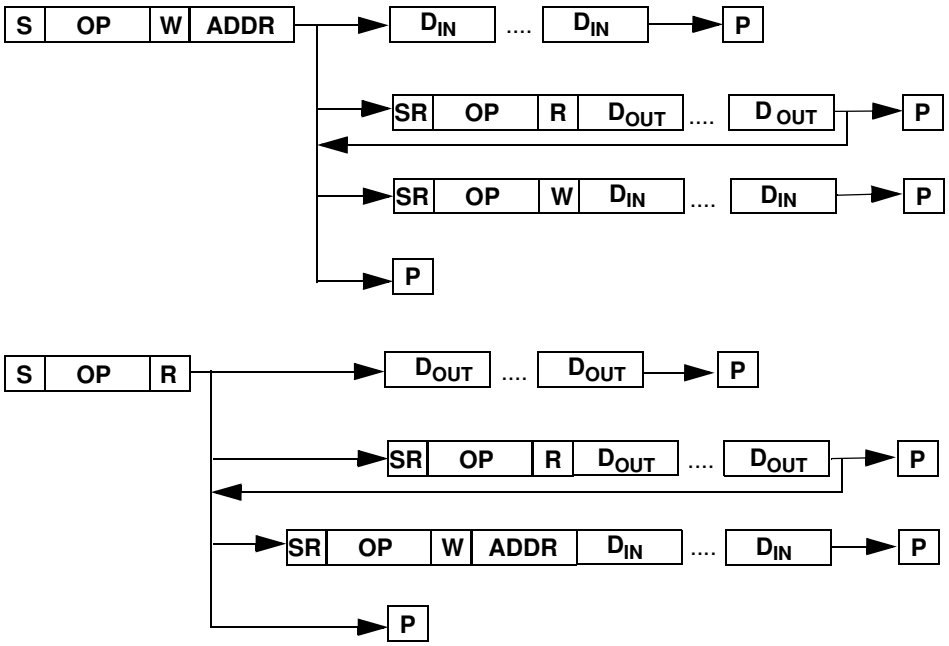
3.2.2.3 I²C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a Stop or Restart condition after the data transfer, the master clocks the next byte pointed to by the address pointer (see **Section 3.2.1 "Byte Mode and Sequential Mode"** for details regarding sequential operation control).

The sequence ends with the master sending a Stop or Restart condition.

The MCP23017 Address Pointer will roll over to address zero after reaching the last register address. Refer to Figure 3-3.

FIGURE 3-3: MCP23017 I²C DEVICE PROTOCOL



3.2.3 SPI INTERFACE

3.2.3.1 SPI Write Operation

The SPI write operation is started by lowering $\overline{CS}$. The Write command (slave address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

3.2.3.2 SPI Read Operation

The SPI read operation is started by lowering $\overline{CS}$. The SPI read command (slave address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

3.2.3.3 SPI Sequential Write/Read

For sequential operations, instead of deselecting the device by raising $\overline{CS}$, the master clocks the next byte pointed to by the Address Pointer. (see **Section 3.2.1 "Byte Mode and Sequential Mode"** for details regarding sequential operation control).

The sequence ends by the raising of $\overline{CS}$.

The MCP23S17 Address Pointer will roll over to address zero after reaching the last register address.

3.3 Hardware Address Decoder

The hardware address pins are used to determine the device address. To address a device, the corresponding address bits in the control byte must match the pin state. The pins must be biased externally.

3.3.1 ADDRESSING I²C DEVICES (**MCP23017**)

The MCP23017 is a slave I²C interface device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address contains four fixed bits and three user-defined hardware address bits (pins A2, A1 and A0). Figure 3-4 shows the control byte format.

3.3.2 ADDRESSING SPI DEVICES (**MCP23S17**)

The MCP23S17 is a slave SPI device. The slave address contains four fixed bits and three user-defined hardware address bits (if enabled via IOCON.HAEN) (pins A2, A1 and A0) with the read/write bit filling out the control byte. Figure 3-5 shows the control byte format. The address pins should be externally biased even if disabled (IOCON.HAEN = 0).

FIGURE 3-4: I²C CONTROL BYTE FORMAT

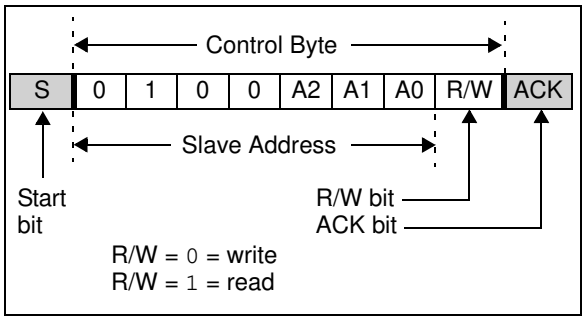


FIGURE 3-5: SPI CONTROL BYTE FORMAT

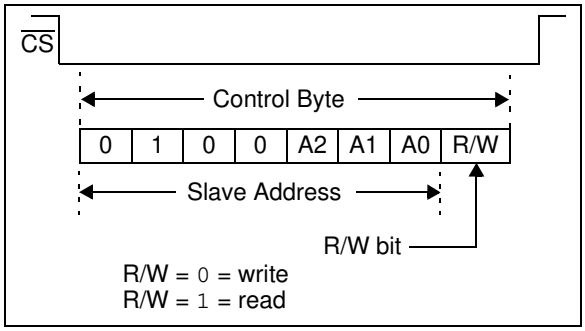
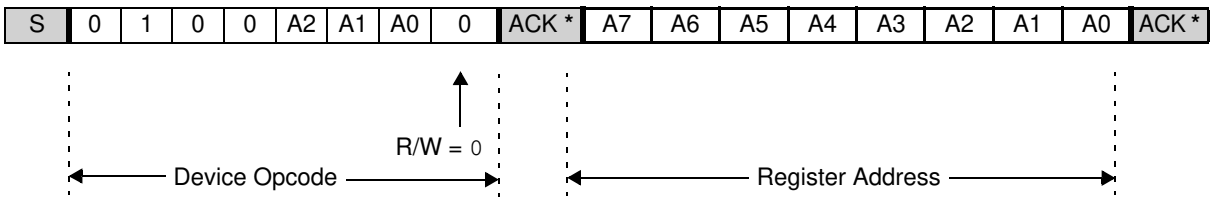
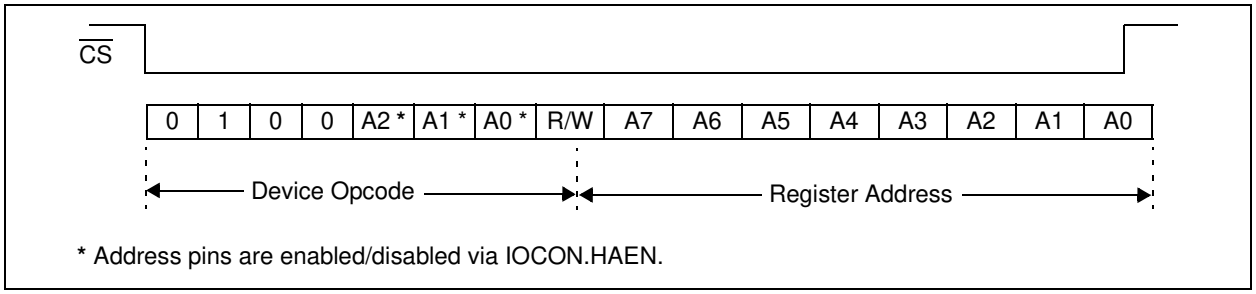


FIGURE 3-6: I²C ADDRESSING REGISTERS



*The ACKs are provided by the MCP23017.

FIGURE 3-7: SPI ADDRESSING REGISTERS



3.4 GPIO Port

The GPIO module is a general purpose, 16-bit wide, bidirectional port that is functionally split into two 8-bit wide ports.

The GPIO module contains the data ports (GPIOn), internal pull-up resistors and the output latches (OLATn).

Reading the GPIOn register reads the value on the port. Reading the OLATn register only reads the latches, not the actual value on the port.

Writing to the GPIOn register actually causes a write to the latches (OLATn). Writing to the OLATn register forces the associated output drivers to drive to the level in OLATn. Pins configured as inputs turn off the associated output driver and put it in high-impedance.

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE GPIO PORTS (BANK = 1)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPPUA	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPIOA	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
IODIRB	10	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLB	11	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENB	12	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPPUB	16	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPIOB	19	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATB	1A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

TABLE 3-3: SUMMARY OF REGISTERS ASSOCIATED WITH THE GPIO PORTS (BANK = 0)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IODIRB	01	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	02	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
IPOLB	03	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	04	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPINTENB	05	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPPUA	0C	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPPUB	0D	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPIOA	12	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
GPIOB	13	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	14	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
OLATB	15	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

3.5 Configuration and Control Registers

There are 21 registers associated with the MCP23X17, as shown in Tables 3-4 and3-5. The two tables show the register mapping with the two BANK bit values. Ten registers are associated with PORTA and ten are associated with PORTB. One register (IOCON) is shared between the two ports. The PORTA registers are identical to the PORTB registers, therefore, they will be referred to without differentiating between the port designation (i.e., they will not have the “A” or “B” designator assigned) in the register tables.

TABLE 3-4: CONTROL REGISTER SUMMARY (IOCON.BANK = 1)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	01	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	02	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVALA	03	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCONA	04	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	05	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
GPPUA	06	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTFA	07	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAPA	08	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIOA	09	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	0A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
IODIRB	10	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLB	11	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENB	12	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVALB	13	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCONB	14	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	15	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
GPPUB	16	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
INTFB	17	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAPB	18	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIOB	19	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATB	1A	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

TABLE 3-5: CONTROL REGISTER SUMMARY (IOCON.BANK = 0)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
IODIRA	00	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IODIRB	01	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	1111 1111
IPOLA	02	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
IPOLB	03	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000 0000
GPINTENA	04	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
GPINTENB	05	GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0	0000 0000
DEFVALA	06	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
DEFVALB	07	DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0	0000 0000
INTCONA	08	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
INTCONB	09	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	0000 0000
IOCON	0A	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
IOCON	0B	BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—	0000 0000
GPPUA	0C	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000
GPPUB	0D	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0000 0000

TABLE 3-5: CONTROL REGISTER SUMMARY (IOCON.BANK = 0) (CONTINUED)

Register Name	Address (hex)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	POR/RST value
INTFA	0E	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTFB	0F	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INTO	0000 0000
INTCAPA	10	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
INTCAPB	11	ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0	0000 0000
GPIOA	12	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
GPIOB	13	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	0000 0000
OLATA	14	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000
OLATB	15	OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0	0000 0000

3.5.1 I/O DIRECTION REGISTER

Controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

REGISTER 3-1: IODIR: I/O DIRECTION REGISTER (ADDR 0x00)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IO<7:0>:** Controls the direction of data I/O <7:0>

1 = Pin is configured as an input.
0 = Pin is configured as an output.

3.5.2 INPUT POLARITY REGISTER

This register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

REGISTER 3-2: IPOL: INPUT POLARITY PORT REGISTER (ADDR 0x01)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IP<7:0>:** Controls the polarity inversion of the input pins <7:0>

1 = GPIO register bit reflects the opposite logic state of the input pin.
0 = GPIO register bit reflects the same logic state of the input pin.

3.5.3 INTERRUPT-ON-CHANGE CONTROL REGISTER

The GPINTEN register controls the interrupt-on-change feature for each pin.

If a bit is set, the corresponding pin is enabled for interrupt-on-change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for interrupt-on-change.

REGISTER 3-3: GPINTEN: INTERRUPT-ON-CHANGE PINS (ADDR 0x02) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GPINT7	GPINT6	GPINT5	GPINT4	GPINT3	GPINT2	GPINT1	GPINT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **GPINT<7:0>:** General purpose I/O interrupt-on-change bits <7:0>
1 = Enables GPIO input pin for interrupt-on-change event.
0 = Disables GPIO input pin for interrupt-on-change event.

Note 1: Refer to INTCON.

3.5.4 DEFAULT COMPARE REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an interrupt to occur.

REGISTER 3-4: DEFVAL: DEFAULT VALUE REGISTER (ADDR 0x03)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DEF7	DEF6	DEF5	DEF4	DEF3	DEF2	DEF1	DEF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **DEF<7:0>:** Sets the compare value for pins configured for interrupt-on-change from defaults <7:0> **(Note 1)**
If the associated pin level is the opposite from the register bit, an interrupt occurs. **(Note 2)**

Note 1: Refer to INTCON.
2: Refer to INTCON and GPINTEN.

3.5.5 INTERRUPT CONTROL REGISTER

The INTCON register controls how the associated pin value is compared for the interrupt-on-change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

REGISTER 3-5: INTCON: INTERRUPT-ON-CHANGE CONTROL REGISTER (ADDR 0x04) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IOC<7:0>:** Controls how the associated pin value is compared for interrupt-on-change <7:0>
1 = Pin value is compared against the associated bit in the DEFVAL register.
0 = Pin value is compared against the previous pin value.

Note 1: Refer to INTCON and GPINTEN.

3.5.6 CONFIGURATION REGISTER

The IOCON register contains several bits for configuring the device:

The BANK bit changes how the registers are mapped (see Tables 3-4 and3-5 for more details).

- If BANK = 1, the registers associated with each port are segregated. Registers associated with PORTA are mapped from address 00h - 0Ah and registers associated with PORTB are mapped from 10h - 1Ah.
- If BANK = 0, the A/B registers are paired. For example, IODIRA is mapped to address 00h and IODIRB is mapped to the next address (address 01h). The mapping for all registers is from 00h -15h.

It is important to take care when changing the BANK bit as the address mapping changes after the byte is clocked into the device. The address pointer may point to an invalid location after the bit is modified.

For example, if the device is configured to automatically increment its internal Address Pointer, the following scenario would occur:

- BANK = 0
- Write 80h to address 0Ah (IOCON) to set the BANK bit
- Once the write completes, the internal address now points to 0Bh which is an invalid address when the BANK bit is set.

For this reason, when changing the BANK bit, it is advised to only perform byte writes to this register.

The **MIRROR** bit controls how the INTA and INTB pins function with respect to each other.

- When MIRROR = 1, the INTn pins are functionally OR'ed so that an interrupt on either port will cause both pins to activate.
- When MIRROR = 0, the INT pins are separated. Interrupt conditions on a port will cause its respective INT pin to activate.

The Sequential Operation (**SEQOP**) controls the incrementing function of the Address Pointer. If the address pointer is disabled, the Address Pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.

The Slew Rate (**DISSLW**) bit controls the slew rate function on the SDA pin. If enabled, the SDA slew rate will be controlled when driving from a high to low.

The Hardware Address Enable (**HAEN**) bit enables/disables hardware addressing on the MCP23S17 only. The address pins (A2, A1 and A0) must be externally biased, regardless of the HAEN bit value.

If enabled (HAEN = 1), the device's hardware address matches the address pins.

If disabled (HAEN = 0), the device's hardware address is A2 = A1 = A0 = 0.

The Open-Drain (**ODR**) control bit enables/disables the INT pin for open-drain configuration. Setting this bit overrides the INTPOL bit.

The Interrupt Polarity (**INTPOL**) sets the polarity of the INT pin. This bit is functional only when the ODR bit is cleared, configuring the INT pin as active push-pull.

REGISTER 3-6: IOCON: I/O EXPANDER CONFIGURATION REGISTER (ADDR 0x05)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
BANK	MIRROR	SEQOP	DISSLW	HAEN	ODR	INTPOL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **BANK:** Controls how the registers are addressed
1 = The registers associated with each port are separated into different banks.
0 = The registers are in the same bank (addresses are sequential).

bit 6 **MIRROR:** INT Pins Mirror bit
1 = The INT pins are internally connected
0 = The INT pins are not connected. INTA is associated with PORTA and INTB is associated with PORTB

bit 5 **SEQOP:** Sequential Operation mode bit
1 = Sequential operation disabled, address pointer does not increment.
0 = Sequential operation enabled, address pointer increments.

bit 4 **DISSLW:** Slew Rate control bit for SDA output
1 = Slew rate disabled
0 = Slew rate enabled

bit 3 **HAEN:** Hardware Address Enable bit (**MCP23S17** only) **(Note 1)**
1 = Enables the MCP23S17 address pins.
0 = Disables the MCP23S17 address pins.

bit 2 **ODR:** Configures the INT pin as an open-drain output
1 = Open-drain output (overrides the INTPOL bit.)
0 = Active driver output (INTPOL bit sets the polarity.)

bit 1 **INTPOL:** This bit sets the polarity of the INT output pin
1 = Active-high
0 = Active-low

bit 0 **Unimplemented:** Read as '0'

Note 1: Address pins are always enabled on the MCP23017.

3.5.7 PULL-UP RESISTOR CONFIGURATION REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set and the corresponding pin is configured as an input, the corresponding port pin is internally pulled up with a 100 kΩ resistor.

REGISTER 3-7: GPPU: GPIO PULL-UP RESISTOR REGISTER (ADDR 0x06)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PU<7:0>** Controls the weak pull-up resistors on each pin (when configured as an input)
1 = Pull-up enabled
0 = Pull-up disabled

3.5.8 INTERRUPT FLAG REGISTER

The INTF register reflects the interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A set bit indicates that the associated pin caused the interrupt.

This register is read-only. Writes to this register will be ignored.

REGISTER 3-8: INTF: INTERRUPT FLAG REGISTER (ADDR 0x07)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **INT<7:0>:** Reflects the interrupt condition on the port. It reflects the change only if interrupts are enabled per GPINTEN<7:0>.
1 = Pin caused interrupt.
0 = Interrupt not pending

3.5.9 INTERRUPT CAPTURED REGISTER

The INTCAP register captures the GPIO port value at the time the interrupt occurred. The register is read-only and is updated only when an interrupt occurs. The register remains unchanged until the interrupt is cleared via a read of INTCAP or GPIO.

REGISTER 3-9: INTCAP: INTERRUPT CAPTURED VALUE FOR PORT REGISTER (ADDR 0x08)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
ICP7	ICP6	ICP5	ICP4	ICP3	ICP2	ICP1	ICP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **ICP<7:0>:** Reflects the logic level on the port pins at the time of interrupt due to pin change <7:0>

1 = Logic-high
0 = Logic-low

3.5.10 PORT REGISTER

The GPIO register reflects the value on the port. Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

REGISTER 3-10: GPIO: GENERAL PURPOSE I/O PORT REGISTER (ADDR 0x09)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **GP<7:0>:** Reflects the logic level on the pins <7:0>

1 = Logic-high
0 = Logic-low

3.5.11 OUTPUT LATCH REGISTER (OLAT)

The OLAT register provides access to the output latches. A read from this register results in a read of the OLAT and not the port itself. A write to this register modifies the output latches that modifies the pins configured as outputs.

REGISTER 3-11: OLAT: OUTPUT LATCH REGISTER 0 (ADDR 0x0A)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OL7	OL6	OL5	OL4	OL3	OL2	OL1	OL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **OL<7:0>:** Reflects the logic level on the output latch <7:0>

1 = Logic-high
0 = Logic-low

3.6 Interrupt Logic

If enabled, the MCP23X17 activates the INTn interrupt output when one of the port pins changes state or when a pin does not match the preconfigured default. Each pin is individually configurable as follows:

- Enable/disable interrupt via GPINTEN
- Can interrupt on either pin change or change from default as configured in DEFVAL

Both conditions are referred to as Interrupt-on-Change (IOC).

The interrupt control module uses the following registers/bits:

- IOCON.MIRROR – controls if the two interrupt pins mirror each other
- GPINTEN – Interrupt enable register
- INTCON – controls the source for the IOC
- DEFVAL – contains the register default for IOC operation

3.6.1 INTA AND INTB

There are two interrupt pins: INTA and INTB. By default, INTA is associated with GPAn pins (PORTA) and INTB is associated with GPBn pins (PORTB). Each port has an independent signal which is cleared if its associated GPIO or INTCAP register is read.

3.6.1.1 Mirroring the INT pins

Additionally, the INTn pins can be configured to mirror each other so that any interrupt will cause both pins to go active. This is controlled via IOCON.MIRROR.

If IOCON.MIRROR = 0, the internal signals are routed independently to the INTA and INTB pads.

If IOCON.MIRROR = 1, the internal signals are OR'ed together and routed to the INTn pads. In this case, the interrupt will only be cleared if the associated GPIO or INTCAP is read (see Table 3-6).

TABLE 3-6: INTERRUPT OPERATION (IOCON.MIRROR = 1)

Interrupt Condition	Read PORTn (1)	Interrupt Result
GPIOA	PORTA	Clear
	PORTB	Unchanged
GPIOB	PORTA	Unchanged
	PORTB	Clear
GPIOA and GPIOB	PORTA	Unchanged
	PORTB	Unchanged
	Both PORTA and PORTB	Clear

Note 1: PORTn = GPIOn or INTCAPn

3.6.2 IOC FROM PIN CHANGE

If enabled, the MCP23X17 generates an interrupt if a mismatch condition exists between the current port value and the previous port value. Only IOC-enabled pins will be compared. Refer to Registers 3-3 and 3-5.

3.6.3 IOC FROM REGISTER DEFAULT

If enabled, the MCP23X17 generates an interrupt if a mismatch occurs between the DEFVAL register and the port. Only IOC enabled pins are compared. Refer to Registers 3-3, 3-4 and 3-5.

3.6.4 INTERRUPT OPERATION

The INTn interrupt output can be configured as active-low, active-high or open-drain via the IOCON register.

Only those pins that are configured as an input (IODIR register) with Interrupt-On-Change (IOC) enabled (IOINTEN register) can cause an interrupt. Pins defined as an output have no effect on the interrupt output pin.

Input change activity on a port input pin that is enabled for IOC generates an internal device interrupt and the device captures the value of the port and copies it into INTCAP. The interrupt remains active until the INTCAP or GPIO register is read. Writing to these registers does not affect the interrupt. The interrupt condition is cleared after the LSb of the data is clocked out during a read command of GPIO or INTCAP.

The first interrupt event causes the port contents to be copied into the INTCAP register. Subsequent interrupt conditions on the port will not cause an interrupt to occur as long as the interrupt is not cleared by a read of INTCAP or GPIO.

Note:	The value in INTCAP can be lost if GPIO is read before INTCAP while another IOC is pending. After reading GPIO, the interrupt will clear and then set due to the pending IOC, causing the INTCAP register to update.

3.6.5 INTERRUPT CONDITIONS

There are two possible configurations that cause interrupts (configured via INTCON):

1. Pins configured for **interrupt-on-pin change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt occurs and after clearing the interrupt condition (i.e., after reading GPIO or INTCAP). For example, an interrupt occurs by an input changing from '1' to '0'. The new initial state for the pin is a logic '0' after the interrupt is cleared.
2. Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTCAP or GPIO is read.

See Figures 3-8 and 3-9 for more information on interrupt operations.

FIGURE 3-8: INTERRUPT-ON-PIN CHANGE

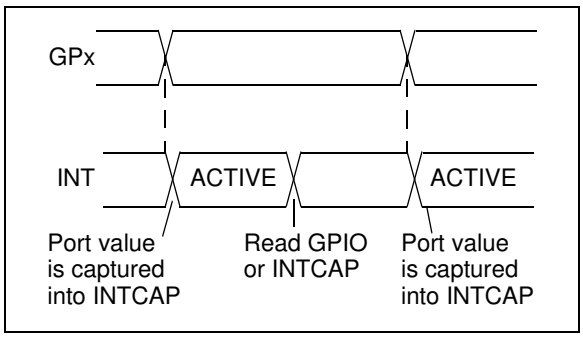


FIGURE 3-9: INTERRUPT-ON-CHANGE FROM REGISTER DEFAULT