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MCP2517FD

External CAN FD Controller with SPI Interface

Features

General

- External CAN FD Controller with SPI Interface
- Arbitration Bit Rate up to 1 Mbps
- Data Bit Rate up to 8 Mbps
- CAN FD Controller modes
  - Mixed CAN 2.0B and CAN FD mode
  - CAN 2.0B mode
- Conforms to ISO 11898-1:2015

Message FIFOs

- 31 FIFOs, configurable as transmit or receive FIFOs
- One Transmit Queue (TXQ)
- Transmit Event FIFO (TEF) with 32 bit time stamp

Message Transmission

- Message transmission prioritization:
  - Based on priority bit field, and/or
  - Message with lowest ID gets transmitted first using the Transmit Queue (TXQ)
- Programmable automatic retransmission attempts: unlimited, 3 attempts or disabled

Message Reception

- 32 Flexible Filter and Mask Objects
- Each object can be configured to filter either:
  - Standard ID + first 18 data bits, or
  - Extended ID
- 32-bit Time Stamp

Special Features

- V_{DD}: 2.7 to 5.5V
- Active current: max. 20 mA at 5.5 V, 40 MHz CAN clock
- Sleep current: 10 µA, typical
- Message objects are located in RAM: 2 KB
- Up to 3 configurable interrupt pins
- Bus Health Diagnostics and Error counters
- Transceiver standby control
- Start of frame pin for indicating the beginning of messages on the bus
- Temperature ranges:
  - High (H): –40°C to +150°C

Oscillator Options

- 40, 20 or 4 MHz crystal, or ceramic resonator; or external clock input
- Clock output with prescaler

SPI Interface

- Up to 20 MHz SPI clock speed
- Supports SPI modes 0,0 and 1,1
- Registers and bit fields are arranged in a way to enable efficient access via SPI

Safety Critical Systems

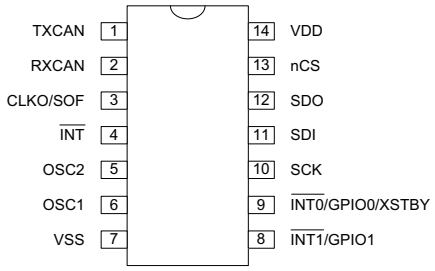
- SPI commands with CRC to detect noise on SPI interface
- Error Correction Code (ECC) protected RAM

Additional Features

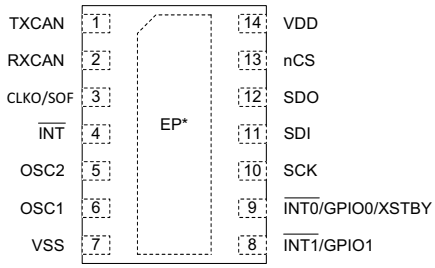
- GPIO pins: $\overline{INT0}$ and $\overline{INT1}$ can be configured as general purpose I/O
- Open drain outputs: TXCAN, $\overline{INT}$, $\overline{INT0}$, and $\overline{INT1}$ pins can be configured as push/pull or open drain outputs

Package Types

MCP2517FD
SOIC14



MCP2517FD
VDFN14 with wettable flanks*



*VDFN14 includes an Exposed Thermal Pad (EP); see Table 1-1

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1.0 DEVICE OVERVIEW

The MCP2517FD is a cost-effective and small-footprint CAN FD controller that can be easily added to a microcontroller with an available SPI interface. Therefore, a CAN FD channel can be easily added to a microcontroller that is either lacking a CAN FD peripheral, or that doesn't have enough CAN FD channels.

The MCP2517FD supports both, CAN frames in the Classical format (CAN2.0B) and CAN Flexible Data Rate (CAN FD) format, as specified in ISO 11898-1:2015.

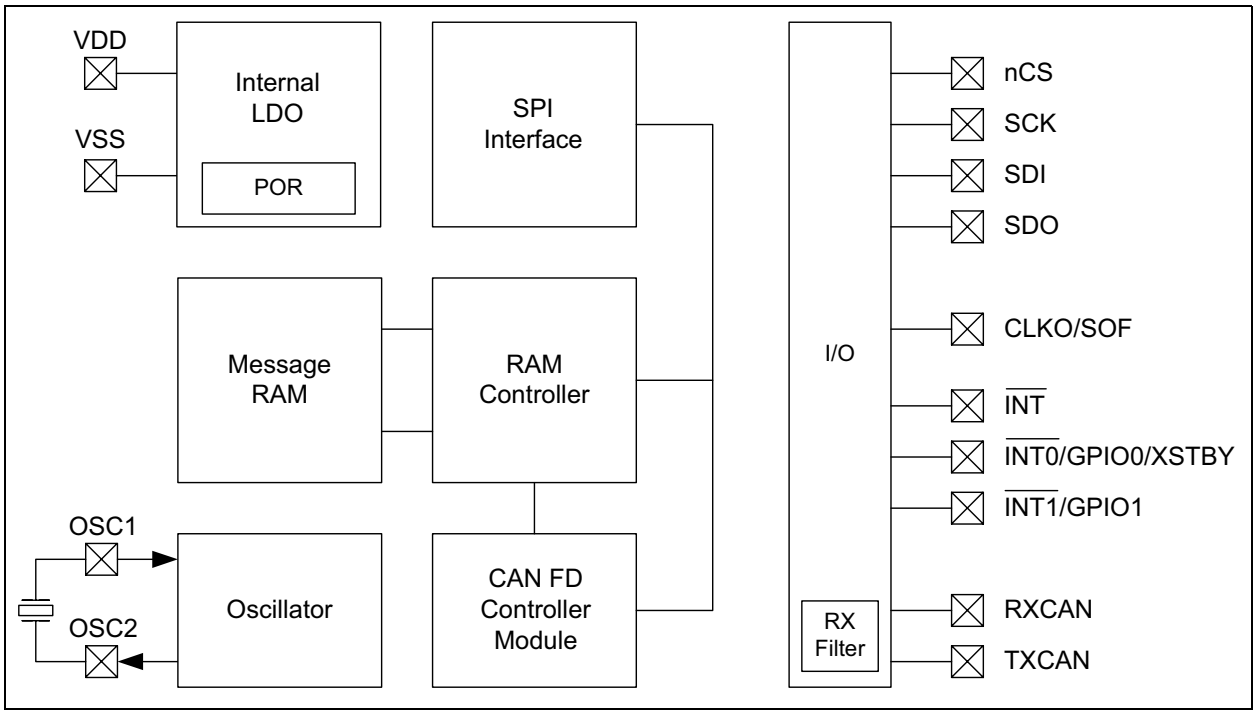
1.1 Block Diagram

Figure 1.1 shows the block diagram of the MCP2517FD. The MCP2517FD contains the following main blocks:

- The CAN FD Controller module implements the CAN FD protocol and contains the FIFOs, and Filters.
- The SPI interface is used to control the device by accessing SFRs and RAM.
- The RAM controller arbitrates the RAM accesses between the SPI and CAN FD Controller module.
- The Message RAM is used to store the data of the Message Objects.
- The oscillator generates the CAN clock.
- The Internal LDO and POR circuit.
- The I/O control.

Note 1: This data sheet summarizes the features of the MCP2517FD. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "MCP25xxFD Family Reference Manual".

FIGURE 1-1: MCP2517FD BLOCK DIAGRAM



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1.2 Pin Out Description

Table 1-1 describes the functions of the pins.

TABLE 1-1: MCP2517FD STANDARD PINOUT VERSION

Pin Name	SOIC	VDFN	Pin Type	Description
TXCAN	1	1	O	Transmit output to CAN FD transceiver
RXCAN	2	2	I	Receive input from CAN FD transceiver
CLKO/SOF	3	3	O	Clock output/Start of Frame output
$\overline{\text{INT}}$	4	4	O	Interrupt output (active low)
OSC2	5	5	O	External oscillator output
OSC1	6	6	I	External oscillator input
VSS	7	7	P	Ground
$\overline{\text{INT1}}$/GPIO1	8	8	I/O	RX Interrupt output (active low)/GPIO
$\overline{\text{INT0}}$/GPIO0/ XSTBY	9	9	I/O	TX Interrupt output (active low)/GPIO/ Transceiver Standby output
SCK	10	10	I	SPI clock input
SDI	11	11	I	SPI data input
SDO	12	12	O	SPI data output
nCS	13	13	I	SPI chip select input
VDD	14	14	P	Positive Supply
EP	-	15	P	Exposed Pad; connect to VSS

Legend: P = Power, I = Input, O = Output

1.3 Typical Application

Figure 1-2 shows an example of a typical application of the MCP2517FD. In this example, the microcontroller operates at 3.3V.

The MCP2517FD interfaces directly with microcontrollers operating at 2.7V to 5.5V. In addition, the MCP2517FD connects directly to high-speed CAN FD transceivers. There are no external level shifters required when connecting VDD of the MCP2517FD and the microcontroller to VIO of the transceiver.

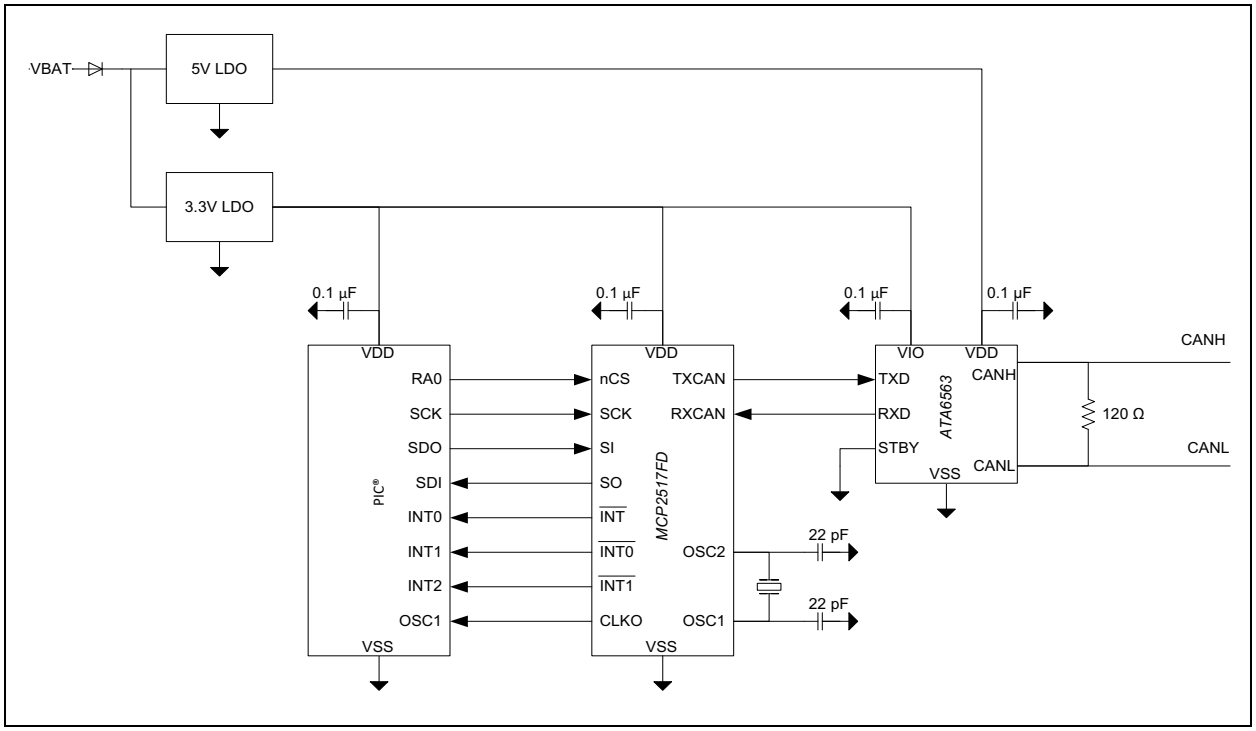
The VDD of the CAN FD transceiver is connected to 5V.

The SPI interface is used to configure and control the CAN FD controller.

The MCP2517FD signals interrupts to the microcontroller using $\overline{INT}$, $\overline{INT0}$ and $\overline{INT1}$. Interrupts need to be cleared by the microcontroller through SPI.

The CLKO pin provides the clock to the microcontroller.

FIGURE 1-2: MCP2517FD INTERFACING WITH A 3.3V MICROCONTROLLER



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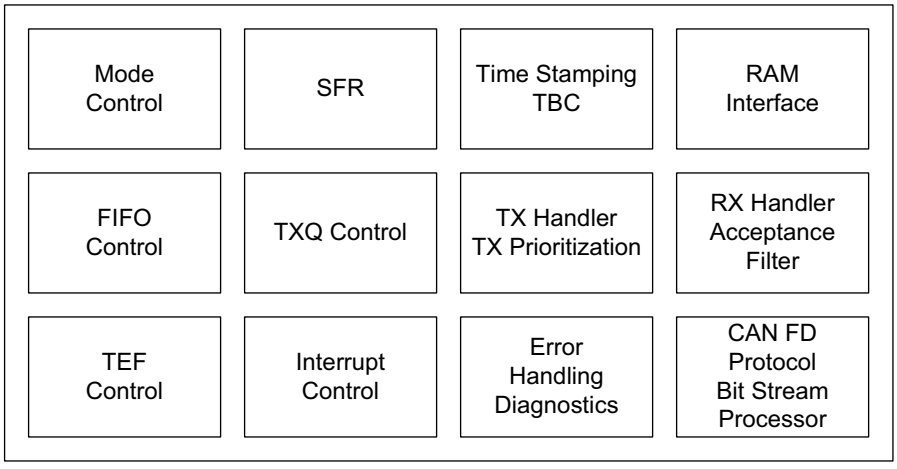
2.0 CAN FD CONTROLLER MODULE

Figure 2-1 shows the main blocks of the CAN FD Controller module:

- The CAN FD Controller module has multiple modes:
  - Configuration
  - Normal CAN FD
  - Normal CAN 2.0
  - Sleep
  - Listen Only
  - Restricted Operation
  - Internal and External Loop back modes
- The CAN FD Bit Stream Processor (BSP) implements the Medium Access Control of the CAN FD protocol described in ISO 11898-1:2015. It serializes and de-serializes the bit stream, encodes and decodes the CAN FD frames, manages the medium access, acknowledges frames, and detects and signals errors.
- The TX Handler prioritizes the messages that are requested for transmission by the Transmit FIFOs. It uses the RAM Interface to fetch the transmit data from RAM and provides it to the BSP for transmission.
- The BSP provides received messages to the RX Handler. The RX Handler uses the Acceptance Filter to filter out messages that shall be stored into Receive FIFOs. It uses the RAM Interface to store received data into RAM.
- Each FIFO can be configured either as a Transmit or Receive FIFO. The FIFO Control keeps track of the FIFO Head and Tail, and calculates the User Address. For a TX FIFO, the User Address points to the address in RAM where the data for the next transmit message shall be stored. For a RX FIFO, the User Address points to the address in RAM where the data of the next receive message shall be read. The User notifies the FIFO that a message was written to or read from RAM by incrementing the Head/Tail of the FIFO.
- The Transmit Queue (TXQ) is a special transmit FIFO that transmits the messages based on the ID of the messages stored in the queue.
- The Transmit Event FIFO (TEF) stores the message IDs of the transmitted messages.
- A free-running Time Base Counter is used to time stamp received messages. Messages in the TEF can also be time stamped.
- The CAN FD Controller module generates interrupts when new messages are received or when messages were transmitted successfully.
- The Special Function Registers (SFR) are used to control and to read the status of the CAN FD Controller module.

Note 1: This data sheet summarizes the features of the CAN FD Controller module. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “MCP25xxFD Family Reference Manual”.

FIGURE 2-1: CAN FD CONTROLLER MODULE BLOCK DIAGRAM



NOTES:

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3.0 MEMORY ORGANIZATION

Figure 3-1 illustrates the main sections of the memory and its address ranges:

- MCP2517FD Special Function Registers (SFR)
- CAN FD Controller Module SFR
- Message Memory (RAM)

The SFR are 32 bit wide. The LSB is located at the lower address, e.g., the LSB of C1CON is located at address 0x000, while its MSB is located at address 0x003.

Table 3-1 lists the MCP2517FD specific registers. The first column contains the address of the SFR.

Table 3-2 lists the registers of the CAN FD Controller Module. The first column contains the address of the SFR.

FIGURE 3-1: MEMORY MAP

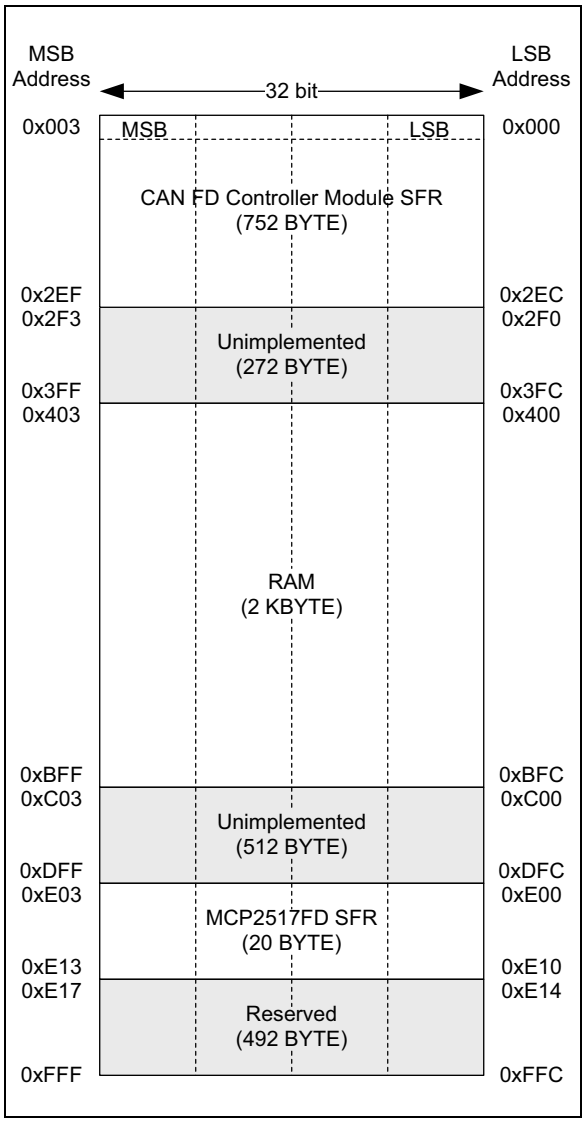

TABLE 3-1: MCP2517FD REGISTER SUMMARY

Address	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
E03	OSC	31:24	—	—	—	—	—	—	—	—
E02		23:16	—	—	—	—	—	—	—	—
E01		15:8	—	—	—	SCLKRDY	—	OSCRDY	—	PLLRDY
E00(1)		7:0	—	CLKODIV<1:0>		SCLKDIV	—	OSCDIS	—	PLLEN
	IOCON	31:24	—	INTOD	SOF	TXCANOD	—	—	PM1	PM0
		23:16	—	—	—	—	—	—	GPIO1	GPIO0
		15:8	—	—	—	—	—	—	LAT1	LAT0
E04		7:0	—	XSTBYEN	—	—	—	—	TRIS1	TRIS0
	CRC	31:24	—	—	—	—	—	—	FERRIE	CRCERRIE
		23:16	—	—	—	—	—	—	FERRIF	CRCERRIF
		15:8	CRC<15:8>							
E08		7:0	CRC<7:0>							
	ECCCON	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	PARITY<6:0>						
E0C		7:0	—	—	—	—	—	DEDIE	SECIE	ECCEN
	ECCSTAT	31:24	—	—	—	—	ERRADDR<11:8>			
		23:16	ERRADDR<7:0>							
		15:8	—	—	—	—	—	—	—	—
E10		7:0	—	—	—	—	—	DEDIF	SECIF	—

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

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TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
03	C1CON	31:24	TXBWS<3:0>				ABAT	REQOP<2:0>		
02		23:16	OPMOD<2:0>			TXQEN	STEF	SERR2LOM	ESIGM	RTXAT
01		15:8	—	—	—	BRSDIS	BUSY	WFT<1:0>		WAKFIL
00[1]		7:0	—	PXEDIS	ISOCRCEN	DNCNT<4:0>				
	C1NBTCFG	31:24	BRP<7:0>							
		23:16	TSEG1<7:0>							
		15:8	—	TSEG2<6:0>						
04		7:0	—	SJW<6:0>						
	C1DBTCFG	31:24	BRP<7:0>							
		23:16	—	—	—	TSEG1<4:0>				
		15:8	—	—	—	—	TSEG2<3:0>			
08		7:0	—	—	—	—	SJW<3:0>			
	C1TDC	31:24	—	—	—	—	—	—	EDGFLTEN	SID11EN
		23:16	—	—	—	—	—	—	TDCMOD<1:0>	
		15:8	—	TDCO<6:0>						
0C		7:0	—	—	TDCV<5:0>					
	C1TBC	31:24	TBC<31:24>							
		23:16	TBC<23:16>							
		15:8	TBC<15:8>							
10		7:0	TBC<7:0>							
	C1TSCON	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	TSRES	TSEOF	TBCEN
		15:8	—	—	—	—	—	—	TBCPRE<9:8>	
14		7:0	TBCPRE<7:0>							
	C1VEC	31:24	—	RXCODE<6:0>						
		23:16	—	TXCODE<6:0>						
		15:8	—	—	—	FILHIT<4:0>				
18		7:0	—	ICODE<6:0>						
	C1INT	31:24	IVMIE	WAKIE	CERRIE	SERRIE	RXOVIE	TXATIE	SPICRCIE	ECCIE
		23:16	—	—	—	TEFIE	MODIE	TBCIE	RXIE	TXIE
		15:8	IVMIF	WAKIF	CERRIF	SERRIF	RXOVIF	TXATIF	SPICRCIF	ECCIF
1C		7:0	—	—	—	TEFIF	MODIF	TBCIF	RXIF	TXIF
	C1RXIF	31:24	RFIF<31:24>							
		23:16	RFIF<23:16>							
		15:8	RFIF<15:8>							
20		7:0	RFIF<7:1>							—
	C1TXIF	31:24	TFIF<31:24>							
		23:16	TFIF<23:16>							
		15:8	TFIF<15:8>							
24		7:0	TFIF<7:0>							
	C1RXOVIF	31:24	RFOVIF<31:24>							
		23:16	RFOVIF<23:16>							
		15:8	RFOVIF<15:8>							
28		7:0	RFOVIF<7:1>							—
	C1TXATIF	31:24	TFATIF<31:24>							
		23:16	TFATIF<23:16>							
		15:8	TFATIF<15:8>							
2C		7:0	TFATIF<7:0>							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	C1TXREQ	31:24	TXREQ<31:24>							
		23:16	TXREQ<23:16>							
		15:8	TXREQ<15:8>							
30		7:0	TXREQ<7:0>							
	C1TREC	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	TXBO	TXBP	RXBP	TXWARN	RXWARN	EWARN
		15:8	TEC<7:0>							
34		7:0	REC<7:0>							
	C1BDIAG0	31:24	DTERRCNT<7:0>							
		23:16	DRERRCNT<7:0>							
		15:8	NTERRCNT<7:0>							
38		7:0	NRERRCNT<7:0>							
	C1BDIAG1	31:24	DLCMM	ESI	DCRCERR	DSTUFERR	DFORMERR	—	DBIT1ERR	DBIT0ERR
		23:16	TXBOERR	—	NCRCERR	NSTUFERR	NFORMERR	NACKERR	NBIT1ERR	NBIT0ERR
		15:8	EFMSGCNT<15:8>							
3C		7:0	EFMSGCNT<7:0>							
	C1TEFCON	31:24	—	—	—	FSIZE<4:0>				
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	—	—	FRESET	—	UINC
40		7:0	—	—	TEFTSEN	—	TEFOVIE	TEFFIE	TEFHIE	TEFNEIE
	C1TEFSTA	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	—	—	—	—	—
44		7:0	—	—	—	—	TEFOVIF	TEFFIF	TEFHIF	TEFNEIF
	C1TEFUA	31:24	TEFUA<31:24>							
		23:16	TEFUA<23:16>							
		15:8	TEFUA<15:8>							
48		7:0	TEFUA<7:0>							
	Reserved(2)	31:24	Reserved<31:24>							
		23:16	Reserved<23:16>							
		15:8	Reserved<15:8>							
4C		7:0	Reserved<7:0>							
	C1TXQCON	31:24	PLSIZE<2:0>			FSIZE<4:0>				
		23:16	—	TXAT<1:0>		TXPRI<4:0>				
		15:8	—	—	—	—	—	FRESET	TXREQ	UINC
50		7:0	TXEN	—	—	TXATIE	—	TXQEIE	—	TXQNIE
	C1TXQSTA	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	TXQCI<4:0>				
54		7:0	TXABT	TXLARB	TXERR	TXATIF	—	TXQEIF	—	TXQNIF
	C1TXQUA	31:24	TXQUA<31:24>							
		23:16	TXQUA<23:16>							
		15:8	TXQUA<15:8>							
58		7:0	TXQUA<7:0>							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

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TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	C1FIFOCON1	31:24	PLSIZE<2:0>			FSIZE<4:0>				
		23:16	—	TXAT<1:0>		TXPRI<4:0>				
		15:8	—	—	—	—	—	FRESET	TXREQ	UINC
5C		7:0	TXEN	RTREN	RXTSEN	TXATIE	RXOVIE	TFERFFIE	TFHRFHIE	TFNRFNIE
	C1FIFOSTA1	31:24	—	—	—	—	—	—	—	—
		23:16	—	—	—	—	—	—	—	—
		15:8	—	—	—	FIFOCI<4:0>				
60		7:0	TXABT	TXLARB	TXERR	TXATIF	RXOVIF	TFERFFIF	TFHRFHIF	TFNRFNIF
	C1FIFOUA1	31:24	FIFOUA<31:24>							
		23:16	FIFOUA<23:16>							
		15:8	FIFOUA<15:8>							
64		7:0	FIFOUA<7:0>							
68	C1FIFOCON2	31:0	same as C1FIFOCON1							
6C	C1FIFOSTA2	31:0	same as C1FIFOSTA1							
70	C1FIFOUA2	31:0	same as C1FIFOUA1							
74	C1FIFOCON3	31:0	same as C1FIFOCON1							
78	C1FIFOSTA3	31:0	same as C1FIFOSTA1							
7C	C1FIFOUA3	31:0	same as C1FIFOUA1							
80	C1FIFOCON4	31:0	same as C1FIFOCON1							
84	C1FIFOSTA4	31:0	same as C1FIFOSTA1							
88	C1FIFOUA4	31:0	same as C1FIFOUA1							
8C	C1FIFOCON5	31:0	same as C1FIFOCON1							
90	C1FIFOSTA5	31:0	same as C1FIFOSTA1							
94	C1FIFOUA5	31:0	same as C1FIFOUA1							
98	C1FIFOCON6	31:0	same as C1FIFOCON1							
9C	C1FIFOSTA6	31:0	same as C1FIFOSTA1							
A0	C1FIFOUA6	31:0	same as C1FIFOUA1							
A4	C1FIFOCON7	31:0	same as C1FIFOCON1							
A8	C1FIFOSTA7	31:0	same as C1FIFOSTA1							
AC	C1FIFOUA7	31:0	same as C1FIFOUA1							
B0	C1FIFOCON8	31:0	same as C1FIFOCON1							
B4	C1FIFOSTA8	31:0	same as C1FIFOSTA1							
B8	C1FIFOUA8	31:0	same as C1FIFOUA1							
BC	C1FIFOCON9	31:0	same as C1FIFOCON1							
C0	C1FIFOSTA9	31:0	same as C1FIFOSTA1							
C4	C1FIFOUA9	31:0	same as C1FIFOUA1							
C8	C1FIFOCON10	31:0	same as C1FIFOCON1							
CC	C1FIFOSTA10	31:0	same as C1FIFOSTA1							
D0	C1FIFOUA10	31:0	same as C1FIFOUA1							
D4	C1FIFOCON11	31:0	same as C1FIFOCON1							
D8	C1FIFOSTA11	31:0	same as C1FIFOSTA1							
DC	C1FIFOUA11	31:0	same as C1FIFOUA1							
E0	C1FIFOCON12	31:0	same as C1FIFOCON1							
E4	C1FIFOSTA12	31:0	same as C1FIFOSTA1							
E8	C1FIFOUA12	31:0	same as C1FIFOUA1							
EC	C1FIFOCON13	31:0	same as C1FIFOCON1							
F0	C1FIFOSTA13	31:0	same as C1FIFOSTA1							
F4	C1FIFOUA13	31:0	same as C1FIFOUA1							
F8	C1FIFOCON14	31:0	same as C1FIFOCON1							
FC	C1FIFOSTA14	31:0	same as C1FIFOSTA1							
100	C1FIFOUA14	31:0	same as C1FIFOUA1							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
104	C1FIFOCON15	31:0	same as C1FIFOCON1							
108	C1FIFOSTA15	31:0	same as C1FIFOSTA1							
10C	C1FIFOUA15	31:0	same as C1FIFOUA1							
110	C1FIFOCON16	31:0	same as C1FIFOCON1							
114	C1FIFOSTA16	31:0	same as C1FIFOSTA1							
118	C1FIFOUA16	31:0	same as C1FIFOUA1							
11C	C1FIFOCON17	31:0	same as C1FIFOCON1							
120	C1FIFOSTA17	31:0	same as C1FIFOSTA1							
124	C1FIFOUA17	31:0	same as C1FIFOUA1							
128	C1FIFOCON18	31:0	same as C1FIFOCON1							
12C	C1FIFOSTA18	31:0	same as C1FIFOSTA1							
130	C1FIFOUA18	31:0	same as C1FIFOUA1							
134	C1FIFOCON19	31:0	same as C1FIFOCON1							
138	C1FIFOSTA19	31:0	same as C1FIFOSTA1							
13C	C1FIFOUA19	31:0	same as C1FIFOUA1							
140	C1FIFOCON20	31:0	same as C1FIFOCON1							
144	C1FIFOSTA20	31:0	same as C1FIFOSTA1							
148	C1FIFOUA20	31:0	same as C1FIFOUA1							
14C	C1FIFOCON21	31:0	same as C1FIFOCON1							
150	C1FIFOSTA21	31:0	same as C1FIFOSTA1							
154	C1FIFOUA21	31:0	same as C1FIFOUA1							
158	C1FIFOCON22	31:0	same as C1FIFOCON1							
15C	C1FIFOSTA22	31:0	same as C1FIFOSTA1							
160	C1FIFOUA22	31:0	same as C1FIFOUA1							
164	C1FIFOCON23	31:0	same as C1FIFOCON1							
168	C1FIFOSTA23	31:0	same as C1FIFOSTA1							
16C	C1FIFOUA23	31:0	same as C1FIFOUA1							
170	C1FIFOCON24	31:0	same as C1FIFOCON1							
174	C1FIFOSTA24	31:0	same as C1FIFOSTA1							
178	C1FIFOUA24	31:0	same as C1FIFOUA1							
17C	C1FIFOCON25	31:0	same as C1FIFOCON1							
180	C1FIFOSTA25	31:0	same as C1FIFOSTA1							
184	C1FIFOUA25	31:0	same as C1FIFOUA1							
188	C1FIFOCON26	31:0	same as C1FIFOCON1							
18C	C1FIFOSTA26	31:0	same as C1FIFOSTA1							
190	C1FIFOUA26	31:0	same as C1FIFOUA1							
194	C1FIFOCON27	31:0	same as C1FIFOCON1							
198	C1FIFOSTA27	31:0	same as C1FIFOSTA1							
19C	C1FIFOUA27	31:0	same as C1FIFOUA1							
1A0	C1FIFOCON28	31:0	same as C1FIFOCON1							
1A4	C1FIFOSTA28	31:0	same as C1FIFOSTA1							
1A8	C1FIFOUA28	31:0	same as C1FIFOUA1							
1AC	C1FIFOCON29	31:0	same as C1FIFOCON1							
1B0	C1FIFOSTA29	31:0	same as C1FIFOSTA1							
1B4	C1FIFOUA29	31:0	same as C1FIFOUA1							
1B8	C1FIFOCON30	31:0	same as C1FIFOCON1							
1BC	C1FIFOSTA30	31:0	same as C1FIFOSTA1							
1C0	C1FIFOUA30	31:0	same as C1FIFOUA1							
1C4	C1FIFOCON31	31:0	same as C1FIFOCON1							
1C8	C1FIFOSTA31	31:0	same as C1FIFOSTA1							
1CC	C1FIFOUA31	31:0	same as C1FIFOUA1							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

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TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
	C1FLTCON0	31:24	FLTEN3	—	—	F3BP<4:0>				
		23:16	FLTEN2	—	—	F2BP<4:0>				
		15:8	FLTEN1	—	—	F1BP<4:0>				
1D0		7:0	FLTEN0	—	—	F0BP<4:0>				
	C1FLTCON1	31:24	FLTEN7	—	—	F7BP<4:0>				
		23:16	FLTEN6	—	—	F6BP<4:0>				
		15:8	FLTEN5	—	—	F5BP<4:0>				
1D4		7:0	FLTEN4	—	—	F4BP<4:0>				
	C1FLTCON2	31:24	FLTEN11	—	—	F11BP<4:0>				
		23:16	FLTEN10	—	—	F10BP<4:0>				
		15:8	FLTEN9	—	—	F9BP<4:0>				
1D8		7:0	FLTEN8	—	—	F8BP<4:0>				
	C1FLTCON3	31:24	FLTEN15	—	—	F15BP<4:0>				
		23:16	FLTEN14	—	—	F14BP<4:0>				
		15:8	FLTEN13	—	—	F13BP<4:0>				
1DC		7:0	FLTEN12	—	—	F12BP<4:0>				
	C1FLTCON4	31:24	FLTEN19	—	—	F19BP<4:0>				
		23:16	FLTEN18	—	—	F18BP<4:0>				
		15:8	FLTEN17	—	—	F17BP<4:0>				
1E0		7:0	FLTEN16	—	—	F16BP<4:0>				
	C1FLTCON5	31:24	FLTEN23	—	—	F23BP<4:0>				
		23:16	FLTEN22	—	—	F22BP<4:0>				
		15:8	FLTEN21	—	—	F21BP<4:0>				
1E4		7:0	FLTEN20	—	—	F20BP<4:0>				
	C1FLTCON6	31:24	FLTEN27	—	—	F27BP<4:0>				
		23:16	FLTEN26	—	—	F26BP<4:0>				
		15:8	FLTEN25	—	—	F25BP<4:0>				
1E8		7:0	FLTEN24	—	—	F24BP<4:0>				
	C1FLTCON7	31:24	FLTEN31	—	—	F31BP<4:0>				
		23:16	FLTEN30	—	—	F30BP<4:0>				
		15:8	FLTEN29	—	—	F29BP<4:0>				
1EC		7:0	FLTEN28	—	—	F28BP<4:0>				
	C1FLTOBJ0	31:24	—	EXIDE	SID11	EID<17:6>				
		23:16	EID<12:5>							
		15:8	EID<4:0>					SID<10:8>		
1F0		7:0	SID<7:0>							
	C1MASK0	31:24	—	MIDE	MSID11	MEID<17:6>				
		23:16	MEID<12:5>							
		15:8	MEID<4:0>					MSID<10:8>		
1F4		7:0	MSID<7:0>							
1F8	C1FLTOBJ1	31:0	same as C1FLTOBJ0							
1FC	C1MASK1	31:0	same as C1MASK0							
200	C1FLTOBJ2	31:0	same as C1FLTOBJ0							
204	C1MASK2	31:0	same as C1MASK0							
208	C1FLTOBJ3	31:0	same as C1FLTOBJ0							
20C	C1MASK3	31:0	same as C1MASK0							
210	C1FLTOBJ4	31:0	same as C1FLTOBJ0							
214	C1MASK4	31:0	same as C1MASK0							
218	C1FLTOBJ5	31:0	same as C1FLTOBJ0							
21C	C1MASK5	31:0	same as C1MASK0							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

TABLE 3-2: CAN FD CONTROLLER MODULE REGISTER SUMMARY (CONTINUED)

Addr.	Name		Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
220	C1FLTOBJ6	31:0	same as C1FLTOBJ0							
224	C1MASK6	31:0	same as C1MASK0							
228	C1FLTOBJ7	31:0	same as C1FLTOBJ0							
22C	C1MASK7	31:0	same as C1MASK0							
230	C1FLTOBJ8	31:0	same as C1FLTOBJ0							
234	C1MASK8	31:0	same as C1MASK0							
238	C1FLTOBJ9	31:0	same as C1FLTOBJ0							
23C	C1MASK9	31:0	same as C1MASK0							
240	C1FLTOBJ10	31:0	same as C1FLTOBJ0							
244	C1MASK10	31:0	same as C1MASK0							
248	C1FLTOBJ11	31:0	same as C1FLTOBJ0							
24C	C1MASK11	31:0	same as C1MASK0							
250	C1FLTOBJ12	31:0	same as C1FLTOBJ0							
254	C1MASK12	31:0	same as C1MASK0							
258	C1FLTOBJ13	31:0	same as C1FLTOBJ0							
25C	C1MASK13	31:0	same as C1MASK0							
260	C1FLTOBJ14	31:0	same as C1FLTOBJ0							
264	C1MASK14	31:0	same as C1MASK0							
268	C1FLTOBJ15	31:0	same as C1FLTOBJ0							
26C	C1MASK15	31:0	same as C1MASK0							
270	C1FLTOBJ16	31:0	same as C1FLTOBJ0							
274	C1MASK16	31:0	same as C1MASK0							
278	C1FLTOBJ17	31:0	same as C1FLTOBJ0							
27C	C1MASK17	31:0	same as C1MASK0							
280	C1FLTOBJ18	31:0	same as C1FLTOBJ0							
284	C1MASK18	31:0	same as C1MASK0							
288	C1FLTOBJ19	31:0	same as C1FLTOBJ0							
28C	C1MASK19	31:0	same as C1MASK0							
290	C1FLTOBJ20	31:0	same as C1FLTOBJ0							
294	C1MASK20	31:0	same as C1MASK0							
298	C1FLTOBJ21	31:0	same as C1FLTOBJ0							
29C	C1MASK21	31:0	same as C1MASK0							
2A0	C1FLTOBJ22	31:0	same as C1FLTOBJ0							
2A4	C1MASK22	31:0	same as C1MASK0							
2A8	C1FLTOBJ23	31:0	same as C1FLTOBJ0							
2AC	C1MASK23	31:0	same as C1MASK0							
2B0	C1FLTOBJ24	31:0	same as C1FLTOBJ0							
2B4	C1MASK24	31:0	same as C1MASK0							
2B8	C1FLTOBJ25	31:0	same as C1FLTOBJ0							
2BC	C1MASK25	31:0	same as C1MASK0							
2C0	C1FLTOBJ26	31:0	same as C1FLTOBJ0							
2C4	C1MASK26	31:0	same as C1MASK0							
2C8	C1FLTOBJ27	31:0	same as C1FLTOBJ0							
2CC	C1MASK27	31:0	same as C1MASK0							
2D0	C1FLTOBJ28	31:0	same as C1FLTOBJ0							
2D4	C1MASK28	31:0	same as C1MASK0							
2D8	C1FLTOBJ29	31:0	same as C1FLTOBJ0							
2DC	C1MASK29	31:0	same as C1MASK0							
2E0	C1FLTOBJ30	31:0	same as C1FLTOBJ0							
2E4	C1MASK30	31:0	same as C1MASK0							
2E8	C1FLTOBJ31	31:0	same as C1FLTOBJ0							
2EC	C1MASK31	31:0	same as C1MASK0							

Note 1: The lower order byte of the 32-bit register resides at the low-order address.

2: Reserved register reads 0.

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3.1 MCP2517FD Specific Registers

- Register 3-1: OSC
- Register 3-2: IOCON
- Register 3-3: CRC
- Register 3-4: ECCCON
- Register 3-5: ECCSTAT

TABLE 3-3: REGISTER LEGEND

Symbol	Description	Symbol	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as '0'	1	Bit is set at Reset
S	Settable bit	0	Bit is cleared at Reset
C	Clearable bit	x	Bit is unknown at Reset

EXAMPLE 3-1:

R/W - 0 indicates the bit is both readable and writable, and reads '0' after a Reset.

REGISTER 3-1: OSC – MCP2517FD OSCILLATOR CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	U-0	U-0	R-0	U-0	R-0	U-0	R-0
—	—	—	SCLKRDY	—	OSCRDY	—	PLLRDY
bit 15							bit 8

U-0	R/W-1	R/W-1	R/W-0	U-0	HS/C-0	U-0	R/W-0
—	CLKODIV<1:0>		SCLKDIV(1)	—	OSCDIS(2)	—	PLLEN(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12 **SCLKRDY:** Synchronized SCLKDIV bit
1 = SCLKDIV 1
0 = SCLKDIV 0

bit 11 **Unimplemented:** Read as ‘0’

bit 10 **OSCRDY:** Clock Ready
1 = Clock is running and stable
0 = Clock not ready or off

bit 9 **Unimplemented:** Read as ‘0’

bit 8 **PLLRDY:** PLL Ready
1 = PLL Locked
0 = PLL not ready

bit 7 **Unimplemented:** Read as ‘0’

bit 6-5 **CLKODIV<1:0>:** Clock Output Divisor
11 =CLKO is divided by 10
10 =CLKO is divided by 4
01 =CLKO is divided by 2
00 =CLKO is divided by 1

bit 4 **SCLKDIV:** System Clock Divisor(1)
1 = SCLK is divided by 2
0 = SCLK is divided by 1

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **OSCDIS:** Clock (Oscillator) Disable(2)
1 = Clock disabled, the device is in Sleep mode.
0 = Enable Clock

Note 1: This bit can only be modified in Configuration mode.
2: Clearing OSCDIS while in Sleep mode will wake-up the device and put it back in Configuration mode.

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REGISTER 3-1: OSC – MCP2517FD OSCILLATOR CONTROL REGISTER (CONTINUED)

bit 1 **Unimplemented:** Read as '0'

bit 0 **PLLEN:** PLL Enable(1)

1 = System Clock from 10x PLL

0 = System Clock comes directly from XTAL oscillator

Note 1: This bit can only be modified in Configuration mode.

2: Clearing OSCDIS while in Sleep mode will wake-up the device and put it back in Configuration mode.

REGISTER 3-2: IOCON – INPUT/OUTPUT CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-1	R/W-1
—	INTOD	SOF	TXCANOD	—	—	PM1	PM0
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
—	—	—	—	—	—	GPIO1	GPIO0
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x
—	—	—	—	—	—	LAT1	LAT0
bit 15							bit 8

U-0	R/W-0	U-0	U-0	U-0	U-0	R/W-1	R/W-1
—	XSTBYEN	—	—	—	—	TRIS1(1)	TRIS0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30 **INTOD:** Interrupt pins Open Drain Mode
- 1 = Open Drain Output
- 0 = Push/Pull Output

bit 29 **SOF:** Start-Of-Frame signal
- 1 = SOF signal on CLKO pin
- 0 = Clock on CLKO pin

bit 28 **TXCANOD:** TXCAN Open Drain Mode
- 1 = Open Drain Output
- 0 = Push/Pull Output

bit 27-26 **Unimplemented:** Read as '0'

bit 25 **PM1:** GPIO Pin Mode
- 1 = Pin is used as GPIO1
- 0 = Interrupt Pin $\overline{INT1}$, asserted when CiINT.RXIF and RXIE are set

bit 24 **PM0:** GPIO Pin Mode
- 1 = Pin is used as GPIO0
- 0 = Interrupt Pin $\overline{INT0}$, asserted when CiINT.TXIF and TXIE are set

bit 23-18 **Unimplemented:** Read as '0'

bit 17 **GPIO1:** GPIO1 Status
- 1 = $V_{GPIO1} > V_{IH}$
- 0 = $V_{GPIO1} < V_{IL}$

bit 16 **GPIO0:** GPIO0 Status
- 1 = $V_{GPIO0} > V_{IH}$
- 0 = $V_{GPIO0} < V_{IL}$

bit 15-10 **Unimplemented:** Read as '0'

Note 1: If PMx = 0, TRISx will be ignored and the pin will be an output.

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REGISTER 3-2: IOCON – INPUT/OUTPUT CONTROL REGISTER (CONTINUED)

bit 9	**LAT1:** GPIO1 Latch 1 = Drive Pin High 0 = Drive Pin Low
bit 8	**LAT0:** GPIO0 Latch 1 = Drive Pin High 0 = Drive Pin Low
bit 7	**Unimplemented:** Read as '0'
bit 6	**XSTBYEN:** Enable Transceiver Standby Pin Control 1 = XSTBY control enabled 0 = XSTBY control disabled
bit 5-2	**Unimplemented:** Read as '0'
bit 1	**TRIS1:** GPIO1 Data Direction(1) 1 = Input Pin 0 = Output Pin
bit 0	**TRIS0:** GPIO0 Data Direction(1) 1 = Input Pin 0 = Output Pin

Note 1: If PMx = 0, TRISx will be ignored and the pin will be an output.

REGISTER 3-3: CRC – CRC REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	FERRIE	CRCERRIE
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	HS/C-0	HS/C-0
—	—	—	—	—	—	FERRIF	CRCERRIF
bit 23							bit 16

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CRC<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CRC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-26 **Unimplemented:** Read as ‘0’

bit 25 **FERRIE:** CRC Command Format Error Interrupt Enable

bit 24 **CRCERRIE:** CRC Error Interrupt Enable

bit 23-18 **Unimplemented:** Read as ‘0’

bit 17 **FERRIF:** CRC Command Format Error Interrupt Flag

1 = Number of Bytes mismatch during “SPI with CRC” command occurred
0 = No SPI CRC command format error occurred

bit 16 **CRCERRIF:** CRC Error Interrupt Flag

1 = CRC mismatch occurred
0 = No CRC error has occurred

bit 15-0 **CRC<15:0>:** Cycle Redundancy Check from last CRC mismatch

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REGISTER 3-4: ECCCON – ECC CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PARITY<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DEDIE	SECIE	ECCEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-15 **Unimplemented:** Read as ‘0’

bit 14-8 **PARITY<6:0>:** Parity bits used during write to RAM when ECC is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **DEDIE:** Double Error Detection Interrupt Enable Flag

bit 1 **SECIE:** Single Error Correction Interrupt Enable Flag

bit 0 **ECCEN:** ECC Enable

1 = ECC enabled
0 = ECC disabled

REGISTER 3-5: ECCSTAT – ECC STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ERRADDR<11:8>			
bit 31							bit 24

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ERRADDR<7:0>							
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	HS/C-0	HS/C-0	U-0
—	—	—	—	—	DEDIF	SECIF	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **Unimplemented:** Read as ‘0’

bit 27-16 **ERRADDR<11:0>:** Address where last ECC error occurred

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2 **DEDIF:** Double Error Detection Interrupt Flag
1 = Double Error was detected
0 = No Double Error Detection occurred

bit 1 **SECIF:** Single Error Correction Interrupt Flag
1 = Single Error was corrected
0 = No Single Error occurred

bit 0 **Unimplemented:** Read as ‘0’

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3.2 CAN FD Controller Module Registers

Configuration Registers

- Register 3-6: CiCON
- Register 3-7: CiNBTCFG
- Register 3-8: CiDBTCFG
- Register 3-9: CiTDC
- Register 3-10: CiTBC
- Register 3-11: CiTSCON

Interrupt and Status Registers

- Register 3-12: CiVEC
- Register 3-13: CiINT
- Register 3-14: CiRXIF
- Register 3-15: CiRXOVIF
- Register 3-16: CiTXIF
- Register 3-17: CiTXATIF
- Register 3-18: CiTXREQ

Error and Diagnostic Registers

- Register 3-19: CiTREC
- Register 3-20: CiBDIAG0
- Register 3-21: CiBDIAG1

Fifo Control and Status Registers

- Register 3-22: CiTEFCON
- Register 3-23: CiTEFSTA
- Register 3-24: CiTEFUA
- Register 3-25: CiTXQCON
- Register 3-26: CiTXQSTA
- Register 3-27: CiTXQUA
- Register 3-28: CiFIFOCONm – m = 1 to 31
- Register 3-29: CiFIFOSTAm – m = 1 to 31
- Register 3-30: CiFIFOUAm – m = 1 to 31

Filter Configuration and Control Registers

- Register 3-31: CiFLTCONm – m = 0 to 7
- Register 3-32: CiFLTOBJm – m = 0 to 31
- Register 3-33: CiMASKm – m = 0 to 31

Note: The ‘i’ shown in the register identifier denotes CANi, e.g., C1CON. The MCP2517FD contains one CAN FD Controller Module.

TABLE 3-4: REGISTER LEGEND

Sym	Description	Sym	Description
R	Readable bit	HC	Cleared by Hardware only
W	Writable bit	HS	Set by Hardware only
U	Unimplemented bit, read as ‘0’	1	Bit is set at Reset
S	Settable bit	0	Bit is cleared at Reset
C	Clearable bit	x	Bit is unknown at Reset

EXAMPLE 3-2:

R/W - 0 indicates the bit is both readable and writable, and reads ‘0’ after a Reset.

REGISTER 3-6: CiCON – CAN CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
TXBWS<3:0>				ABAT	REQOP<2:0>		
bit 31							bit 24

R-1	R-0	R-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
OPMOD<2:0>			TXQEN(1)	STEF(1)	SERR2LOM(1)	ESIGM(1)	RTXAT(1)
bit 23							bit 16

U-0	U-0	U-0	R/W-0	R-0	R/W-1	R/W-1	R/W-1
—	—	—	BRSDIS	BUSY	WFT<1:0>		WAKFIL(1)
bit 15							bit 8

U-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PXEDIS(1)	ISOCRCEN(1)	DNCNT<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 31-28 **TXBWS<3:0>**: Transmit Bandwidth Sharing bits
Delay between two consecutive transmissions (in arbitration bit times)
0000 = No delay
0001 = 2
0010 = 4
0011 = 8
0100 = 16
0101 = 32
0110 = 64
0111 = 128
1000 = 256
1001 = 512
1010 = 1024
1011 = 2048
1111–1100 = 4096

bit 27 **ABAT**: Abort All Pending Transmissions bit
1 = Signal all transmit FIFOs to abort transmission
0 = Module will clear this bit when all transmissions were aborted

bit 26-24 **REQOP<2:0>**: Request Operation Mode bits
000 = Set Normal CAN FD mode; supports mixing of CAN FD and Classic CAN 2.0 frames
001 = Set Sleep mode
010 = Set Internal Loopback mode
011 = Set Listen Only mode
100 = Set Configuration mode
101 = Set External Loopback mode
110 = Set Normal CAN 2.0 mode; possible error frames on CAN FD frames
111 = Set Restricted Operation mode

Note 1: These bits can only be modified in Configuration mode.

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REGISTER 3-6: CiCON – CAN CONTROL REGISTER (CONTINUED)

bit 23-21 **OPMOD<2:0>**: Operation Mode Status bits
000 = Module is in Normal CAN FD mode; supports mixing of CAN FD and Classic CAN 2.0 frames
001 = Module is in Sleep mode
010 = Module is in Internal Loopback mode
011 = Module is in Listen Only mode
100 = Module is in Configuration mode
101 = Module is in External Loopback mode
110 = Module is Normal CAN 2.0 mode; possible error frames on CAN FD frames
111 = Module is Restricted Operation mode

bit 20 **TXQEN**: Enable Transmit Queue bit(1)
1 = Enables TXQ and reserves space in RAM
0 = Don't reserve space in RAM for TXQ

bit 19 **STEF**: Store in Transmit Event FIFO bit(1)
1 = Saves transmitted messages in TEF and reserves space in RAM
0 = Don't save transmitted messages in TEF

bit 18 **SERR2LOM**: Transition to Listen Only Mode on System Error bit(1)
1 = Transition to Listen Only Mode
0 = Transition to Restricted Operation Mode

bit 17 **ESIGM**: Transmit ESI in Gateway Mode bit(1)
1 = ESI is transmitted recessive when ESI of message is high or CAN controller error passive
0 = ESI reflects error status of CAN controller

bit 16 **RTXAT**: Restrict Retransmission Attempts bit(1)
1 = Restricted retransmission attempts, CiFIFOCONm.TXAT is used
0 = Unlimited number of retransmission attempts, CiFIFOCONm.TXAT will be ignored

bit 15-13 **Unimplemented**: Read as '0'

bit 12 **BRSDIS**: Bit Rate Switching Disable bit
1 = Bit Rate Switching is Disabled, regardless of BRS in the Transmit Message Object
0 = Bit Rate Switching depends on BRS in the Transmit Message Object

bit 11 **BUSY**: CAN Module is Busy bit
1 = The CAN module is transmitting or receiving a message
0 = The CAN module is inactive

bit 10-9 **WFT<1:0>**: Selectable Wake-up Filter Time bits
00 = T00FILTER
01 = T01FILTER
10 = T10FILTER
11 = T11FILTER

Note: Please refer to Table 7-5.

bit 8 **WAKFIL**: Enable CAN Bus Line Wake-up Filter bit(1)
1 = Use CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 7 **Unimplemented**: Read as '0'

bit 6 **PXEDIS**: Protocol Exception Event Detection Disabled bit(1)
A recessive "res bit" following a recessive FDF bit is called a Protocol Exception.
1 = Protocol Exception is treated as a Form Error.
0 = If a Protocol Exception is detected, the CAN FD Controller Module will enter Bus Integrating state.

bit 5 **ISOCRCEN**: Enable ISO CRC in CAN FD Frames bit(1)
1 = Include Stuff Bit Count in CRC Field and use Non-Zero CRC Initialization Vector according to ISO 11898-1:2015
0 = Do NOT include Stuff Bit Count in CRC Field and use CRC Initialization Vector with all zeros

Note 1: These bits can only be modified in Configuration mode.