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MCP2542FD/4FD, MCP2542WFD/4WFD

CAN FD Transceiver with Wake-Up Pattern (WUP) Option

Features

- Supports CAN 2.0 and CAN with Flexible Data Rate (CAN FD) Physical Layer Transceiver Requirements
- Optimized for CAN FD at 2, 5 and 8 Mbps Operation
  - Maximum propagation delay: 120 ns
  - Loop delay symmetry: -10%/+10% (2 Mbps)
- MCP2542FD/4FD:
  - Wake-up on CAN activity, 3.6 µs filter time
- MCP2542WFD/4WFD:
  - Wake-up on Pattern (WUP), as specified in ISO11898-2:2015, 3.6 µs activity filter time
- Implements ISO11898-2:2003, ISO11898-5:2007, and ISO/DIS11898-2:2015
- Qualification: AEC-Q100 Rev. G, Grade 0 (-40°C to +150°C)
- Very Low Standby Current (4 µA, typical)
- V_{IO} Supply Pin to Interface Directly to CAN Controllers and Microcontrollers with 1.8V to 5V I/O
- CAN Bus Pins are Disconnected when Device is Unpowered
  - An unpowered node or brown-out event will not load the CAN bus
  - Device is unpowered if V_{DD} or V_{IO} drop below its POR level
- Detection of Ground Fault:
  - Permanent Dominant detection on T_{XD}
  - Permanent Dominant detection on bus
- Automatic Thermal Shutdown Protection
- Suitable for 12V and 24V Systems
- Meets or Exceeds Stringent Automotive Design Requirements Including "*Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications*", Version 1.3, May 2012
  - Conducted emissions @ 2 Mbps with Common-Mode Choke (CMC)
  - Direct Power Injection (DPI) @ 2 Mbps with CMC
- Meets SAE J2962/2 "*Communication Transceiver Qualification Requirements - CAN*"
  - Radiated emissions @ 2 Mbps without a CMC
- High Electrostatic Discharge (ESD) Protection on CANH and CANL, meeting IEC61000-4-2 up to ±13 kV
- Temperature ranges:
  - Extended (E): -40°C to +125°C
  - High (H): -40°C to +150°C

Description

The MCP2542FD/4FD and MCP2542WFD/4WFD CAN transceiver family is designed for high-speed CAN FD applications up to 8 Mbps communication speed. The maximum propagation delay was improved to support longer bus length.

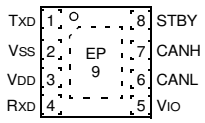
The device meets the automotive requirements for CAN FD bit rates exceeding 2 Mbps, low quiescent current, electromagnetic compatibility (EMC) and electrostatic discharge (ESD).

Applications

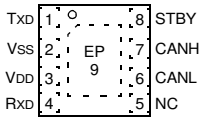
CAN 2.0 and CAN FD networks in Automotive, Industrial, Aerospace, Medical, and Consumer applications.

Package Types

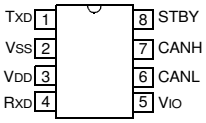
MCP2542FD
MCP2542WFD
3x3 DFN*



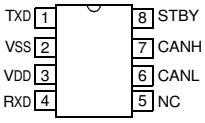
MCP2544FD
MCP2544WFD
3x3 DFN*



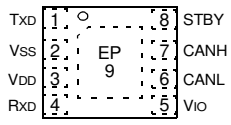
MCP2542FD
MCP2542WFD
8-Lead SOIC



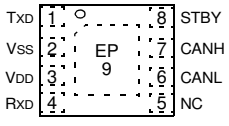
MCP2544FD
MCP2544WFD
8-Lead SOIC



MCP2542FD
MCP2542WFD
2x3 TDFN*



MCP2544FD
MCP2544WFD
2x3 TDFN*



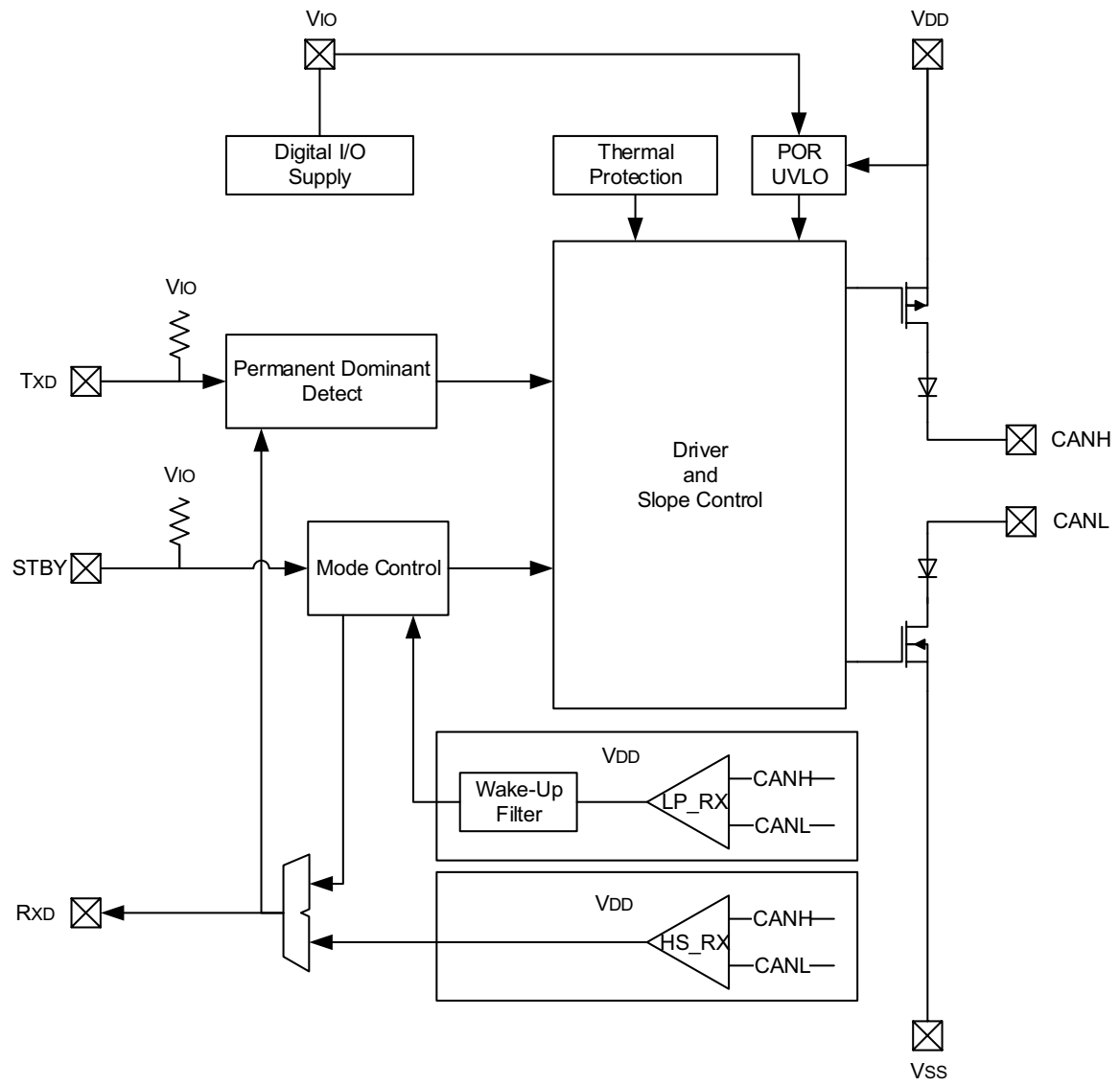
* Includes Exposed Thermal Pad (EP); see Table 1-1.

MCP2542FD/4FD, MCP2542WFD/4WFD Family Members

Device	V_{IO} pin	WUP	Description
MCP2542FD	Yes	No	
MCP2544FD	No	No	Internal level shifter on digital I/O pins
MCP2542WFD	Yes	Yes	Wake-Up on Pattern (see **Section 1.6.5**)
MCP2544WFD	No	Yes	Internal level shifter on digital I/O pins; Wake-Up on Pattern

Note: For ordering information, see the **Product Identification System** section.

Block Diagram



Note 1: There is one receiver implemented. The receiver can operate in Low-Power or High-Speed mode.

2: Only MCP2542FD and MCP2542WFD have the V_{IO} pin.

3: In the MCP2544FD and MCP2544WFD, the supply for the digital I/O is internally connected to V_{DD}.

1.0 DEVICE OVERVIEW

The MCP2542FD/4FD and MCP2542WFD/4WFD devices serve as the interface between a CAN protocol controller and the physical bus. The devices provide differential transmit and receive capability for the CAN protocol controller. The devices are fully compatible with the ISO11898-2 and ISO11898-5 standards, and with the ISO/DIS11898-2:2015 working draft.

Excellent Loop Delay Symmetry supports data rates up to 8 Mbps for CAN FD. The maximum propagation delay was improved to support longer bus length.

Typically, each node in a CAN system must have a device to convert the digital signals generated by a CAN controller to signals suitable for transmission over the bus cabling (differential output). It also provides a buffer between the CAN controller and the high-voltage spikes that can be generated on the CAN bus by outside sources.

The MCP2542FD/4FD wakes up on CAN activity (basic wake-up). The CAN activity filter time is 3.6 µs maximum.

The MCP2542WFD/4WFD wakes up after receiving two consecutive dominant states separated by a recessive state: WUP. The minimum duration of each dominant and recessive state is t_{FILTER}. The complete WUP has to be detected within $t_{WAKE(TO)}$.

1.1 Transmitter Function

The CAN bus has two states: Dominant and Recessive. A Dominant state occurs when the differential voltage between CANH and CANL is greater than $V_{DIFF(D)(I)}$. A Recessive state occurs when the differential voltage is less than $V_{DIFF(R)(I)}$. The Dominant and Recessive states correspond to the Low and High states of the TXD input pin, respectively. However, a Dominant state initiated by another CAN node will override a Recessive state on the CAN bus.

1.2 Receiver Function

In Normal mode, the RXD output pin reflects the differential bus voltage between CANH and CANL. The Low and High states of the RXD output pin correspond to the Dominant and Recessive states of the CAN bus, respectively.

1.3 Internal Protection

CANH and CANL are protected against battery short circuits and electrical transients that can occur on the CAN bus. This feature prevents destruction of the transmitter output stage during such a fault condition.

The device is further protected from excessive current loading by thermal shutdown circuitry that disables the output drivers when the junction temperature exceeds a nominal limit of +175°C.

All other parts of the chip remain operational, and the chip temperature is lowered due to the decreased power dissipation in the transmitter outputs. This protection is essential to protect against bus line short-circuit-induced damage. Thermal protection is only active during Normal mode.

1.4 Permanent Dominant Detection

The MCP2542FD/4FD and MCP2542WFD/4WFD device prevents two conditions:

- Permanent Dominant condition on TXD
- Permanent Dominant condition on the bus

In Normal mode, if the MCP2542FD/4FD and MCP2542WFD/4WFD detects an extended Low state on the TXD input, it will disable the CANH and CANL output drivers in order to prevent the corruption of data on the CAN bus. The drivers will remain disabled until TXD goes High. The high-speed receiver is active and data on the CAN bus is received on RXD.

In Standby mode, if the MCP2542FD/4FD and MCP2542WFD/4WFD detects an extended dominant condition on the bus, it will set the RXD pin to a Recessive state. This allows the attached controller to go to Low-Power mode until the dominant issue is corrected. RXD is latched High until a Recessive state is detected on the bus and the Wake-Up function is enabled again.

1.5 Power-On Reset (POR) and Undervoltage Detection

The MCP2542FD/4FD and MCP2542WFD/4WFD have POR detection on both supply pins: V_{DD} and V_{IO}. Typical POR thresholds to deassert the reset are 1.2V and 3.0V for V_{IO} and V_{DD}, respectively.

When the device is powered on, CANH and CANL remain in a high-impedance state until V_{DD} exceeds its undervoltage level. Once powered on, CANH and CANL will enter a high-impedance state if the voltage level at V_{DD} drops below the undervoltage level, providing voltage brown-out protection during normal operation.

In Normal mode, the receiver output is forced to Recessive state during an undervoltage condition on V_{DD}. In Standby mode, the low-power receiver is designed to work down to 1.7V V_{IO}. Therefore, the low-power receiver remains operational down to V_{PORL} on V_{DD} (MCP2544FD and MCP2544WFD). The MCP2542FD and MCP2542WFD transfers data to the RXD pin down to 1.7V on the V_{IO} supply.

1.6 Mode Control

The main difference between the MCP2542FD/4FD and MCP2542WFD/4WFD is the wake-up method.

Figure 1-1 shows the state diagram of the MCP2542FD/4FD. The devices wake up on CAN activity.

Figure 1-2 shows the state diagram of the MCP2542WFD/4WFD. The devices wake up on a WUP.

1.6.1 UNPOWERED MODE (POR)

The MCP2542FD/4FD and MCP2542WFD/4WFD enter Unpowered mode under the following conditions:

- After powering up the device, or
- If V_{DD} drops below V_{PORL}, or
- If V_{IO} drops below V_{PORL_VIO}.

In Unpowered mode, the CAN bus will be biased to ground using a high impedance. The MCP2542FD/4FD and MCP2542WFD/4WFD are not able to communicate on the bus or detect a wake-up event.

1.6.2 WAKE MODE

The MCP2542FD/4FD and MCP2542WFD/4WFD transitions from Unpowered mode to Wake mode when V_{DD} and V_{IO} are above their PORH levels. From Normal mode, the device will also enter Wake mode if V_{DD} is smaller than V_{UVL}, or if the band gap output voltage is not within valid range. Additionally, the device will transition from Standby mode to Wake mode if STBY is pulled Low.

In Wake mode, the CAN bus is biased to ground and RXD is always high.

1.6.3 NORMAL MODE

When V_{DD} exceeds V_{UVH}, the band gap is within valid range and TXD is High, the device transitions into Normal mode. During POR, when the microcontroller powers up, the TXD pin could be unintentionally pulled down by the microcontroller powering up. To avoid driving the bus during a POR of the microcontroller, the transceiver proceeds to Normal mode only after TXD is high.

In Normal mode, the driver block is operational and can drive the bus pins. The slopes of the output signals on CANH and CANL are optimized to reduce Electromagnetic Emissions (EME). The CAN bus is biased to $V_{DD}/2$.

The high-speed differential receiver is active.

1.6.4 STANDBY MODE

The device may be placed in Standby mode by applying a high level to the STBY pin. In Standby mode, the transmitter and the high-speed part of the receiver are switched off to minimize power consumption.

The low-power receiver and the wake-up block are enabled in order to monitor the bus for activity. The CAN bus is biased to ground.

The RXD pin remains HIGH until a wake-up event has occurred.

The MCP2542FD/4FD uses Basic Wake-Up: one dominant phase for a minimum time of t_{FILTER} will wake up the device.

The MCP2542WFD/4WFD will only wake up if it detects a complete WUP. The WUP method is described in the next section.

After a wake-up event was detected, the CAN controller gets interrupted by a negative edge on the RXD pin.

The CAN controller must put the MCP2542FD/4FD and MCP2542WFD/4WFD back into Normal mode by deasserting the STBY pin in order to enable high-speed data communication.

The CAN bus Wake-Up function requires both supply voltages, V_{DD} and V_{IO}, to be in valid range.

1.6.5 REMOTE WAKE-UP VIA CAN BUS (WUP)

The MCP2542WFD/4WFD wakes up from Standby/Silent mode when a dedicated wake-up pattern (WUP) is detected on the CAN bus. The wake-up pattern is specified in ISO11898-6 and ISO/DIS11898-2:2015 (see Figure 1-2 and Figure 2-11).

The Wake-Up Pattern consists of three events:

- a Dominant phase of at least t_{FILTER}, followed by
- a Recessive phase of at least t_{FILTER}, followed by
- a Dominant phase of at least t_{FILTER}

The complete pattern must be received within $t_{WAKE(TO)}$. Otherwise, the internal wake-up logic is reset and the complete wake-up pattern must be retransmitted in order to trigger a wake-up event.

FIGURE 1-1: MCP2542FD/4FD STATE DIAGRAM: BASIC WAKE-UP

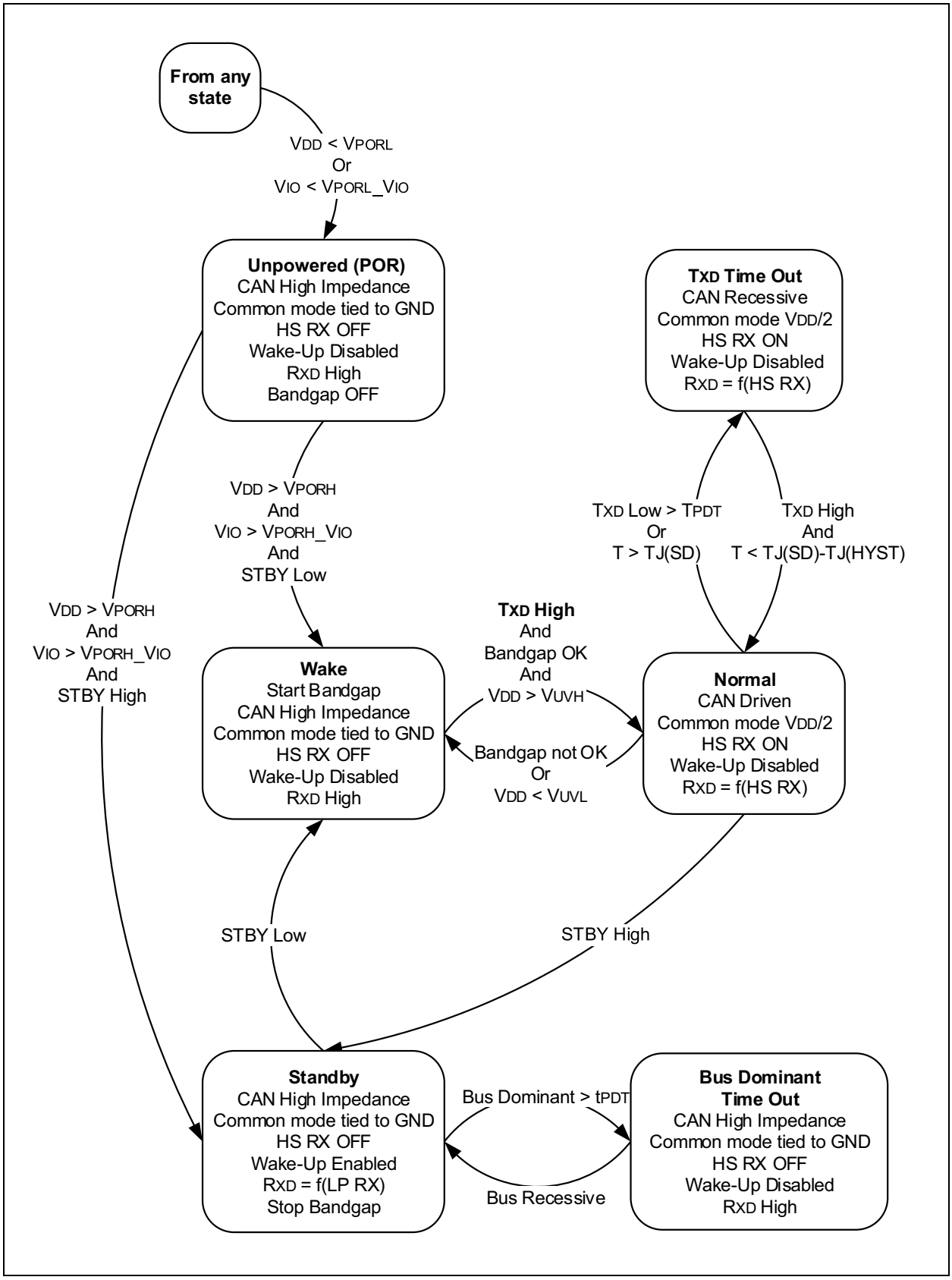
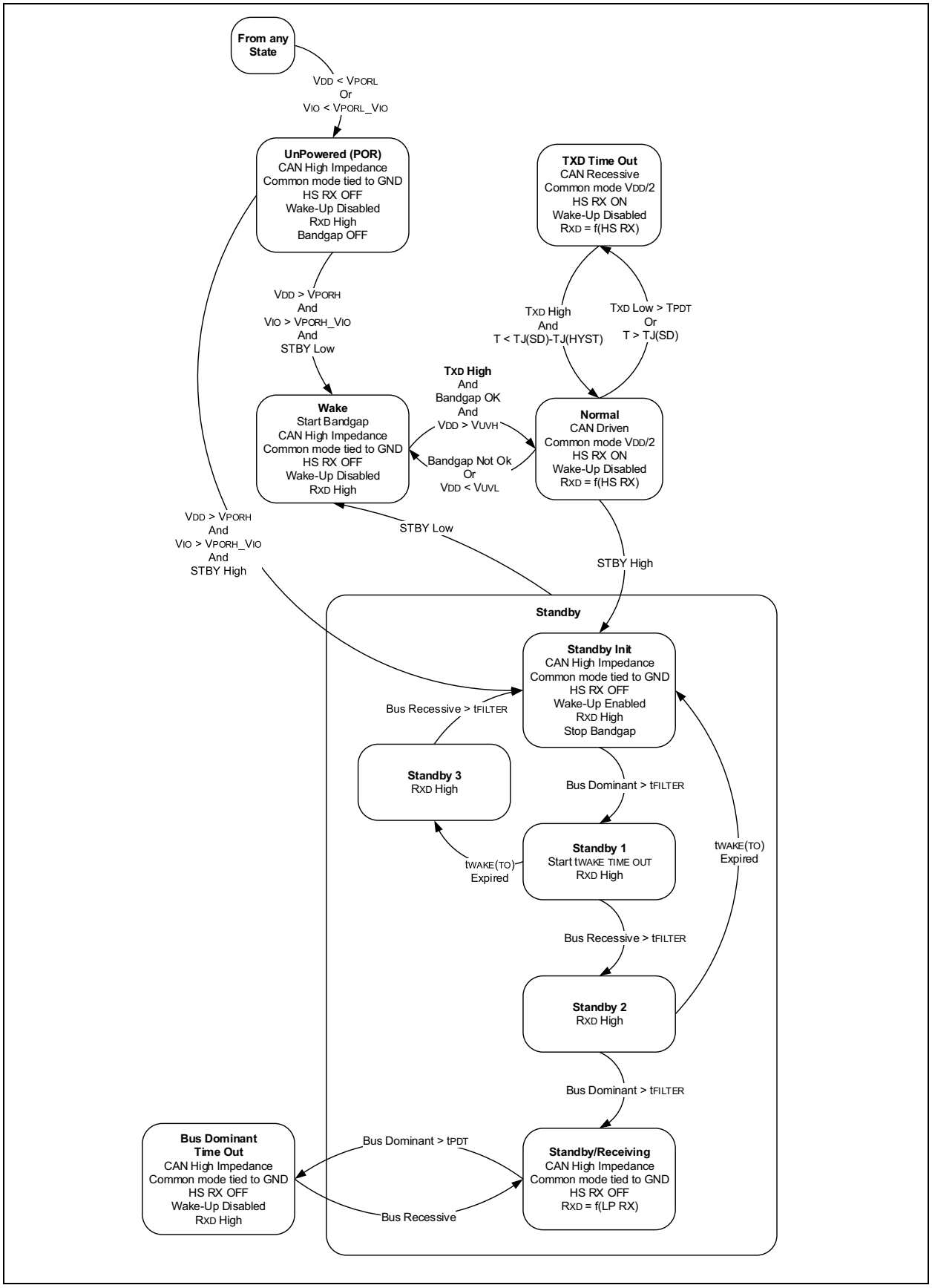


FIGURE 1-2: MCP2542WFD/4WFD STATE DIAGRAM: WAKE-UP PATTERN



1.7 Pin Descriptions

The description of the pins are listed in Table 1-1.

TABLE 1-1: MCP2542/4FD AND MCP2542/4WFD PIN DESCRIPTIONS

MCP2542FD MCP2542WFD 3x3 DFN, 2x3TDFN	MCP2542FD MCP2542WFD SOIC	MCP2544FD MCP2544WFD 3x3 DFN, 2x3TDFN	MCP2544FD MCP2544WFD SOIC	Symbol	Pin Function
1	1	1	1	TXD	Transmit Data Input
2	2	2	2	VSS	Ground
3	3	3	3	VDD	Supply Voltage
4	4	4	4	RXD	Receive Data Output
—	—	5	5	NC	No Connect
5	5	—	—	VIO	Digital I/O Supply Pin
6	6	6	6	CANL	CAN Low-Level Voltage I/O
7	7	7	7	CANH	CAN High-Level Voltage I/O
8	8	8	8	STBY	Standby Mode Input
9	—	9	—	EP	Exposed Thermal Pad

1.7.1 TRANSMITTER DATA INPUT PIN (TXD)

The CAN transceiver drives the differential output pins CANH and CANL according to TXD. It is usually connected to the transmitter data output of the CAN controller device. When TXD is Low, CANH and CANL are in the Dominant state. When TXD is High, CANH and CANL are in the Recessive state, provided that another CAN node is not driving the CAN bus with a Dominant state. TXD is connected from an internal pull-up resistor (nominal 33 kΩ) to VIO in the MCP2542FD and MCP2542WFD, and to VDD in the MCP2544FD and MCP2544WFD.

1.7.2 GROUND SUPPLY PIN (VSS)

Ground supply pin.

1.7.3 SUPPLY VOLTAGE PIN (VDD)

Positive supply voltage pin. Supplies transmitter and receiver, including the wake-up receiver.

1.7.4 RECEIVER DATA OUTPUT PIN (RXD)

RXD is a CMOS-compatible output that drives High or Low depending on the differential signals on the CANH and CANL pins, and is usually connected to the receiver data input of the CAN controller device. RXD is High when the CAN bus is Recessive, and Low in the Dominant state. RXD is supplied by VIO in the MCP2542FD and MCP2542WFD and by VDD in the MCP2544FD and MCP2544WFD.

1.7.5 NC PIN (MCP2544FD AND MCP2544WFD)

No Connect. This pin can be left open or connected to VSS.

1.7.6 VIO PIN (MCP2542FD AND MCP2542WFD)

Supply for digital I/O pins. In the MCP2544FD and MCP2544WFD, the supply for the digital I/O (TXD, RXD and STBY) is internally connected to VDD.

1.7.7 DIGITAL I/O

The MCP2542FD/4FD and MCP2542WFD/4WFD enable easy interfacing to MCU with I/O ranges from 1.8V to 5V.

1.7.7.1 MCP2544FD and MCP2544WFD

The VIH(MIN) and VIL(MAX) for STBY and TXD are independent of VDD. They are set at levels that are compatible with 3V and 5V microcontrollers.

The RXD pin is always driven to VDD, therefore a 3V microcontroller will need a 5V tolerant input.

1.7.7.2 MCP2542FD and MCP2542WFD

VIH and VIL for STBY and TXD depend on VIO. The RXD pin is driven to VIO.

1.7.8 CAN LOW PIN (CANL)

The CANL output drives the Low side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANL disconnects from the bus when MCP2542FD/4FD and MCP2542WFD/4WFD are not powered.

1.7.9 CAN HIGH PIN (CANH)

The CANH output drives the high side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANH disconnects from the bus when MCP2542FD/4FD and MCP2542WFD/4WFD are not powered.

1.7.10 STANDBY MODE INPUT PIN (STBY)

This pin selects between Normal or Standby mode. In Standby mode, the transmitter and high-speed receiver are turned off, only the low-power receiver and wake-up filter are active. STBY is connected from an internal MOS pull-up resistor to V_{IO} in the MCP2542FD and MCP2542WFD, and to V_{DD} in the MCP2544FD and MCP2544WFD. The value of the MOS pull-up resistor depends on the supply voltage. Typical values are 660 kΩ for 5V, 1.1 MΩ for 3.3V and 4.4 MΩ for 1.8V.

1.7.11 EXPOSED THERMAL PAD (EP)

It is recommended to connect this pad to V_{SS} to enhance electromagnetic immunity and thermal resistance.

1.8 Typical Applications

In order to meet the EMC/EMI requirements, a Common Mode Choke (CMC) may be required for data rates greater than 1 Mbps. Figure 1-3 and Figure 1-4 illustrate examples of typical applications of the devices.

FIGURE 1-3: MCP2544WFD WITH NC AND SPLIT TERMINATION

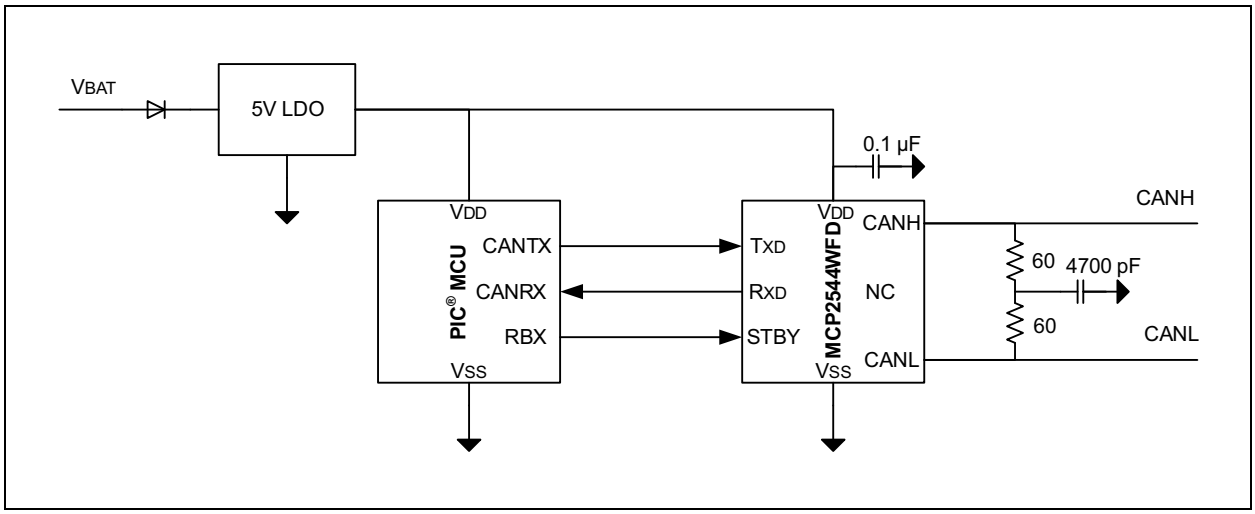
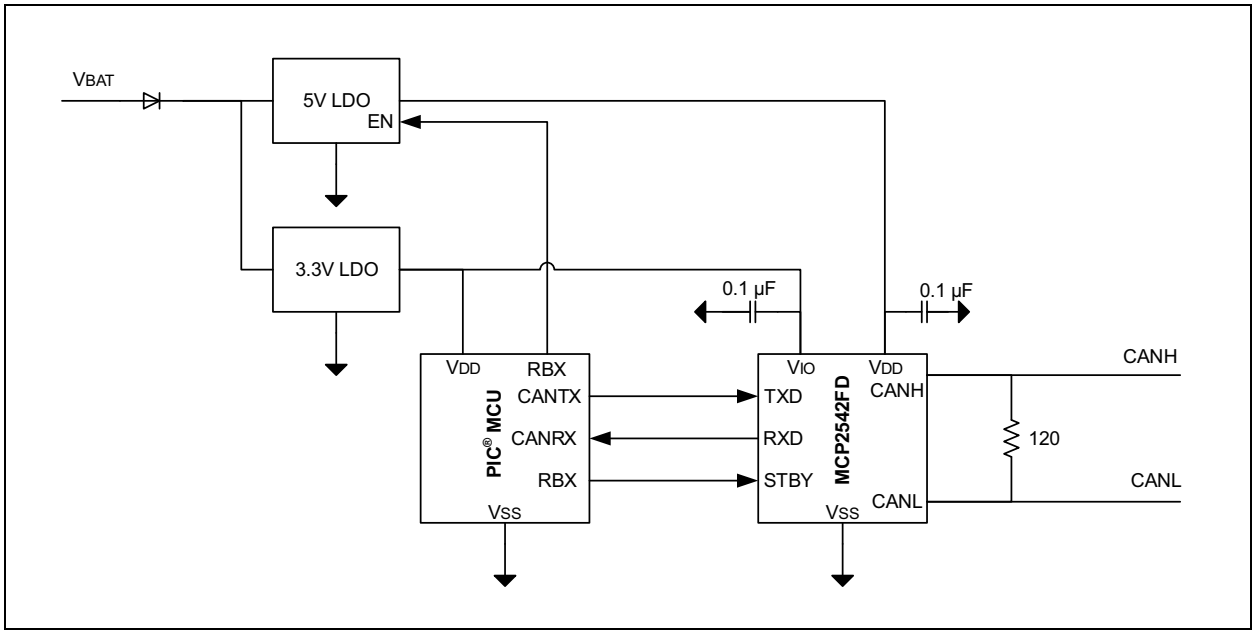


FIGURE 1-4: MCP2542FD WITH VIO PIN



NOTES:

2.0 ELECTRICAL CHARACTERISTICS

2.1 Terms and Definitions

A number of terms are defined in ISO-11898 that are used to describe the electrical characteristics of a CAN transceiver device. These terms and definitions are summarized in this section.

2.1.1 BUS VOLTAGE

V_{CANL} and V_{CANH} denote the voltages of the bus line wires CANL and CANH relative to the ground of each individual CAN node.

2.1.2 COMMON MODE BUS VOLTAGE RANGE

Boundary voltage levels of V_{CANL} and V_{CANH} with respect to ground, for which proper operation will occur, if up to the maximum number of CAN nodes are connected to the bus.

2.1.3 DIFFERENTIAL INTERNAL CAPACITANCE, C_{DIFF} (OF A CAN NODE)

Capacitance seen between CANL and CANH during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.4 DIFFERENTIAL INTERNAL RESISTANCE, R_{DIFF} (OF A CAN NODE)

Resistance seen between CANL and CANH during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.5 DIFFERENTIAL VOLTAGE, V_{DIFF} (OF CAN BUS)

Differential voltage of the two-wire CAN bus, with value equal to $V_{DIFF} = V_{CANH} – V_{CANL}$.

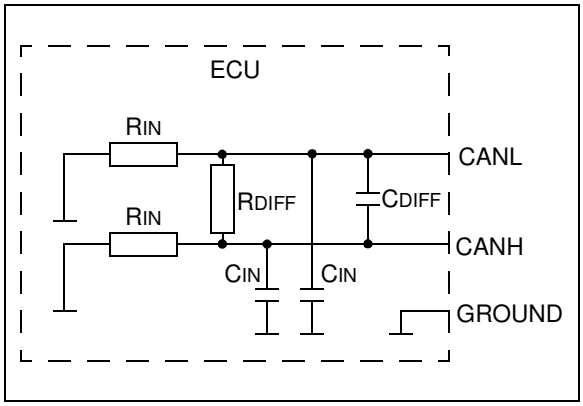
2.1.6 INTERNAL CAPACITANCE, C_{IN} (OF A CAN NODE)

Capacitance seen between CANL (or CANH) and ground during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.7 INTERNAL RESISTANCE, R_{IN} (OF A CAN NODE)

Resistance seen between CANL (or CANH) and ground during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

FIGURE 2-1: PHYSICAL LAYER DEFINITIONS



2.2 Absolute Maximum Ratings†

V_{DD} 7.0V
V_{IO} 7.0V
DC Voltage at T_{XD}, R_{XD}, STBY and V_{SS} ..... -0.3V to V_{IO} + 0.3V
DC Voltage at CANH and CANL ..... -58V to +58V
Transient Voltage on CANH and CANL (ISO-7637) (Figure 2-5) ..... -150V to +100V
Differential Bus Input Voltage $V_{DIFF(I)}$ (t = 60 days, continuous) ..... -5V to +10V
Differential Bus Input Voltage $V_{DIFF(I)}$ (1000 pulses, t = 0.1 ms, V_{CANH} = +18V) ..... +17V
Dominant State Detection $V_{DIFF(I)}$ (10000 pulses, t = 1 ms) ..... +9V
Storage temperature ..... -55°C to +150°C
Operating ambient temperature ..... -40°C to +150°C
Virtual Junction Temperature, T_{VJ} (IEC60747-1) ..... -40°C to +190°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on CANH and CANL pins (IEC 61000-4-2) ..... ±13 kV
ESD protection on CANH and CANL pins (IEC 801; Human Body Model) ..... ±8 kV
ESD protection on all other pins (IEC 801; Human Body Model) ..... ±4 kV
ESD protection on all pins (IEC 801; Machine Model) ..... ±400V
ESD protection on all pins (IEC 801; Charge Device Model) ..... ±750V

† Notice: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: DC CHARACTERISTICS

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (**Note 2**), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply						
V_{DD} Pin						
Voltage Range	V_{DD}	4.5	—	5.5	V	
Supply Current	I_{DD}	—	2.5	5	mA	Recessive; V_{TXD} = V_{DD}
		—	55	70		Dominant; V_{TXD} = 0V
Standby Current	I_{DDS}	—	4	15	µA	**MCP2544FD** and **MCP2544WFD,** Bus Recessive
		—	4	16		**MCP2542FD** and **MCP2542WFD,** Includes I_{IO}
Maximum Supply Current	I_{DDMAX}	—	95	140	mA	Fault condition: V_{TXD} = V_{SS}; V_{CANH} = V_{CANL} = -5V to +18V (**Note 1**)
High Level of the POR Comparator for V_{DD}	V_{PORH}	—	3.0	3.95	V	**Note 1**
Low Level of the POR Comparator for V_{DD}	V_{PORL}	1.0	2.0	3.2	V	**Note 1**
Hysteresis of POR Comparator for V_{DD}	V_{PORD}	0.2	0.9	2.0	V	**Note 1**
High Level of the UV Comparator for V_{DD}	V_{UVH}	4.0	4.25	4.4	V	
Low Level of the UV Comparator for V_{DD}	V_{UVL}	3.6	3.8	4.0	V	
Hysteresis of UV comparator	V_{UVD}	—	0.4	—	V	**Note 1**
V_{IO} Pin						
Digital Supply Voltage Range	V_{IO}	1.7	—	5.5	V	
Supply Current on V_{IO}	I_{IO}	—	7	20	µA	Recessive; V_{TXD} = V_{IO}
		—	200	400		Dominant; V_{TXD} = 0V
Standby Current	I_{DDS}	—	0.3	2	µA	Bus Recessive (**Note 1**)
High Level of the POR Comparator for V_{IO}	V_{PORH_VIO}	0.8	1.2	1.7	V	
Low Level of the POR Comparator for VIO	V_{PORL_VIO}	0.7	1.1	1.4	V	
Hysteresis of POR Comparator for V_{IO}	V_{PORD_VIO}	—	0.2	—	V	
Bus Line (CANH; CANL) Transmitter						
CANH; CANL: Recessive Bus Output Voltage	$V_{O(R)}$	2.0	0.5 V_{DD}	3.0	V	V_{TXD} = V_{DD}; No load
CANH; CANL: Bus Output Voltage in Standby	$V_{O(S)}$	-0.1	0.0	+0.1	V	STBY = V_{TXD} = V_{DD}; No load

Note 1: Characterized; not 100% tested.

2: Only MCP2542FD and MCP2542WFD have a V_{IO} pin. For the MCP2544FD and MCP2544WFD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, and tested from -2V to 7V.

TABLE 2-1: DC CHARACTERISTICS (CONTINUED)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (**Note 2**), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Recessive Output Current	$I_{O(R)}$	-5	—	+5	mA	-24V < V_{CAN} < +24V
CANH: Dominant Output Voltage	$V_{O(D)}$	2.75	3.50	4.50	V	T_{XD} = 0; R_L = 50 to 65Ω
CANL: Dominant Output Voltage		0.50	1.50	2.25		R_L = 50Ω to 65Ω
Driver Symmetry (V_{CANH}+V_{CANL})/V_{DD}	V_{SYM}	0.9	1.0	1.1	V	1 MHz square wave, Recessive and Dominant states, and transition (**Note 1**)
Dominant: Differential Output Voltage	$V_{O(DIFF)(D)}$	1.5	2.0	3.0	V	V_{TXD} = V_{SS}; R_L = 50Ω to 65Ω (Figure 2-2, Figure 2-4, **Section 3.0**) (**Note 1**)
		1.4	2.0	3.3		V_{TXD} = V_{SS}; R_L = 45Ω to 70Ω (Figure 2-2, Figure 2-4, **Section 3.0**) (**Note 1**)
		1.3	2.0	3.3		V_{TXD} = V_{SS}; R_L = 40Ω to 75Ω (Figure 2-2, Figure 2-4)
		1.5	—	5.0		V_{TXD} = V_{SS}; R_L = 2240Ω (Figure 2-2, Figure 2-4, **Section 3.0**) (**Note 1**)
Recessive: Differential Output Voltage	$V_{O(DIFF)(R)}$	-500	0	50	mV	V_{TXD} = V_{DD}, no load, Normal. (Figure 2-2, Figure 2-4)
	$V_{O(DIFF)(S)}$	-200	0	200		V_{TXD} = V_{DD}, no load, Standby. Figure 2-2, Figure 2-4
CANH: Short-Circuit Output Current	$I_{O(SC)}$	-115	-85	—	mA	V_{TXD} = V_{SS}; V_{CANH} = -3V; CANL: floating
CANL: Short Circuit Output Current		—	75	+115	mA	V_{TXD} = V_{SS}; V_{CANL} = +18V; CANH: floating
Bus Line (CANH; CANL) Receiver						
Recessive Differential Input Voltage	$V_{DIFF(R)(I)}$	-4.0	—	+0.5	V	Normal Mode; -12V < $V_{(CANH, CANL)}$ < +12V; see Figure 2-6 (**Note 3**)
		-4.0	—	+0.4		Standby Mode; -12V < $V_{(CANH, CANL)}$ < +12V; see Figure 2-6 (**Note 3**)
Dominant Differential Input Voltage	$V_{DIFF(D)(I)}$	0.9	—	9.0	V	Normal Mode; -12V < $V_{(CANH, CANL)}$ < +12V; see Figure 2-6 (**Note 3**)
		1.1	—	9.0		Standby Mode; -12V < $V_{(CANH, CANL)}$ < +12V; see Figure 2-6 (**Note 3**)

Note 1: Characterized; not 100% tested.

2: Only MCP2542FD and MCP2542WFD have a V_{IO} pin. For the MCP2544FD and MCP2544WFD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, and tested from -2V to 7V.

TABLE 2-1: DC CHARACTERISTICS (CONTINUED)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (**Note 2**), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Differential Receiver Threshold	$V_{TH(DIFF)}$	0.5	0.7	0.9	V	Normal Mode; -12V < V(CANH, CANL) < +12V; see Figure 2-6 (**Note 3**)
		0.4	0.7	0.9		Standby Mode; -12V < V(CANH, CANL) < +12V; see Figure 2-6 (**Note 3**)
Differential Input Hysteresis	$V_{HYS(DIFF)}$	30	—	200	mV	Normal mode, see Figure 2-6, (**Note 1**)
Single Ended Input Resistance	R_{CAN_H}, R_{CAN_L}	6	—	50	kΩ	**Note 1**
Internal Resistance Matching $m_R=2*(R_{CANH}-R_{CANL})/(R_{CANH}+R_{CANL})$	m_R	-3	0	+3	%	V_{CANH} = V_{CANL} (**Note 1**)
Differential Input Resistance	R_{DIFF}	12	25	100	kΩ	**Note 1**
Internal Capacitance	C_{IN}	—	20	—	pF	1 Mbps (**Note 1**)
Differential Internal Capacitance	C_{DIFF}	—	10	—	pF	1 Mbps (**Note 1**)
CANH, CANL: Input Leakage	I_{LI}	-5	—	+5	µA	V_{DD} = V_{TXD} = V_{STBY} = 0V. For **MCP2542FD** and **MCP2542WFD**, V_{IO} = 0V. V_{CANH} = V_{CANL} = 5 V.
Digital Input Pins (T_{XD}, STBY)						
High-Level Input Voltage	V_{IH}	2.0	—	V_{IO} + 0.3	V	**MCP2544FD** and **MCP2544WFD**
		0.7 V_{IO}	—	V_{IO} + 0.3		**MCP2542FD** and **MCP2542WFD**
Low-Level Input Voltage	V_{IL}	-0.3	—	0.8	V	**MCP2544FD** and **MCP2544WFD**
		-0.3	—	0.3V_{IO}		**MCP2542FD** and **MCP2542WFD**
High-Level Input Current	I_{IH}	-1	—	+1	µA	
T_{XD}: Low-Level Input Current	$I_{IL(TXD)}$	-270	-150	-30	µA	
STBY: Low-Level Input Current	$I_{IL(STBY)}$	-30	—	-1	µA	

Note 1: Characterized; not 100% tested.

2: Only MCP2542FD and MCP2542WFD have a V_{IO} pin. For the MCP2544FD and MCP2544WFD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, and tested from -2V to 7V.

TABLE 2-1: DC CHARACTERISTICS (CONTINUED)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (**Note 2**), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Receive Data (R_{XD}) Output						
High-Level Output Voltage	V_{OH}	V_{DD} - 0.4	—	—	V	**MCP2544FD** and **MCP2544WFD**: I_{OH} = -2 mA; typical -4 mA
		V_{IO} - 0.4	—	—		**MCP2542FD** and **MCP2542WFD:** V_{IO} = 2.7V to 5.5V, I_{OH} = -1 mA; V_{IO} = 1.7V to 2.7V, I_{OH} = -0.5 mA, typical -2 mA
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; typical 8 mA
Thermal Shutdown						
Shutdown Junction Temperature	$T_{J(SD)}$	165	175	185	°C	-12V < V(CANH, CANL) < +12V (**Note 1**)
Shutdown Temperature Hysteresis	$T_{J(HYST)}$	15	—	30	°C	-12V < V(CANH, CANL) < +12V (**Note 1**)

Note 1: Characterized; not 100% tested.

2: Only MCP2542FD and MCP2542WFD have a V_{IO} pin. For the MCP2544FD and MCP2544WFD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, and tested from -2V to 7V.

FIGURE 2-2: PHYSICAL BIT REPRESENTATION AND SIMPLIFIED BIAS IMPLEMENTATION

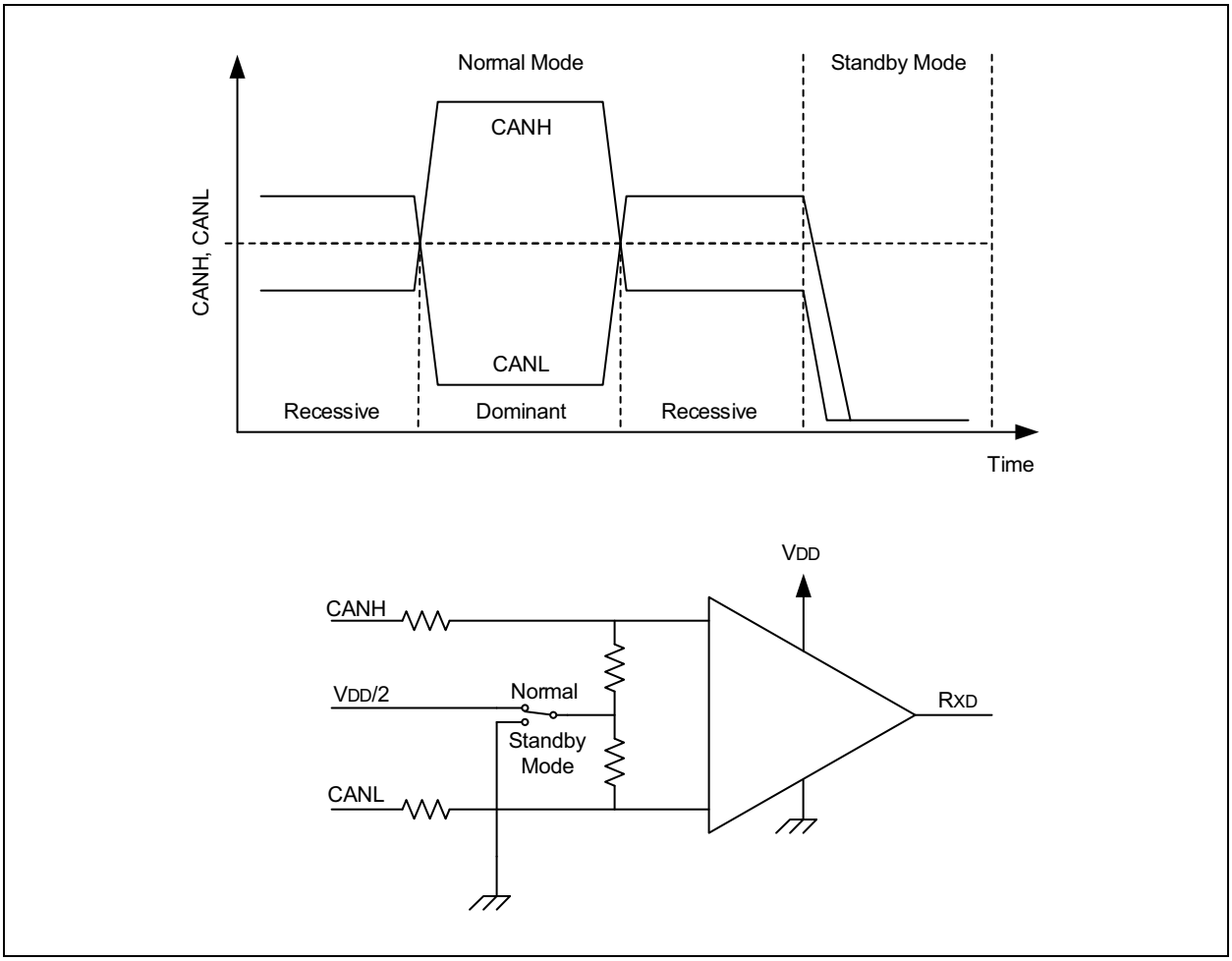


TABLE 2-2: AC CHARACTERISTICS

AC Characteristics		**Electrical Characteristics:** Unless otherwise indicated, Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (**Note 2**), R_L = 60Ω, C_L = 100 pF. Maximum $V_{DIFF(D)(I)}$ = 3V.					
Param. No.	**Parameter**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
1	Bit Time	t_{BIT}	0.125	—	69.44	µs	
2	Nominal Bit Rate	NBR	14.4	—	8000	kbps	
3	Delay T_{XD} Low to Bus Dominant	$t_{TXD-BUSON}$	—	50	85	ns	**Note 1**
4	Delay T_{XD} High to Bus Recessive	$t_{TXD-BUSOFF}$	—	40	85	ns	**Note 1**
5	Delay Bus Dominant to R_{XD}	$t_{BUSON-RXD}$	—	70	85	ns	**Note 1**
6	Delay Bus Recessive to R_{XD}	$t_{BUSOFF-RXD}$	—	110	145	ns	**Note 1**

Note 1: Characterized, not 100% tested.

2: Not in ISO 11898-2:2015, but needs to be characterized.

TABLE 2-2: AC CHARACTERISTICS (CONTINUED)

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (**Note 2**), R_L = 60Ω, C_L = 100 pF. Maximum $V_{DIFF(D)(I)}$ = 3V.					
Param. No.	**Parameter**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
7	Propagation Delay T_{XD} to R_{XD} Worst Case of $t_{LOOP(R)}$ and $t_{LOOP(F)}$ Figure 2-10	$t_{TXD - RXD}$	—	90	120	ns	
			—	115	150		R_L = 150Ω, C_L = 200 pF(**Note 1**)
7a	Propagation Delay, Rising Edge	$t_{LOOP(R)}$	—	90	120	ns	
7b	Propagation Delay, Falling Edge	$t_{LOOP(F)}$	—	80	120	ns	
8a	Recessive Bit Time on R_{XD} – 1 Mbps, Loop Delay Symmetry (**Note 2**)	$t_{BIT(RXD)}$, 1M	900	985	1100	ns	$t_{BIT(TXD)}$ = 1000 ns (Figure 2-10)
			800	960	1255		$t_{BIT(TXD)}$ = 1000 ns (Figure 2-10), R_L = 150Ω, C_L = 200 pF (**Note 1**)
8b	Recessive Bit Time on R_{XD} – 2 Mbps, Loop Delay Symmetry	$t_{BIT(RXD)}$, 2M	450	490	550	ns	$t_{BIT(TXD)}$ = 500 ns (Figure 2-10)
			400	460	550		$t_{BIT(TXD)}$ = 500 ns (Figure 2-10), R_L = 150Ω, C_L = 200 pF (**Note 1**)
8c	Recessive Bit Time on R_{XD} – 5 Mbps, Loop Delay Symmetry	$t_{BIT(RXD)}$, 5M	160	190	220	ns	$t_{BIT(TXD)}$ = 200 ns (Figure 2-10)
8d	Recessive Bit Time on R_{XD} – 8 Mbps, Loop Delay Symmetry (**Note 2**)	$t_{BIT(RXD)}$, 8M	85	100	135	ns	$t_{BIT(TXD)}$ = 120 ns (Figure 2-10) (**Note 1**)
9	CAN Activity Filter Time (Standby)	t_{FILTER}	0.5	1.7	3.6	µs	$V_{DIFF(D)(I)}$ = 1.2V to 3V
10	Delay Standby to Normal Mode	t_{WAKE}	—	7	30	µs	Negative edge on STBY
11	Permanent Dominant Detect Time	t_{PDT}	0.8	1.9	5	ms	T_{XD} = 0V
12	Permanent Dominant Timer Reset	t_{PDTR}	—	5	—	ns	The shortest recessive pulse on T_{XD} or CAN bus to reset Permanent Dominant Timer
13a	Transmitted Bit Time on Bus – 1 Mbps (**Note 2**)	$t_{BIT(BUS)}$, 1M	870	1000	1060	ns	$t_{BIT(TXD)}$ = 1000 ns (Figure 2-10)
			870	1000	1060		$t_{BIT(TXD)}$ = 1000 ns (Figure 2-10), R_L = 150Ω, C_L = 200 pF (**Note 1**)

Note 1: Characterized, not 100% tested.

2: Not in ISO 11898-2:2015, but needs to be characterized.

TABLE 2-2: AC CHARACTERISTICS (CONTINUED)

AC Characteristics		**Electrical Characteristics:** Unless otherwise indicated, Extended (E): T_{AMB} = -40°C to +125°C and High (H): T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (**Note 2**), R_L = 60Ω, C_L = 100 pF. Maximum $V_{DIFF(D)(I)}$ = 3V.					
Param. No.	**Parameter**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
13b	Transmitted Bit Time on Bus – 2 Mbp	$t_{BIT(BUS)}$, 2M	435	515	530	ns	$t_{BIT(TXD)}$ = 500 ns (Figure 2-10)
			435	480	550		$t_{BIT(TXD)}$ = 500 ns (Figure 2-10) R_L = 150Ω, C_L = 200 pF (**Note 1**)
13c	Transmitted Bit Time on Bus – 5 Mbps	$t_{BIT(BUS)}$, 5M	155	200	210	ns	$t_{BIT(TXD)}$ = 200ns (Figure 2-10) (**Note 1**)
13d	Transmitted Bit Time on Bus - 8Mbps (**Note 2**)	$t_{BIT(BUS)}$, 8M	100	125	140	ns	$t_{BIT(TXD)}$ = 120 ns (Figure 2-10) (**Note 1**)
14a	Receiver Timing Symmetry – 1 Mbps (**Note 2**)	$t_{DIFF(REC)}$, 1M = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$	-65	0	40	ns	$t_{BIT(TXD)}$ = 1000 ns (Figure 2-10)
			-130	0	80		$t_{BIT(TXD)}$ = 1000ns (Figure 2-10), R_L = 150Ω, C_L = 200 pF (**Note 1**)
14b	Receiver Timing Symmetry – 2 Mbps	$t_{DIFF(REC)}$, 2M	-65	0	40	ns	$t_{BIT(TXD)}$ = 500 ns (Figure 2-10)
			-70	0	40		$t_{BIT(TXD)}$ = 500 ns (Figure 2-10), R_L = 150Ω, C_L = 200 pF (**Note 1**)
14c	Receiver Timing Symmetry – 5 Mbps	$t_{DIFF(REC)}$, 5M	-45	0	15	ns	$t_{BIT(TXD)}$ = 200 ns (Figure 2-10) (**Note 1**)
14d	Receiver Timing Symmetry – 8 Mbps (**Note 2**) $t_{DIFF(REC),8M}$	$t_{DIFF(REC)}$, 8M	-45	0	10	ns	$t_{BIT(TXD)}$ = 120 ns (Figure 2-10) (**Note 1**)
15	WUP Time Out	$t_{WAKE(TO)}$	1	1.9	5	ms	**MCP2542WFD/4WFD** (Figure 2-11)
16	Delay Bus Dominant/Recessive to R_{XD} (Standby mode)	$t_{BUS-RXD(S)}$	—	0.5	—	µs	

Note 1: Characterized, not 100% tested.

2: Not in ISO 11898-2:2015, but needs to be characterized.

FIGURE 2-3: TEST LOAD CONDITIONS

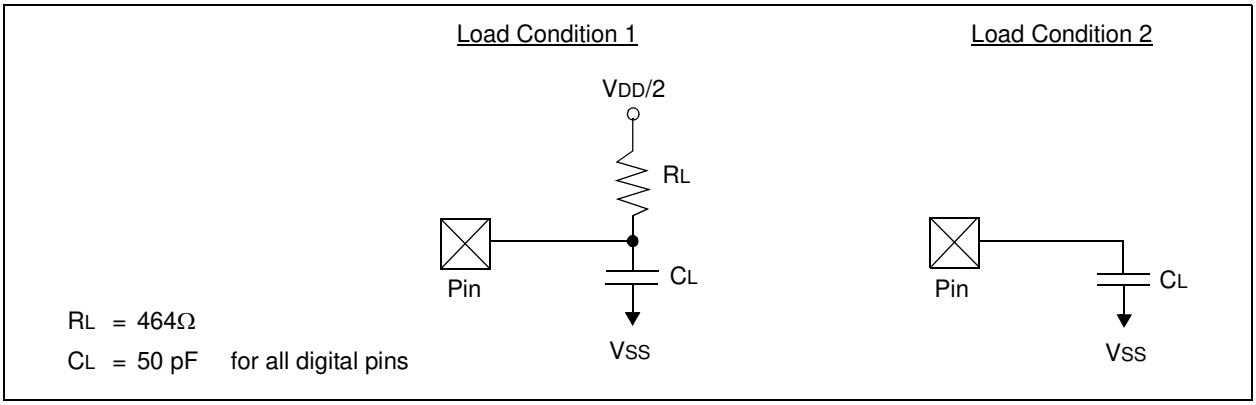
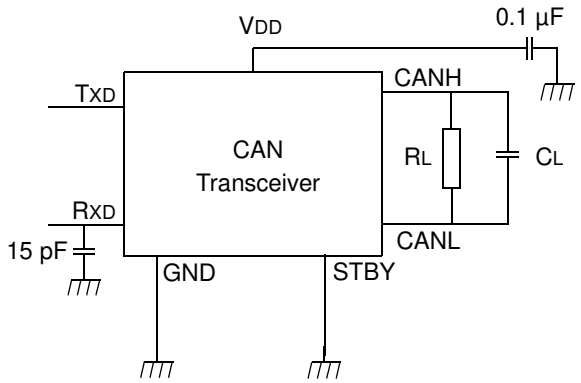
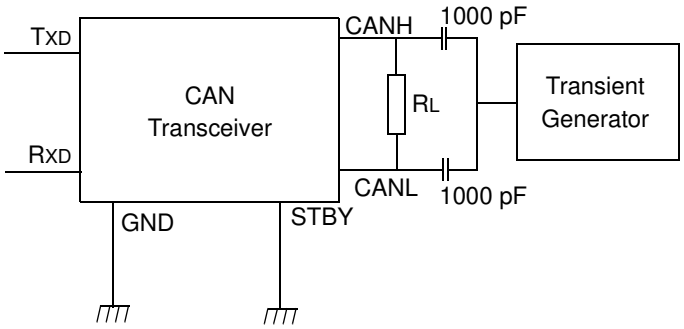


FIGURE 2-4: TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS



Note: On MCP2544FD and MCP2544WFD, VIO is connected to VDD.

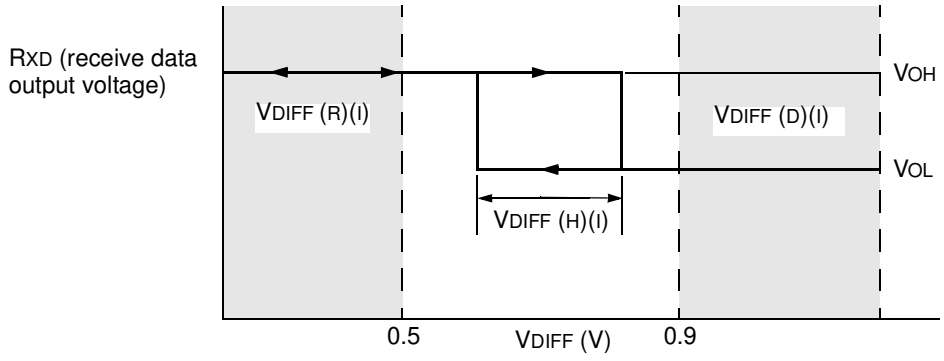
FIGURE 2-5: TEST CIRCUIT FOR AUTOMOTIVE TRANSIENTS



Note 1: On MCP2544FD and MCP2544WFD, VIO is connected to VDD.

2: The wave forms of the applied transients shall be in accordance with ISO-7637, Part 1, test pulses 1, 2, 3a and 3b.

FIGURE 2-6: HYSTERESIS OF THE RECEIVER



2.3 Timing Diagrams and Specifications

FIGURE 2-7: TIMING DIAGRAM FOR AC CHARACTERISTICS

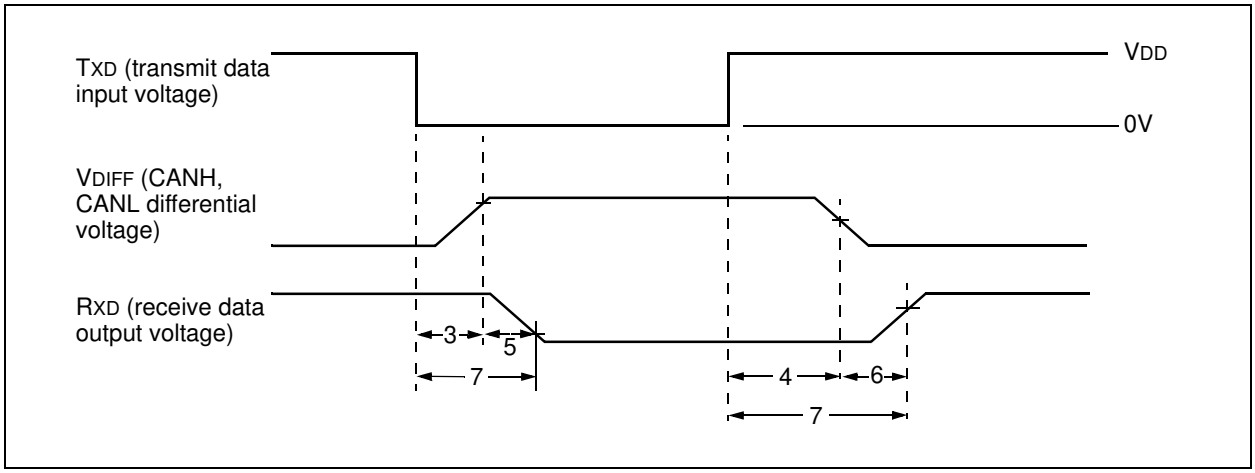


FIGURE 2-8: TIMING DIAGRAM FOR WAKEUP FROM STANDBY

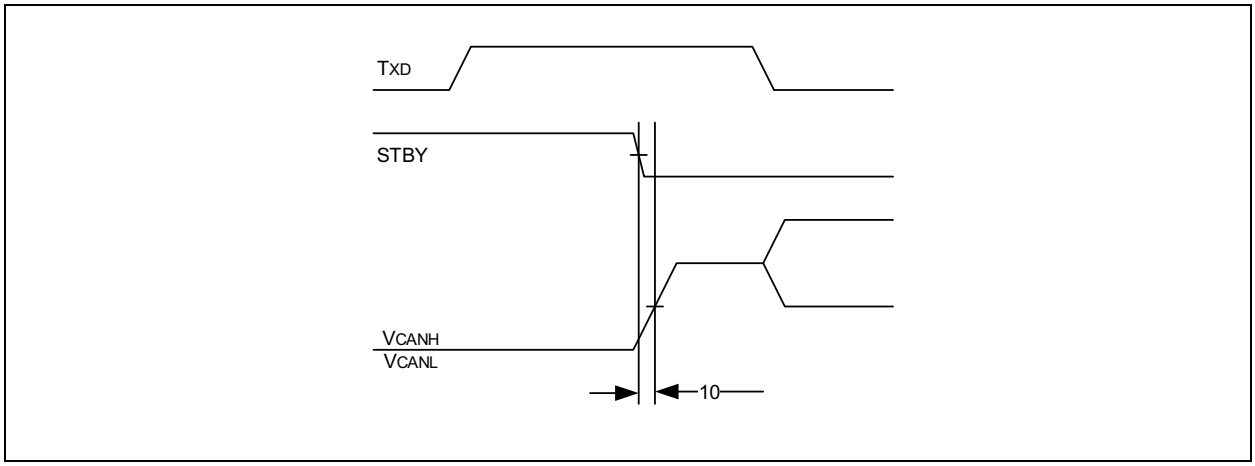


FIGURE 2-9: PERMANENT DOMINANT TIMER RESET DETECT

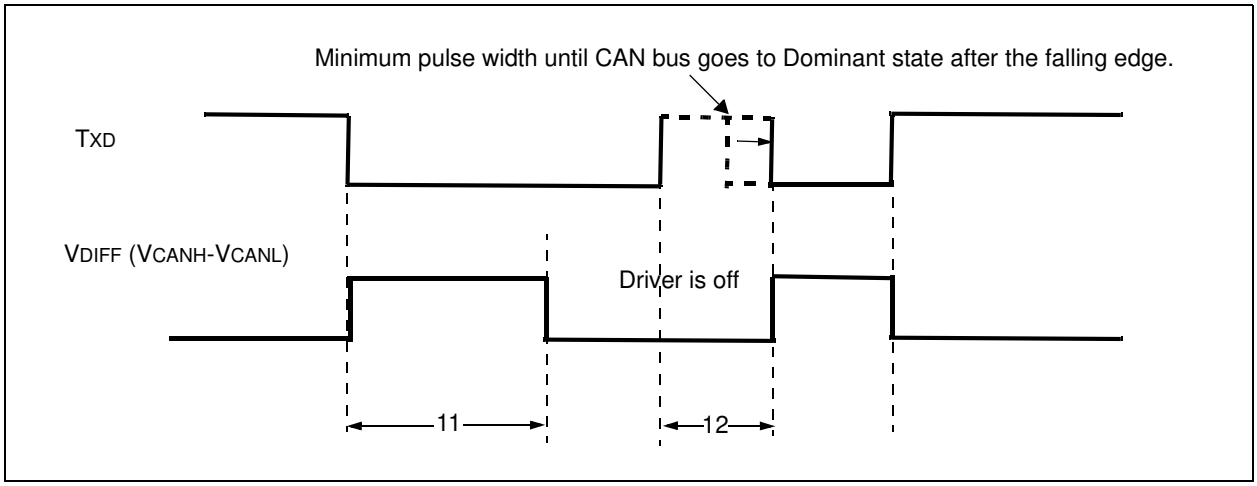


FIGURE 2-10: TIMING DIAGRAM FOR LOOP DELAY SYMMETRY

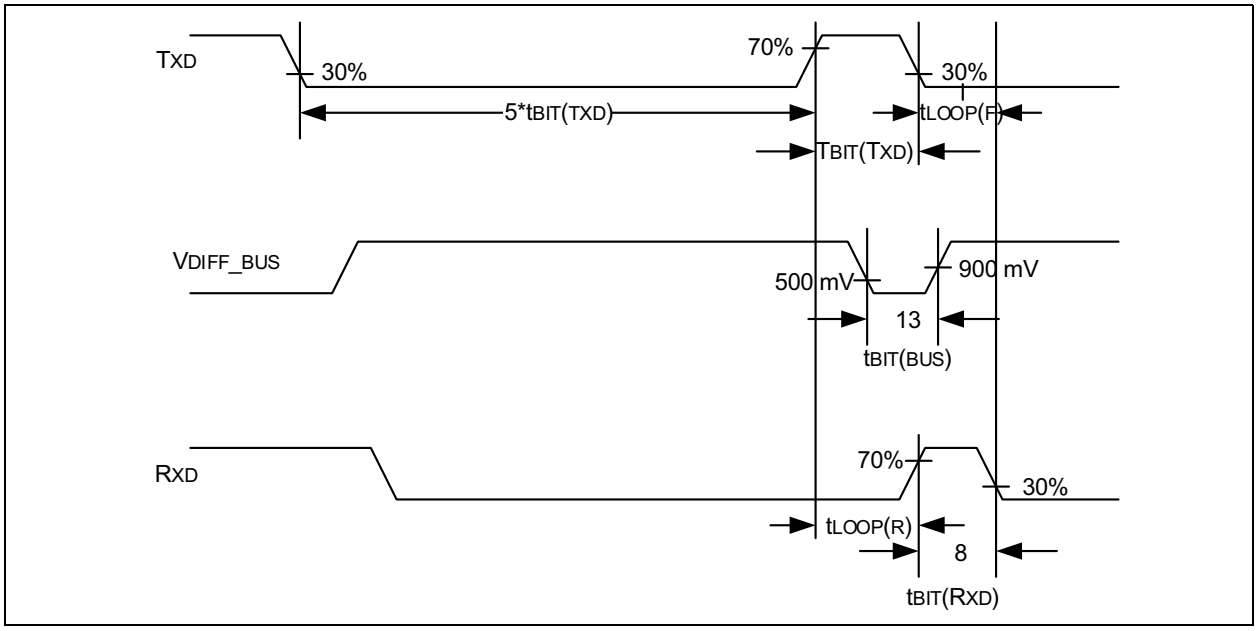


FIGURE 2-11: TIMING DIAGRAM FOR WAKE-UP PATTERN (WUP)

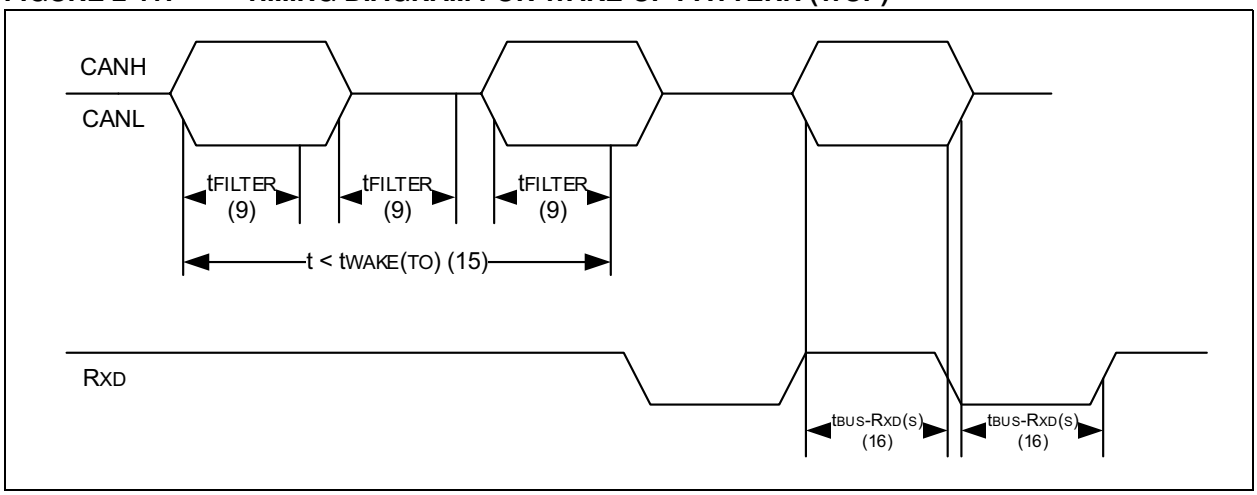


TABLE 2-1: THERMAL SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Temperature Ranges						
Specified Temperature Range	TA	-40	—	+125	°C	
		-40	—	+150		
Operating Temperature Range	TA	-40	—	+150	°C	
Storage Temperature Range	TA	-65	—	+155	°C	
Package Thermal Resistances						
Thermal Resistance, 8LD DFN (3x3)	θJA	—	56.7	—	°C/W	
Thermal Resistance, 8LD SOIC	θJA	—	149.5	—	°C/W	
Thermal Resistance, 8LD TDFN (2x3)	θJA	—	53	—	°C/W	

3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

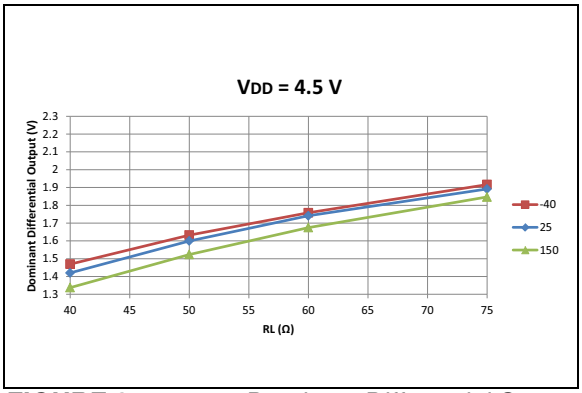


FIGURE 3-1: *Dominant Differential Output vs. RL (V_{DD} = 4.5V).*

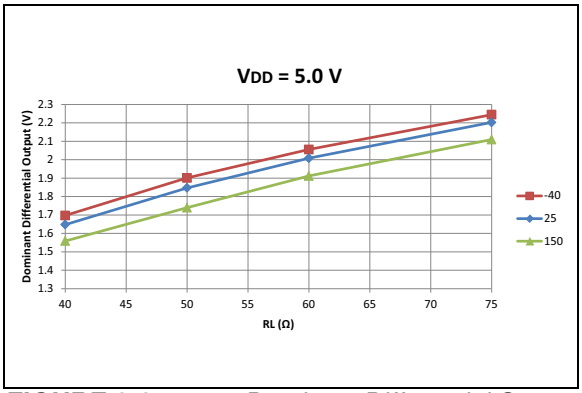


FIGURE 3-2: *Dominant Differential Output vs. RL (V_{DD} = 5.0V).*

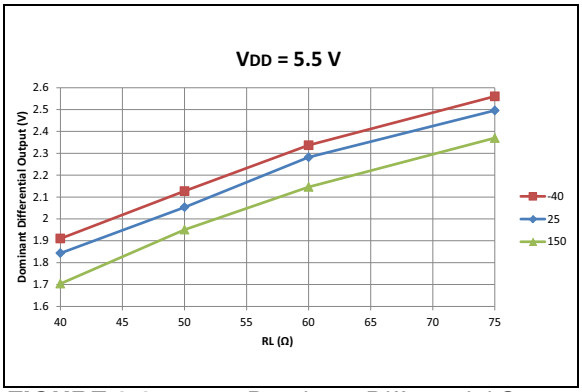


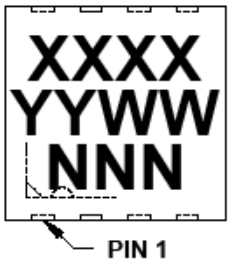
FIGURE 3-3: *Dominant Differential Output vs. RL (V_{DD} = 5.5V).*

NOTES:

4.0 PACKAGING INFORMATION

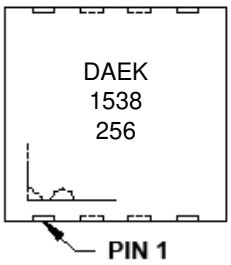
4.1 Package Marking Information

8-Lead DFN (03x03x0.9 mm)

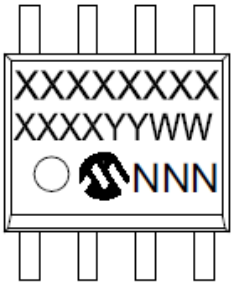


Part Number	Code
MCP2542FD-E/MF	DAEK
MCP2542FDT-H/MF	DAEK
MCP2542FD-H/MF	DAEK
MCP2542FDT-E/MF	DAEK
MCP2542WFD-E/MF	DAEH
MCP2542WFDT-H/MF	DAEH
MCP2542WFD-H/MF	DAEH
MCP2542WFDT-E/MF	DAEH
MCP2544FD-E/MF	DAEJ
MCP2544FDT-H/MF	DAEJ
MCP2544FD-H/MF	DAEJ
MCP2544FDT-E/MF	DAEJ
MCP2544WFD-E/MF	DAEG
MCP2544WFDT-H/MF	DAEG
MCP2544WFD-H/MF	DAEG
MCP2544WFDT-E/MF	DAEG

Example:

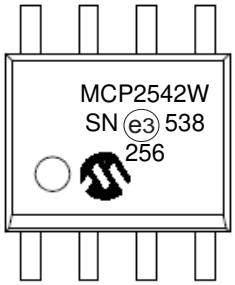


8-Lead SOIC (150 mil)



Part Number	Code
MCP2542WFD-E/SN	MCP2542
MCP2542WFDT-H/SN	MCP2542W
MCP2542WFD-H/SN	MCP2542W
MCP2542WFDT-E/SN	MCP2542
MCP2542FD-E/SN	MCP2542W
MCP2542FDT-H/SN	MCP2542W
MCP2542FD-H/SN	MCP2542W
MCP2542FDT-E/SN	MCP2542W
MCP2544WFD-E/SN	MCP2544W
MCP2544WFDT-H/SN	MCP2544WFD
MCP2544WFD-H/SN	MCP2544WFD
MCP2544WFD-E/SN	MCP2544W
MCP2544FD-E/SN	MCP2544
MCP2544FDT-H/SN	MCP2544
MCP2544FD-H/SN	MCP2544
MCP2544FDT-E/SN	MCP2544

Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC® designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.