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MCP2557FD/8FD

CAN FD Transceiver with Silent Mode

Features

- Silent Mode is Useful in the Following Applications:
  - Disables transmitter in redundant systems
  - Implements babbling idiot protection
  - Tests connection of bus medium
  - Prevents a faulty CAN controller from disrupting all network communications
- Optimized for CAN FD at 2, 5 and 8 Mbps Operation:
  - Maximum propagation delay: 120 ns
  - Loop delay symmetry: ±10%(2 Mbps)
- Meets or Exceeds Stringent Automotive Design Requirements Including “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications”, Version 1.3, May 2012:
  - Conducted emissions at 2 Mbps with Common-Mode Choke (CMC)
  - DPI at 2 Mbps with CMC
- Meets SAE J2962/2 “Communication Transceivers Qualification Requirements – CAN”
  - Passes radiated emissions at 2 Mbps without a CMC
- Meets Latest ISO/DIS-11898-2:2015
- Meets Latest SAE J2284-4 and -5 Working Drafts
- Digital Inputs of the MCP2557FD are Compatible to 3.3V and 5V Microcontrollers. RXD Output Requires a 5V Tolerant Microcontroller Input
- Functional Behavior Predictable Under all Supply Conditions:
  - Device is in Unpowered mode if VDD drops below Power-on Reset (POR) level
  - Device is in Unpowered mode if VIO drops below POR level

Applications

CAN 2.0 and CAN FD networks in Automotive, Industrial, Aerospace, Medical, and Consumer applications.

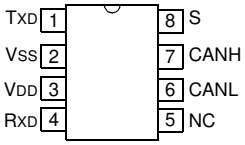
Description

The MCP2557FD/8FD CAN transceiver family is designed for high-speed CAN FD applications with up to 8 Mbps communication speed. The maximum propagation delay was improved to support longer bus length.

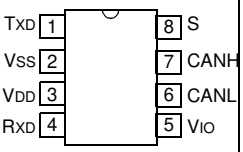
The device meets automotive requirements for CAN FD bit rates exceeding 2 Mbps, low quiescent current, electromagnetic compatibility (EMC) and electrostatic discharge (ESD).

Package Types

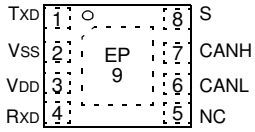
MCP2557FD
SOIC



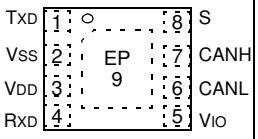
MCP2558FD
SOIC



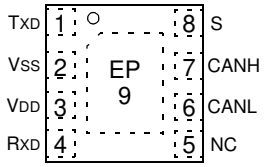
MCP2557FD
2x3 TDFN*



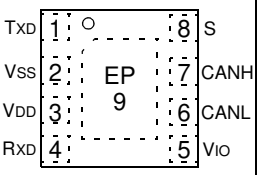
MCP2558FD
2x3 TDFN*



MCP2557FD
3x3 DFN*



MCP2558FD
3x3 DFN*



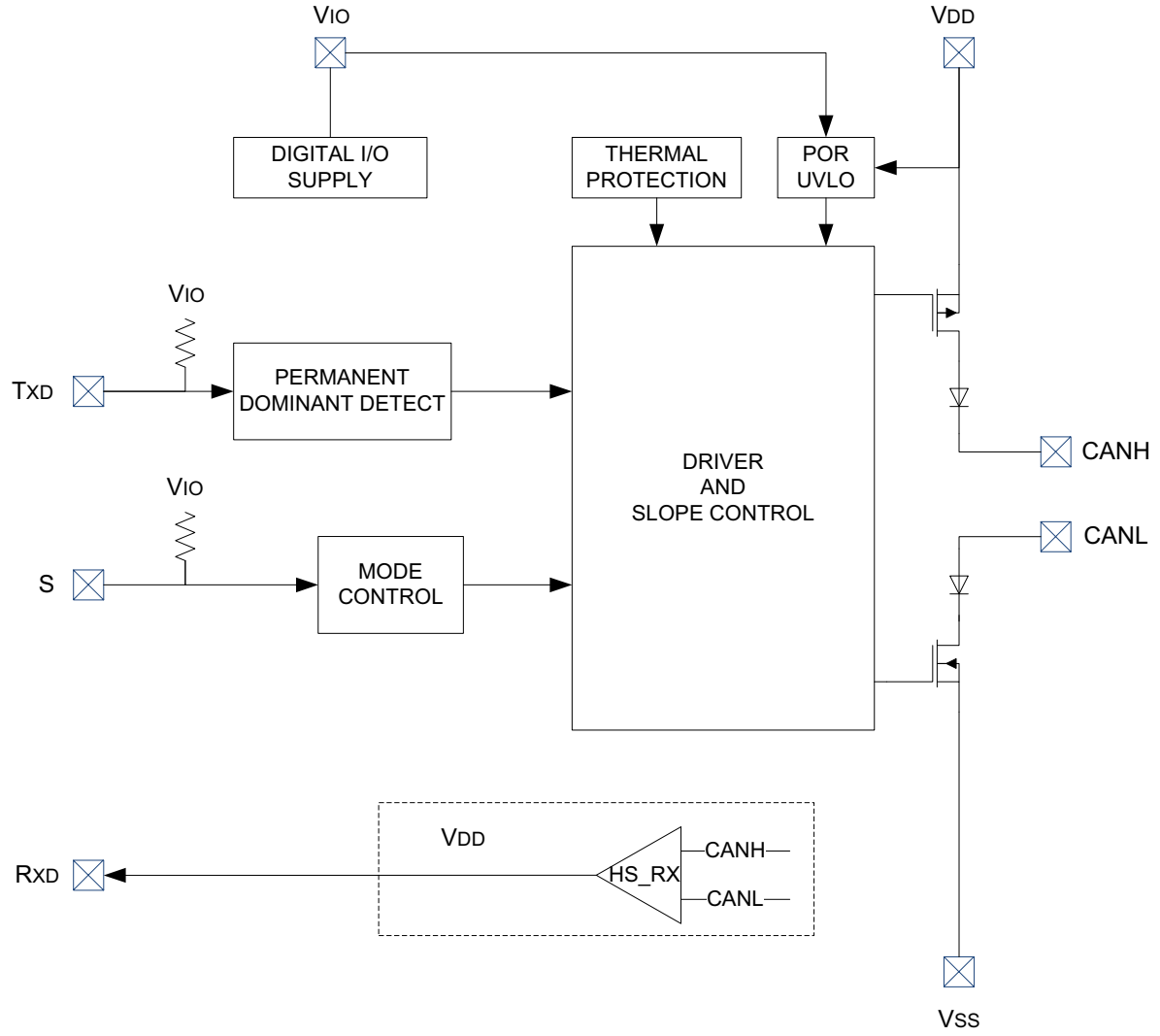
*Includes Exposed Thermal Pad (EP); see Table 1-1.

MCP2557FD/8FD Family Members

Device	VIO Pin	NC	TTL I/O	VIO I/O	Description
MCP2557FD	N/A	Yes	Yes	N/A	—
MCP2558FD	Yes	N/A	N/A	Yes	Internal level shifter on digital I/O pins.

Note: For ordering information, see the Product Identification System section.

Block Diagram



Note: Only the MCP2558FD has the VIO pin. In the MCP2557FD, the supply for the digital I/O is internally connected to VDD.

1.0 DEVICE OVERVIEW

The MCP2557FD/8FD CAN transceiver family is designed for high-speed CAN FD applications with up to 8 Mbps communication speed. The product offers a Silent mode controlled by the Silent mode pin. The Silent mode is used to disable the CAN transmitter. This ensures that the device doesn't drive the CAN bus. The MCP2557FD/8FD device provides differential transmit and receive capability for the CAN protocol controller, and is fully compatible with specification ISO/DIS-11898-2:2015.

The loop delay symmetry is tested to support data rates that are up to 8 Mbps for CAN FD (Flexible Data rate). The maximum propagation delay was improved to support longer bus length.

Typically, each node in a CAN system must have a device convert the digital signals generated by a CAN controller to signals suitable for transmission over the bus cabling (differential output). It also provides a buffer between the CAN controller and the high-voltage spikes that can be generated on the CAN bus by outside sources.

1.1 Transmitter Function

The CAN bus has two states: Dominant and Recessive. A Dominant state occurs when the differential voltage between CANH and CANL is greater than $V_{DIFF(D)(I)}$. A Recessive state occurs when the differential voltage is less than $V_{DIFF(R)(I)}$. The Dominant and Recessive states correspond to the Low and High states of the TXD input pin, respectively. However, a Dominant state initiated by another CAN node will override a Recessive state on the CAN bus.

1.2 Receiver Function

The RXD output pin reflects the differential bus voltage between CANH and CANL. The Low and High states of the RXD output pin correspond to the Dominant and Recessive states of the CAN bus, respectively.

1.3 Internal Protection

CANH and CANL are protected against battery short circuits and electrical transients that can occur on the CAN bus. This feature prevents destruction of the transmitter output stage during such a fault condition.

The device is further protected from excessive current loading by thermal shutdown circuitry that disables the output drivers when the junction temperature exceeds a nominal limit of +175°C.

All other parts of the chip remain operational, and the chip temperature is lowered due to the decreased power dissipation in the transmitter outputs. This protection is essential to guard against bus line short-circuit-induced damage. Thermal protection is only active during Normal mode.

1.4 Permanent Dominant Detection

The MCP2557FD/8FD device prevents a permanent dominant condition on TXD.

In Normal mode, if the MCP2557FD/8FD detects an extended Low state on the TXD input, it will disable the CANH and CANL output drivers in order to prevent data corruption on the CAN bus. The drivers will remain disabled until TXD goes High. The high-speed receiver is active, and data on the CAN bus is received on RXD.

The condition has a time-out of 1.9 ms (typical). This implies a maximum bit time of 128 µs (7.8 kHz), allowing up to 18 consecutive dominant bits on the bus.

1.5 Power-on Reset (POR) and Undervoltage Detection

The MCP2557FD/8FD have POR detection on both supply pins, V_{DD} and V_{IO}. Typical POR thresholds to deassert the reset are 1.2V and 3.0V for V_{IO} and V_{DD}, respectively.

When the device is powered on, CANH and CANL remain in a high-impedance state until V_{DD} exceeds its undervoltage level. Once powered on, CANH and CANL will enter a high-impedance state if the voltage level at V_{DD} drops below the undervoltage level, providing voltage brown-out protection during normal operation.

The receiver output is forced to a Recessive state during an undervoltage condition on V_{DD}.

1.6 Mode Control

Figure 1-1 shows the state diagram of the MCP2557FD/8FD.

1.6.1 UNPOWERED MODE (POR)

The MCP2557FD/8FD enters Unpowered mode if any of the following conditions occur:

- After powering up the device
- If V_{DD} drops below V_{PORL}
- If V_{IO} drops below V_{PORL_VIO}

In Unpowered mode, the CAN bus will be biased to ground using a high impedance. The MCP2557FD/8FD is not able to communicate on the bus.

1.6.2 WAKE MODE

The MCP2557FD/8FD transitions from Unpowered mode to Wake mode when V_{DD} and V_{IO} are above their PORH levels. From Normal mode, if V_{DD} is smaller than V_{UVL}, or if the bandgap output voltage is not within valid range, the device will also enter Wake mode.

In Wake mode, the CAN bus is biased to ground and RXD is always high.

1.6.3 NORMAL MODE

When V_{DD} exceeds V_{UVH}, the band gap is within valid range and TXD is High, the device transitions into Normal mode. During POR, when the microcontroller powers up, the TXD pin could be unintentionally pulled down by the microcontroller powering up. To avoid driving the bus during a POR of the microcontroller, the transceiver proceeds to Normal mode only after TXD is high.

In Normal mode, the driver block is operational and can drive the bus pins. The slopes of the output signals on CANH and CANL are optimized to reduce Electromagnetic Emissions (EME). The CAN bus is biased to $V_{DD}/2$.

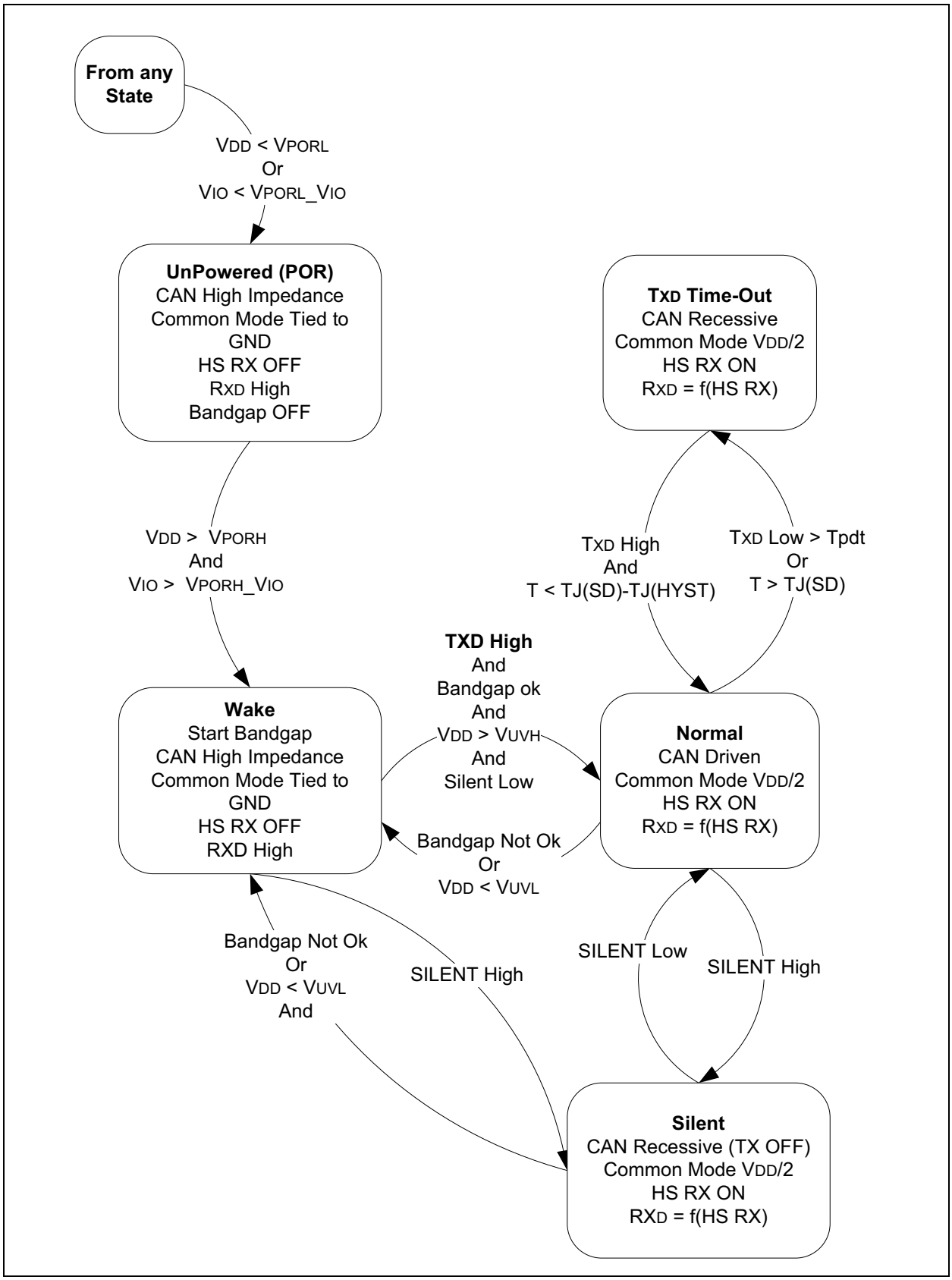
The high-speed differential receiver is active.

1.6.4 SILENT MODE

The device may be placed in Silent mode by applying a high level to the ‘S’ pin (pin 8). In Silent mode, the transmitter is disabled and the CAN bus is biased to $V_{DD}/2$. The high-speed differential receiver is active.

The CAN controller must put the MCP2557FD/8FD back into Normal mode to enable the transmitter.

FIGURE 1-1: MCP2557FD/8FD STATE DIAGRAM



1.7 Pin Descriptions

The descriptions of the pins are listed in Table 1-1.

TABLE 1-1: MCP2557FD/8FD PIN DESCRIPTIONS

MCP2557FD 3 x 3 DFN, 2 x 3 TDFN	**MCP2557FD** SOIC	**MCP2558FD** 3 x 3 DFN, 2 x 3 TDFN	**MCP2558FD** SOIC	**Symbol**	**Pin Function**
1	1	1	1	TXD	Transmit Data Input
2	2	2	2	VSS	Ground
3	3	3	3	VDD	Supply Voltage
4	4	4	4	RXD	Receive Data Output
5	5	—	—	NC	No Connect (**MCP2557FD** only)
—	—	5	5	VIO	Digital I/O Supply Pin (**MCP2558FD** only)
6	6	6	6	CANL	CAN Low-Level Voltage I/O
7	7	7	7	CANH	CAN High-Level Voltage I/O
8	8	8	8	S	Silent Mode Input
9	—	9	—	EP	Exposed Thermal Pad

1.7.1 TRANSMITTER DATA INPUT PIN (TXD)

The CAN transceiver drives the differential output pins CANH and CANL according to TXD. It is usually connected to the transmitter data output of the CAN controller device. When TXD is Low, CANH and CANL are in the Dominant state. When TXD is High, CANH and CANL are in the Recessive state, provided that another CAN node is not driving the CAN bus with a Dominant state. TXD is connected from an internal pull-up resistor (nominal 33 kΩ) to VDD or VIO, in the MCP2557FD or MCP2558FD, respectively.

1.7.2 GROUND SUPPLY PIN (VSS)

Ground supply pin.

1.7.3 SUPPLY VOLTAGE PIN (VDD)

Positive supply voltage pin. Supplies transmitter and receiver.

1.7.4 RECEIVER DATA OUTPUT PIN (RXD)

RXD is a CMOS-compatible output that drives High or Low depending on the differential signals on the CANH and CANL pins, and is usually connected to the receiver data input of the CAN controller device. RXD is High when the CAN bus is Recessive, and Low in the Dominant state. RXD is supplied by VDD or VIO, in the MCP2557FD or MCP2558FD, respectively.

1.7.5 NC PIN (MCP2557FD)

No Connect. This pin can be left open or connected to VSS.

1.7.6 VIO PIN (MCP2557FD)

Supply for digital I/O pins. In the MCP2557FD, the supply for the digital I/O (TXD, RXD and S) is internally connected to VDD.

1.7.7 DIGITAL I/O

The MCP2557FD/8FD enable easy interfacing to MCUs with I/O ranges from 1.8V to 5V.

1.7.7.1 MCP2557FD

The VIH(MIN) and VIL(MAX) for TXD are independent of VDD. They are set at levels that are compatible with 3V and 5V microcontrollers.

The RXD pin is always driven to VDD; therefore, a 3V microcontroller will need a 5V tolerant input.

1.7.7.2 MCP2558FD

VIH and VIL for S and TXD depend on VIO. The RXD pin is driven to VIO.

1.7.8 CAN LOW PIN (CANL)

The CANL output drives the Low side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANL disconnects from the bus when the MCP2557FD/8FD devices are not powered.

1.7.9 CAN HIGH PIN (CANH)

The CANH output drives the high side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANH disconnects from the bus when the MCP2557FD/8FD devices are not powered.

1.7.10 SILENT MODE INPUT PIN (S)

This pin sets Normal or Silent mode. In Silent mode, the transmitter is off and the high-speed receiver is active. The CAN bus common mode voltage is $V_{DD}/2$ when in Silent mode.

The 'S' pin (pin 8) is connected to an internal MOS pull-up resistor to V_{DD} or V_{IO}, in the MCP2557FD or MCP2558FD, respectively. The value of the MOS pull-up resistor depends on the supply voltage. Typical values are 660 kΩ for 5V, 1.1 MΩ for 3.3V and 4.4 MΩ for 1.8V

1.7.11 EXPOSED THERMAL PAD (EP)

It is recommended to connect this pad to V_{SS} to enhance electromagnetic immunity and thermal resistance.

1.8 TYPICAL APPLICATION

Figure 1-2 shows a typical application for the MCP2557FD with the NC pin and a split termination.

Figure 1-3 illustrates a typical application for the MCP2558FD.

FIGURE 1-2: MCP2557FD WITH NC AND SPLIT TERMINATION

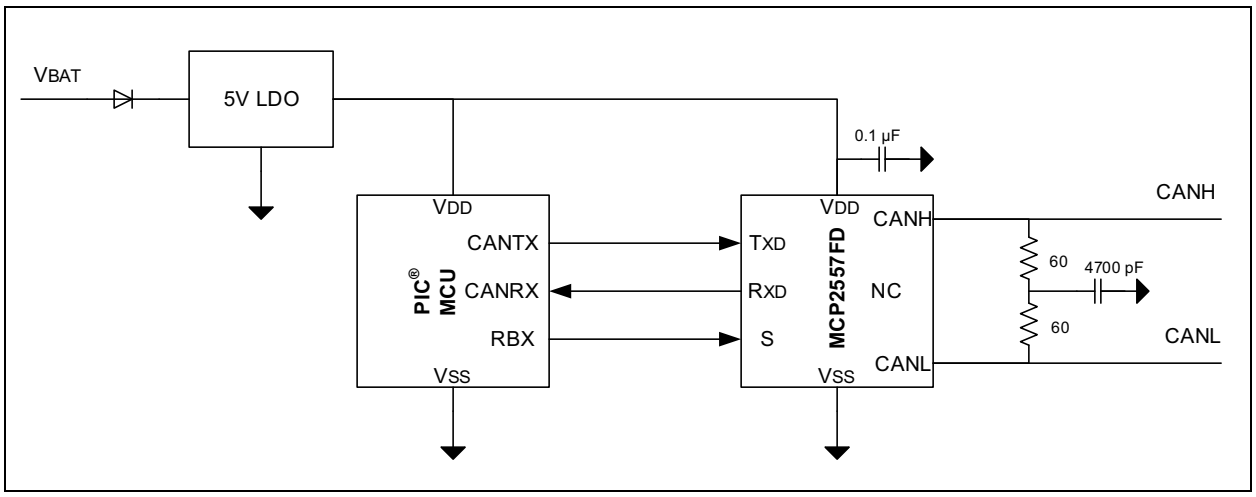
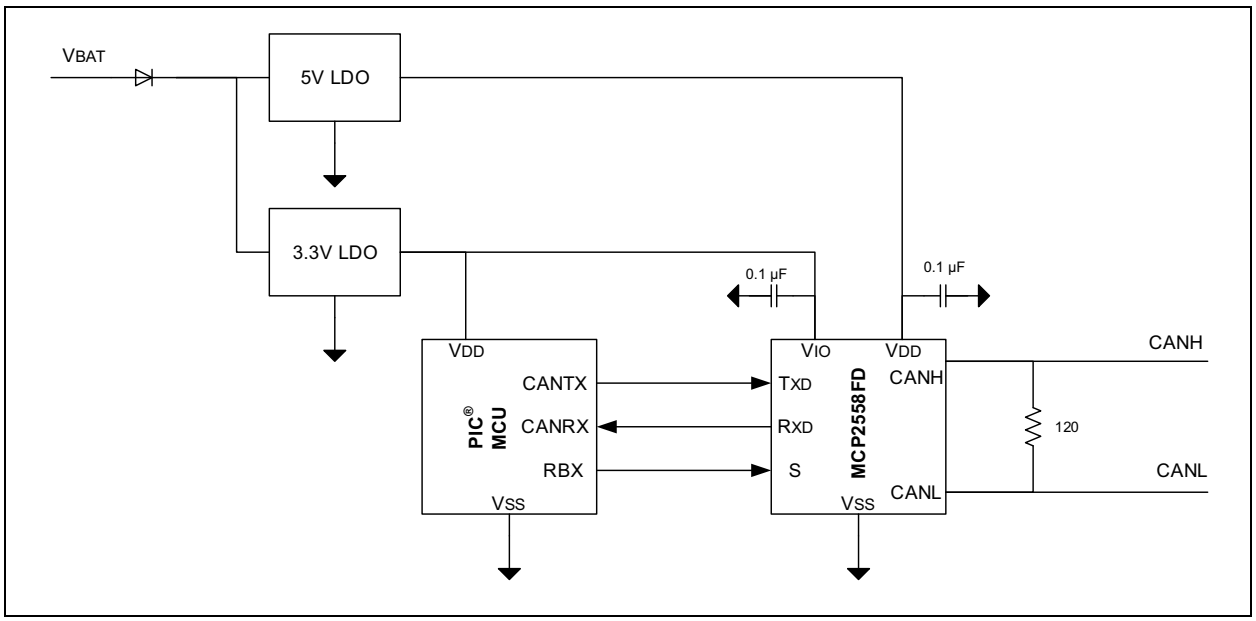


FIGURE 1-3: MCP2558FD WITH VIO PIN



2.0 ELECTRICAL CHARACTERISTICS

2.1 Terms and Definitions

A number of terms are defined in ISO/DIS-11898 that are used to describe the electrical characteristics of a CAN transceiver device. These terms and definitions are summarized in this section.

2.1.1 BUS VOLTAGE

V_{CANL} and V_{CANH} denote the voltages of the bus line wires CANL and CANH relative to the ground of each individual CAN node.

2.1.2 COMMON MODE BUS VOLTAGE RANGE

Boundary voltage levels of V_{CANL} and V_{CANH} with respect to ground, for which proper operation will occur, if the maximum number of CAN nodes are connected to the bus.

2.1.3 DIFFERENTIAL INTERNAL CAPACITANCE, C_{DIFF} (OF A CAN NODE)

Capacitance seen between CANL and CANH during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.4 DIFFERENTIAL INTERNAL RESISTANCE, R_{DIFF} (OF A CAN NODE)

Resistance seen between CANL and CANH during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.5 DIFFERENTIAL VOLTAGE, V_{DIFF} (OF CAN BUS)

Differential voltage of the two-wire CAN bus, with value equal to $V_{DIFF} = V_{CANH} – V_{CANL}$.

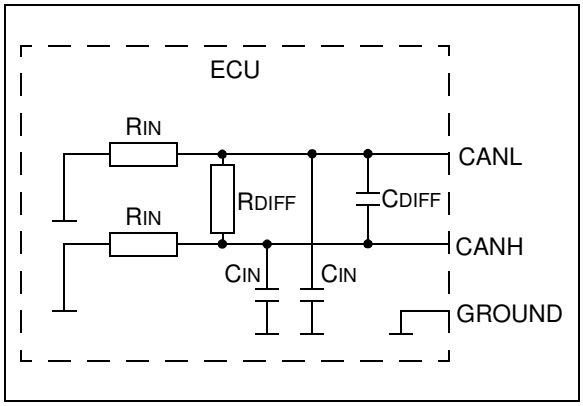
2.1.6 INTERNAL CAPACITANCE, C_{IN} (OF A CAN NODE)

Capacitance seen between CANL (or CANH) and ground during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.7 INTERNAL RESISTANCE, R_{IN} (OF A CAN NODE)

Resistance seen between CANL (or CANH) and ground during the Recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

FIGURE 2-1: PHYSICAL LAYER DEFINITIONS



2.2 Absolute Maximum Ratings†

V_{DD} 7.0V
V_{IO} 7.0V
DC Voltage at T_{XD}, R_{XD}, S and V_{SS} ..... -0.3V to V_{IO} + 0.3V
DC Voltage at CANH, and CANL ..... -58V to +58V
Transient Voltage on CANH, and CANL (ISO/DIS-7637) (Figure 2-5) ..... -150V to +100V
Differential Bus Input Voltage V_{DIFF}(I) (t = 60 days, continuous) ..... -5V to +10V
Differential Bus Input Voltage V_{DIFF}(I) (1000 pulses, t = 0.1 ms, V_{CANH} = +18V) ..... +17V
Dominant State Detection V_{DIFF}(I) (10000 pulses, t = 1 ms) ..... +9V
Storage temperature ..... -55°C to +150°C
Operating ambient temperature ..... -40°C to +150°C
Virtual Junction Temperature, T_{VJ} (IEC60747-1) ..... -40°C to +190°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD protection on CANH and CANL pins (IEC 61000-4-2) ..... ±13 kV
ESD protection on CANH and CANL pins (IEC 801; Human Body Model) ..... ±8 kV
ESD protection on all other pins (IEC 801; Human Body Model) ..... ±4 kV
ESD protection on all pins (IEC 801; Machine Model) ..... ±400V
ESD protection on all pins (IEC 801; Charge Device Model) ..... ±750V

† Notice: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 2-1: DC CHARACTERISTICS

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply						
V_{DD} Pin						
Voltage Range	V_{DD}	4.5	—	5.5	V	
Supply Current	I_{DD}	—	2.5	5	mA	Recessive; V_{TXD} = V_{DD}
		—	55	70		Dominant; V_{TXD} = 0V
Silent Current	I_{DDS}	—	1	3	mA	**MCP2557FD**
		—	1	3		**MCP2558FD** Includes I_{IO}
Maximum Supply Current	I_{DDMAX}	—	95	140	mA	Fault condition: V_{TXD} = V_{SS}; V_{CANH} = V_{CANL} = -5V to +18V
High Level of the POR Comparator for V_{DD}	V_{PORH}	—	3.0	3.95	V	Note 1
Low Level of the POR Comparator for V_{DD}	V_{PORL}	1.0	2.0	3.2	V	Note 1
Hysteresis of POR Comparator for V_{DD}	V_{PORD}	0.2	0.9	2.0	V	Note 1
High Level of the UV Comparator for V_{DD}	V_{UVH}	4.0	4.25	4.4	V	
Low Level of the UV Comparator for V_{DD}	V_{UVL}	3.6	3.8	4.0	V	
Hysteresis of UV comparator	V_{UVD}	—	0.4	—	V	Note 1
V_{IO} Pin						
Digital Supply Voltage Range	V_{IO}	1.7	—	5.5	V	
Supply Current on V_{IO}	I_{IO}	—	7	30	µA	Recessive; V_{TXD} = V_{IO}
		—	200	400		Dominant; V_{TXD} = 0V
High Level of the POR Comparator for V_{IO}	V_{PORH_VIO}	0.8	1.2	1.7	V	
Low Level of the POR Comparator for VIO	V_{PORL_VIO}	0.7	1.1	1.4	V	
Hysteresis of POR Comparator for V_{IO}	V_{PORD_VIO}	—	0.2	—	V	
Bus Line (CANH; CANL) Transmitter						
CANH; CANL: Recessive Bus Output Voltage	$V_{O(R)}$	2.0	0.5 V_{DD}	3.0	V	V_{TXD} = V_{DD}; No load
Recessive Output Current	$I_{O(R)}$	-5	—	+5	mA	-24V < V_{CAN} < +24V
CANH: Dominant Output Voltage	$V_{O(D)}$	2.75	3.50	4.50	V	T_{XD} = 0; R_L = 50 to 65Ω
CANL: Dominant Output Voltage		0.50	1.50	2.25		R_L = 50Ω to 65Ω
Driver Symmetry (V_{CANH}+V_{CANL})/V_{DD}	V_{SYM}	0.9	1.0	1.1	V	1 MHz square wave, Recessive and Dominant states, and transition (Note 1)

Note 1: Characterized; not 100% tested.

2: Only MCP2558FD has a V_{IO} pin. For MCP2557FD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, and tested from -2V to 7V.

TABLE 2-1: DC CHARACTERISTICS (CONTINUED)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Dominant: Differential Output Voltage	$V_{O(DIFF)(D)}$	1.5	2.0	3.0	V	V_{TXD} = V_{SS}; R_L = 50Ω to 65Ω (Figure 2-2, Figure 2-4) (Note 1)
		1.4	2.0	3.0		V_{TXD} = V_{SS}; R_L = 45Ω to 70Ω (Figure 2-2, Figure 2-4, Section 3) (Note 1)
		1.3	2.0	3.0		V_{TXD} = V_{SS}; R_L = 40Ω to 75Ω (Figure 2-2, Figure 2-4, Section 3)
		1.5	—	5.0		V_{TXD} = V_{SS}; R_L = 2240Ω (Figure 2-2, Figure 2-4, Section 3) (Note 1)
Recessive: Differential Output Voltage	$V_{O(DIFF)(R)}$	-500	0	50	mV	V_{TXD} = V_{DD}, no load (Figure 2-2, Figure 2-4)
CANH: Short-Circuit Output Current	$I_{O(SC)}$	-115	-85	—	mA	V_{TXD} = V_{SS}; V_{CANH} = -3V; CANL: floating
CANL: Short Circuit Output Current		—	75	+115	mA	V_{TXD} = V_{SS}; V_{CANL} = +18V; CANH: floating
Bus Line (CANH; CANL) Receiver						
Recessive Differential Input Voltage	$V_{DIFF(R)(I)}$	-4.0	—	+0.5	V	-12V < $V_{(CANH, CANL)}$ < +12V; see Figure 2-6 (Note 3)
Dominant Differential Input Voltage	$V_{DIFF(D)(I)}$	0.9	—	9.0	V	-12V < $V_{(CANH, CANL)}$ < +12V; see Figure 2-6 (Note 3)
Differential Receiver Threshold	$V_{TH(DIFF)}$	0.5	0.7	0.9	V	-12V < $V_{(CANH, CANL)}$ < +12V; see Figure 2-6 (Note 3)
Differential Input Hysteresis	$V_{HYS(DIFF)}$	30	—	200	mV	See Figure 2-6, (Note 1)
Single Ended Input Resistance	R_{CAN_H}, R_{CAN_L}	6	—	50	kΩ	Note 1
Internal Resistance Matching m_R=2*(R_{CANH}-R_{CANL})/(R_{CANH}+R_{CANL})	m_R	-3	0	+3	%	V_{CANH} = V_{CANL} (Note 1)
Differential Input Resistance	R_{DIFF}	12	25	100	kΩ	Note 1
Internal Capacitance	C_{IN}	—	20	—	pF	1 Mbps (Note 1)
Differential Internal Capacitance	C_{DIFF}	—	10	—	pF	1 Mbps (Note 1)
CANH, CANL: Input Leakage	I_{LI}	-5	—	+5	µA	V_{DD} = V_{TXD} = V_S = 0V. For **MCP2558FD**, V_{IO} = 0V. V_{CANH} = V_{CANL} = 5 V.
Digital Input Pins (T_{XD}, S)						
High-Level Input Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V	**MCP2557FD**
		0.7 V_{IO}	—	V_{IO} + 0.3		**MCP2558FD**

Note 1: Characterized; not 100% tested.

2: Only MCP2558FD has a V_{IO} pin. For MCP2557FD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, and tested from -2V to 7V.

TABLE 2-1: DC CHARACTERISTICS (CONTINUED)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF; unless otherwise specified.					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Low-Level Input Voltage	V_{IL}	-0.3	—	0.8	V	**MCP2557FD**
		-0.3	—	0.3V_{IO}		**MCP2558FD**
High-Level Input Current	I_{IH}	-1	—	+1	µA	
TXD: Low-Level Input Current	$I_{IL(TXD)}$	-270	-150	-30	µA	
S: Low-Level Input Current	$I_{IL(S)}$	-30	—	-1	µA	
Receive Data (RXD) Output						
High-Level Output Voltage	V_{OH}	V_{DD} - 0.4	—	—	V	**MCP2557FD**: I_{OH} = -2 mA; typical -4 mA
		V_{IO} - 0.4	—	—		**MCP2558FD:** V_{IO} = 2.7V to 5.5V, I_{OH} = -1 mA; V_{IO} = 1.7V to 2.7V, I_{OH} = -0.5 mA, typical -2 mA
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; typical 8 mA
Thermal Shutdown						
Shutdown Junction Temperature	$T_{J(SD)}$	165	175	185	°C	-12V < V(CANH, CANL) < +12V (Note 1)
Shutdown Temperature Hysteresis	$T_{J(HYST)}$	15	—	30	°C	-12V < V(CANH, CANL) < +12V (Note 1)

Note 1: Characterized; not 100% tested.

2: Only MCP2558FD has a V_{IO} pin. For MCP2557FD, V_{IO} is internally connected to V_{DD}.

3: -12V to 12V is ensured by characterization, and tested from -2V to 7V.

FIGURE 2-2: PHYSICAL BIT REPRESENTATION AND SIMPLIFIED BIAS IMPLEMENTATION

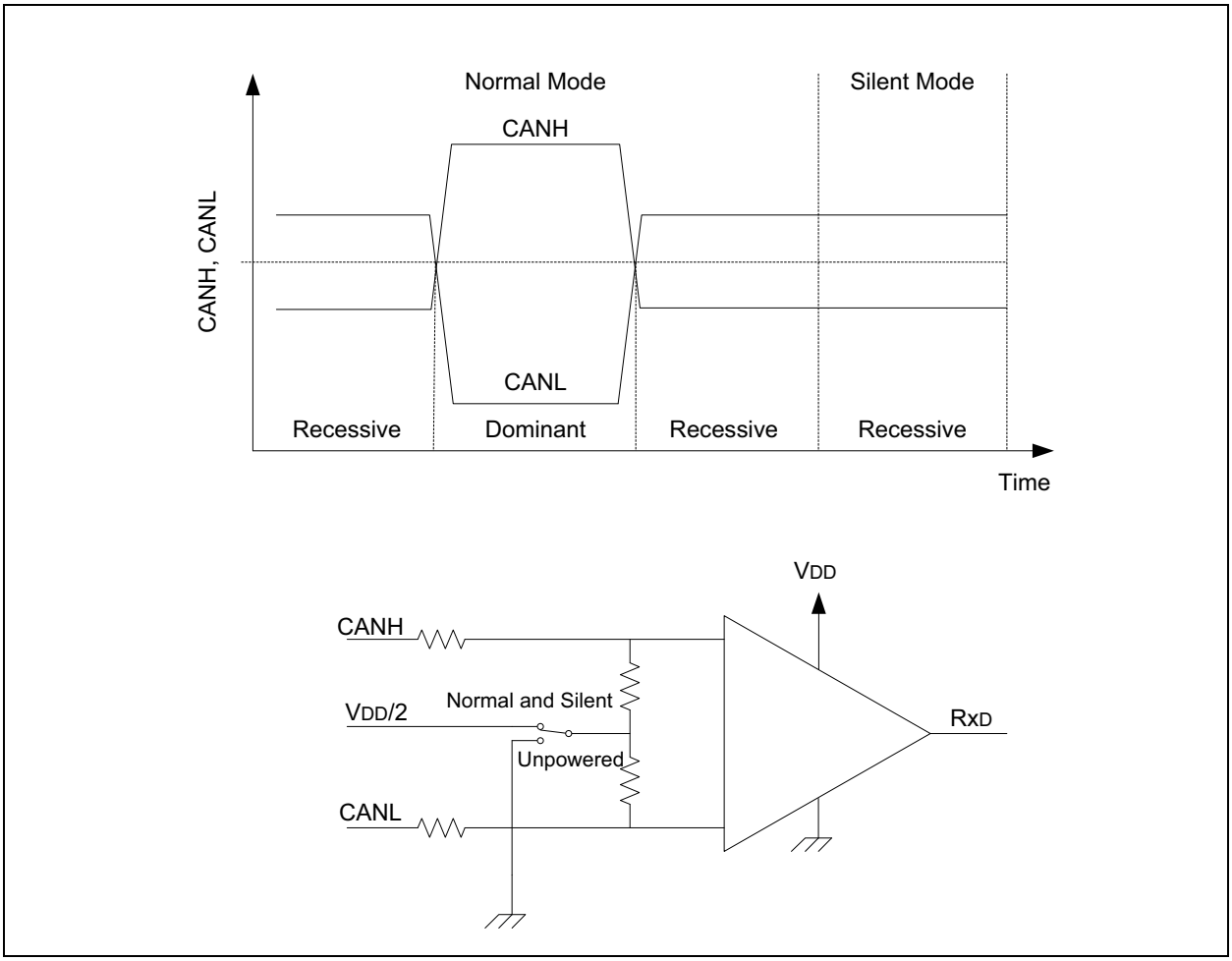


TABLE 2-2: AC CHARACTERISTICS

AC Characteristics		**Electrical Characteristics:** Unless otherwise indicated, T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF. Maximum $V_{DIFF(D)(I)}$ = 3V.					
Param. No.	**Parameter**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
1	Bit Time	t_{BIT}	0.125	—	69.44	µs	
2	Nominal Bit Rate	NBR	14.4	—	8000	kbps	
3	Delay T_{XD} Low to Bus Dominant	$t_{TXD-BUSON}$	—	50	85	ns	Note 1
4	Delay T_{XD} High to Bus Recessive	$t_{TXD-BUSOFF}$	—	40	85	ns	Note 1
5	Delay Bus Dominant to R_{XD}	$t_{BUSON-RXD}$	—	70	85	ns	Note 1
6	Delay Bus Recessive to R_{XD}	$t_{BUSOFF-RXD}$	—	110	145	ns	Note 1

Note 1: Characterized, not 100% tested.

2: Not in ISO/DIS-11898-2:2015, but needs to be characterized.

TABLE 2-2: AC CHARACTERISTICS (CONTINUED)

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF. Maximum $V_{DIFF(D)(I)}$ = 3V.					
Param. No.	**Parameter**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
7	Propagation Delay TXD to RXD Worst Case of tLOOP(R) and tLOOP(F) Figure 2-9	tTXD - RXD	—	90	120	ns	
			—	115	150		R_L = 150Ω, C_L = 200 pF(Note 1)
7a	Propagation Delay, Rising Edge	tLOOP(R)	—	90	120	ns	
7b	Propagation Delay, Falling Edge	tLOOP(F)	—	80	120	ns	
8a	Recessive Bit Time on RXD – 1 Mbps, Loop Delay Symmetry (Note 2)	tBIT(RXD), 1M	900	985	1100	ns	tBIT(TXD) = 1000 ns (Figure 2-9)
			800	960	1255		tBIT(TXD) = 1000 ns (Figure 2-9), R_L = 150Ω, C_L = 200 pF (Note 1)
8b	Recessive Bit Time on RXD – 2 Mbps, Loop Delay Symmetry	tBIT(RXD), 2M	450	490	550	ns	tBIT(TXD) = 500 ns (Figure 2-9)
			400	460	550		tBIT(TXD) = 500 ns (Figure 2-9), R_L = 150Ω, C_L = 200 pF (Note 1)
8c	Recessive Bit Time on RXD – 5 Mbps, Loop Delay Symmetry	tBIT(RXD), 5M	160	190	220	ns	tBIT(TXD) = 200 ns (Figure 2-9)
8d	Recessive Bit Time on RXD – 8 Mbps, Loop Delay Symmetry (Note 2)	tBIT(RXD), 8M	85	100	135	ns	tBIT(TXD) = 120 ns (Figure 2-9) (Note 1)
10	Delay Silent to Normal Mode	tWAKE	—	7	30	µs	Negative edge on S
11	Permanent Dominant Detect Time	tPDT	0.8	1.9	5	ms	TXD = 0V
12	Permanent Dominant Timer Reset	tPDTR	—	5	—	ns	The shortest recessive pulse on TXD or CAN bus to reset Permanent Dominant Timer
13a	Transmitted Bit Time on Bus – 1 Mbps (Note 2)	tBIT(BUS), 1M	870	1000	1060	ns	tBIT(TXD) = 1000 ns (Figure 2-9)
			870	1000	1060		tBIT(TXD) = 1000 ns (Figure 2-9), R_L = 150Ω, C_L = 200 pF (Note 1)
13b	Transmitted Bit Time on Bus – 2 Mbp	tBIT(BUS), 2M	435	515	530	ns	tBIT(TXD) = 500 ns (Figure 2-9)
			435	480	550		tBIT(TXD) = 500 ns (Figure 2-9) R_L = 150Ω, C_L = 200 pF (Note 1)

Note 1: Characterized, not 100% tested.

2: Not in ISO/DIS-11898-2:2015, but needs to be characterized.

TABLE 2-2: AC CHARACTERISTICS (CONTINUED)

AC Characteristics		Electrical Characteristics: Unless otherwise indicated, T_{AMB} = -40°C to +150°C; V_{DD} = 4.5V to 5.5V, V_{IO} = 1.7V to 5.5V (Note 2), R_L = 60Ω, C_L = 100 pF. Maximum $V_{DIFF(D)(I)}$ = 3V.					
Param. No.	**Parameter**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
13c	Transmitted Bit Time on Bus – 5 Mbps	$t_{BIT(BUS)}$, 5M	155	200	210	ns	$t_{BIT(TXD)}$ = 200 ns (Figure 2-9) (Note 1)
13d	Transmitted Bit Time on Bus - 8Mbps (Note 2)	$t_{BIT(BUS)}$, 8M	100	125	140	ns	$t_{BIT(TXD)}$ = 120 ns (Figure 2-9) (Note 1)
14a	Receiver Timing Symmetry – 1 Mbps (Note 2)	$t_{DIFF(REC)}$, 1M = $t_{BIT(RXD)}$ - $t_{BIT(BUS)}$	-65	0	40	ns	$t_{BIT(TXD)}$ = 1000 ns (Figure 2-9)
			-130	0	80		$t_{BIT(TXD)}$ = 1000 ns (Figure 2-9), R_L = 150Ω, C_L = 200 pF (Note 1)
14b	Receiver Timing Symmetry – 2 Mbps	$t_{DIFF(REC)}$, 2M	-65	0	40	ns	$t_{BIT(TXD)}$ = 500 ns (Figure 2-9)
			-70	0	40		$t_{BIT(TXD)}$ = 500 ns (Figure 2-9), R_L = 150Ω, C_L = 200 pF (Note 1)
14c	Receiver Timing Symmetry – 5 Mbps	$t_{DIFF(REC)}$, 5M	-45	0	15	ns	$t_{BIT(TXD)}$ = 200 ns (Figure 2-9) (Note 1)
14d	Receiver Timing Symmetry – 8 Mbps (Note 2) $t_{DIFF(REC),8M}$	$t_{DIFF(REC)}$, 8M	-45	0	10	ns	$t_{BIT(TXD)}$ = 120 ns (Figure 2-9) (Note 1)

Note 1: Characterized, not 100% tested.

2: Not in ISO/DIS-11898-2:2015, but needs to be characterized.

FIGURE 2-3: TEST LOAD CONDITIONS

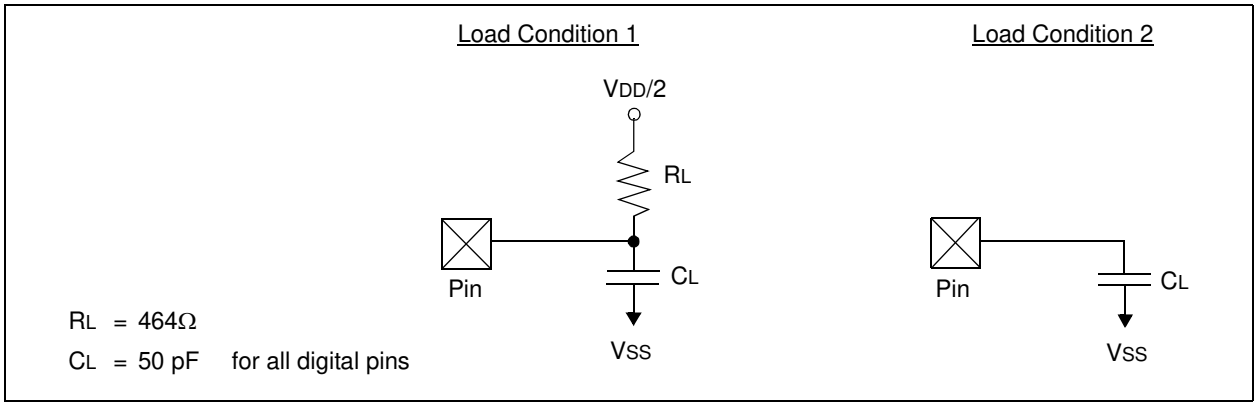
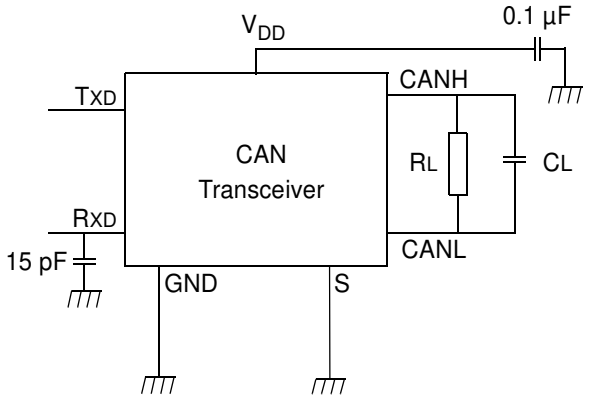
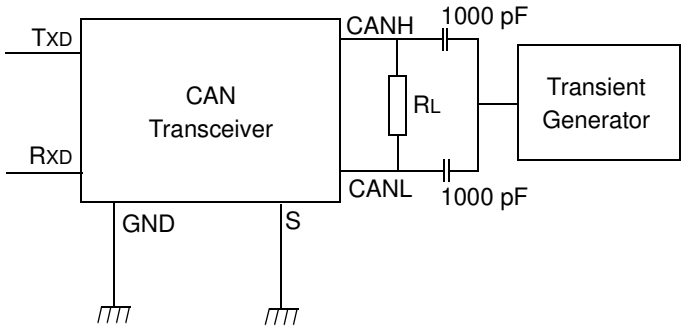


FIGURE 2-4: TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS



Note: On MCP2558FD, VIO is connected to VDD.

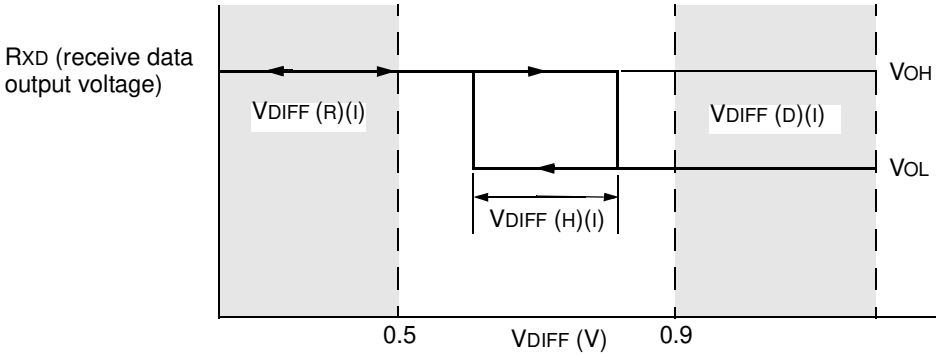
FIGURE 2-5: TEST CIRCUIT FOR AUTOMOTIVE TRANSIENTS



Note 1: On MCP2558FD, VIO is connected to VDD.

2: The wave forms of the applied transients should comply with ISO/DIS-7637, Part 1, test pulses 1, 2, 3a and 3b.

FIGURE 2-6: HYSTERESIS OF THE RECEIVER



2.3 Timing Diagrams and Specifications

FIGURE 2-7: TIMING DIAGRAM FOR AC CHARACTERISTICS

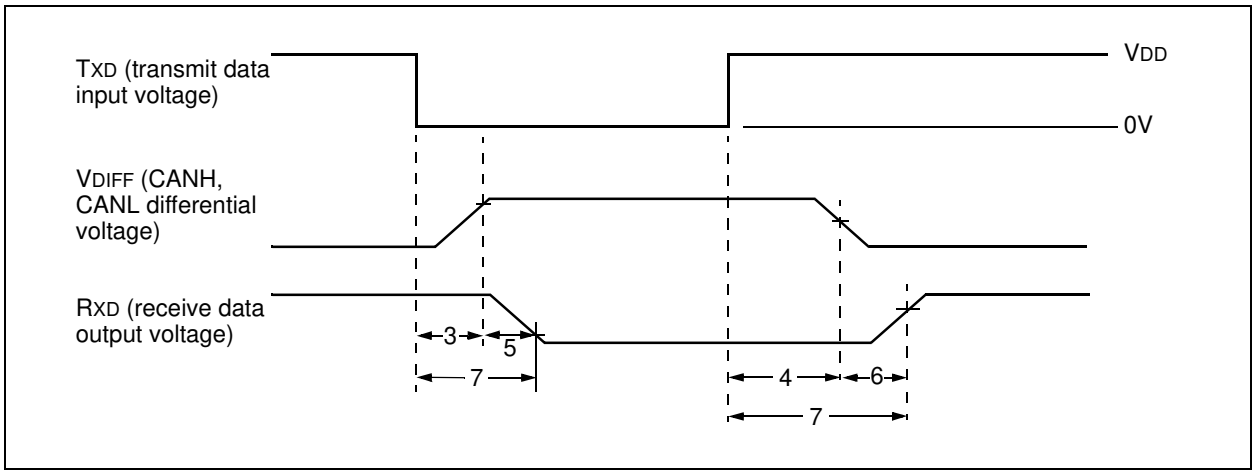


FIGURE 2-8: PERMANENT DOMINANT TIMER RESET DETECT

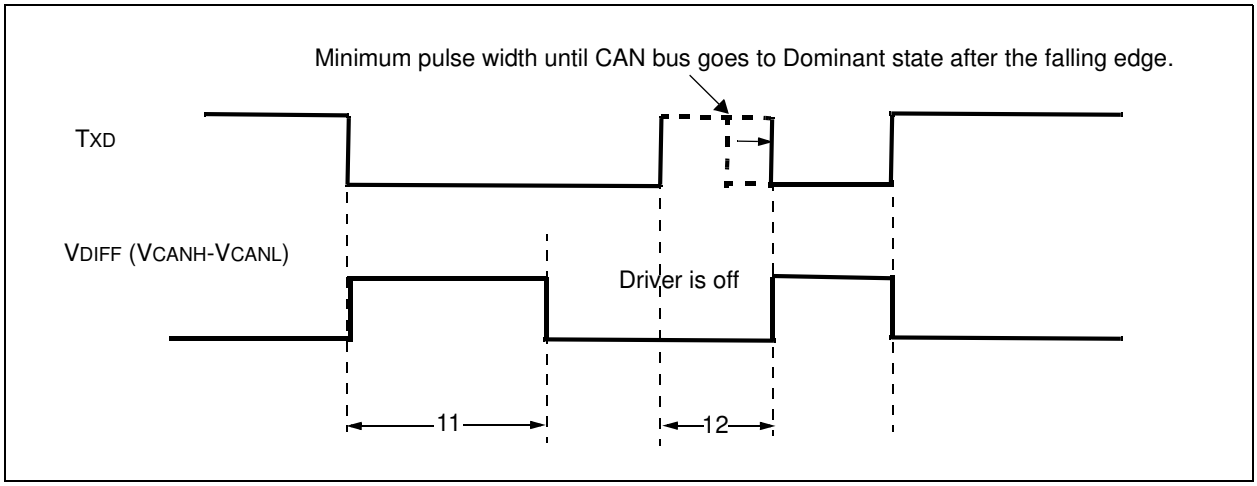
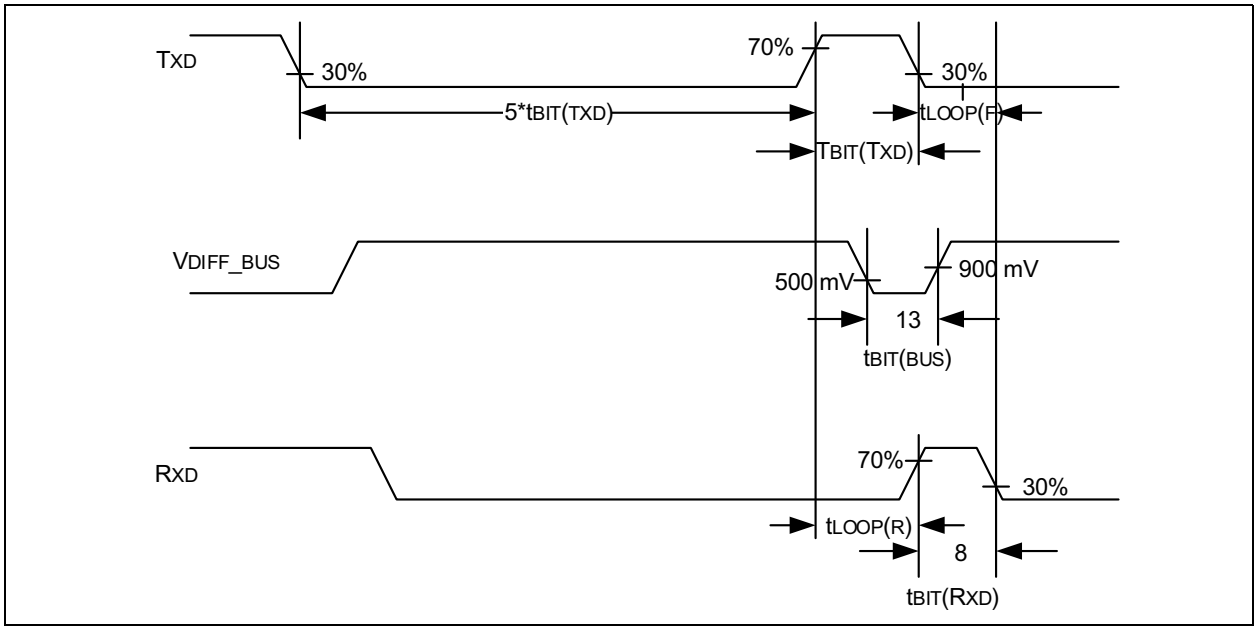


FIGURE 2-9: TIMING DIAGRAM FOR LOOP DELAY SYMMETRY



2.4 Thermal Specifications

Parameter	Sym.	Min.	Typ.	Max.	Units
Temperature Ranges					
Specified Temperature Range	T_A	-40	—	+150	°C
Operating Temperature Range	T_A	-40	—	+150	°C
Storage Temperature Range	T_A	-65	—	+155	°C
Package Thermal Resistances					
Thermal Resistance, 8LD DFN (3x3)	θ_{JA}	—	56.7	—	°C/W
Thermal Resistance, 8LD SOIC	θ_{JA}	—	149.5	—	°C/W
Thermal Resistance, 8LD TDFN (2x3)	θ_{JA}	—	53	—	°C/W

3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

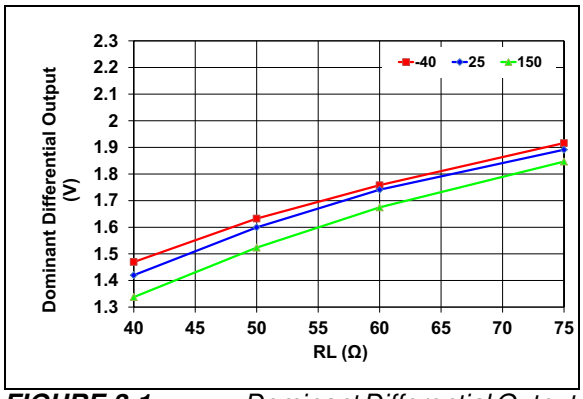


FIGURE 3-1: *Dominant Differential Output vs. RL (V_{DD} = 4.5V).*

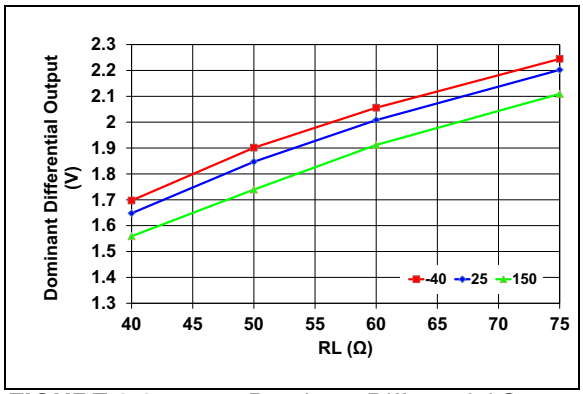


FIGURE 3-2: *Dominant Differential Output vs. RL (V_{DD} = 5.0V).*

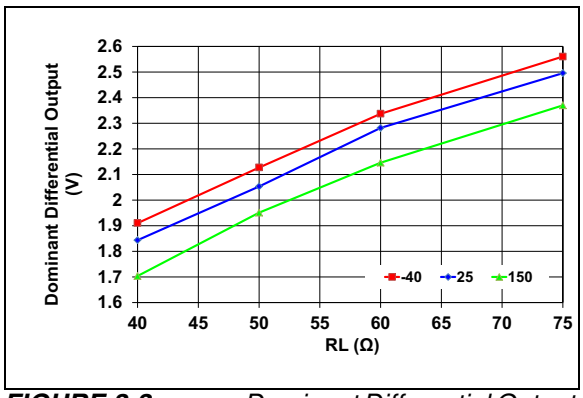
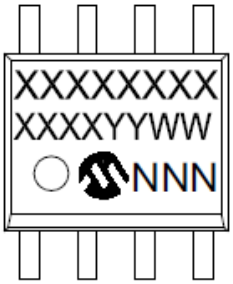


FIGURE 3-3: *Dominant Differential Output vs. RL (V_{DD} = 5.5V).*

4.0 PACKAGING INFORMATION

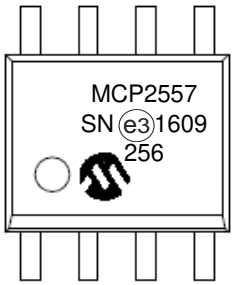
4.1 Package Marking Information

8-Lead SOIC (150 mil)



Part Number	Code
MCP2557FDT-H/SN	MCP2557
MCP2557FD-H/SN	MCP2557
MCP2558FDT-H/SN	MCP2558
MCP2558FD-H/SN	MCP2558

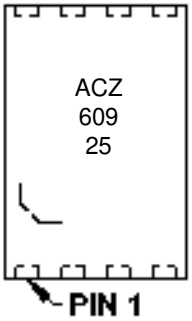
Example:



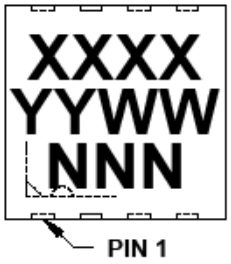
8-Lead TDFN (02x03x0.8 mm)

Part Number	Code
MCP2557FDT-H/MNY	ACZ
MCP2558FDT-H/MNY	ADA

Example:

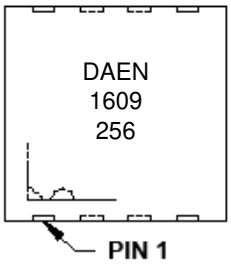


8-Lead DFN (03x03x0.9 mm)



Part Number	Code
MCP2557FDT-H/MF	DAEO
MCP2557FD-H/MF	DAEO
MCP2558FDT-H/MF	DAEQ
MCP2558FD-H/MF	DAEQ

Example:

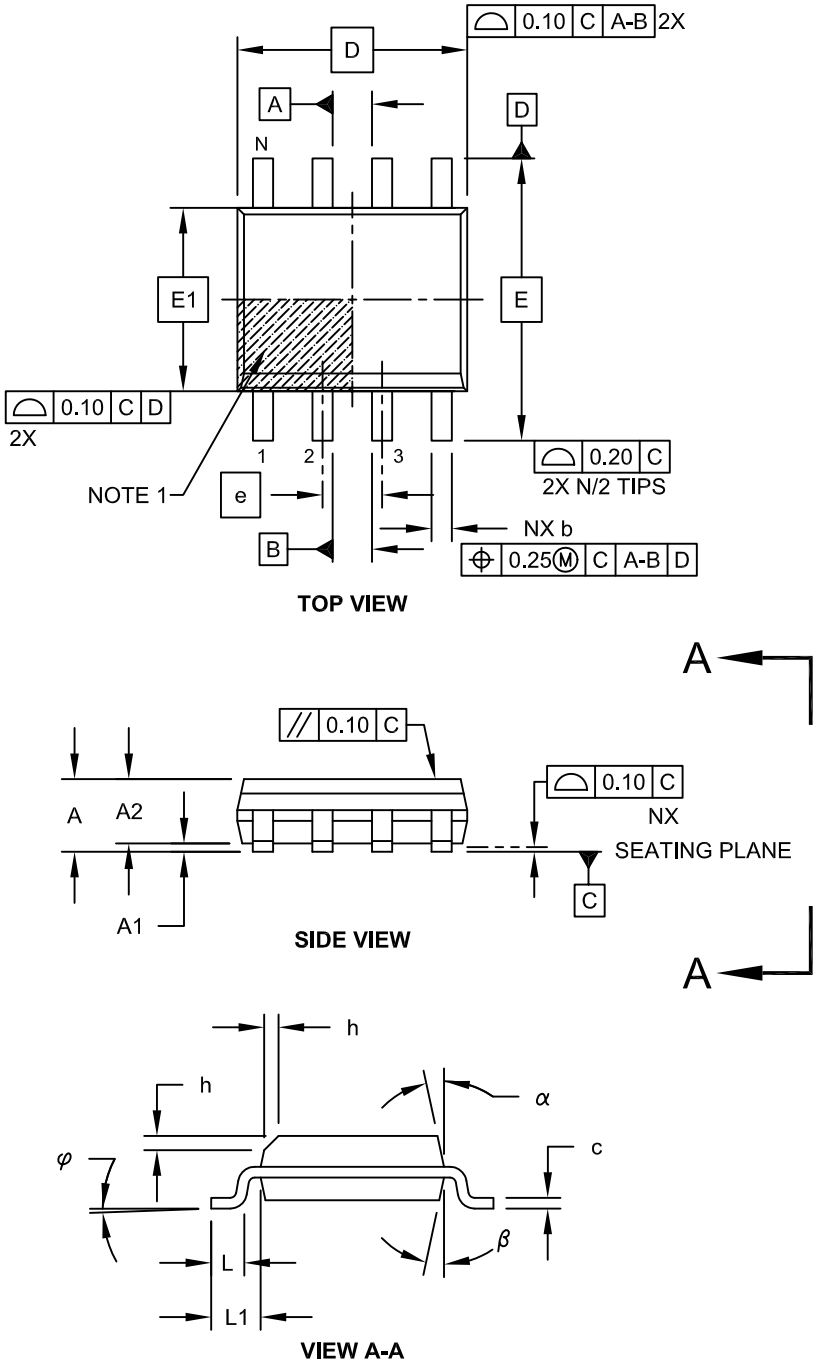


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC® designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

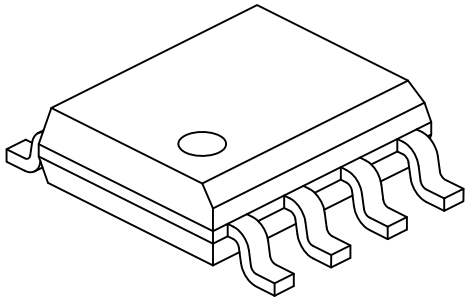
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

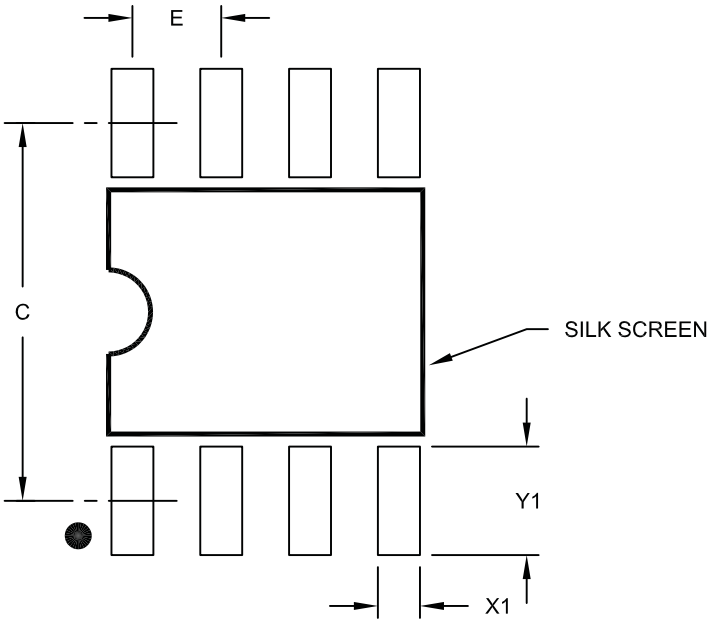
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

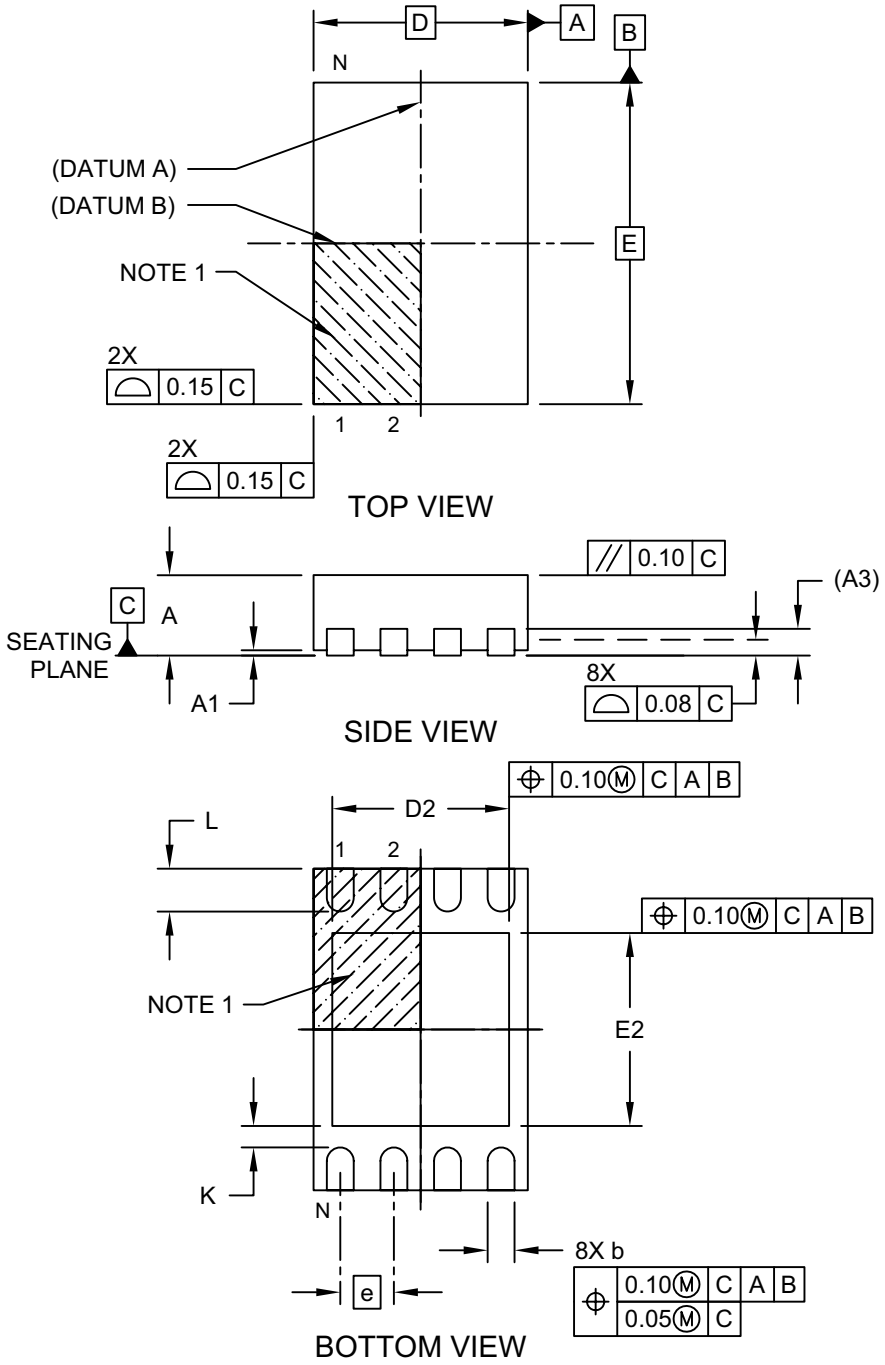
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129-MN Rev D Sheet 2 of 2