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## 16-Bit, Multi-Channel $\Delta\Sigma$ Analog-to-Digital Converter with I<sup>2</sup>C™ Interface and On-Board Reference

### Features

- 16-bit  $\Delta\Sigma$  ADC with Differential Inputs:
  - 2 channels: MCP3426 and MCP3427
  - 4 channels: MCP3428
- Differential Input Full Scale Range:  $-V_{REF}$  to  $+V_{REF}$
- Self Calibration of Internal Offset and Gain per Each Conversion
- On-Board Voltage Reference ( $V_{REF}$ ):
  - Accuracy:  $2.048V \pm 0.05\%$
  - Drift: 15 ppm/°C
- On-Board Programmable Gain Amplifier (PGA):
  - Gains of 1, 2, 4 or 8
- INL: 10 ppm of Full Scale Range
- Programmable Data Rate Options:
  - 15 SPS (16 bits)
  - 60 SPS (14 bits)
  - 240 SPS (12 bits)
- One-Shot or Continuous Conversion Options
- Low Current Consumption ( $V_{DD} = 3V$ ):
  - Continuous Conversion: 135  $\mu A$  typical
  - One-Shot Conversion with 1 SPS:
    - 9  $\mu A$  typical for 16 bit mode
    - 2.25  $\mu A$  typical for 14 bit mode
    - 0.56  $\mu A$  typical for 12 bit mode
- On-Board Oscillator
- I<sup>2</sup>C™ Interface:
  - Standard, Fast and High Speed Modes
  - User configurable two external address selection pins for MCP3427 and MCP3428
- Single Supply Operation: 2.7V to 5.5V
- Extended Temperature Range: -40°C to +125°C

### Typical Applications

- Portable Instrumentation and Consumer Goods
- Temperature Sensing with RTD, Thermistor, and Thermocouple
- Bridge Sensing for Pressure, Strain, and Force
- Weigh Scales and Battery Fuel Gauges
- Factory Automation Equipment

### Description

The MCP3426, MCP3427 and MCP3428 devices (MCP3426/7/8) are the low noise and high accuracy 16 Bit Delta-Sigma Analog-to-Digital ( $\Delta\Sigma$  A/D) Converter family members of the MCP342X series from Microchip Technology Inc. These devices can convert analog inputs to digital codes with up to 16 bits of resolution.

The MCP3426 and MCP3427 devices have two differential input channels and the MCP3428 has four differential input channels. All electrical properties of these three devices are the same except the differences in the number of input channels and I<sup>2</sup>C address bit selection options.

These devices can output analog-to-digital conversion results at rates of 15 (16-bit mode), 60 (14-bit mode), or 240 (12-bit mode) samples per second depending on the user controllable configuration bit settings using the two-wire I<sup>2</sup>C serial interface. During each conversion, the device calibrates offset and gain errors automatically. This provides accurate conversion results from conversion to conversion over variations in temperature and power supply fluctuation.

The device has an on-board 2.048V reference voltage, which enables an input range of  $\pm 2.048V$  differentially (full scale range = 4.096V/PGA).

The user can select the gain of the on-board programmable gain amplifier (PGA) using the configuration register bits (gain of x1, x2, x4, or x8). This allows the MCP3426/7/8 devices to convert a very weak input signal with high resolution.

The MCP3426/7/8 devices have two conversion modes: (a) One-Shot Conversion mode and (b) Continuous Conversion mode. In the One-Shot conversion mode, the device performs a single conversion and enters a low current standby (shutdown) mode automatically until it receives another conversion command. This reduces current consumption greatly during idle periods. In continuous conversion mode, the conversion takes place continuously at the configured conversion speed. The device updates its output buffer with the most recent conversion data.

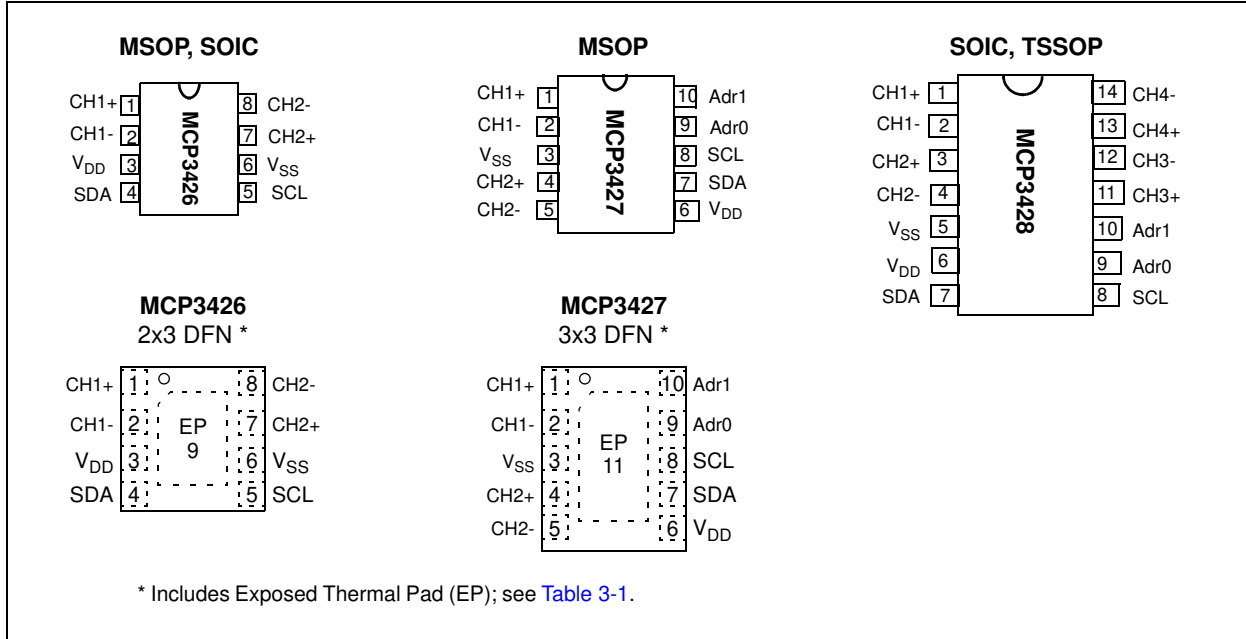
The devices operate from a single 2.7V to 5.5V power supply and have a two-wire I<sup>2</sup>C compatible serial interface for a standard (100 kHz), fast (400 kHz), or high-speed (3.4 MHz) mode.

# MCP3426/7/8

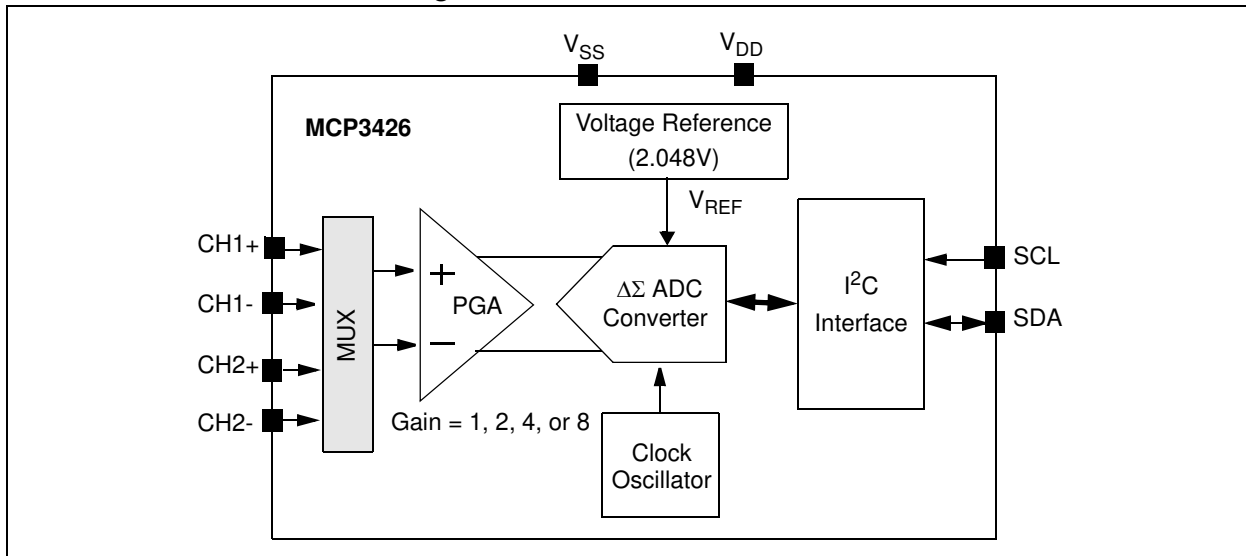
The I<sup>2</sup>C address bits for the MCP3427 and MCP3428 are selected by using two external I<sup>2</sup>C address selection pins (Adr0 and Adr1). The user can configure the device to one of eight available addresses by connecting these two address selection pins to V<sub>DD</sub>, V<sub>SS</sub> or float. The I<sup>2</sup>C address bits of the MCP3426 are programmed at the factory during production.

The MCP3426 is available in 8-pin SOIC, DFN, and MSOP packages. The MCP3427 is available in 10-pin DFN, and MSOP packages. The MCP3428 is available in 14-pin SOIC and TSSOP packages.

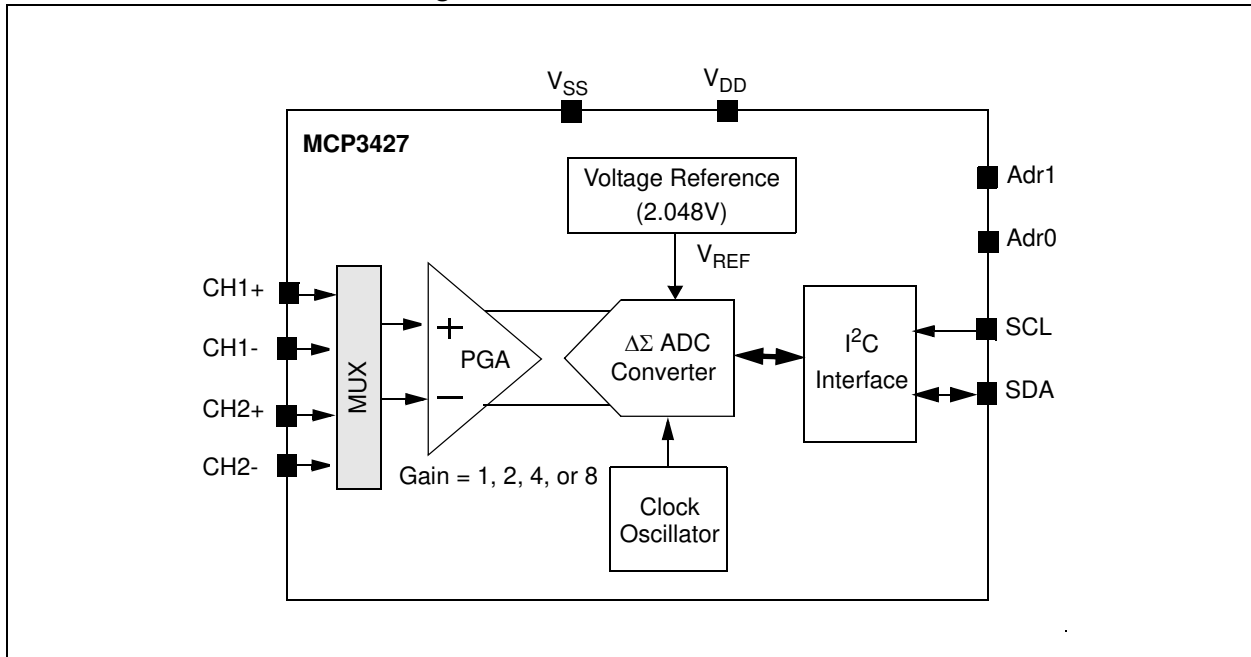
## Package Types



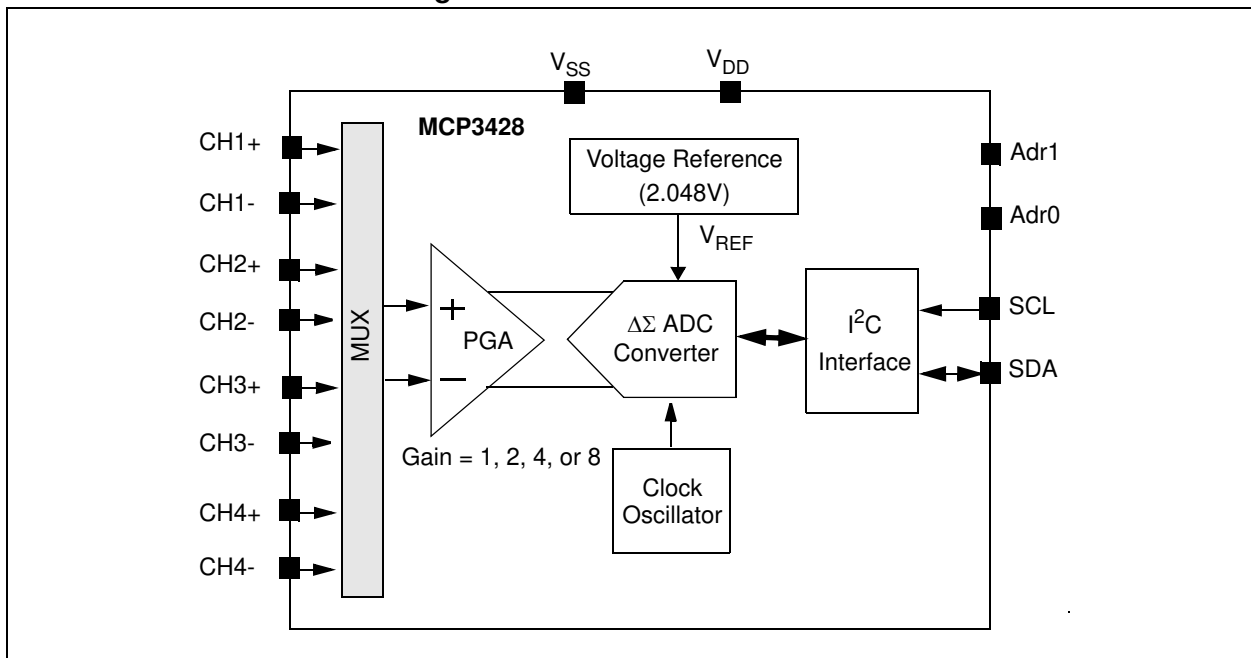
## MCP3426 Functional Block Diagram



## MCP3427 Functional Block Diagram



## MCP3428 Functional Block Diagram



# MCP3426/7/8

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NOTES:

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings†

V <sub>DD</sub> .....	7.0V
All inputs and outputs .....	V <sub>SS</sub> -0.4V to V <sub>DD</sub> +0.4V
Differential Input Voltage .....	V <sub>DD</sub> - V <sub>SS</sub>
Output Short Circuit Current .....	Continuous
Current at Input Pins .....	±2 mA
Current at Output and Supply Pins .....	±10 mA
Storage Temperature .....	-65°C to +150°C
Ambient Temp. with power applied .....	-55°C to +125°C
ESD protection on all pins .....	≥ 6 kV HBM, ≥ 400V MM
Maximum Junction Temperature (T <sub>J</sub> ) .....	+150°C

†**Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise specified, all parameters apply for T<sub>A</sub> = -40°C to +85°C, V<sub>DD</sub> = +5.0V, V<sub>SS</sub> = 0V, CHn+ = CHn- = V<sub>REF</sub>/2, V<sub>INCOM</sub> = V<sub>REF</sub>/2. All ppm units use 2\*V<sub>REF</sub> as differential full scale range.

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Analog Inputs</b>						
Differential Full Scale Input Voltage Range	FSR	—	±2.048/PGA	—	V	V <sub>IN</sub> = [CHn+ - CHn-]
Maximum Input Voltage Range		V <sub>SS</sub> -0.3	—	V <sub>DD</sub> +0.3	V	<b>(Note 1)</b>
Differential Input Impedance	Z <sub>IND</sub> (f)	—	2.25/PGA	—	MΩ	During normal mode operation <b>(Note 2)</b>
Common Mode input Impedance	Z <sub>INC</sub> (f)	—	25	—	MΩ	PGA = 1, 2, 4, 8
<b>System Performance</b>						
Resolution and No Missing Codes (Effective Number of Bits) <b>(Note 3)</b>		12	—	—	Bits	DR = 240 SPS
		14	—	—	Bits	DR = 60 SPS
		16	—	—	Bits	DR = 15 SPS
Data Rate <b>(Note 4)</b>	DR	176	240	328	SPS	12 bits mode
		44	60	82	SPS	14 bits mode
		11	15	20.5	SPS	16 bits mode
Output Noise		—	2.5	—	μV <sub>RMS</sub>	T <sub>A</sub> = +25°C, DR = 15 SPS, PGA = 1, V <sub>IN+</sub> = V <sub>IN-</sub> = GND
Integral Non-Linearity	INL	—	10	—	ppm of FSR	DR = 15 SPS <b>(Note 5)</b>
Internal Reference Voltage	V <sub>REF</sub>	—	2.048	—	V	
Gain Error <b>(Note 6)</b>		—	0.1	—	%	PGA = 1, DR = 15 SPS
PGA Gain Error Match <b>(Note 6)</b>		—	0.1	—	%	Between any 2 PGA settings
Gain Error Drift <b>(Note 6)</b>		—	15	—	ppm/°C	PGA=1, DR=15 SPS

- Note 1:** Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.
- 2:** This input impedance is due to 3.2 pF internal input sampling capacitor.
- 3:** This parameter is ensured by design and not 100% tested.
- 4:** The total conversion speed includes auto-calibration of offset and gain.
- 5:** INL is the difference between the endpoints line and the measured code at the center of the quantization band.
- 6:** Includes all errors from on-board PGA and V<sub>REF</sub>.
- 7:** This parameter is ensured by characterization and not 100% tested.
- 8:** MCP3427 and MCP3428 only.
- 9:** Addr\_Float voltage is applied at address pin.
- 10:** No voltage is applied at address pin (left “floating”).

# MCP3426/7/8

## ELECTRICAL CHARACTERISTICS (CONTINUED)

<b>Electrical Specifications:</b> Unless otherwise specified, all parameters apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{DD} = +5.0\text{V}$ , $V_{SS} = 0\text{V}$ , $\text{CHn}^+ = \text{CHn}^- = V_{REF}/2$ , $V_{INCOM} = V_{REF}/2$ . All ppm units use $2 \cdot V_{REF}$ as differential full scale range.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Offset Error	$V_{OS}$	—	30	—	$\mu\text{V}$	PGA = 1 DR = 15 SPS
Offset Drift vs. Temperature		—	50	—	$\text{nV}/^{\circ}\text{C}$	
Common-Mode Rejection		—	105	—	dB	at DC and PGA = 1,
		—	110	—	dB	at DC and PGA = 8, $T_A = +25^{\circ}\text{C}$
Gain vs. $V_{DD}$		—	5	—	$\text{ppm}/\text{V}$	$T_A = +25^{\circ}\text{C}$ , $V_{DD} = 2.7\text{V}$ to $5.5\text{V}$ , PGA = 1
Power Supply Rejection at DC Input		—	100	—	dB	$T_A = +25^{\circ}\text{C}$ , $V_{DD} = 2.7\text{V}$ to $5.5\text{V}$ , PGA = 1
<b>Power Requirements</b>						
Voltage Range	$V_{DD}$	2.7	—	5.5	V	
Supply Current during Conversion	$I_{DDA}$	—	145	180	$\mu\text{A}$	$V_{DD} = 5.0\text{V}$
		—	135	—	$\mu\text{A}$	$V_{DD} = 3.0\text{V}$
Supply Current during Standby Mode	$I_{DDS}$	—	0.3	1	$\mu\text{A}$	$V_{DD} = 5.0\text{V}$
<b>I<sup>2</sup>C Digital Inputs and Digital Outputs</b>						
High level input voltage	$V_{IH}$	$0.7V_{DD}$	—	$V_{DD}$	V	at SDA and SCL pins
Low level input voltage	$V_{IL}$	—	—	$0.3V_{DD}$	V	at SDA and SCL pins
Low level output voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 3\text{ mA}$
Hysteresis of Schmidt Trigger for inputs ( <b>Note 7</b> )	$V_{HYST}$	$0.05V_{DD}$	—	—	V	$f_{SCL} = 100\text{ kHz}$
Supply Current when I <sup>2</sup> C bus line is active	$I_{DDB}$	—	—	10	$\mu\text{A}$	Device is in standby mode while I <sup>2</sup> C bus is active
Input Leakage Current	$I_{ILH}$	—	—	1	$\mu\text{A}$	$V_{IH} = 5.5\text{V}$
	$I_{ILL}$	-1	—	—	$\mu\text{A}$	$V_{IL} = \text{GND}$
<b>Logic Status of I<sup>2</sup>C Address Pins (Note 8)</b>						
Adr0 and Adr1 Pins	Addr_Low	$V_{SS}$	—	$0.2V_{DD}$	V	The device reads logic low.
Adr0 and Adr1 Pins	Addr_High	$0.75V_{DD}$	—	$V_{DD}$	V	The device reads logic high.
Adr0 and Adr1 Pins	Addr_Float	$0.35V_{DD}$	—	$0.6V_{DD}$	V	Read pin voltage if voltage is applied to the address pin. ( <b>Note 9</b> )
		—	$V_{DD}/2$	—		Device outputs float output voltage ( $V_{DD}/2$ ) on the address pin, if left "floating". ( <b>Note 10</b> )
<b>Pin Capacitance and I<sup>2</sup>C Bus Capacitance</b>						
Pin capacitance	$C_{PIN}$	—	4	10	pF	
I <sup>2</sup> C Bus Capacitance	$C_b$	—	—	400	pF	

- Note 1:** Any input voltage below or greater than this voltage causes leakage current through the ESD diodes at the input pins. This parameter is ensured by characterization and not 100% tested.
- Note 2:** This input impedance is due to 3.2 pF internal input sampling capacitor.
- Note 3:** This parameter is ensured by design and not 100% tested.
- Note 4:** The total conversion speed includes auto-calibration of offset and gain.
- Note 5:** INL is the difference between the endpoints line and the measured code at the center of the quantization band.
- Note 6:** Includes all errors from on-board PGA and  $V_{REF}$ .
- Note 7:** This parameter is ensured by characterization and not 100% tested.
- Note 8:** MCP3427 and MCP3428 only.
- Note 9:** Addr\_Float voltage is applied at address pin.
- Note 10:** No voltage is applied at address pin (left "floating").

## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated,  $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{DD} = +5.0\text{V}$ ,  $V_{SS} = 0\text{V}$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Specified Temperature Range	$T_A$	-40	—	+85	$^{\circ}\text{C}$	
Operating Temperature Range	$T_A$	-40	—	+125	$^{\circ}\text{C}$	
Storage Temperature Range	$T_A$	-65	—	+150	$^{\circ}\text{C}$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 8L-DFN (2x3)	$\theta_{JA}$	—	84.5	—	$^{\circ}\text{C}/\text{W}$	
Thermal Resistance, 8L-MSOP	$\theta_{JA}$	—	211	—	$^{\circ}\text{C}/\text{W}$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	149.5	—	$^{\circ}\text{C}/\text{W}$	
Thermal Resistance, 10L-DFN (3x3)	$\theta_{JA}$	—	57	—	$^{\circ}\text{C}/\text{W}$	
Thermal Resistance, 10L-MSOP	$\theta_{JA}$	—	202	—	$^{\circ}\text{C}/\text{W}$	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	120	—	$^{\circ}\text{C}/\text{W}$	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	$^{\circ}\text{C}/\text{W}$	



# MCP3426/7/8

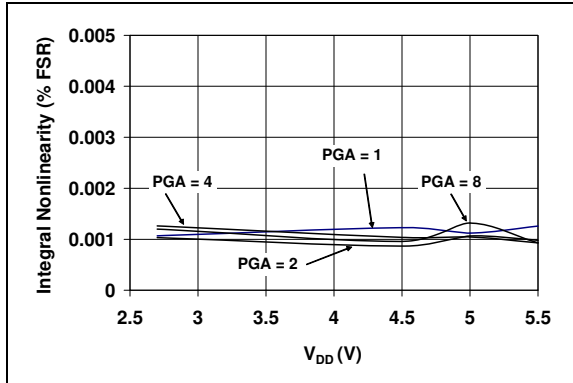
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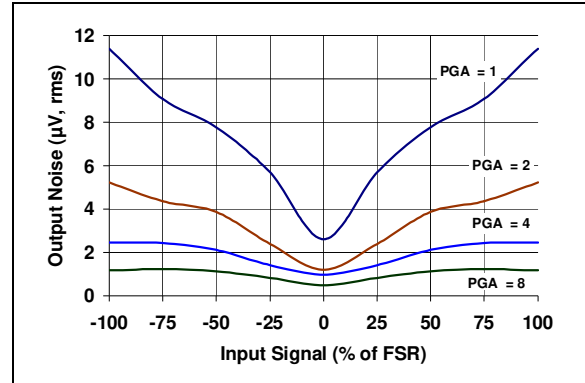
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

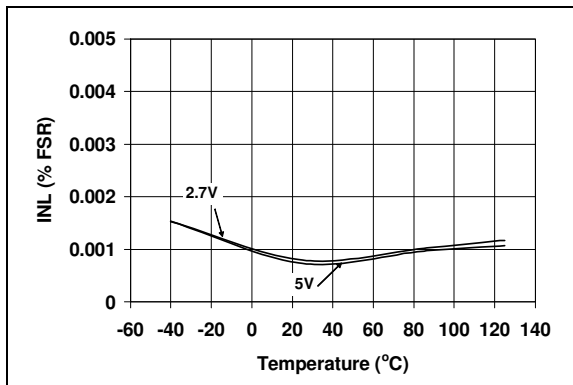
**Note:** Unless otherwise indicated,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +5.0\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $\text{CHn}+ = \text{CHn}- = V_{REF}/2$ ,  $V_{INCOM} = V_{REF}/2$ .



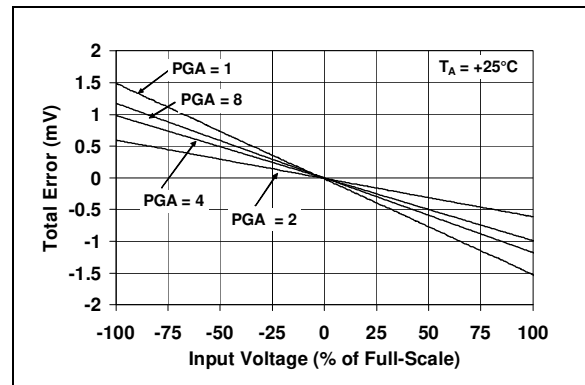
**FIGURE 2-1:** INL vs. Supply Voltage ( $V_{DD}$ ).



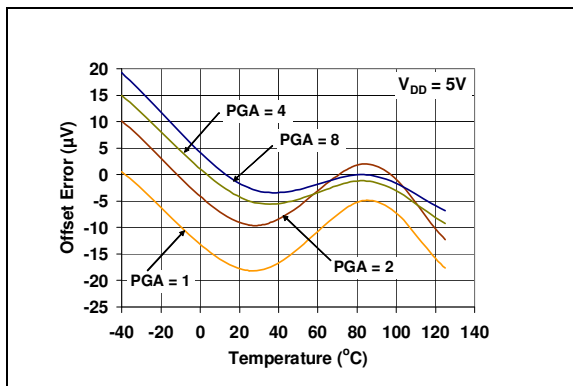
**FIGURE 2-4:** Output Noise vs. Input Voltage.



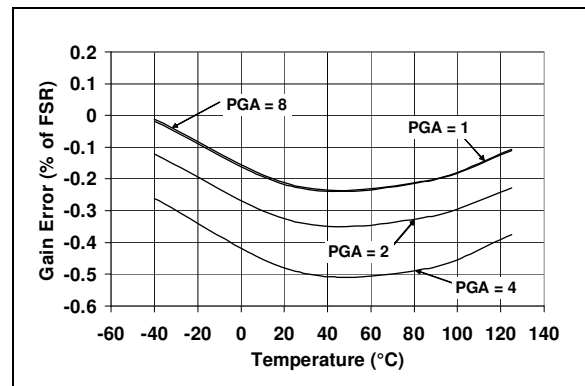
**FIGURE 2-2:** INL vs. Temperature.



**FIGURE 2-5:** Total Error vs. Input Voltage.



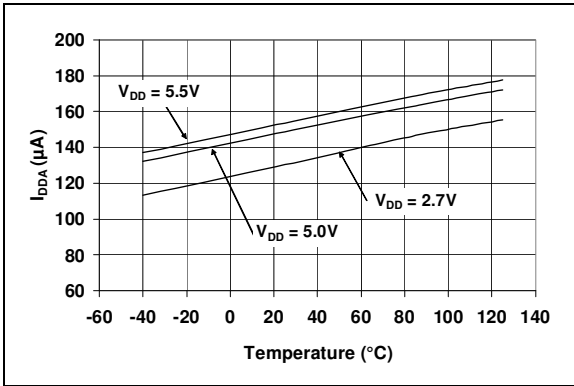
**FIGURE 2-3:** Offset Error vs. Temperature.



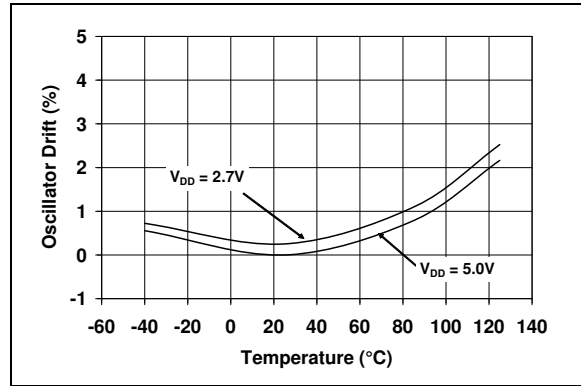
**FIGURE 2-6:** Gain Error vs. Temperature.

# MCP3426/7/8

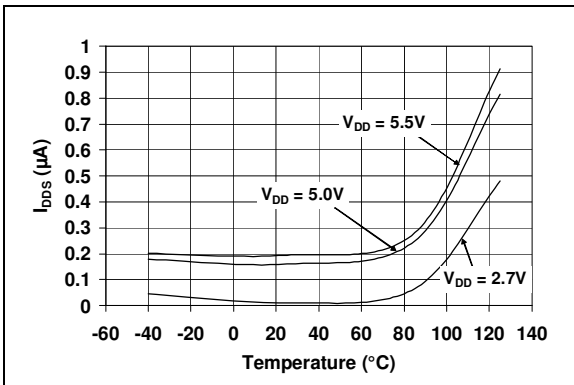
**Note:** Unless otherwise indicated,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +5.0\text{V}$ ,  $V_{SS} = 0\text{V}$ ,  $\text{CHn+} = \text{CHn-} = V_{\text{REF}}/2$ ,  $V_{\text{INCOM}} = V_{\text{REF}}/2$ .



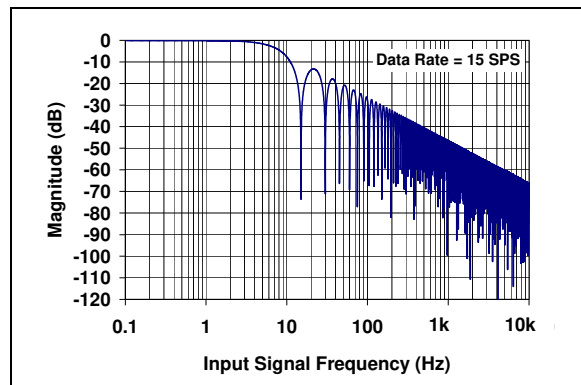
**FIGURE 2-7:**  $I_{DDA}$  vs. Temperature.



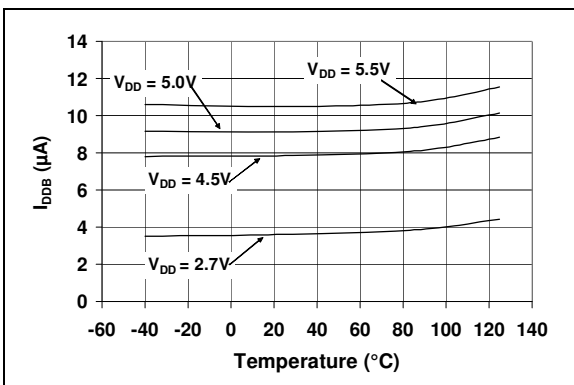
**FIGURE 2-10:** Oscillator Drift vs. Temperature.



**FIGURE 2-8:**  $I_{DDS}$  vs. Temperature.



**FIGURE 2-11:** Frequency Response.



**FIGURE 2-9:**  $I_{DDB}$  vs. Temperature.

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

MCP3426		MCP3427		MCP3428	Sym	Function
DFN	MSOP, SOIC	DFN	MSOP	SOIC, TSSOP		
1	1	1	1	1	CH1+	Positive Differential Analog Input Pin of Channel 1
2	2	2	2	2	CH1-	Negative Differential Analog Input Pin of Channel 1
7	7	4	4	3	CH2+	Positive Differential Analog Input Pin of Channel 2
8	8	5	5	4	CH2-	Negative Differential Analog Input Pin of Channel 2
6	6	3	3	5	V <sub>SS</sub>	Ground Pin
3	3	6	6	6	V <sub>DD</sub>	Positive Supply Voltage Pin
4	4	7	7	7	SDA	Bidirectional Serial Data Pin of the I <sup>2</sup> C Interface
5	5	8	8	8	SCL	Serial Clock Pin of the I <sup>2</sup> C Interface
—	—	9	9	9	Adr0	I <sup>2</sup> C Address Selection Pin. See <b>Section 5.3.2</b> .
—	—	10	10	10	Adr1	I <sup>2</sup> C Address Selection Pin. See <b>Section 5.3.2</b> .
—	—	—	—	11	CH3+	Positive Differential Analog Input Pin of Channel 3
—	—	—	—	12	CH3-	Negative Differential Analog Input Pin of Channel 3
—	—	—	—	13	CH4+	Positive Differential Analog Input Pin of Channel 4
—	—	—	—	14	CH4-	Negative Differential Analog Input Pin of Channel 4
9	—	11	—	—	EP	Exposed Thermal Pad (EP); must be connected to V <sub>SS</sub>

### 3.1 Analog Inputs (CHn+, CHn-)

CHn+ and CHn- are differential input pins for channel n. The user can also connect CHn- pin to V<sub>SS</sub> for a single-ended operation. See [Figure 6-4](#) for differential and single-ended connection examples.

The maximum voltage range on each differential input pin is from V<sub>SS</sub>-0.3V to V<sub>DD</sub>+0.3V. Any voltage below or above this range will cause leakage currents through the Electrostatic Discharge (ESD) diodes at the input pins.

This ESD current can cause unexpected performance of the device. The input voltage at the input pins should be within the specified operating range defined in **Section 1.0 “Electrical Characteristics”** and **Section 4.0 “Description of Device Operation”**.

See **Section 4.5 “Input Voltage Range”** for more details of the input voltage range.

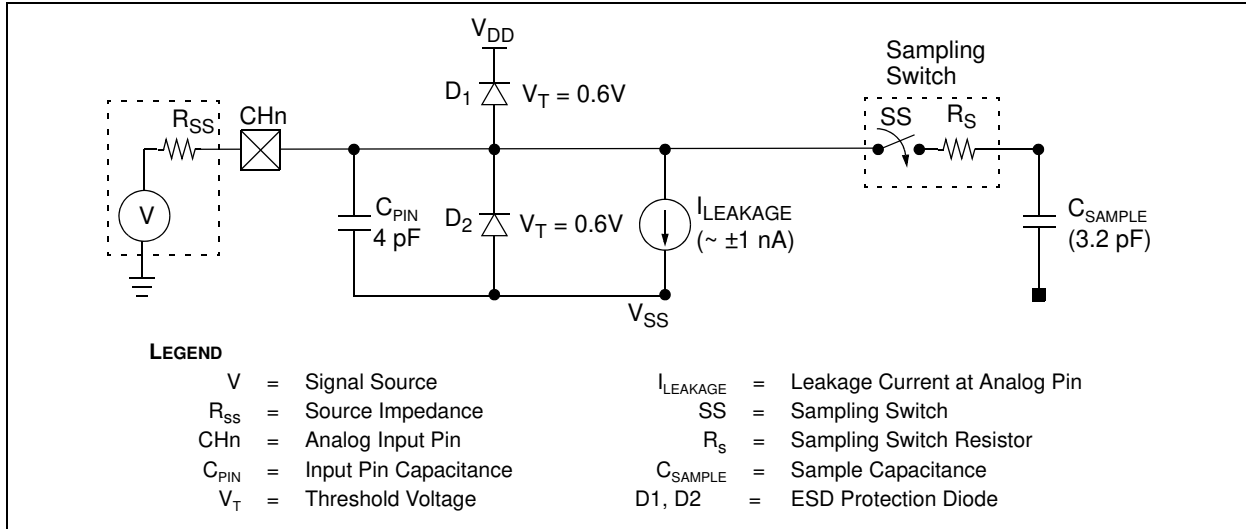
[Figure 3-1](#) shows the input structure of the device. The device uses a switched capacitor input stage at the front end. C<sub>PIN</sub> is the package pin capacitance and typically about 4 pF. D<sub>1</sub> and D<sub>2</sub> are the ESD diodes. C<sub>SAMPLE</sub> is the differential input sampling capacitor.

### 3.2 Supply Voltage (V<sub>DD</sub>, V<sub>SS</sub>)

V<sub>DD</sub> is the power supply pin for the device. This pin requires an appropriate bypass ceramic capacitor of about 0.1 μF to ground to attenuate high frequency noise presented in application circuit board. An additional 10 μF capacitor (tantalum) in parallel is also recommended to further attenuate current spike noises. The supply voltage (V<sub>DD</sub>) must be maintained in the 2.7V to 5.5V range for specified operation.

V<sub>SS</sub> is the ground pin and the current return path of the device. The user must connect the V<sub>SS</sub> pin to a ground plane through a low impedance connection. If an analog ground path is available in the application PCB (printed circuit board), it is highly recommended that the V<sub>SS</sub> pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

# MCP3426/7/8



**FIGURE 3-1:** Equivalent Analog Input Circuit.

### 3.3 Serial Clock Pin (SCL)

SCL is the serial clock pin of the I<sup>2</sup>C interface. The device acts only as a slave and the SCL pin accepts only external serial clocks. The input data from the Master device is shifted into the SDA pin on the rising edges of the SCL clock and output from the slave device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V<sub>DD</sub> line to the SCL pin. Refer to **Section 5.3 “I<sup>2</sup>C Serial Communications”** for more details on I<sup>2</sup>C Serial Interface communication.

### 3.4 Serial Data Pin (SDA)

SDA is the serial data pin of the I<sup>2</sup>C interface. The SDA pin is used for input and output data. In read mode, the conversion result is read from the SDA pin (output). In write mode, the device configuration bits are written (input) through the SDA pin. The SDA pin is an open-drain N-channel driver. Therefore, it needs a pull-up resistor from the V<sub>DD</sub> line to the SDA pin. Except for start and stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 5.3 “I<sup>2</sup>C Serial Communications”** for more details on I<sup>2</sup>C Serial Interface communication.

The typical range of the pull-up resistor value for SCL and SDA is from 5 kΩ to 10 kΩ for standard (100 kHz) and fast (400 kHz) modes, and less than 1 kΩ for high speed mode (3.4 MHz).

### 3.5 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the V<sub>SS</sub> pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

## 4.0 DESCRIPTION OF DEVICE OPERATION

### 4.1 General Overview

The MCP3426/7/8 devices are differential multi-channel low-power, 16-Bit Delta-Sigma A/D converters with an I<sup>2</sup>C serial interface. The devices contain an input channel selection multiplexer (mux), a programmable gain amplifier (PGA), an on-board voltage reference (2.048V), and an internal oscillator.

When the device powers up (POR is set), it automatically resets the configuration bits to default settings.

#### 4.1.1 DEVICE DEFAULT SETTINGS ARE:

- Conversion bit resolution: 12 bits (240 sps)
- Input channel: Channel 1
- PGA gain setting: x1
- Continuous conversion

Once the device is powered-up, the user can reprogram the configuration bits using I<sup>2</sup>C serial interface any time. The configuration bits are stored in the volatile memory.

#### 4.1.2 USER SELECTABLE OPTIONS ARE:

- Conversion bit resolution: 12, 14, or 16 bits
- Input channel selection: CH1, CH2, CH3, or CH4.
- PGA Gain selection: x1, x2, x4, or x8
- Continuous or one-shot conversion

In the Continuous Conversion mode, the device converts the inputs continuously. While in the One-Shot Conversion mode, the device converts the input one time and stays in the low-power standby mode until it receives another command for a new conversion. During the standby mode, the device consumes less than 1  $\mu$ A maximum.

### 4.2 Power-On-Reset (POR)

The device contains an internal Power-On-Reset (POR) circuit that monitors power supply voltage ( $V_{DD}$ ) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

The device resets all configuration register bits to default settings as soon as the POR is set.

The POR has built-in hysteresis and a timer to give a high degree of immunity to potential ripples and noises on the power supply. A 0.1  $\mu$ F decoupling capacitor should be mounted as close as possible to the  $V_{DD}$  pin for additional transient immunity.

The threshold voltage is set at 2.2V with a tolerance of approximately  $\pm 5\%$ . If the supply voltage falls below this threshold, the device will be held in a reset condition. The typical hysteresis value is approximately 200 mV.

The POR circuit is shut down during the low-power standby mode. Once a power-up event has occurred, the device requires additional delay time (approximately 300  $\mu$ s) before a conversion takes place. During this time, all internal analog circuitries are settled before the first conversion occurs. Figure 4-1 illustrates the conditions for power-up and power-down events under typical start-up conditions.

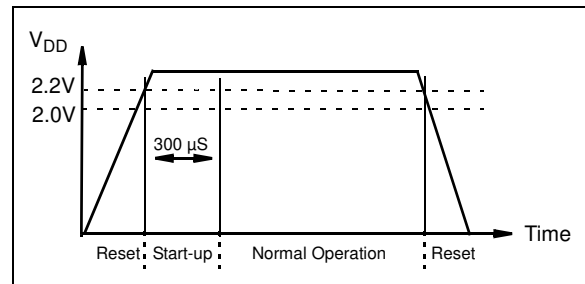


FIGURE 4-1: POR Operation.

### 4.3 Internal Voltage Reference

The device contains an on-board 2.048V voltage reference. This reference voltage is for internal use only and not directly measurable. The specification of the reference voltage is part of the device's gain and drift specifications. Therefore, there is no separate specification for the on-board reference.

### 4.4 Analog Input Channels

The user can select the input channel using the configuration register bits. Each channel can be used for differential or single-ended input.

Each input channel has a switched capacitor input structure. The internal sampling capacitor (3.2 pF for PGA = 1) is charged and discharged to process a conversion. The charging and discharging of the input sampling capacitor creates dynamic input currents at each input pin. The current is a function of the differential input voltages, and inversely proportional to the internal sampling capacitance, sampling frequency, and PGA setting.

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## 4.5 Input Voltage Range

The differential ( $V_{IN}$ ) and common mode voltage ( $V_{INCOM}$ ) at the input pins without considering PGA setting are defined by:

$$V_{IN} = (CH_{n+}) - (CH_{n-})$$
$$V_{INCOM} = \frac{(CH_{n+}) + (CH_{n-})}{2}$$

Where:

n = nth input channel (n=1, 2, 3, or 4)

The input signal levels are amplified by the internal programmable gain amplifier (PGA) at the front end of the  $\Delta\Sigma$  modulator.

The user needs to consider two conditions for the input voltage range: (a) Differential input voltage range and (b) Absolute maximum input voltage range.

### 4.5.1 DIFFERENTIAL INPUT VOLTAGE RANGE

The device performs conversions using its internal reference voltage ( $V_{REF} = 2.048V$ ). Therefore, the absolute value of the differential input voltage ( $V_{IN}$ ), with PGA setting is included, needs to be less than the internal reference voltage. The device will output saturated output codes (all 0s or all 1s except sign bit) if the absolute value of the input voltage ( $V_{IN}$ ), with PGA setting is included, is greater than the internal reference voltage ( $V_{REF} = 2.048V$ ). The input full scale voltage range is given by:

#### EQUATION 4-1:

$$-V_{REF} \leq (V_{IN} \cdot PGA) \leq (V_{REF} - 1LSB)$$

Where:

$$V_{IN} = CH_{n+} - CH_{n-}$$
$$V_{REF} = 2.048V$$

If the input voltage level is greater than the above limit, the user can use a voltage divider and bring down the input level within the full scale range. See [Figure 6-7](#) for more details of the input voltage divider circuit.

### 4.5.2 ABSOLUTE MAXIMUM INPUT VOLTAGE RANGE

The input voltage at each input pin must be less than the following absolute maximum input voltage limits:

- Input voltage <  $V_{DD} + 0.3V$
- Input voltage >  $V_{SS} - 0.3V$

Any input voltage outside this range can turn on the input ESD protection diodes, and result in input leakage current, causing conversion errors, or permanently damage the device.

Care must be taken in setting the input voltage ranges so that the input voltage does not exceed the absolute maximum input voltage range.

## 4.6 Input Impedance

The device uses a switched-capacitor input stage using a 3.2 pF sampling capacitor. This capacitor is switched (charged and discharged) at a rate of the sampling frequency that is generated by on-board clock. The differential input impedance varies with the PGA settings. The typical differential input impedance during a normal mode operation is given by:

$$Z_{IN}(f) = 2.25 M\Omega / PGA$$

Since the sampling capacitor is only switching to the input pins during a conversion process, the above input impedance is only valid during conversion periods. In a low power standby mode, the above impedance is not presented at the input pins. Therefore, only a leakage current due to ESD diode is presented at the input pins.

The conversion accuracy can be affected by the input signal source impedance when any external circuit is connected to the input pins. The source impedance adds to the internal impedance and directly affects the time required to charge the internal sampling capacitor. Therefore, a large input source impedance connected to the input pins can degrade the system performance, such as offset, gain, and Integral Non-Linearity (INL) errors. Ideally, the input source impedance should be zero. This can be achievable by using an operational amplifier with a closed-loop output impedance of tens of ohms.

## 4.7 Aliasing and Anti-aliasing Filter

Aliasing occurs when the input signal contains time-varying signal components with frequency greater than half the sample rate. In the aliasing conditions, the device can output unexpected output codes. For applications that are operating in electrical noise environments, the time-varying signal noise or high frequency interference components can be easily added to the input signals and cause aliasing. Although the device has an internal first order sinc filter, the filter response ([Figure 2-11](#)) may not give enough attenuation to all aliasing signal components. To avoid the aliasing, an external anti-aliasing filter, which can be accomplished with a simple RC low-pass filter, is typically used at the input pins. The low-pass filter cuts off the high frequency noise components and provides a band-limited input signal to the input pins.

## 4.8 Self-Calibration

The device performs a self-calibration of offset and gain for each conversion. This provides reliable conversion results from conversion-to-conversion over variations in temperature as well as power supply fluctuations.

## 4.9 Digital Output Codes and Conversion to Real Values

### 4.9.1 DIGITAL OUTPUT CODE FROM DEVICE

The digital output code is proportional to the input voltage and PGA settings. The output data format is a binary two's complement. With this code scheme, the MSB can be considered a sign indicator. When the MSB is a logic '0', the input is positive. When the MSB is a logic '1', the input is negative. The following is an example of the output code:

(a) for a negative full scale input voltage: 100...000

Example:  $(CHn+ - CHn-) \cdot PGA = -2.048V$

(b) for a zero differential input voltage: 000...000

Example:  $(CHn+ - CHn-) = 0$

(c) for a positive full scale input voltage: 011...111

Example:  $(CHn+ - CHn-) \cdot PGA = 2.048V$

The MSB (sign bit) is always transmitted first through the I<sup>2</sup>C serial data line. The resolution for each conversion is 16, 14, or 12 bits depending on the conversion rate selection bit settings by the user.

The output codes will not roll-over even if the input voltage exceeds the maximum input range. In this case, the code will be locked at 0111...11 for all voltages greater than  $(V_{REF} - 1 \text{ LSB})/PGA$  and 1000...00 for voltages less than  $-V_{REF}/PGA$ . Table 4-2 shows an example of output codes of various input levels for 16-bit conversion mode. Table 4-3 shows an example of minimum and maximum output codes for each conversion rate option.

The number of output code is given by:

#### EQUATION 4-2:

$$\begin{aligned} \text{Number of Output Code} &= \\ &= (\text{Maximum Code} + 1) \times PGA \times \frac{(CHn+ - CHn-)}{2.048V} \end{aligned}$$

Where:

See Table 4-3 for Maximum Code

The LSB of the data conversion is given by:

#### EQUATION 4-3:

$$LSB = \frac{2 \times V_{REF}}{2^N} = \frac{2 \times 2.048V}{2^N}$$

Where:

N = Resolution, which is programmed in the Configuration Register: 12, 14, or 16.

Table 4-1 shows the LSB size of each conversion rate setting. The measured unknown input voltage is obtained by multiplying the output codes with LSB. See the following section for the input voltage calculation using the output codes.

**TABLE 4-1: RESOLUTION SETTINGS VS. LSB**

Resolution Setting	LSB
12 bits	1 mV
14 bits	250 $\mu$ V
16 bits	62.5 $\mu$ V

**TABLE 4-2: EXAMPLE OF OUTPUT CODE FOR 16 BITS (NOTE 1, NOTE 2)**

Input Voltage: [CHn+ - CHn-] $\cdot$ PGA	Digital Output Code
$\geq V_{REF}$	0111111111111111
$V_{REF} - 1 \text{ LSB}$	0111111111111111
2 LSB	000000000000010
1 LSB	000000000000001
0	000000000000000
-1 LSB	111111111111111
-2 LSB	111111111111110
$-V_{REF}$	100000000000000
$< -V_{REF}$	100000000000000

**Note 1:** MSB is a sign indicator:

0: Positive input ( $CHn+ > CHn-$ )  
1: Negative input ( $CHn+ < CHn-$ )

**2:** Output data format is binary two's complement.

**TABLE 4-3: MINIMUM AND MAXIMUM OUTPUT CODES (NOTE)**

Resolution Setting	Data Rate	Minimum Code	Maximum Code
12	240 SPS	-2048	2047
14	60 SPS	-8192	8191
16	15 SPS	-32768	32767

**Note:** Maximum n-bit code =  $2^{N-1} - 1$   
Minimum n-bit code =  $-1 \times 2^{N-1}$



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## 4.9.2 CONVERTING THE DEVICE OUTPUT CODE TO INPUT SIGNAL VOLTAGE

When the user gets the digital output codes from the device as described in **Section 4.9.1 “Digital output code from device”**, the next step is converting the digital output codes to a measured input voltage. [Equation 4-4](#) shows an example of converting the output codes to its corresponding input voltage.

If the sign indicator bit (MSB) is '0', the input voltage is obtained by multiplying the output code with the LSB and divided by the PGA setting.

If the sign indicator bit (MSB) is '1', the output code needs to be converted to two's complement before multiplied by LSB and divided by the PGA setting. [Table 4-4](#) shows an example of converting the device output codes to input voltage.

## EQUATION 4-4: CONVERTING OUTPUT CODES TO INPUT VOLTAGE

**If MSB = 0 (Positive Output Code):**

$$\text{Input Voltage} = (\text{Output Code}) \cdot \frac{\text{LSB}}{\text{PGA}}$$

**If MSB = 1 (Negative Output Code):**

$$\text{Input Voltage} = (2\text{'s complement of Output Code}) \cdot \frac{\text{LSB}}{\text{PGA}}$$

Where:

LSB = See [Table 4-1](#)

2's complement = 1's complement + 1

**TABLE 4-4: EXAMPLE OF CONVERTING OUTPUT CODE TO VOLTAGE (WITH 16 BIT SETTING)**

Input Voltage [CHn+ - CHn-] • PGA	Digital Output Code	MSB	Example of Converting Output Codes to Input Voltage
$\geq V_{REF}$	0111111111111111	0	$(2^{14}+2^{13}+2^{12}+2^{11}+2^{10}+2^9+2^8+2^7+2^6+2^5+2^4+2^3+2^2+2^1+2^0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = 2.048 \text{ (V) for PGA} = 1$
$V_{REF} - 1 \text{ LSB}$	0111111111111111	0	$(2^{14}+2^{13}+2^{12}+2^{11}+2^{10}+2^9+2^8+2^7+2^6+2^5+2^4+2^3+2^2+2^1+2^0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = 2.048 \text{ (V) for PGA} = 1$
2 LSB	0000000000000010	0	$(0+0+0+0+0+0+0+0+0+0+0+0+0+0+2^1+0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = 125 \text{ (}\mu\text{V) for PGA} = 1$
1 LSB	0000000000000001	0	$(0+0+0+0+0+0+0+0+0+0+0+0+0+0+2^0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = 62.5 \text{ (}\mu\text{V) for PGA} = 1$
0	0000000000000000	0	$(0+0+0+0+0+0+0+0+0+0+0+0+0+0+0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = 0 \text{ V (V) for PGA} = 1$
-1 LSB	1111111111111111	1	$-(0+0+0+0+0+0+0+0+0+0+0+0+0+0+2^0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = -62.5 \text{ (}\mu\text{V) for PGA} = 1$
-2 LSB	1111111111111110	1	$-(0+0+0+0+0+0+0+0+0+0+0+0+0+0+2^1+0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = -125 \text{ (}\mu\text{V) for PGA} = 1$
$-V_{REF}$	1000000000000000	1	$-(2^{15}+0+0+0+0+0+0+0+0+0+0+0+0+0+0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = -2.048 \text{ (V) for PGA} = 1$
$\leq -V_{REF}$	1000000000000000	1	$-(2^{15}+0+0+0+0+0+0+0+0+0+0+0+0+0+0) \times \text{LSB} (62.5\mu\text{V}) / \text{PGA} = -2.048 \text{ (V) for PGA} = 1$

**Note:** MSB = sign bit (1: “-”, 0: “+”)

## 5.0 USING THE DEVICES

### 5.1 Operating Modes

The user operates the device by setting up the device configuration register using a write command (see Figure 5-3) and reads the conversion data using a read command (see Figure 5-4). The device operates in two modes: (a) Continuous Conversion Mode or (b) One-Shot Conversion Mode (single conversion). This mode selection is made by setting the  $\overline{O/C}$  bit in the Configuration Register. Refer to **Section 5.2 “Configuration Register”** for more information.

#### 5.1.1 CONTINUOUS CONVERSION MODE ( $\overline{O/C}$ BIT = 1)

The device performs a Continuous Conversion if the  $\overline{O/C}$  bit is set to logic “high”. Once the conversion is completed,  $\overline{RDY}$  bit is toggled to ‘0’ and the result is placed at the output data register. The device immediately begins another conversion and overwrites the output data register with the most recent result. The device clears the data ready flag ( $\overline{RDY}$  bit = 0) when the conversion is completed. The device sets the ready flag bit ( $\overline{RDY}$  bit = 1), if the latest conversion result has been read by the Master.

- **When writing configuration register:**
  - Setting  $\overline{RDY}$  bit in continuous mode does not affect anything.
- **When reading conversion data:**
  - $\overline{RDY}$  bit = 0 means the latest conversion result is ready.
  - $\overline{RDY}$  bit = 1 means the conversion result is not updated since the last reading. A new conversion is under processing and the  $\overline{RDY}$  bit will be cleared when the new conversion result is ready.

#### 5.1.2 ONE-SHOT CONVERSION MODE ( $\overline{O/C}$ BIT = 0)

Once the One-Shot Conversion (single conversion) Mode is selected, the device performs only one conversion, updates the output data register, clears the data ready flag ( $\overline{RDY}$  = 0), and then enters a low power standby mode. A new One-Shot Conversion is started again when the device receives a new write command with  $\overline{RDY}$  = 1.

- **When writing configuration register:**
  - The  $\overline{RDY}$  bit needs to be set to begin a new conversion in one-shot mode.
- **When reading conversion data:**
  - $\overline{RDY}$  bit = 0 means the latest conversion result is ready.
  - $\overline{RDY}$  bit = 1 means the conversion result is not updated since the last reading. A new conversion is under processing and the  $\overline{RDY}$  bit will be cleared when the new conversion is done.

This One-Shot Conversion Mode is highly recommended for low power operating applications where the conversion result is needed by request on demand. During the low current standby mode, the device consumes less than 1  $\mu\text{A}$  maximum (or 300 nA typical). For example, if the user collects 16-bit conversion data once a second in One-Shot Conversion mode, the device draws only about one-fifteenth of the operating currents for the continuous conversion mode. In this example, the device consumes approximately 9  $\mu\text{A}$  ( $135 \mu\text{A} / 15 \text{ SPS} = 9 \mu\text{A}$ ), when the device performs only one conversion per second (1 SPS) in 16-bit conversion mode with 3V power supply.

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## 5.2 Configuration Register

The device has an 8-bit wide configuration register to select for: input channel, conversion mode, conversion rate, and PGA gain. This register allows the user to change the operating condition of the device and check the status of the device operation.

The user can rewrite the configuration byte any time during the device operation. Register 5-1 shows the configuration register bits.

**REGISTER 5-1: CONFIGURATION REGISTER**

R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
$\overline{\text{RDY}}$	C1	C0	$\overline{\text{O/C}}$	S1	S0	G1	G0
1 *	0 *	0 *	1 *	0 *	0 *	0 *	0 *
bit 7						bit 0	

\* Default Configuration after Power-On Reset

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7

**$\overline{\text{RDY}}$ :** Ready Bit

This bit is the data ready flag. In read mode, this bit indicates if the output register has been updated with a latest conversion result. In One-Shot Conversion mode, writing this bit to "1" initiates a new conversion.

**Reading  $\overline{\text{RDY}}$  bit with the read command:**

1 = Output register has not been updated.

0 = Output register has been updated with the latest conversion result.

**Writing  $\overline{\text{RDY}}$  bit with the write command:**

Continuous Conversion mode: No effect

One-Shot Conversion mode:

1 = Initiate a new conversion.

0 = No effect.

bit 6-5

**C1-C0:** Channel Selection Bits

00 = Select Channel 1 (**Default**)

01 = Select Channel 2

10 = Select Channel 3 (**MCP3428 only, treated as "00" by the MCP3426/MCP3427**)

11 = Select Channel 4 (**MCP3428 only, treated as "01" by the MCP3426/MCP3427**)

bit 4

**$\overline{\text{O/C}}$ :** Conversion Mode Bit

1 = Continuous Conversion Mode (**Default**). The device performs data conversions continuously.

0 = One-Shot Conversion Mode. The device performs a single conversion and enters a low power standby mode until it receives another write or read command.

bit 3-2

**S1-S0:** Sample Rate Selection Bit

00 = 240 SPS (12 bits) (**Default**)

01 = 60 SPS (14 bits)

10 = 15 SPS (16 bits)

bit 1-0

**G1-G0:** PGA Gain Selection Bits

00 = x1 (**Default**)

01 = x2

10 = x4

11 = x8

If the configuration byte is read repeatedly by clocking continuously after reading the data bytes (i.e., after the 4th byte in the 16-bit conversion mode), the state of the RDY bit indicates whether the device is ready with new conversion result. When the Master finds the RDY bit is cleared, it can send a not-acknowledge (NAK) bit and a stop bit to exit the current read operation and send a new read command for the latest conversion data. Once the conversion data has been read, the ready bit toggles to '1' until the next new conversion data is ready. The conversion data in the output register is overwritten every time a new conversion is completed.

Figure 5-3 shows an example of writing configuration register, and Figure 5-4 shows an example of reading conversion data. The user can rewrite the configuration byte any time for a new setting. Table 5-1 and Table 5-2 show the examples of the configuration bit operation.

**TABLE 5-1: WRITE CONFIGURATION BITS**

R/W	O/C	RDY	Operation
0	0	0	No effect if all other bits remain the same - operation continues with the previous settings.
0	0	1	Initiate One-Shot Conversion.
0	1	0	Initiate Continuous Conversion.
0	1	1	Initiate Continuous Conversion.

**TABLE 5-2: READ CONFIGURATION BITS**

R/W	O/C	RDY	Operation
1	0	0	New conversion result in One-Shot conversion mode has just been read. The RDY bit remains low until set by a new write command.
1	0	1	One-Shot Conversion is in progress. The conversion result is not updated yet. The RDY bit stays high until the current conversion is completed.
1	1	0	New conversion result in Continuous Conversion mode has just been read. The RDY bit changes to high after reading the conversion data.
1	1	1	The conversion result in Continuous Conversion mode was already read. The next new conversion data is not ready. The RDY bit stays high until a new conversion is completed.

## 5.3 I<sup>2</sup>C Serial Communications

The device communicates with the Master (microcontroller) through a serial I<sup>2</sup>C (Inter-Integrated Circuit) interface and support standard (100 kbits/sec), fast (400 kbits/sec) and high-speed (3.4 Mbits/sec) modes. The serial I<sup>2</sup>C is a bidirectional 2-wire data bus communication protocol using open-drain SCL and SDA lines.

The device can only be addressed as a slave. Once addressed, it can receive configuration bits with a write command or transmit the latest conversion results with a read command. The serial clock pin (SCL) is an input only and the serial data pin (SDA) is bidirectional. The Master starts communication by sending a START bit and terminates the communication by sending a STOP bit. In read mode, the device releases the SDA line after receiving NAK and STOP bits.

An example of a hardware connection diagram is shown in Figure 6-1. More details of the I<sup>2</sup>C bus characteristic is described in Section 5.6 "I<sup>2</sup>C Bus Characteristics".

### 5.3.1 I<sup>2</sup>C DEVICE ADDRESSING

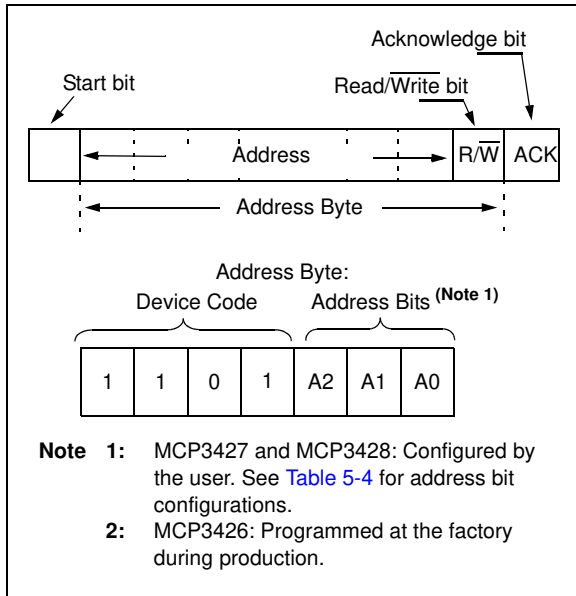
The first byte after the START bit is always the address byte of the device, which includes the device code (4 bits), address bits (3 bits), and R/W bit. The device code for the devices is 1101, which is programmed at the factory. The I<sup>2</sup>C address bits (A2, A1, A0 bits) are as follows:

- MCP3426: Programmed at factory
- MCP3427 and MCP3428: Programmed by the user. It is determined by the logic status of the two external address selection pins on the user's application board (Adr0 and Adr1 pins). The Master must know the Adr0 and Adr1 pin conditions before sending read or write command. See Section 5.3.2 "Device Address Bits (A2, A1, A0) and Address Selection Pins (MCP3427 and MCP3428)" for more details

Figure 5-1 shows the details of the address byte.

The three I<sup>2</sup>C address bits allow up to eight devices on the same I<sup>2</sup>C bus line. The (R/W) bit determines if the Master device wants to read the conversion data or write to the Configuration register. If the (R/W) bit is set (read mode), the device outputs the conversion data in the following clocks. If the (R/W) bit is cleared (write mode), the device expects a configuration byte in the following clocks. When the device receives the correct address byte, it outputs an acknowledge bit after the R/W bit.

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**FIGURE 5-1:** Address Byte.

## 5.3.2 DEVICE ADDRESS BITS (A2, A1, A0) AND ADDRESS SELECTION PINS (MCP3427 AND MCP3428)

The MCP3427 and MCP3428 have two external device address pins (Adr1, Adr0). These pins can be set to a logic high (or tied to  $V_{DD}$ ), low (or tied to  $V_{SS}$ ), or left floating (not connected to anything, or tied to  $V_{DD}/2$ ). These combinations of logic level using the two pins allow eight possible addresses. Table 5-3 shows the device address depending on the logic status of the address selection pins.

The device samples the logic status of the Adr0 and Adr1 pins in the following events:

- Device power-up.
- General Call Reset (See Section 5.4 “General Call”).
- General Call Latch (See Section 5.4 “General Call”).

The device samples the logic status (address pins) during the above events, and latches the values until a new latch event occurs. During normal operation (after the address pins are latched), the address pins are internally disabled from the rest of the internal circuit.

It is recommended to issue a General Call Reset or General Call Latch command once after the device has powered up. This will ensure that the device reads the address pins in a stable condition, and avoid latching the address bits while the power supply is ramping up. This might cause inaccurate address pin detection.

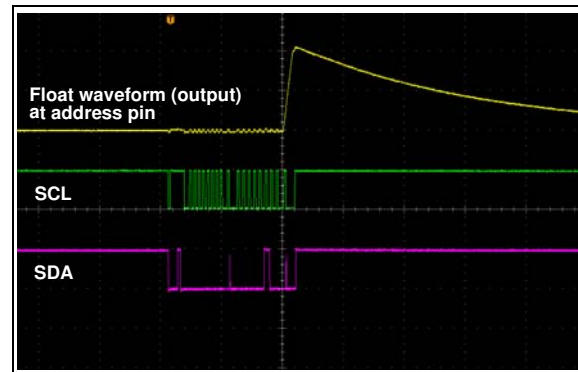
### When the address pin is left “floating”:

When the address pin is left “floating”, the address pin momentarily outputs a short pulse with an amplitude of about  $V_{DD}/2$  during the latch event. The device also latches this pin voltage at the same time.

If the “floating” pin is connected to a large parasitic capacitance ( $> 20$  pF) or to a long PCB trace, this short floating voltage output can be altered. As a result, the device may not latch the pin correctly.

It is strongly recommended to keep the “floating” pin pad as short as possible in the customer application PCB and minimize the parasitic capacitance to the pin as small as possible ( $< 20$  pF).

Figure 5-2 shows an example of the Latch voltage output at the address pin when the address pin is left “floating”. The waveform at the Adr0 pin is captured by using an oscilloscope probe with 15 pF of capacitance. The device latches the floating condition immediately after the General Call Latch command.



**FIGURE 5-2:** General Call Latch Command and Voltage Output at Address Pin Left “Floating” (MCP3427 and MCP3428).

**TABLE 5-3: ADDRESS BITS VS. ADDRESS SELECTION PINS FOR (MCP3427 AND MCP3428 ONLY) (NOTE 1, 2, 3)**

I <sup>2</sup> C Device Address Bits			Logic Status of Address Selection Pins	
A2	A1	A0	Adr0 Pin	Adr1 Pin
0	0	0	0 (Addr_Low)	0 (Addr_Low)
0	0	1	0 (Addr_Low)	Float
0	1	0	0 (Addr_Low)	1 (Addr_High)
1	0	0	1 (Addr_High)	0 (Addr_Low)
1	0	1	1 (Addr_High)	Float
1	1	0	1 (Addr_High)	1 (Addr_High)
0	1	1	Float	0 (Addr_Low)
1	1	1	Float	1 (Addr_High)
0	0	0	Float	Float

**Note 1:** Float: (a) Leave pin without connecting to anything (left floating), or (b) apply Addr\_Float voltage.

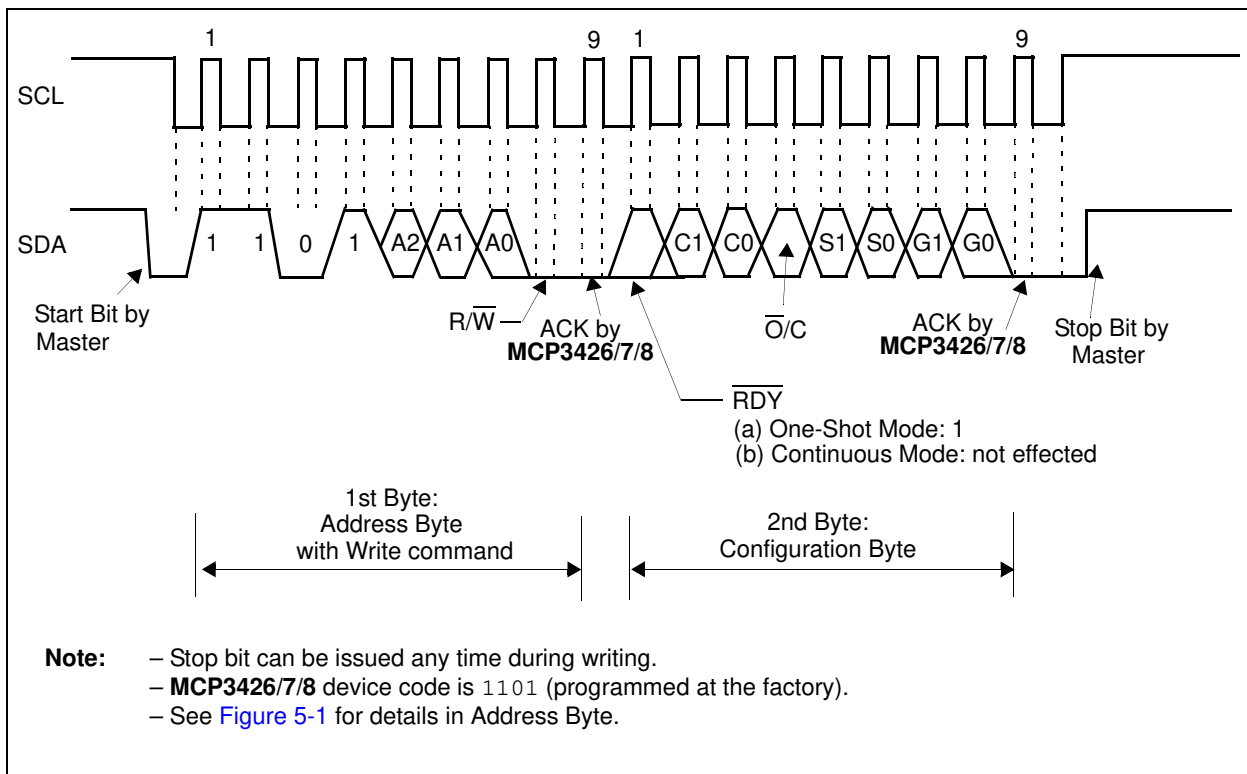
**2:** The user can tie the pins to V<sub>SS</sub> or V<sub>DD</sub>:  
 - Tie to V<sub>SS</sub> for Addr\_Low  
 - Tie to V<sub>DD</sub> for Addr\_High

**3:** See Addr\_Low, Addr\_High, and Addr\_Float parameters in **Electrical Characteristics Table**.

### 5.3.3 WRITING A CONFIGURATION BYTE TO THE DEVICE

When the Master sends an address byte with the  $\overline{R/\overline{W}}$  bit low ( $R/\overline{W} = 0$ ), the device expects one configuration byte following the address. Any byte sent after this second byte will be ignored. The user can change the operating mode of the device by writing the configuration register bits.

If the device receives a write command with a new configuration setting, the device immediately begins a new conversion and updates the conversion data.



**FIGURE 5-3: Timing Diagram For Writing To The MCP3426/7/8.**

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## 5.3.4 READING OUTPUT CODES AND CONFIGURATION BYTE FROM THE DEVICE

When the Master sends a read command ( $\overline{R/\overline{W}} = 1$ ), the device outputs both the conversion data and configuration bytes. Each byte consists of 8 bits with one acknowledge (ACK) bit. The ACK bit after the address byte is issued by the device and the ACK bits after each conversion data bytes are issued by the Master.

When the device receives a read command, it outputs two data bytes followed by a configuration register. In 16-bit conversion mode, the MSB (= sign bit) of the first data byte is D15. In 14-bit conversion mode, the first two bits in the first data byte are repeated MSB bits and can be ignored, and the 3rd bit (D13) is the MSB (=sign bit) of the conversion data. In 12-bit conversion mode, the first four bits are repeated MSB bits and can be ignored. The 5th bit (D11) of the byte represents the MSB (= sign bit) of the conversion data. [Table 5-4](#) summarizes the conversion data output of each conversion mode.

The configuration byte follows the output data bytes. The device repeatedly outputs the configuration byte only if the Master sends clocks repeatedly after the data bytes.

The device terminates the current outputs when it receives a Not-Acknowledge (NAK) with a repeated start or a stop bit at the end of each output byte. It is not required to read the configuration byte. However, the Master may read the configuration byte to check the RDY bit condition. The Master may continuously send clock (SCL) to repeatedly read the configuration byte (to check the RDY bit status).

[Figure 5-4](#) shows the timing diagram for reading the ADC conversion data.

**TABLE 5-4: OUTPUT CODES OF EACH RESOLUTION OPTION**

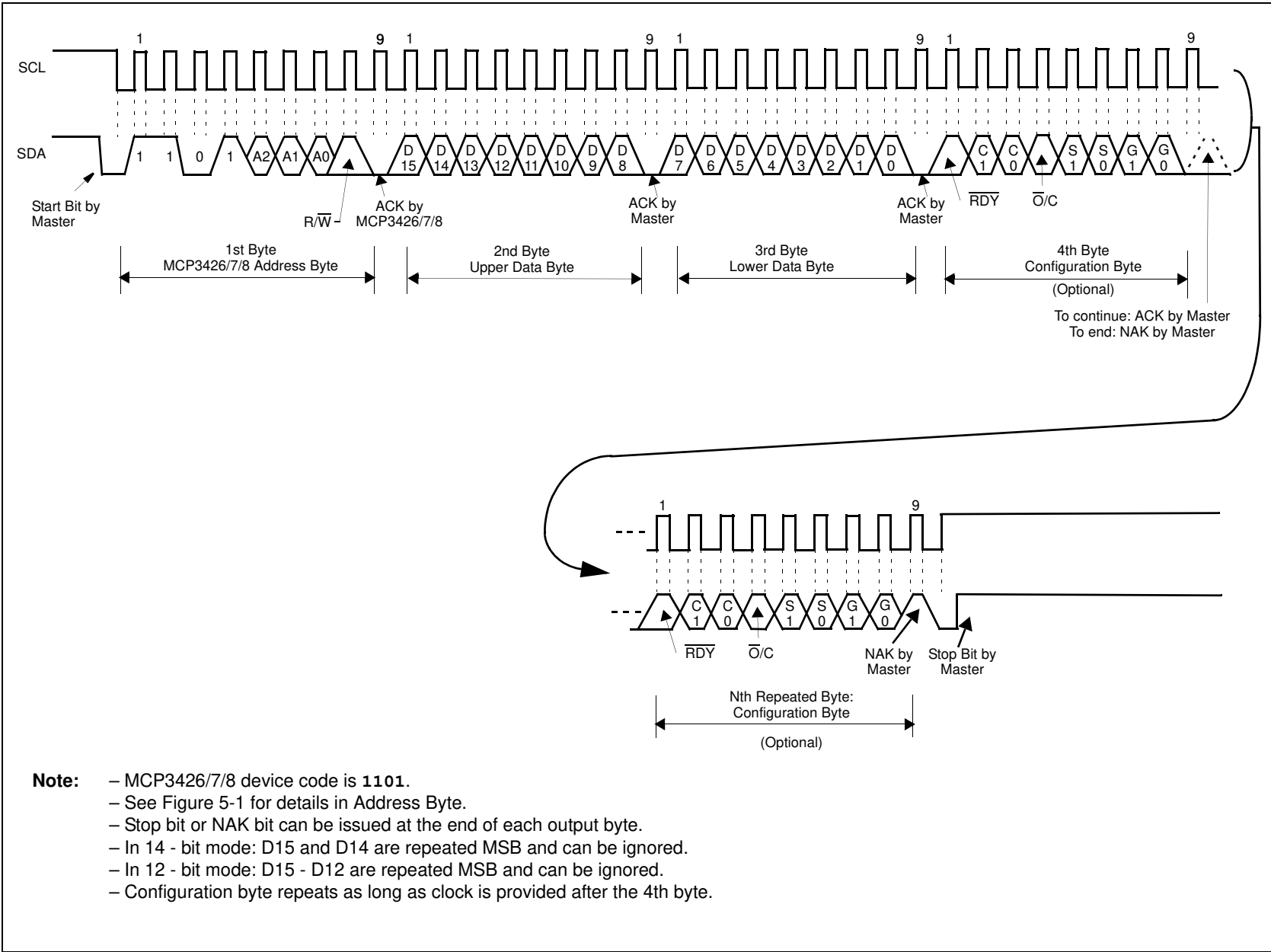
Conversion Option	Digital Output Codes
16-bits	D15 ~ D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte. <b>(Note 1)</b>
14-bits	MMD13D ~ D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte. <b>(Note 2)</b>
12-bits	MMMMD11 ~ D8 (1st data byte) - D7 ~ D0 (2nd data byte) - Configuration byte. <b>(Note 3)</b>

**Note 1:** D15 is MSB (= sign bit).

**2:** D13 is MSB (= sign bit), M is repeated MSB of the data byte.

**3:** D11 is MSB (= sign bit), M is repeated MSB of the data byte.

**FIGURE 5-4:** Timing Diagram For Reading From The MCP3426/7/8 With 12-Bit to 16-Bit Modes.





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## 5.4 General Call

The device acknowledges the general call address (0x00 in the first byte). The meaning of the general call address is always specified in the second byte. Refer to [Figure 5-5](#). The device supports the following three general calls.

For more information on the general call, or other I<sup>2</sup>C modes, refer to the Phillips I<sup>2</sup>C specification.

### 5.4.1 GENERAL CALL RESET

The general call reset occurs if the second byte is `'00000110'` (06h). At the acknowledgement of this byte, the device will abort current conversion and perform the following tasks:

(a) Internal reset similar to a Power-On-Reset (POR). All configuration and data register bits are reset to default values.

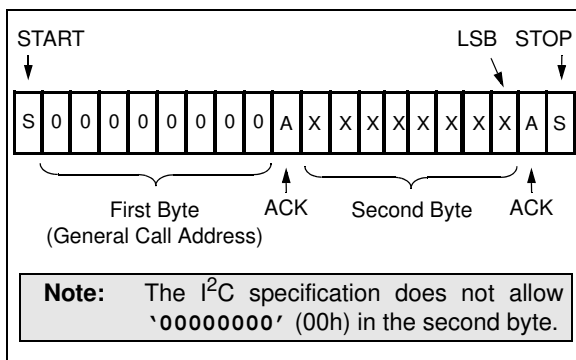
(b) Latch the logic status of external address selection pins (Adr0 and Adr1 pins).

### 5.4.2 GENERAL CALL LATCH (MCP3427 AND MCP3428)

The general call latch occurs if the second byte is `'00000100'` (04h). The device will latch the logic status of the external address selection pins (Adr0 and Adr1 pins), but will not perform a reset.

### 5.4.3 GENERAL CALL CONVERSION

The general call conversion occurs if the second byte is `'00001000'` (08h). All devices on the bus initiate a conversion simultaneously. When the device receives this command, the configuration will be set to the One-Shot Conversion mode and a single conversion will be performed. The PGA and data rate settings are unchanged with this general call.



**FIGURE 5-5:** General Call Address Format.

## 5.5 High-Speed (HS) Mode

The I<sup>2</sup>C specification requires that a high-speed mode device must be 'activated' to operate in high-speed mode. This is done by sending a special address byte of `"00001xxx"` following the START bit. The "xxx" bits are unique to the High-Speed (HS) mode Master. This byte is referred to as the High-Speed (HS) Master Mode Code (HSMMC). The MCP3426/7/8 devices do not acknowledge this byte. However, upon receiving this code, the device switches on its HS mode filters and communicates up to 3.4 MHz on SDA and SCL bus lines. The device will switch out of the HS mode on the next STOP condition.

For more information on the HS mode, or other I<sup>2</sup>C modes, refer to the Phillips I<sup>2</sup>C specification.

## 5.6 I<sup>2</sup>C Bus Characteristics

The I<sup>2</sup>C specification defines the following bus protocol:

- Data transfer may be initiated only when the bus is not busy
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition

Accordingly, the following bus conditions have been defined using [Figure 5-6](#).

### 5.6.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

### 5.6.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

### 5.6.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations can be ended with a STOP condition.

### 5.6.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

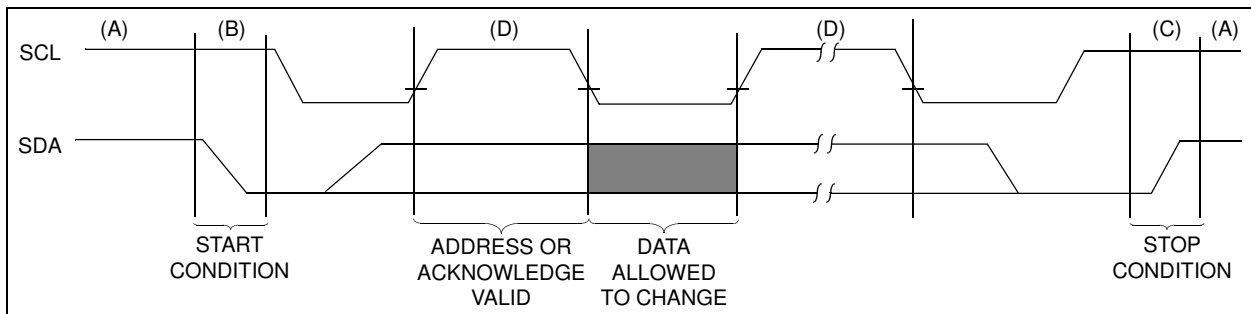
Each data transfer is initiated with a START condition and terminated with a STOP condition.

## 5.6.5 ACKNOWLEDGE AND NON-ACKNOWLEDGE

The Master (microcontroller) and the slave (MCP3426/7/8) use an acknowledge pulse (ACK) as a hand shake of communication for each byte. The ninth clock pulse of each byte is used for the acknowledgement. The clock pulse is always provided by the Master (microcontroller) and the acknowledgement is issued by the receiving device of the byte (Note: The transmitting device must release the SDA line during the acknowledge pulse.). The acknowledgement is achieved by pulling-down the SDA line "LOW" during the 9th clock pulse by the receiving device.

During reads, the Master (microcontroller) can terminate the current read operation by not providing an acknowledge bit (not Acknowledge (NAK)) on the last byte. In this case, the MCP3426/7/8 devices release the SDA line to allow the Master (microcontroller) to generate a STOP or repeated START condition.

The non-acknowledgement (NAK) is issued by providing the SDA line to "HIGH" during the 9th clock pulse.



**FIGURE 5-6:** Data Transfer Sequence on I<sup>2</sup>C Serial Bus.