Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# MCP3550/1/3

## Low-Power, Single-Channel 22-Bit Delta-Sigma ADCs

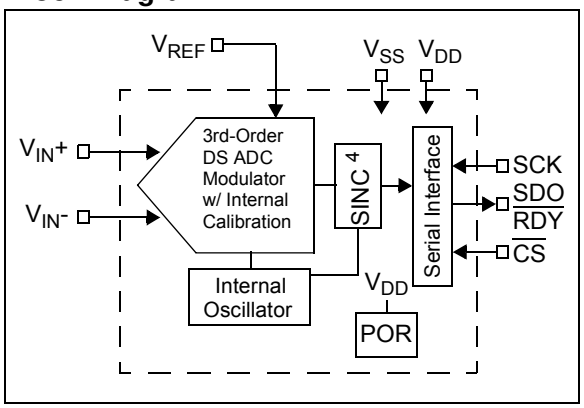
### Features:

- 22-Bit ADC in Small 8-pin MSOP Package with Automatic Internal Offset and Gain Calibration
- Low-Output Noise of 2.5 $\mu V_{RMS}$ with Effective Resolution of 21.9 Bits (MCP3550/1)
- 3 µV Typical Offset Error
- 2 ppm Typical Full Scale Error
- 6 ppm Maximum INL Error
- Total Unadjusted Error Less Than 10 ppm
- No Digital Filter Settling Time, Single-Command Conversions through 3-wire SPI Interface
- Ultra-Low Conversion Current (MCP3550/1):
  - 100 µA Typical ($V_{DD}$ = 2.7V)
  - 120 µA Typical ($V_{DD}$ = 5.0V)
- Differential Input with $V_{SS}$ to $V_{DD}$ Common Mode Range
- 2.7V to 5.5V Single-Supply Operation
- Extended Temperature Range:
  - -40°C to +125°C

### Applications:

- Weigh Scales
- Direct Temperature Measurement
- 6-digit DVMs
- Instrumentation
- Data Acquisition
- Strain Gauge Measurement

### Block Diagram




### Description:

The Microchip Technology Inc. MCP3550/1/3 devices are 2.7V to 5.5V low-power, 22-bit Delta-Sigma Analog-to-Digital Converters (ADCs). The devices offer output noise as low as 2.5 $\mu V_{RMS}$, with a total unadjusted error of 10 ppm. The family exhibits 6 ppm Integral Non-Linearity (INL) error, 3 µV offset error and less than 2 ppm full scale error. The MCP3550/1/3 devices provide high accuracy and low noise performance for applications where sensor measurements (such as pressure, temperature and humidity) are performed. With the internal oscillator and high oversampling rate, minimal external components are required for high-accuracy applications.

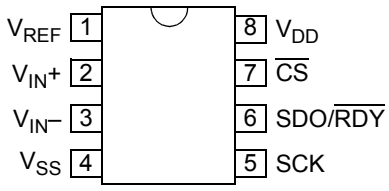
This product line has fully differential analog inputs, making it compatible with a wide variety of sensor, industrial control or process control applications.

The MCP3550/1/3 devices operate from -40°C to +125°C and are available in the space-saving 8-pin MSOP and SOIC packages.

### Package Types

**MCP3550/1/3**

**MSOP, SOIC**



**NOTES:**

# 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings †

$V_{DD}$.....7.0V
All inputs and outputs w.r.t $V_{SS}$ .... ..... -0.3V to $V_{DD}$+ 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current ..... Continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±10 mA
Storage Temperature .....-65°C to +150°C
Ambient temp. with power applied .....-55°C to +125°C
ESD protection on all pins (HBM, MM) ..... ≥ 6 kV, ≥ 400V
Maximum Junction Temperature ($T_J$). .....+150°C

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at -40°C ≤ $T_A$ ≤ +85°C, $V_{DD}$ = 2.7V or 5.0V. $V_{REF}$ = 2.5V. $V_{IN}$+ = $V_{IN}$- = $V_{CM}$ = $V_{REF}$/2. All ppm units use 2*$V_{REF}$ as full scale range. Unless otherwise noted, specification applies to entire MCP3550/1/3 family.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Noise Performance (MCP3550/1)** | | | | | | |
| No Missing Codes | NMC | 22 | — | — | bits | At DC (**Note 5**) |
| Output Noise | $e_N$ | — | 2.5 | — | $\mu V_{RMS}$ | |
| Effective Resolution | ER | — | 21.9 | — | bits RMS | $V_{REF}$ = 5V |
| **Noise Performance (MCP3553)** | | | | | | |
| No Missing Codes | NMC | 20 | — | — | bits | At DC (**Note 5**) |
| Output Noise | $e_N$ | — | 6 | — | $\mu V_{RMS}$ | |
| Effective Resolution | ER | — | 20.6 | — | bits RMS | $V_{REF}$ = 5V |
| **Conversion Times** | | | | | | |
| MCP3550-50 | $t_{CONV}$ | -2.0% | 80 | +2.0% | ms | |
| MCP3550-60 | $t_{CONV}$ | -2.0% | 66.67 | +2.0% | ms | |
| MCP3551 | $t_{CONV}$ | -2.0% | 73.1 | +2.0% | ms | |
| MCP3553 | $t_{CONV}$ | -2.0% | 16.67 | +2.0% | ms | |
| **Accuracy** | | | | | | |
| Integral Non-Linearity | INL | — | ±2 | 6 | ppm | $T_A$ = +25°C only (**Note 2**) |
| Offset Error | $V_{OS}$ | -12 | ±3 | +12 | µV | $T_A$ = +25°C |
| | | — | ±4 | — | µV | $T_A$ = +85°C |
| | | — | ±6 | — | µV | $T_A$ = +125°C |
| Positive Full-Scale Error | $V_{FS,P}$ | -10 | ±2 | +10 | ppm | $T_A$ = +25°C only |
| Negative Full-Scale Error | $V_{FS,N}$ | -10 | ±2 | +10 | ppm | $T_A$ = +25°C only |
| Offset Drift | | — | 0.040 | — | ppm/°C | |
| Positive/Negative Full-Scale Error Drift | | — | 0.028 | — | ppm/°C | |

**Note 1:** This parameter is established by characterization and not 100% tested.
**2:** INL is the difference between the endpoint's line and the measured code at the center of the quantization band.
**3:** This current is due to the leakage current and the current due to the offset voltage between $V_{IN}$+ and $V_{IN}$-.
**4:** Input impedance is inversely proportional to clock frequency; typical values are for the MCP3550/1 device. $V_{REF}$ = 5V.
**5:** Characterized by design, but not tested.
**6:** Rejection performance depends on internal oscillator accuracy; see **Section 4.0 "Device Overview"** for more information on oscillator and digital filter design. MCP3550/1 device rejection specifications characterized from 49 to 61 Hz.

## DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at -40°C ≤ $T_A$ ≤ +85°C, $V_{DD}$ = 2.7V or 5.0V. $V_{REF}$ = 2.5V. $V_{IN}+ = V_{IN}- = V_{CM} = V_{REF}/2$. All ppm units use 2*$V_{REF}$ as full scale range. Unless otherwise noted, specification applies to entire MCP3550/1/3 family.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Rejection Performance**(1,6) | | | | | | |
| Common Mode DC Rejection | | — | -135 | — | dB | $V_{CM}$ range from 0 to $V_{DD}$ |
| Power Supply DC Rejection | | — | -115 | — | dB | |
| Common Mode 50/60 Hz Rejection | CMRR | — | -135 | — | dB | $V_{CM}$ varies from 0V to $V_{DD}$ |
| Power Supply 50/60 Hz Rejection | PSRR | — | -85 | — | dB | **MCP3551** only, $V_{DD}$ varies from 4.5V to 5.5V |
| Power Supply 50/60 Hz Rejection | PSRR | — | -120 | — | dB | **MCP3550-50** or **MCP3550-60** only at 50 or 60 Hz respectively, $V_{DD}$ varies from 4.5V to 5.5V |
| Normal Mode 50 and 60 Hz Rejection | NMRR | — | -85 | — | dB | **MCP3551** only, $0 < V_{CM} < V_{DD}$, $-V_{REF} < V_{IN} = (V_{IN}+ - V_{IN}-) < +V_{REF}$ |
| Normal Mode 50 or 60 Hz Rejection | NMRR | — | -120 | — | dB | **MCP3550-50** or **MCP3550-60** only at 50 or 60 Hz respectively, $0 < V_{CM} < V_{DD}$, $-V_{REF} < V_{IN} = (V_{IN}+ - V_{IN}-) < +V_{REF}$ |
| **Analog Inputs** | | | | | | |
| Differential Input Range | $V_{IN+} - V_{IN-}$ | $-V_{REF}$ | — | $+V_{REF}$ | V | |
| Absolute/Common Mode Voltages | | $V_{SS}$ - 0.3 | — | $V_{DD}$ + 0.3 | V | |
| Analog Input Sampling Capacitor | | — | 10 | — | pF | **Note 5** |
| Differential Input Impedance | | — | 2.4 | — | MΩ | |
| Shutdown Mode Leakage Current | | — | 1 | — | nA | $V_{IN}+ = V_{IN}- = V_{DD}$; $\overline{CS} = V_{DD}$ (**Note 3**) |
| **Reference Input** | | | | | | |
| Voltage Range | | 0.1 | — | $V_{DD}$ | V | |
| Reference Input Sampling Capacitor | | — | 15 | — | pF | **Note 5** |
| Reference Input Impedance | | — | 2.4 | — | MΩ | **Note 4** |
| Shutdown Mode Reference Leakage Current | | — | 1 | — | nA | $V_{IN}+ = V_{IN}- = V_{SS}$; $\overline{CS} = V_{DD}$ |
| **Power Requirements** | | | | | | |
| Power Supply Voltage Range | $V_{DD}$ | 2.7 | — | 5.5 | V | |
| **MCP3550-50, MCP3551** Supply Current | $I_{DD}$ | — | 120 | 170 | µA | $V_{DD}$ = 5V |
| | | — | 100 | — | µA | $V_{DD}$ = 2.7V |
| **MCP3550-60, MCP3553** Supply Current | $I_{DD}$ | — | 140 | 185 | µA | $V_{DD}$ = 5V |
| | | — | 120 | — | µA | $V_{DD}$ = 2.7V |
| Supply Current, Sleep Mode | $I_{DDSL}$ | — | 10 | | µA | |
| Supply Current, Shutdown Mode | $I_{DDS}$ | — | — | 1 | µA | $\overline{CS}$ = SCK = $V_{DD}$ |
| **Serial Interface** | | | | | | |
| Voltage Input High ($\overline{CS}$, SCK) | $V_{IH}$ | 0.7 $V_{DD}$ | — | — | V | |
| Voltage Input Low ($\overline{CS}$, SCK) | $V_{IL}$ | — | — | 0.4 | V | |
| Voltage Output High (SDO/$\overline{RDY}$) | $V_{OH}$ | $V_{DD}$ - 0.5 | — | — | V | $V_{OH}$ = 1 mA, $V_{DD}$ = 5.0V |

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** INL is the difference between the endpoint's line and the measured code at the center of the quantization band.

**3:** This current is due to the leakage current and the current due to the offset voltage between $V_{IN}+$ and $V_{IN}-$.

**4:** Input impedance is inversely proportional to clock frequency; typical values are for the MCP3550/1 device. $V_{REF}$ = 5V.

**5:** Characterized by design, but not tested.

**6:** Rejection performance depends on internal oscillator accuracy; see **Section 4.0 "Device Overview"** for more information on oscillator and digital filter design. MCP3550/1 device rejection specifications characterized from 49 to 61 Hz.

## DC CHARACTERISTICS (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at -40°C ≤ $T_A$ ≤ +85°C, $V_{DD}$ = 2.7V or 5.0V. $V_{REF}$ = 2.5V. $V_{IN}$+ = $V_{IN}$- = $V_{CM}$ = $V_{REF}$/2. All ppm units use 2*$V_{REF}$ as full scale range. Unless otherwise noted, specification applies to entire MCP3550/1/3 family.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Voltage Output Low (SDO/$\overline{RDY}$) | $V_{OL}$ | — | — | 0.4 | V | $V_{OH}$ = -1 mA, $V_{DD}$ = 5.0V |
| Input leakage Current ($\overline{CS}$, SCK) | $I_{LI}$ | -1 | — | 1 | µA | |
| Internal Pin Capacitance ($\overline{CS}$, SCK, SDO/$\overline{RDY}$) | $C_{INT}$ | — | 5 | — | pF | **Note 1** |

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** INL is the difference between the endpoint's line and the measured code at the center of the quantization band.

**3:** This current is due to the leakage current and the current due to the offset voltage between $V_{IN}$+ and $V_{IN}$-.

**4:** Input impedance is inversely proportional to clock frequency; typical values are for the MCP3550/1 device. $V_{REF}$ = 5V.

**5:** Characterized by design, but not tested.

**6:** Rejection performance depends on internal oscillator accuracy; see **Section 4.0 "Device Overview"** for more information on oscillator and digital filter design. MCP3550/1 device rejection specifications characterized from 49 to 61 Hz.

## TEMPERATURE CHARACTERISTICS

**Electrical Specifications:** Unless otherwise indicated

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 8L-MSOP | $\theta_{JA}$ | — | 211 | — | °C/W | |
| Thermal Resistance, 8L-SOIC | $\theta_{JA}$ | — | 149.5 | — | °C/W | |

## SERIAL TIMINGS

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at -40°C ≤ $T_A$ ≤ +85°C, $V_{DD}$ = 3.3V or 5.0V, SDO load = 50 pF.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| CLK Frequency | $f_{SCK}$ | — | — | 5 | MHz | |
| CLK High | $t_{HI}$ | 90 | — | — | ns | |
| CLK Low | $t_{LO}$ | 90 | — | — | ns | |
| CLK fall to output data valid | $t_{DO}$ | 0 | — | 90 | ns | |
| $\overline{CS}$ low to indicate $\overline{RDY}$ state | $t_{RDY}$ | 0 | — | 50 | ns | |
| $\overline{CS}$ minimum low time | $t_{CSL}$ | 8 | — | — | µs | **Note** |
| $\overline{RDY}$ flag setup time | $t_{SU}$ | 20 | — | — | ns | |
| $\overline{CS}$ rise to output disable | $t_{DIS}$ | 20 | — | — | ns | |
| $\overline{CS}$ disable time | $t_{CSD}$ | 90 | — | — | ns | |
| Power-up to $\overline{CS}$ LOW | $t_{PUCSL}$ | — | 10 | — | µs | |
| $\overline{CS}$ High to Shutdown Mode | $t_{CSHSD}$ | — | 10 | — | µs | |

**Note:** This parameter is established by characterization and not 100% tested.

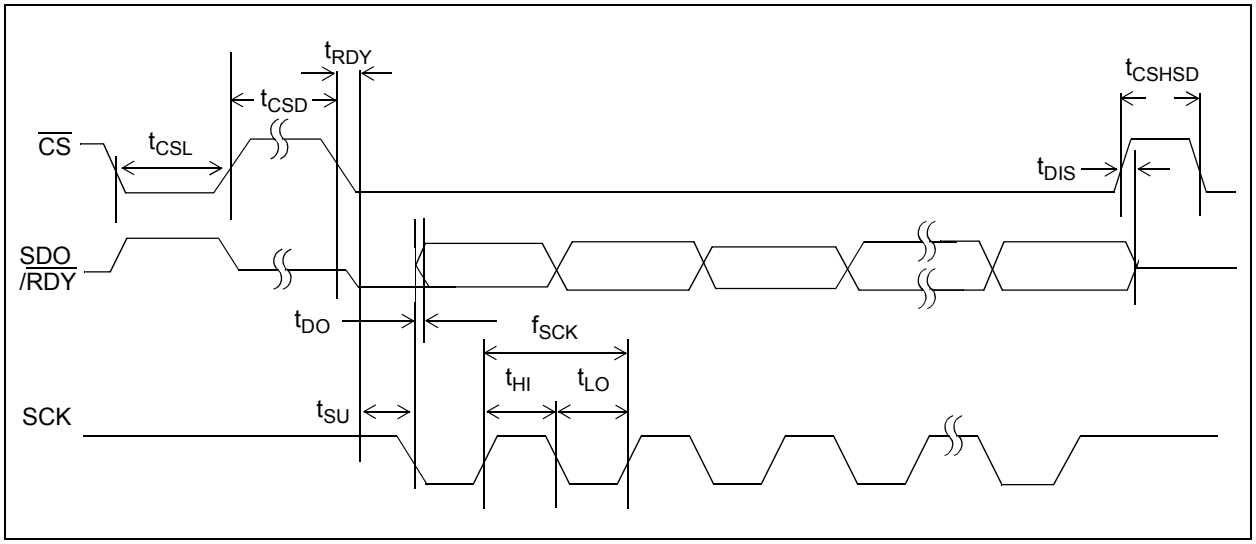



***FIGURE 1-1:*** *Serial Timing.*

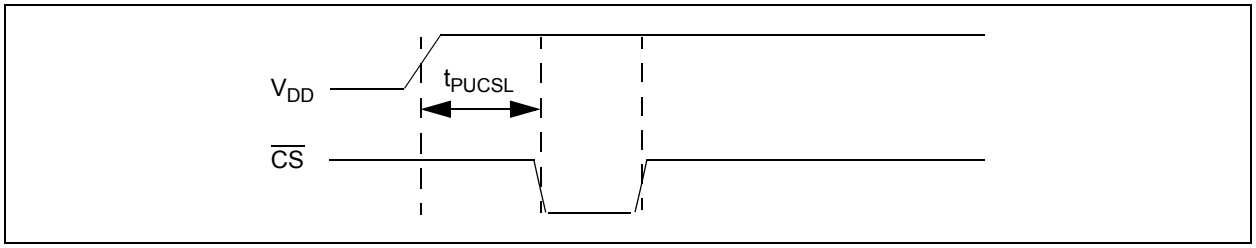



***FIGURE 1-2:*** *Power-Up Timing.*

## 2.0 TYPICAL PERFORMANCE CURVES

| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |
|---|---|

**Note:** Unless otherwise specified, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{REF}$ = 2.5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{REF}$/2, $V_{IN}$+ = $V_{IN}$-.
All ppm units use 2*$V_{REF}$ as full scale range. Unless otherwise noted, graphs apply to entire MCP3550/1/3 family.

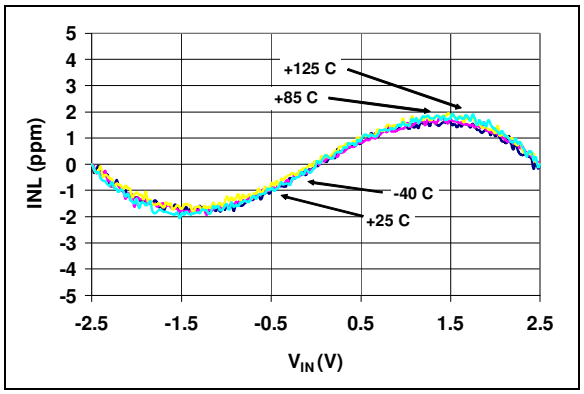



***FIGURE 2-1:*** *INL Error vs. Input Voltage ($V_{DD}$ = 2.7V).*

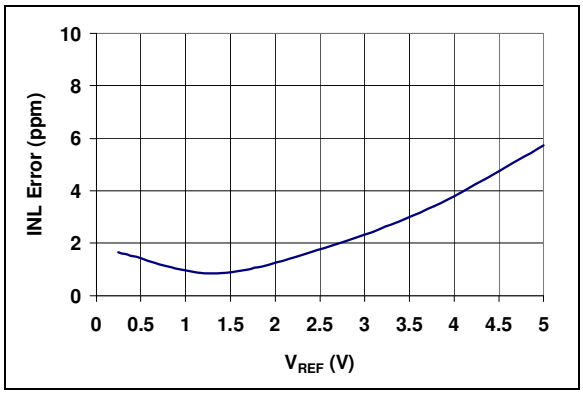



***FIGURE 2-4:*** *Maximum INL Error vs. $V_{REF}$.*

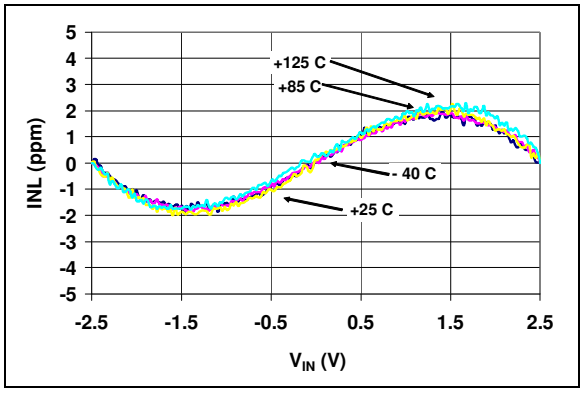



***FIGURE 2-2:*** *INL Error vs. Input Voltage ($V_{DD}$ = 5.0V).*

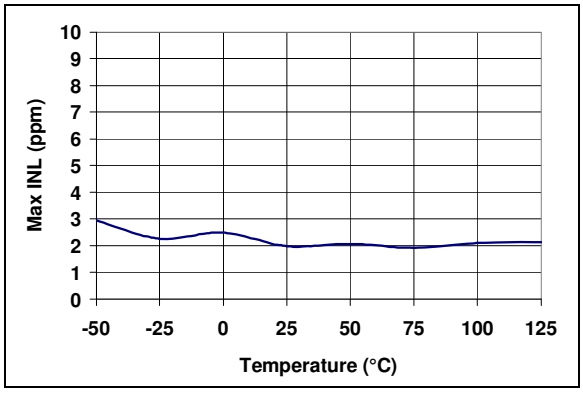



***FIGURE 2-5:*** *Maximum INL Error vs. Temperature.*

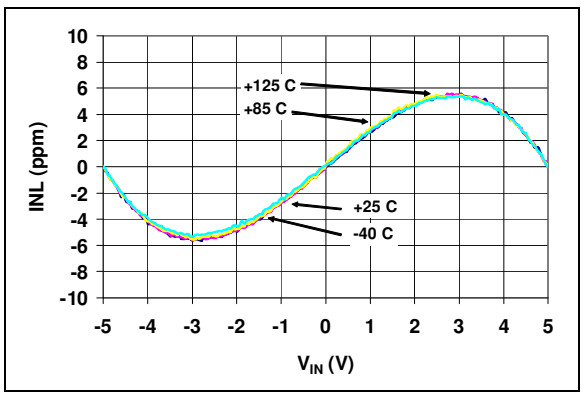



***FIGURE 2-3:*** *INL Error vs. Input Voltage ($V_{DD}$ = 5.0V, $V_{REF}$ = 5V).*

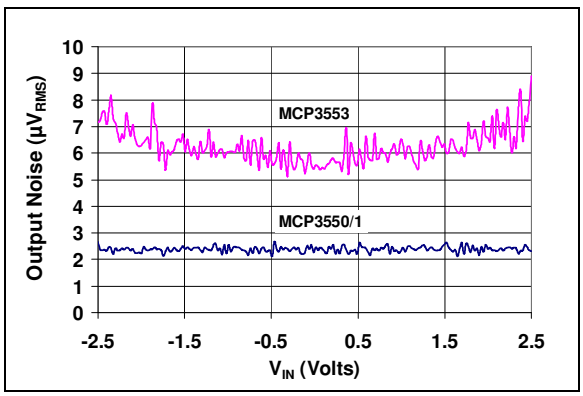



***FIGURE 2-6:*** *Output Noise vs. Input Voltage ($V_{DD}$ = 2.7V).*

**Note:** Unless otherwise specified, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{REF}$ = 2.5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{REF}$/2, $V_{IN}$+ = $V_{IN}$-.
All ppm units use 2*$V_{REF}$ as full scale range. Unless otherwise noted, graphs apply to entire MCP3550/1/3 family.

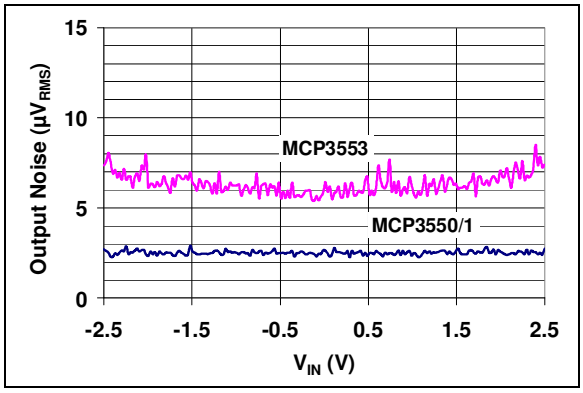



***FIGURE 2-7:*** *Output Noise vs. Input Voltage ($V_{DD}$ = 5.0V).*

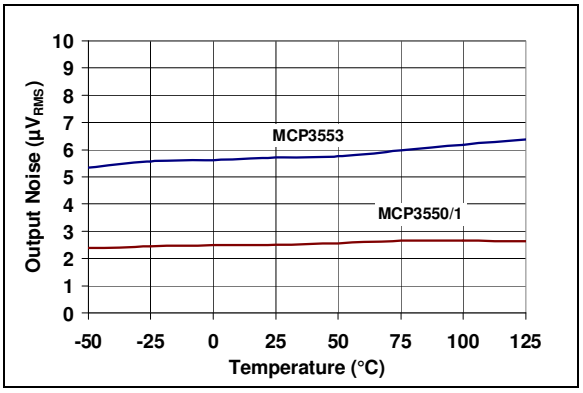



***FIGURE 2-10:*** *Output Noise vs. Temperature.*

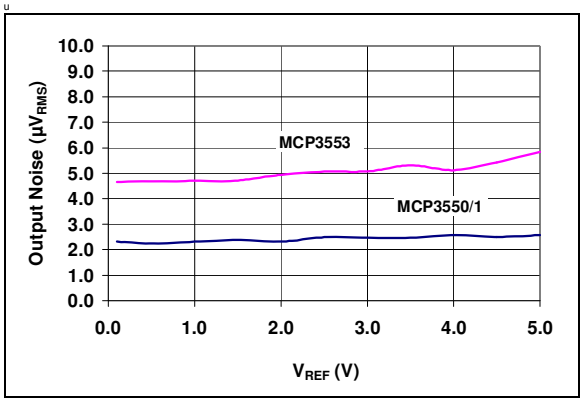



***FIGURE 2-8:*** *Output Noise vs. $V_{REF}$.*

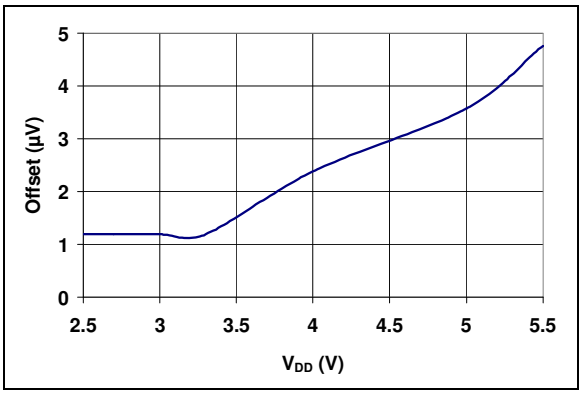



***FIGURE 2-11:*** *Offset Error vs $V_{DD}$ ($V_{CM}$ = 0V).*

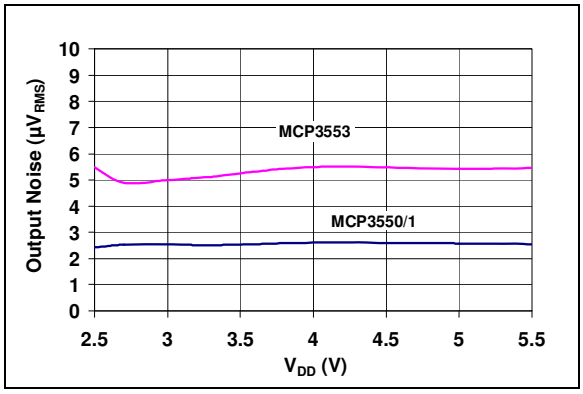



***FIGURE 2-9:*** *Output Noise vs.$V_{DD}$.*

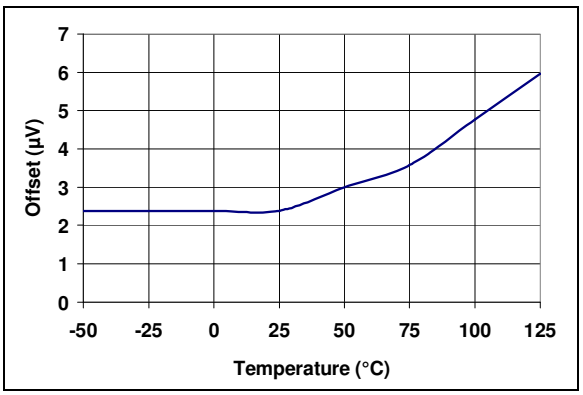



***FIGURE 2-12:*** *Offset Error vs. Temperature ($V_{REF}$ = 5.0V).*

**Note:** Unless otherwise specified, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{REF}$ = 2.5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{REF}$/2, $V_{IN}$+ = $V_{IN}$-. All ppm units are ratioed against 2*$V_{REF}$ . Unless otherwise noted, graphs apply to entire MCP3550/1/3 family.

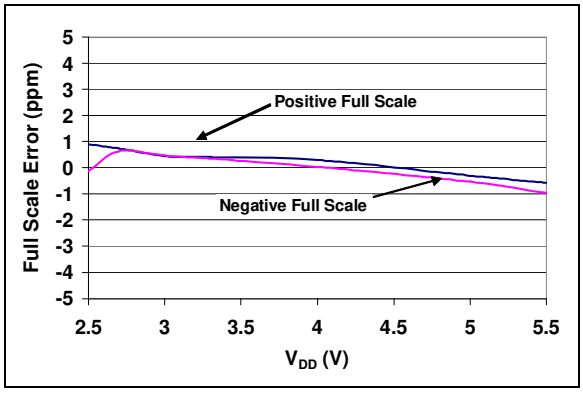



***FIGURE 2-13:*** *Full Scale Error vs. $V_{DD}$.*

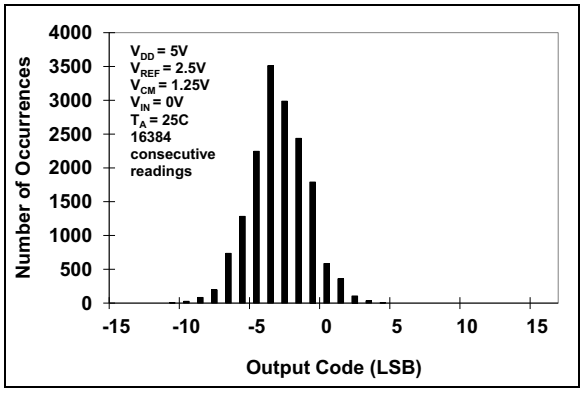



***FIGURE 2-16:*** *MCP3550/1 Output Noise Histogram.*

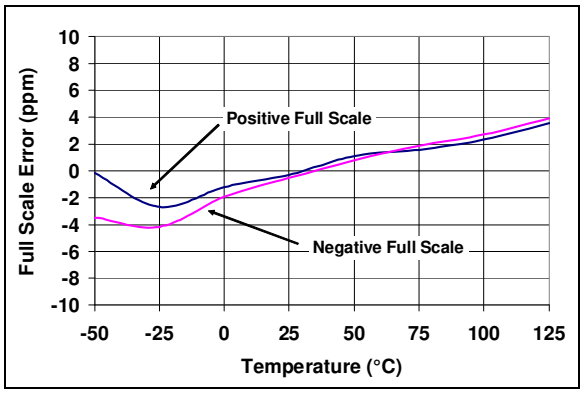



***FIGURE 2-14:*** *Full Scale Error vs. Temperature.*

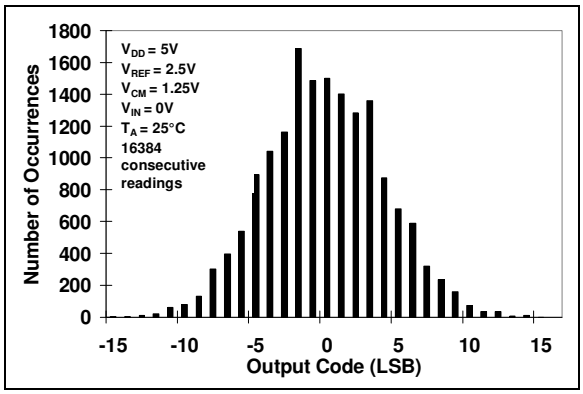



***FIGURE 2-17:*** *MCP3553 Output Noise Histogram.*

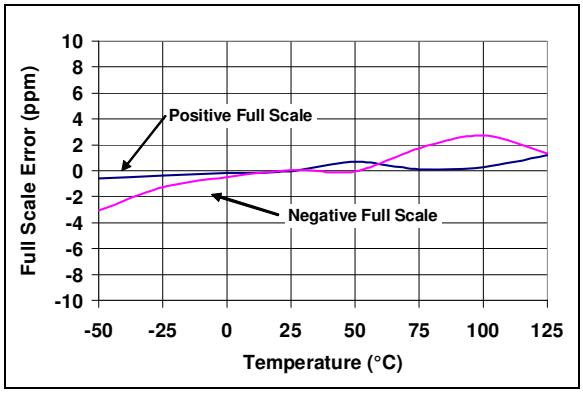



***FIGURE 2-15:*** *Full Scale Error vs. Temperature ($V_{REF}$ = 5.0V).*

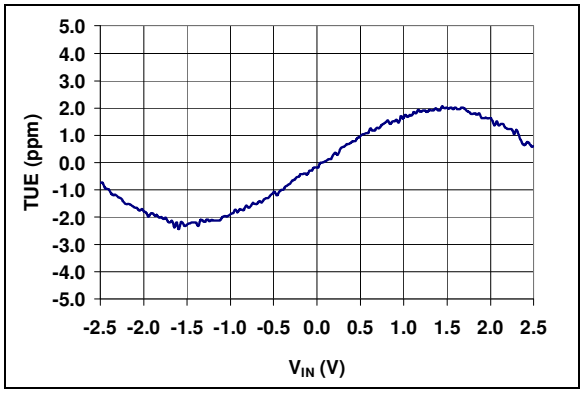



***FIGURE 2-18:*** *Total Unadjusted Error (TUE) vs. Input Voltage ($V_{DD}$ = 2.7V).*

**Note:** Unless otherwise specified, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{REF}$ = 2.5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{REF}$/2, $V_{IN}$+ = $V_{IN}$-.
All ppm units use 2*$V_{REF}$ as full scale range. Unless otherwise noted, graphs apply to entire MCP3550/1/3 family.

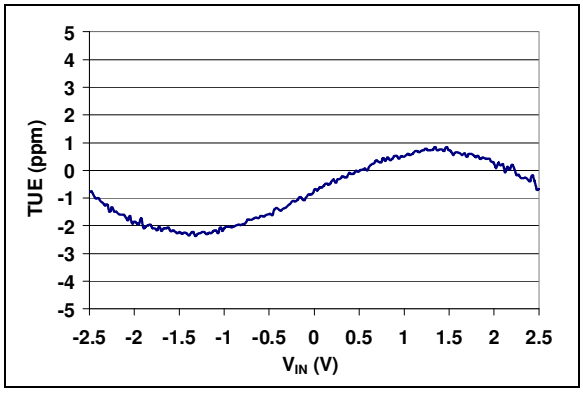



***FIGURE 2-19:*** *Total Unadjusted Error (TUE) vs. Input Voltage.*

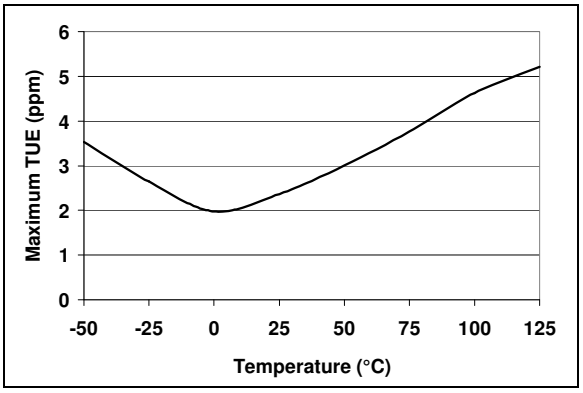



***FIGURE 2-22:*** *Maximum TUE vs. Temperature.*

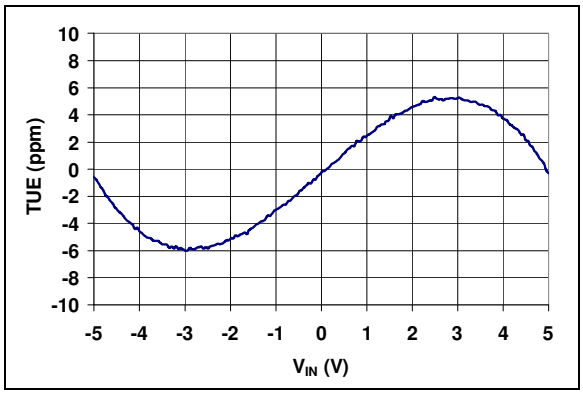



***FIGURE 2-20:*** *Total Unadjusted Error (TUE) vs. Input Voltage ($V_{REF}$ = 5.0V).*

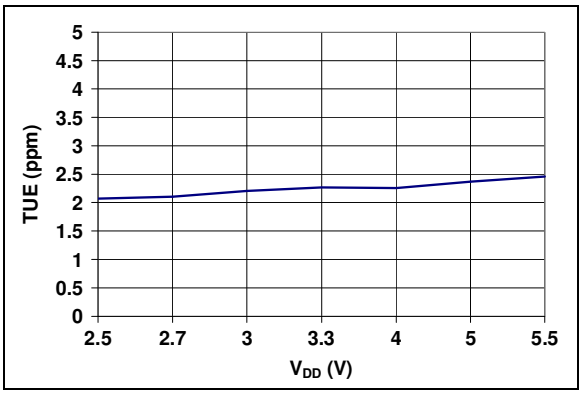



***FIGURE 2-23:*** *Maximum TUE vs. $V_{DD}$.*

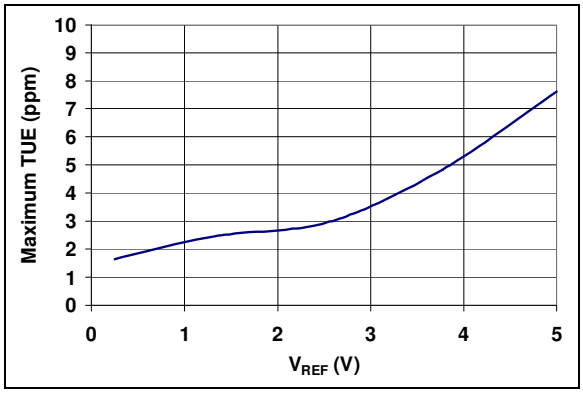



***FIGURE 2-21:*** *Maximum TUE vs. $V_{REF}$.*

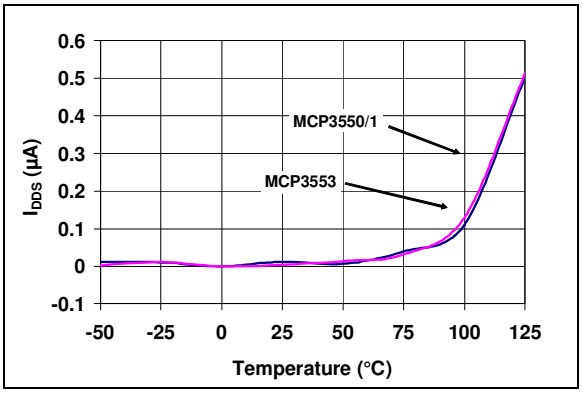



***FIGURE 2-24:*** *$I_{DDS}$ vs. Temperature.*

**Note:** Unless otherwise specified, $T_A$ = +25°C, $V_{DD}$ = 5V, $V_{REF}$ = 2.5V, $V_{SS}$ = 0V, $V_{CM}$ = $V_{REF}$/2, $V_{IN}$+ = $V_{IN}$-.
All ppm units use 2*$V_{REF}$ as full scale range. Unless otherwise noted, graphs apply to entire MCP3550/1/3 family.

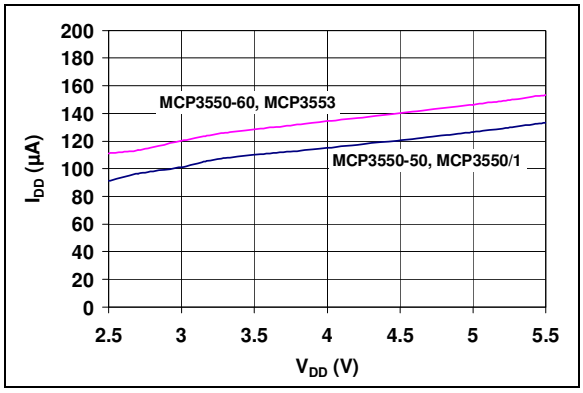



***FIGURE 2-25:*** *$I_{DD}$ vs. $V_{DD}$.*

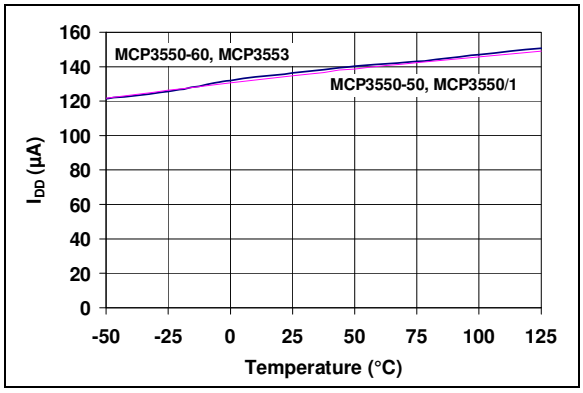



***FIGURE 2-26:*** *$I_{DD}$ vs. Temperature.*

**NOTES:**

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| MCP3550/1/3 MSOP, SOIC | Symbol | I/O/P | Description |
|---|---|---|---|
| 1 | $V_{REF}$ | I | Reference Voltage Analog Input pin |
| 2 | $V_{IN}$+ | I | Non-inverting Analog Input pin |
| 3 | $V_{IN}$- | I | Inverting Analog Input pin |
| 4 | $V_{SS}$ | P | Ground pin |
| 5 | SCK | I | Serial Clock Digital Input pin |
| 6 | SDO/$\overline{RDY}$ | O | Data/Ready Digital Output pin |
| 7 | $\overline{CS}$ | I | Chip Select Digital Input pin |
| 8 | $V_{DD}$ | P | Positive Supply Voltage pin |

Type Identification: I = Input; O = Output; P = Power

### 3.1 Voltage Reference ($V_{REF}$)

The MCP3550/1/3 devices accept single-ended reference voltages from 0.1V to $V_{DD}$. Since the converter output noise is dominated by thermal noise, which is independent of the reference voltage, the output noise is not significantly improved by diminishing the reference voltage at the $V_{REF}$ input pin. A reduced voltage reference will significantly improve the INL performance (see Figure 2-4); the INL max error is proportional to $V_{REF}^2$.

### 3.2 Analog Inputs ($V_{IN}$+, $V_{IN}$-)

The MCP3550/1/3 devices accept a fully differential analog input voltage to be connected on the $V_{IN}$+ and $V_{IN}$- input pins. The differential voltage that is converted is defined by $V_{IN} = V_{IN}+ - V_{IN}-$. The differential voltage range specified for ensured accuracy is from $-V_{REF}$ to $+V_{REF}$. However, the converter will still output valid and usable codes with the inputs overranged by up to 12% (see **Section 5.0 "Serial Interface"**) at room temperature. This overrange is clearly specified by two overload bits in the output code.

The absolute voltage range on these input pins extends from $V_{SS}$ – 0.3V to $V_{DD}$ + 0.3V. Any voltage above or below this range will create leakage currents through the Electrostatic Discharge (ESD) diodes. This current will increase exponentially, degrading the accuracy and noise performance of the device. The common mode of the analog inputs should be chosen such that both the differential analog input range and the absolute voltage range on each pin are within the specified operating range defined in **Section 1.0 "Electrical Characteristics"**.

### 3.3 Supply Voltage ($V_{DD}$, $V_{SS}$)

$V_{DD}$ is the power supply pin for the analog and digital circuitry within the MCP3550/1/3. This pin requires an appropriate bypass capacitor of 0.1 µF. The voltage on this pin should be maintained in the 2.7V to 5.5V range for specified operation. $V_{SS}$ is the ground pin and the current return path for both analog and digital circuitry of the MCP3550/1/3. If an analog ground plane is available, it is recommended that this device be tied to the analog ground plane of the Printed Circuit Board (PCB).

### 3.4 Serial Clock (SCK)

SCK synchronizes data communication with the device. The device operates in both SPI mode 1,1 and SPI mode 0,0. Data is shifted out of the device on the falling edge of SCK. Data is latched in on the rising edge of SCK. During $\overline{CS}$ high times, the SCK pin can idle either high or low.

### 3.5 Data Output (SDO/$\overline{RDY}$)

SDO/$\overline{RDY}$ is the output data pin for the device. Once a conversion is complete, this pin will go active-low, acting as a ready flag. Subsequent falling clock edges will then place the 24-bit data word (two overflow bits and 22 bits of data, see **Section 5.0 "Serial Interface"**) on the SPI bus through the SDO pin. Data is clocked out on the falling edge of SCK.

### 3.6 Chip Select ($\overline{CS}$)

$\overline{CS}$ gates all communication to the device and can be used to select multiple devices that share the same SCK and SDO/$\overline{RDY}$ pins. This pin is also used to control the internal conversions, which begin on the falling edge of $\overline{CS}$. Raising $\overline{CS}$ before the first internal conversion is complete places the device in Single Conversion mode. Leaving $\overline{CS}$ low will place the device in Continuous Conversion mode (i.e., additional internal conversions will automatically occur). $\overline{CS}$ may be tied permanently low for two-wire Continuous Conversion mode operation. SDO/$\overline{RDY}$ enters a high-impedance state with $\overline{CS}$ high.

## 4.0 DEVICE OVERVIEW

The MCP3550/1/3 devices are 22-bit delta-sigma ADCs that include fully differential analog inputs, a third-order delta-sigma modulator, a fourth-order modified SINC decimation filter, an on-chip, low-noise internal oscillator, a power supply monitoring circuit and an SPI 3-wire digital interface. These devices can be easily used to measure low-frequency, low-level signals such as those found in pressure transducers, temperature, strain gauge, industrial control or process control applications. The power supply range for this product family is 2.7V to 5.5V; the temperature range is -40°C to +125°C. The functional block diagram for the MCP3550/1/3 devices is shown in Figure 4-1.

A Power-On Reset (POR) monitoring circuit is included to ensure proper power supply voltages during the conversion process. The clock source for the part is internally generated to ±0.5% over the full-power supply voltage range and industrial temperature range. This stable clock source allows for superior conversion repeatability and minimal drift across conversions.

The MCP3550/1/3 devices employ a delta-sigma conversion technique to realize up to 22 bits of no missing code performance with 21.9 Effective Number of Bits (ENOB). These devices provide single-cycle conversions with no digital filter settling time. Every conversion includes an internal offset and gain auto-calibration to reduce device error. These calibrations are transparent to the user and are done in real-time during the conversion. Therefore, these devices do not require any additional time or conversion to proceed, allowing easy usage of the devices for multiplexed applications. The MCP3550/1/3 devices incorporate a fourth-order digital decimation filter in order to allow superior averaging performance, as well as excellent line frequency rejection capabilities. The oversampling frequency also reduces any external anti-aliasing filter requirements.

The MCP3550/1/3 devices communicate with a simple 3-wire SPI interface. The interface controls the conversion start event, with an added feature of an auto-conversion at system power-up by tying the $\overline{CS}$ pin to logic-low. The device can communicate with bus speeds of up to 5 MHz, with 50 pF capacitive loading. The interface offers two conversion modes: Single Conversion mode for multiplexed applications and a Continuous Conversion mode for multiple conversions in series. Every conversion is independent of each other. That is, all internal registers are flushed between conversions. When the device is not converting, it automatically goes into Shutdown mode and, while in this mode, consumes less than 1 µA.

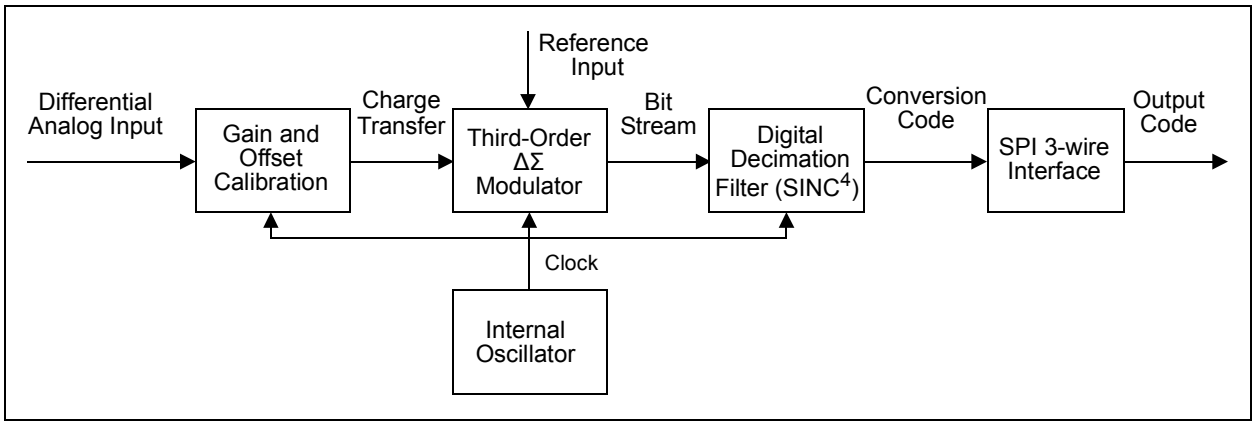



***FIGURE 4-1:*** *MCP3550/1/3 Functional Block Diagram.*

## 4.1 MCP3550/1/3 Delta-Sigma Modulator with Internal Offset and Gain Calibration

The converter core of the MCP3550/1/3 devices is a third-order delta-sigma modulator with automatic gain and offset error calibrations. The modulator uses a 1-bit DAC structure. The delta-sigma modulator processes the sampled charges through switched capacitor structures controlled by a very low drift oscillator for reduced clock jitter.

During the conversion process, the modulator outputs a bit stream with the bit frequency equivalent to the $f_{OSC}/4$ (see Table 4-1). The high oversampling implemented in the modulator ensures very high resolution and high averaging factor to achieve low-noise specifications. The bit stream output of the modulator is then processed by the digital decimation filter in order to provide a 22-bit output code at a data rate of 12.5 Hz for the MCP3550-50, 15 Hz for the MCP3550-60, 13.75 Hz for the MCP3551 and 60 Hz for the MCP3553. Since the oversampling ratio is lower with the MCP3553 device, a much higher output data rate is achieved while still achieving 20 bits No Missing Codes (NMC) and 20.6 ENOB.

A self-calibration of offset and gain occurs at the onset of every conversion. The conversion data available at the output of the device is always calibrated for offset and gain through this process. This offset and gain auto-calibration is performed internally and has no impact on the speed of the converter since the offset and gain errors are calibrated in real-time during the conversion. The real-time offset and gain calibration schemes do not affect the conversion process.

## 4.2 Digital Filter

The MCP3550/1/3 devices include a digital decimation filter, which is a fourth-order modified SINC filter. This filter averages the incoming bit stream from the modulator and outputs a 22-bit conversion word in binary two's complement. When all bits have been processed by the filter, the output code is ready for SPI communication, the $\overline{RDY}$ flag is set on the SDO/$\overline{RDY}$ pin and all the internal registers are reset in order to process the next conversion.

Like the commonly used SINC filter, the modified SINC filter in the MCP3550/1/3 family has the main notch frequency located at $f_S/(OSR*L)$, where $f_S$ is the bit stream sample frequency. OSR is the Oversampling Ratio and L is the order of the filter.

The MCP3550-50 device has the main filter notch located at 50 Hz. For the MCP3550-60 device, the notch is located at 60 Hz. The MCP3551 device has its notch located at 55 Hz, and for the MCP3553 device, the main notch is located at 240 Hz, with an OSR of 128. (see Table 4-1 for rejection performance).

The digital decimation SINC filter has been modified in order to offer staggered zeros in its transfer function. This modification is intended to widen the main notch in order to be less sensitive to oscillator deviation or line-frequency drift. The MCP3551 filter has staggered zeros spread in order to reject both 50 Hz and 60 Hz line frequencies simultaneously (see Figure 4-2).

**TABLE 4-1: DATA RATE, OUTPUT NOISE AND DIGITAL FILTER SPECIFICATIONS BY DEVICE**

| Device | Output Data Rate ($t_{CONV}$) (Note) | Output Noise ($\mu V_{RMS}$) | Primary Notch (Hz) | Sample Frequency ($f_S$) | Internal Clock $f_{OSC}$ | 50/60 Hz Rejection |
|---|---|---|---|---|---|---|
| MCP3550-50 | 80.00 ms | 2.5 | 50 | 25600 Hz | 102.4 kHz | -120 dB min. at 50 Hz |
| MCP3550-60 | 66.67 ms | 2.5 | 60 | 30720 Hz | 122.88 kHz | -120 dB min. at 60 Hz |
| MCP3551 | 72.73 ms | 2.5 | 55 | 28160 Hz | 112.64 kHz | -82 dB min. from 48 Hz to 63 Hz. -82 dB at 50 Hz and -88 dB at 60 Hz |
| MCP3553 | 16.67 ms | 6 | 240 | 30720 Hz | 122.88 kHz | Not Applicable |

**Note:** For the first conversion after exiting Shutdown, $t_{CONV}$ must include an additional 144 $f_{OSC}$ periods before the conversion is complete and the $\overline{RDY}$ (Ready) flag appears on SDO/$\overline{RDY}$.

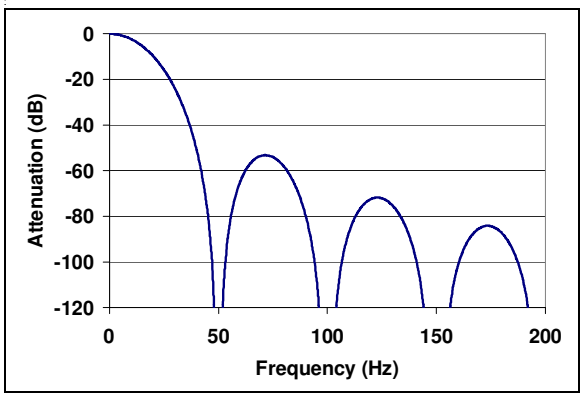



***FIGURE 4-2:*** *SINC Filter Response, MCP3550-50 Device.*

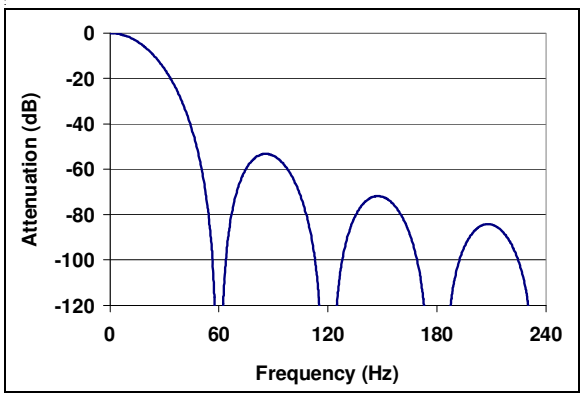



***FIGURE 4-3:*** *SINC Filter Response, MCP3550-60 Device.*

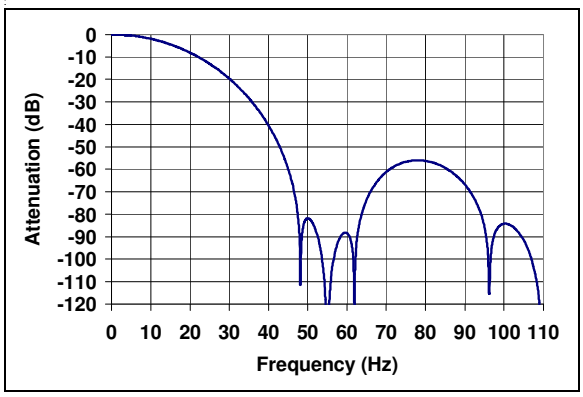



***FIGURE 4-4:*** *SINC Filter Response, MCP3551 Device, Simultaneous 50/60 Hz Rejection.*

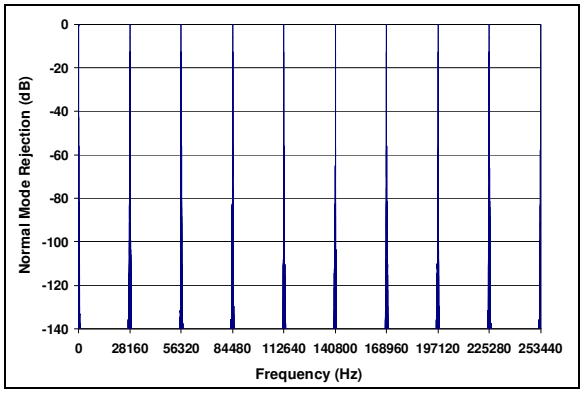



***FIGURE 4-5:*** *SINC Filter Response at Integer Multiples of the Sampling Frequency ($f_s$).*

## 4.3 Internal Oscillator

The MCP3550/1/3 devices include a highly stable and accurate internal oscillator that provides clock signals to the delta-sigma ADC with minimum jitter. The oscillator is a specialized structure with a low temperature coefficient across the full range of specified operation. See Table 4-1 for oscillator frequencies.

The conversion time is an integer multiple of the internal clock period and, therefore, has the same accuracy as the internal clock frequency. The internal oscillator frequency is 102.4 kHz ±1% for the MCP3550-50, 112.64 kHz ±1% for the MCP3551, and 122.88 kHz ±1% for the MCP3550-60 and MCP3553 devices, across the full power supply voltage and specified temperature ranges.

The notch of the digital filter is proportional to the internal oscillator frequency, with the exact notch frequency equivalent to the oscillator accuracy (< 1% deviation). This high accuracy, combined with wide notches, will ensure that the MCP3551 will have simultaneous 50 Hz and 60 Hz line frequency rejection and the MCP3550-50 or MCP3550-60 devices will have greater than 120 dB rejection (at either 50 or 60 Hz) by the digital filtering, even when jitter is present.

The internal oscillator is held in the reset condition when the part is in Shutdown mode to ensure very low power consumption (< 1 µA in Shutdown mode). The internal oscillator is independent of all serial digital interface edges (i.e., state machine processing the digital SPI interface is asynchronous with respect to the internal clock edges).

## 4.4 Differential Analog Inputs

The MCP3550/1/3 devices accept a fully differential analog input voltage to be connected to the $V_{IN+}$ and $V_{IN-}$ input pins. The differential voltage that is converted is defined by $V_{IN} = V_{IN}+ – V_{IN}-$. The differential voltage range specified for ensured accuracy is from $-V_{REF}$ to $+V_{REF}$.

The converter will output valid and usable codes from -112% to 112% of output range (see **Section 5.0 "Serial Interface"**) at room temperature. The ±12% overrange is clearly specified by two overload bits in the output code: OVH and OVL. This feature allows for system calibration of a positive gain error.

The absolute voltage range on these input pins extends from $V_{SS}$ - 0.3V to $V_{DD}$ + 0.3V. If the input voltages are above or below this range, the leakage currents of the ESD diodes will increase exponentially, degrading the accuracy and noise performance of the converter. The common mode of the analog inputs should be chosen such that both the differential analog input range and absolute voltage range on each pin are within the specified operating range defined in **Section 1.0 "Electrical Characteristics"**.

Both the analog differential inputs and the reference input have switched-capacitor input structures. The input capacitors are charged and discharged alternatively with the input and the reference in order to process a conversion. The charge and discharge of the input capacitors create dynamic input currents at the $V_{IN}+$ and $V_{IN}-$ input pins inversely proportional to the sampling capacitor. This current is a function of the differential input voltages and their respective common modes. The typical value of the differential input impedance is 2.4 MΩ, with $V_{CM}$ = 2.5V, $V_{DD} = V_{REF}$ = 5V. The DC leakage current caused by the ESD input diodes, even though on the order of 1 nA, can cause additional offset errors proportional to the source resistance at the $V_{IN}+$ and $V_{IN}-$ input pins.

From a transient response standpoint and as a first-order approximation, these input structures form a simple RC filtering circuit with the source impedance in series with the $R_{ON}$ (switched resistance when closed) of the input switch and the sampling capacitor. In order to ensure the accuracy of the sampled charge, proper settling time of the input circuit has to be considered. Slow settling of the input circuit will create additional gain error. As a rule of thumb, in order to obtain 1 ppm absolute measurement accuracy, the sampling period must be 14 times greater than the input circuit RC time constant.

## 4.5 Voltage Reference Input Pin

The MCP3550/1/3 devices accept a single-ended external reference voltage, to be connected on the $V_{REF}$ input pin. Internally, the reference voltage for the ADC is a differential voltage with the non-inverting input connected to the $V_{REF}$ pin and the inverting input connected to the $V_{SS}$ pin. The value of the reference voltage is $V_{REF}$ - $V_{SS}$ and the common mode of the reference is always ($V_{REF}$ - $V_{SS}$)/2.

The MCP3550/1/3 devices accept a single-ended reference voltage from 0.1V to $V_{DD}$. The converter output noise is dominated by thermal noise that is independent of the reference voltage. Therefore, the output noise is not significantly improved by lowering the reference voltage at the $V_{REF}$ input pin. However, a reduced reference voltage will significantly improve the INL performance since the INL max error is proportional to $V_{REF}^2$ (see Figure 2-4).

The charge and discharge of the input capacitor create dynamic input currents at the $V_{REF}$ input pin inversely proportional to the sampling capacitor, which is a function of the input reference voltage. The typical value of the single-ended input impedance is 2.4 MΩ, with $V_{DD} = V_{REF}$ = 5V. The DC leakage current caused by the ESD input diodes, though on the order of 1 nA typically, can cause additional gain error proportional to the source resistance at the $V_{REF}$ pin.

## 4.6 Power-On Reset (POR)

The MCP3550/1/3 devices contain an internal Power-On Reset (POR) circuit that monitors power supply voltage $V_{DD}$ during operation. This circuit ensures correct device start-up at system power-up and power-down events. The POR has built-in hysteresis and a timer to give a high degree of immunity to potential ripple and noise on the power supplies, as well as to allow proper settling of the power supply during power-up. A 0.1 µF decoupling capacitor should be mounted as close as possible to the $V_{DD}$ pin, providing additional transient immunity.

The threshold voltage is set at 2.2V, with a tolerance of approximately ±5%. If the supply voltage falls below this threshold, the MCP3550/1/3 devices will be held in a reset condition or in Shutdown mode. When the part is in Shutdown mode, the power consumption is less than 1 µA. The typical hysteresis value is around 200 mV in order to prevent reset during brown-out or other glitches on the power supply.

Once a power-up event has occurred, the device must require additional time before a conversion can take place. During this time, all internal analog circuitry must settle before the first conversion can occur. An internal timer counts 32 internal clock periods before the internal oscillator can provide clock to the conversion process. This allows all internal analog circuitry to settle to their proper operating point. This timing is typically less than 300 µs, which is negligible compared to one conversion time (e.g. 72.7 ms for the MCP3551). Figure 4-6 illustrates the conditions for a power-up and power-down event under typical start-up conditions.

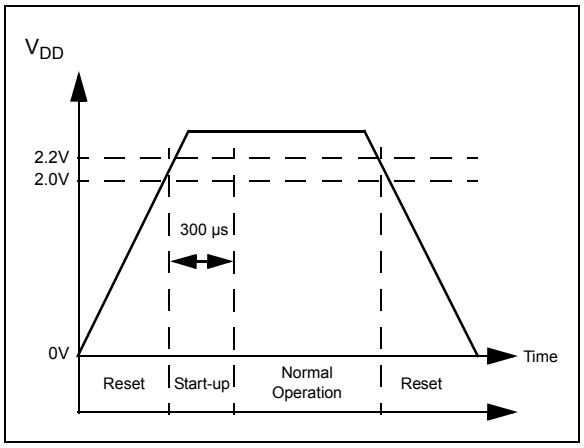



***FIGURE 4-6:*** *Power-On Reset Operation.*

## 4.7 Shutdown Mode

When not internally converting, the two modes of operation for the MCP3550/1/3 devices are the Shutdown and Sleep modes. During Shutdown mode, all internal analog circuitry, including the POR, is turned off and the device consumes less than 1 µA. When exiting Shutdown mode, the device must require additional time before a conversion can take place. During this time, all internal analog circuitry must settle before the first conversion can occur. An internal timer counts 32 internal clock periods before the internal oscillator can provide clock to the conversion process. This allows all internal analog circuitry to settle to their proper operating point. This timing is typically less than 300 µs, which is negligible compared to one conversion time (72.7 ms for MCP3551).

## 4.8 Sleep Mode

During Sleep mode, the device is not converting and is awaiting data retrieval; the internal analog circuitry is still running and the device typically consumes 10 µA. In order to restart a conversion while in Sleep mode, toggling $\overline{CS}$ to a logic-high (placing the part in Shutdown mode) and then back to a logic-low will restart the conversion. Sleep can only be entered in Single Conversion mode. Once a conversion is complete in Single Conversion mode, the device automatically enters Sleep mode.

**NOTES:**

# 5.0 SERIAL INTERFACE

## 5.1 Overview

Serial communication between the microcontroller and the MCP3550/1/3 devices is achieved using $\overline{CS}$, SCK and SDO/$\overline{RDY}$. There are two modes of operation: Single Conversion and Continuous Conversion. $\overline{CS}$ controls the conversion start. There are 24 bits in the data word: 22 bits of conversion data and two overflow bits. The conversion process takes place via the internal oscillator and the status of this conversion must be detected. The typical method of communication is shown in Figure 5-1. The status of the internal conversion is the SDO/$\overline{RDY}$ pin and is available with $\overline{CS}$ low. A High state on SDO/$\overline{RDY}$ means the device is busy converting, while a Low state means the conversion is finished and data is ready for transfer using SCK. SDO/$\overline{RDY}$ remains in a high-impedance state when $\overline{CS}$ is held high. $\overline{CS}$ must be low when clocking out the data using SCK and SDO/$\overline{RDY}$.

Bit 22 is Overflow High (OVH) when $V_{IN} > V_{REF} - 1$ LSB, OVH toggles to logic '1', detecting an overflow high in the analog input voltage.

Bit 23 is Overflow Low (OVL) when $V_{IN} < -V_{REF}$, OVL toggles to logic '1', detecting an overflow low in the analog input voltage. The state OVH = OVL = '1' is not defined and should be considered as an interrupt for the SPI interface meaning erroneous communication.

Bit 21 to bit 0 represents the output code in 22-bit binary two's complement. Bit 21 is the sign bit and is logic '0' when the differential analog input is positive and logic '1' when the differential analog input is negative. From Bit 20 to bit 0, the output code is given MSb first (MSb is bit 20 and LSB is Bit 0). When the analog input value is comprised between $-V_{REF}$ and $V_{REF} - 1$ LSB, the two overflow bits are set to logic '0'. The relationship between input voltage and output code is shown in Figure 5-1.

The delta-sigma modulator saturation point for the differential analog input is located at around ±112% of $V_{REF}$ (at room temperature), meaning that the modulator will still give accurate output codes with an overrange of 12% below or above the reference voltage. Unlike the usual 22-bit device, the 22-bit output code will not lock at 0x1FFFFF for positive sign inputs or 0x200000 for negative sign inputs in order to take advantage of the overrange capabilities of the device. This can be practical for closed-loop operations, for instance. In case of an overflow, the output code becomes a 23-bit two's complement output code, where the sign bit will be the OVL bit. If an overflow high or low is detected, OVL (bit 23) becomes the sign bit (instead of bit 21), the MSb is then bit 21 and the converter can be used as a 23-bit two's complement code converter, with output code from bits B21 to B0, and OVL as the sign bit. Figure 5-1 summarizes the output coding data format with or without overflow high and low.

| Analog Input Voltage | OVL | OVH | Digital Output Code | | | | | | | | | | | | | | | | | | | | Decimal Code | Hexa |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | B23 | B22 | B21 | B20 | B19 | B18 | B17 | B16 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | *B[23:0]* |
| Vref +1 LSB | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2097153 | 600001 |
| Vref | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2097152 | 600000 |
| Vref - 1 LSB | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2097151 | 1FFFFF |
| 2 LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | 000002 |
| 1 LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 000001 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000000 |
| -1 LSB | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -1 | 3FFFFF |
| -2 LSB | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -2 | 3FFFFE |
| -Vref | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -2097152 | 200000 |
| -Vref -1LSB | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -2097153 | 9FFFFF |
| -Vref -2LSB | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -2097154 | 9FFFFE |

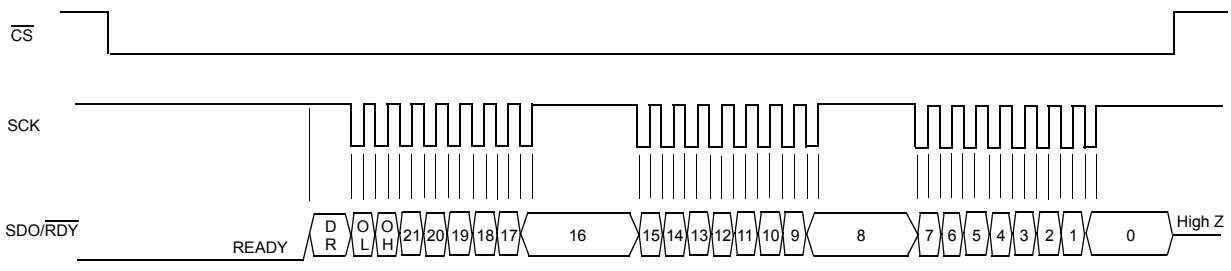



***FIGURE 5-1:*** *Typical Serial Device Communication and Example Digital Output Codes for Specific Analog Input Voltages.*

## 5.2 Controlling Internal Conversions and the Internal Oscillator

During Shutdown mode, on the falling edge of $\overline{CS}$, the conversion process begins. During this process, the internal oscillator clocks the delta-sigma modulator and the SINC filter until a conversion is complete. This conversion time is $t_{CONV}$ and the timing is shown in Figure 5-2. At the end of $t_{CONV}$, the digital filter has settled completely and there is no latency involved with the digital SINC filter of the MCP3550/1/3.

The two modes of conversion for the MCP3550/1/3 devices are Single Conversion and Continuous Conversion. In Single Conversion mode, a consecutive conversion will not automatically begin. Instead, after a single conversion is complete and the SINC filter have settled, the device puts the data into the output register and enters shutdown.

In Continuous Conversion mode, a consecutive conversion will be automatic. In this mode, the device is continuously converting, independent of the serial interface. The most recent conversion data will always be available in the Output register.

When the device exits Shutdown, there is an internal power-up delay that must be observed.

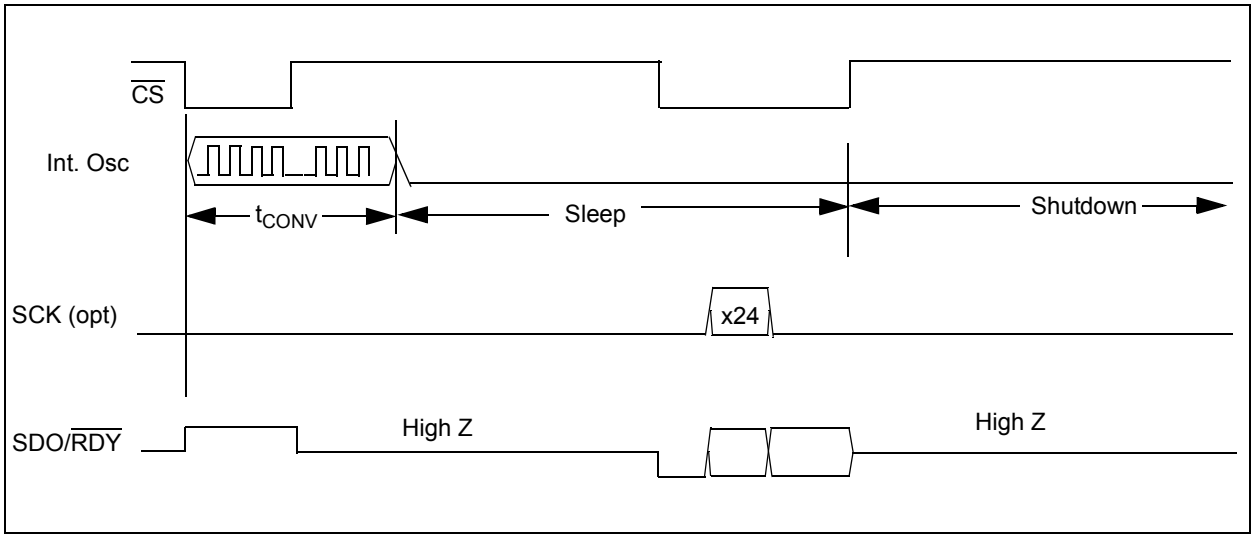



***FIGURE 5-2:*** *Single Conversion Mode.*

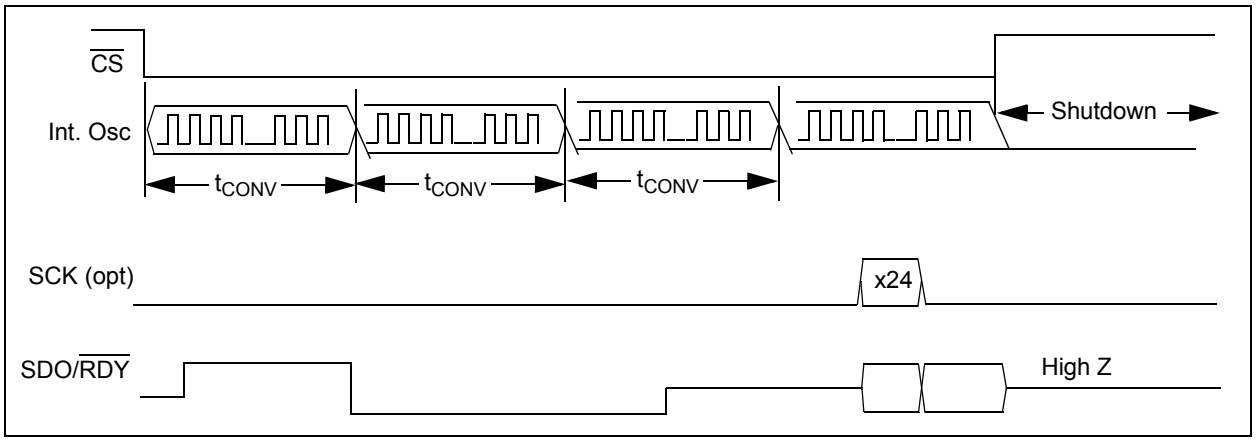



***FIGURE 5-3:*** *Continuous Conversion Mode.*

## 5.3 Single Conversion Mode

If a rising edge of Chip Select ($\overline{CS}$) occurs during $t_{CONV}$, a subsequent conversion will **not** take place and the device will enter low-power Shutdown mode after $t_{CONV}$ completes. This is referred to as Single Conversion mode. This operation is demonstrated in Figure 5-2. Note that a falling edge of $\overline{CS}$ during the same conversion that detected a rising edge, as in Figure 5-2, will not initiate a new conversion. The data must be read during sleep mode, with CSN low, and will be lost as soon as the part enters in shutdown mode (with a rising edge of CSN). After the final data bit has been clocked out on the 25th clock, the SDO/$\overline{RDY}$ pin will go active-high.

### 5.3.1 READY FUNCTION OF SDO/$\overline{RDY}$ PIN, SINGLE CONVERSION MODE

At every falling edge of $\overline{CS}$ during the internal conversion, the state of the internal conversion is latched on the SDO/$\overline{RDY}$ pin to give ready or busy information. A High state means the device is currently performing an internal conversion and data cannot be clocked out. A Low state means the device has finished its conversion and the data is ready for retrieval on the falling edge of SCK. This operation is demonstrated in Figure 5-4. Note that the device has been put into Single Conversion mode with the first rising edge of $\overline{CS}$.

| **Note:** | The Ready state is latched on each falling edge of $\overline{CS}$ and will not dynamically update if $\overline{CS}$ is held low. $\overline{CS}$ must be toggled high through low. |
|---|---|

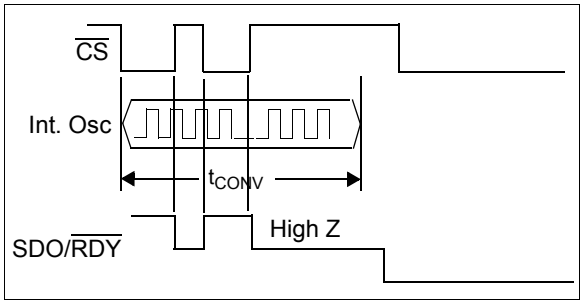



***FIGURE 5-4:*** *$\overline{RDY}$ Functionality in Single Conversion Mode.*

## 5.4 Continuous Conversion Mode

If no rising edge of $\overline{CS}$ occurs during any given conversion per Figure 5-3, a subsequent conversion will take place and the contents of the previous conversion will be overwritten. This operation is demonstrated in Figure 5-5. Once conversion output data has started to be clocked out, the output buffer is not refreshed until all 24 bits have been clocked. A complete read must occur in order to read the next conversion in this mode. The subsequent conversion data to be read will then be the most recent conversion. The conversion time is fixed and cannot be shortened by the rising edge of $\overline{CS}$. This rising edge will place the part in Shutdown mode and all conversion data will be lost.

The transfer of data from the SINC filter to the output buffer is demonstrated in Figure 5-5. If the previous conversion data is not clocked out of the device, it will be lost and replaced by the new conversion. When the device is in Continuous Conversion mode, the most recent conversion data is always present at the output register for data retrieval.

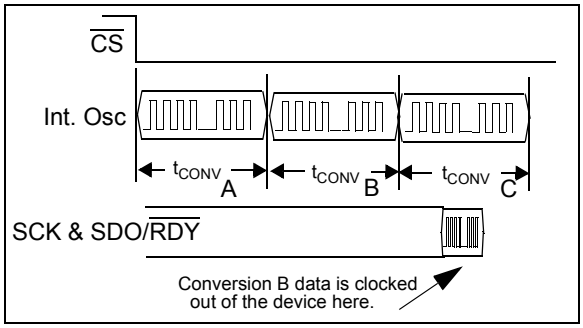



***FIGURE 5-5:*** *Most Current Continuous Conversion Mode Data.*

If a conversion is in process, it cannot be terminated with the rising edge of $\overline{CS}$. SDO/$\overline{RDY}$ must first transition to a Low state, which will indicate the end of conversion.

### 5.4.1 READY FUNCTION OF SDO/$\overline{\text{RDY}}$ PIN IN CONTINUOUS CONVERSION MODE

The device enters Continuous Conversion mode if no rising edge of $\overline{\text{CS}}$ is seen during $t_{CONV}$ and consecutive conversions ensue. SDO/$\overline{\text{RDY}}$ will be high, indicating that a conversion is in process. When a conversion is complete, SDO/$\overline{\text{RDY}}$ will change to a Low state. With the Low state of SDO/$\overline{\text{RDY}}$ after this first conversion, the conversion data can be accessed with the combination of SCK and SDO/$\overline{\text{RDY}}$. If the data ready event happens during the clocking out of the data, the data ready bit will be displayed after the complete 24-bit word communication (i.e., the data ready event will not interrupt a data transfer).

If 24 bits of data are required from this conversion, they must be accessed during this communication. You can terminate data transition by bringing $\overline{\text{CS}}$ high, but the remaining data will be lost and the converter will go into Shutdown mode. Once the data has been transmitted by the converter, the SDO/$\overline{\text{RDY}}$ pin will remain in the LSB state until the 25th falling edge of SCK. At this point, SDO/$\overline{\text{RDY}}$ is released from the Data Acquisition mode and changed to the $\overline{\text{RDY}}$ state.

| | |
|---|---|
| **Note:** | The $\overline{\text{RDY}}$ state is not latched to $\overline{\text{CS}}$ in this mode; the RDY flag dynamically updates on the SDO/$\overline{\text{RDY}}$ pin and remains in this state until data is clocked out using the SCK pin. |

### 5.4.2 2-WIRE CONTINUOUS CONVERSION OPERATION, ($\overline{\text{CS}}$ TIED PERMANENTLY LOW)

It is possible to use only two wires to communicate with the MCP3550/1/3 devices. In this state, the device is always in Continuous Conversion mode, with internal conversions continuously occurring. This mode can be entered by having $\overline{\text{CS}}$ low during power-up or changing it to a low position after power-up. If $\overline{\text{CS}}$ is low at power-up, the first conversion of the converter is initiated approximately 300 µs after the power supply has stabilized.

## 5.5 Using The MCP3550/1/3 with Microcontroller (MCU) SPI Ports

It is required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Figure 5-6 depicts the operation shown in SPI mode 1,1, which requires that the SCK from the MCU idles in the High state, while Figure 5-7 shows the similar case of SPI Mode 0,0, where the clock idles in the Low state. The waveforms in the figures are examples of an MCU operating the SPI port in 8-bit mode, and the MCP3550/1/3 devices do not require data in 8-bit groups.

In SPI mode 1,1, data is read using only 24 clocks or three byte transfers. The data ready bit must be read by testing the SDO/$\overline{RDY}$ line prior to a falling edge of the clock.

In SPI mode 0,0, data is read using 25 clocks or four byte transfers. Please note that the data ready bit is included in the transfer as the first bit in this mode.

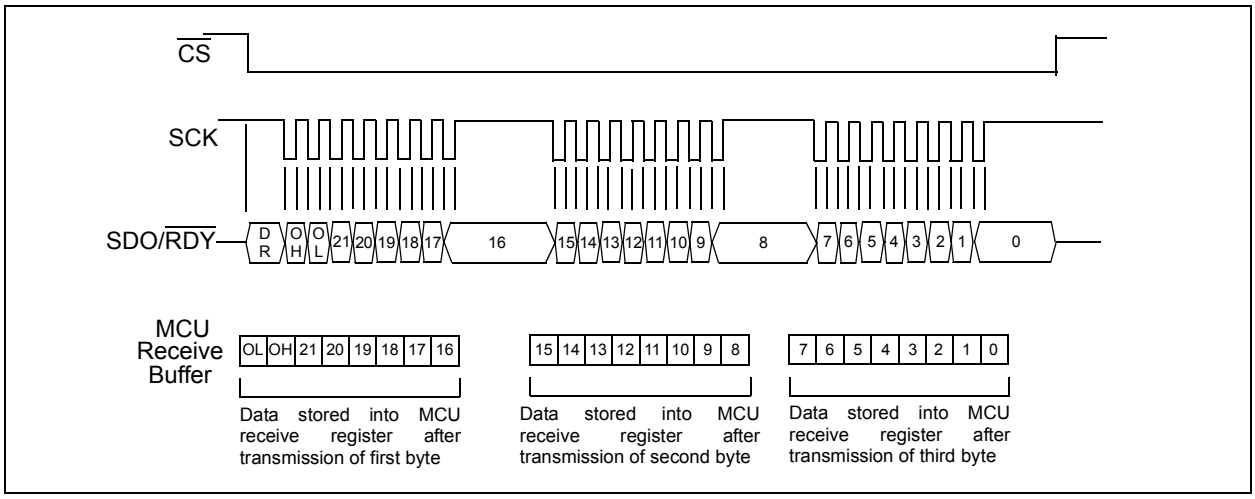



***FIGURE 5-6:*** *SPI Communication – Mode 1,1.*

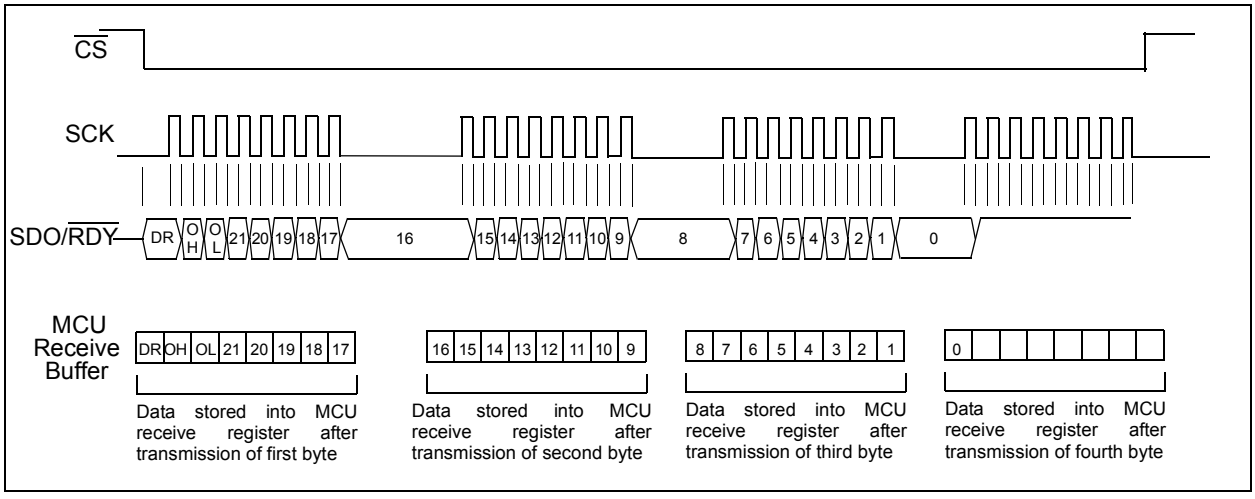



***FIGURE 5-7:*** *SPI Communication – Mode 0,0.*