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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MCP37231/21-200
MCP37D31/21-200

200 Msps, 16-/14-Bit Low-Power ADC with 8-Channel MUX

Features

- Sample Rates:
  - 200 Msps for single-channel mode
  - 200 Msps/number of channels used
- SNR with f_{IN} = 15 MHz and -1 dBFS:
  - 74.7 dBFS (typical) at 200 Msps
- SFDR with f_{IN} = 15 MHz and -1 dBFS:
  - 90 dBc (typical) at 200 Msps
- Power Dissipation with LVDS Digital I/O:
  - 490 mW at 200 Msps
- Power Dissipation with CMOS Digital I/O:
  - 436 mW at 200 Msps, Output Clock = 100 MHz
- Power Dissipation Excluding Digital I/O:
  - 390 mW at 200 Msps
- Power-Saving Modes:
  - 144 mW during Standby
  - 28 mW during Shutdown
- Supply Voltage:
  - Digital Section: 1.2V, 1.8V
  - Analog Section: 1.2V, 1.8V
- Selectable Full-Scale Input Range: up to 2.975 V_{P-P}
- Input Channel Bandwidth: 500 MHz
- Channel-to-Channel Crosstalk in Multi-Channel Mode (Input = 15 MHz, -1 dBFS): >95 dB
- Output Data Format:
  - Parallel CMOS, DDR LVDS
  - Serialized DDR LVDS (16-bit, octal-channel mode)
- Optional Output Data Randomizer
- Serial Peripheral Interface (SPI)
- Digital Signal Post-Processing (DSPP) Options:
  - Decimation filters for improved SNR
  - Fractional Delay Recovery (FDR) for time-delay corrections in multi-channel operations (dual-/octal-channel modes)
  - Phase, Offset and Gain adjust of individual channels
  - Digital Down-Conversion (DDC) with I/Q or $f_S/8$ output (MCP37D31/21-200)
  - Continuous wave beamforming for octal-channel mode (MCP37D31/21-200)
- Built-In ADC Linearity Calibration Algorithms:
  - Harmonic Distortion Correction (HDC)
  - DAC Noise Cancellation (DNC)
  - Dynamic Element Matching (DEM)
  - Flash Error Calibration
- AutoSync Mode to Synchronize Multiple Devices to the Same Clock
- Package Options:
  - VTLA-124 (9 mm x 9 mm x 0.9 mm)
  - TFBGA-121 (8 mm x 8 mm x 1.08 mm)
- No External Reference Decoupling Capacitor Required for TFBGA Package
- Industrial Temperature Range: -40°C to +85°C

Typical Applications

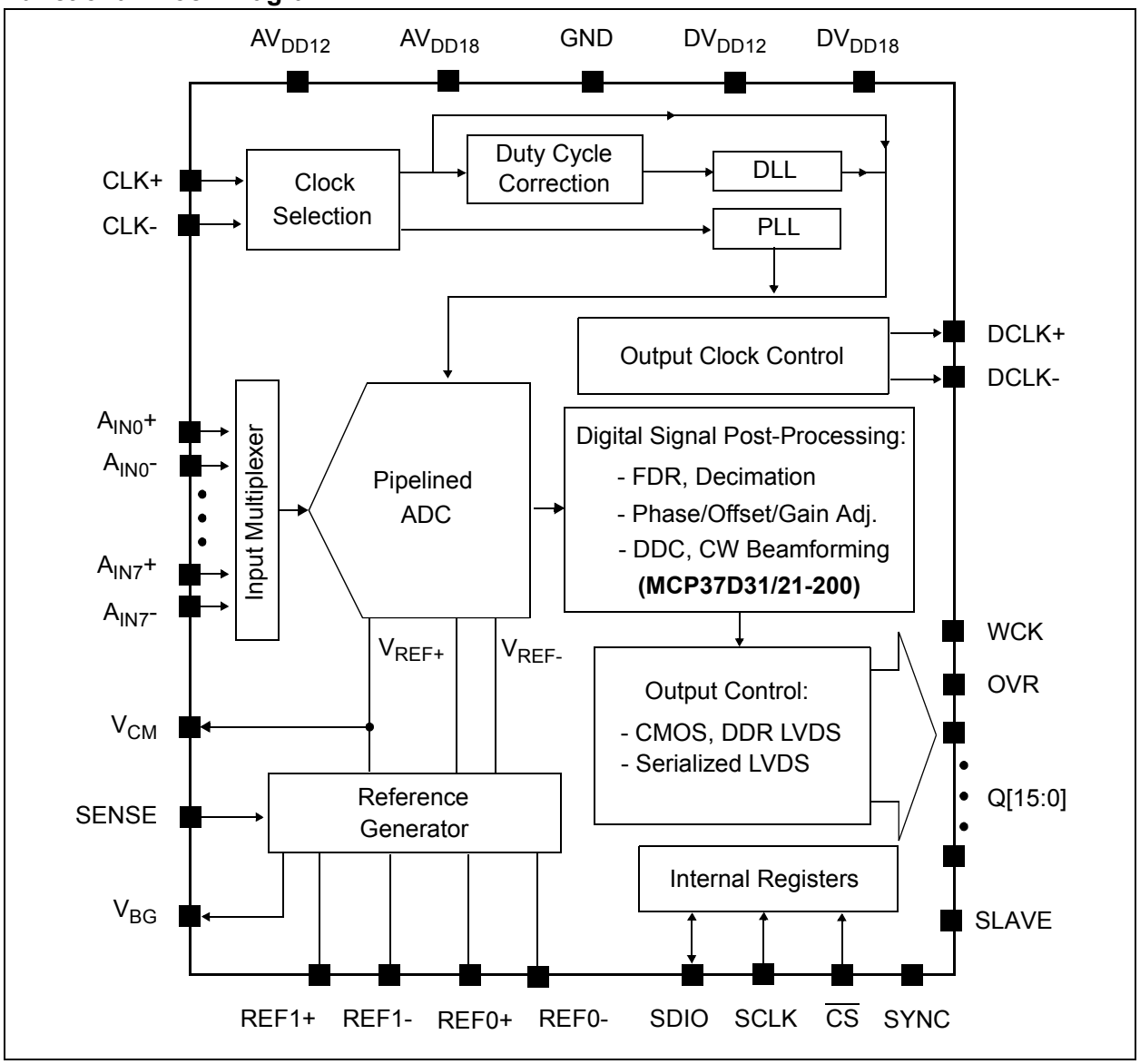
- Communication Instruments
- Cellular Base Stations
- Radar
- Ultrasound and Sonar Imaging
- Scanners and Low-Power Portable Instruments
- Industrial and Consumer Data Acquisition System

MCP372XX/MCP37DXX Family Comparison[1]:

Part Number	Sample Rate	Resolution	Digital Decimation[2]	Digital Down-Conversion[3]	CW Beamforming[4]	Noise-Shaping Requantizer[2]
MCP37231-200	200 Msps	16	Yes	No	No	No
MCP37221-200	200 Msps	14	Yes	No	No	No
MCP37211-200	200 Msps	12	Yes	No	No	Yes
MCP37D31-200	200 Msps	16	Yes	Yes	Yes	No
MCP37D21-200	200 Msps	14	Yes	Yes	Yes	No
MCP37D11-200	200 Msps	12	Yes	Yes	Yes	Yes

Note 1: Devices in the same package type are pin-to-pin compatible.
2: Available in single- and dual-channel mode.
3: Available in single- and dual-channel mode, and octal-channel mode when CW beamforming is enabled.
4: Available in octal-channel mode.

Functional Block Diagram



Description

The MCP37231/21-200 is Microchip's baseline 16-/14-bit 200 Msps pipelined ADC family, featuring built-in high-order digital decimation filters, gain and offset adjustment per channel and fractional delay recovery.

The MCP37D31/21-200 device family features digital down-conversion and CW beamforming capability, in addition to the features offered by the MCP37231/21-200.

All devices feature harmonic distortion correction and DAC noise cancellation that enable high-performance specifications with SNR of 74.7 dBFS (typical), and SFDR of 90 dBc (typical).

These A/D converters exhibit industry-leading low-power performance with only 490 mW operation while using the LVDS interface at 200 Msps. This superior low-power operation coupled with high dynamic performance makes these devices ideal for various high-performance, high-speed data acquisition systems, including communications equipment, radar and portable instrumentation.

The output decimation filter option improves SNR performance up to 93.5 dBFS with the 512x decimation setting. The digital down-conversion option, in conjunction with the decimation and quadrature output options, offers great flexibility in digital communication system design, including cellular base-stations and narrow-band communications. Gain, phase and DC offset can be adjusted independently for each input channel, allowing for simplified implementation of CW beamforming and ultrasound Doppler imaging applications.

These devices can have up to eight differential input channels through an input MUX. The sampling rate is up to 200 Msps when a single channel is used, or 25 Msps per channel when all eight input channels are used.

In dual or octal-channel mode, the Fractional Delay Recovery (FDR) feature digitally corrects the difference in sampling instance between different channels, so that all inputs appear to have been sampled at the same time.

The device samples the analog input on the rising edge of the clock. The digital output code is available after 28 clock cycles of data latency. Latency will increase if any of the digital signal post-processing (DSPP) options are enabled.

AutoSync mode offers a great design flexibility when multiple devices are used in applications. It allows multiple devices to sample input synchronously at the same clock.

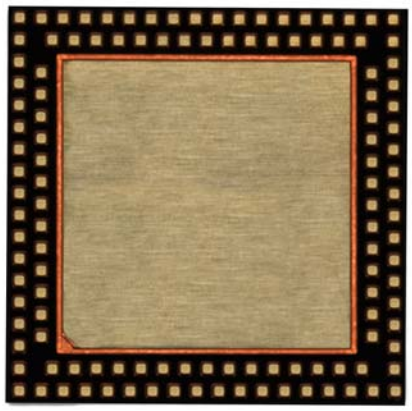
The differential full-scale analog input range is programmable up to 2.975 V_{P-P}. The ADC output data can be coded in two's complement or offset binary representation, with or without the data randomizer option. The output data is available as full-rate CMOS or Double-Data-Rate (DDR) LVDS. Additionally, a serialized LVDS option is also available for the 16-bit octal-channel mode.

These devices also include various features designed to maximize flexibility in the user's applications and minimize system cost, such as a programmable PLL clock, output data rate control and phase alignment and programmable digital pattern generation. The device's operational modes and feature sets are configured by setting up the user-programmable registers.

The device is available in Pb-free VTLA-124 and TFBGA-121 packages. The device operates over the commercial temperature range of -40°C to +85°C.

Package Types

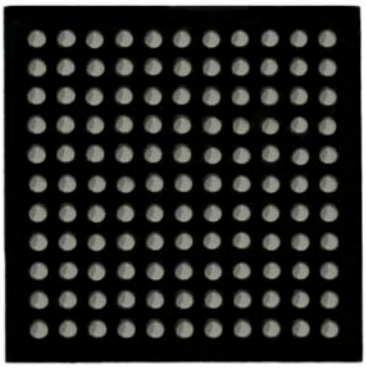
Bottom View



Dimension: 9 mm x 9 mm x 0.9 mm

(a) VTLA-124 Package.

Bottom View

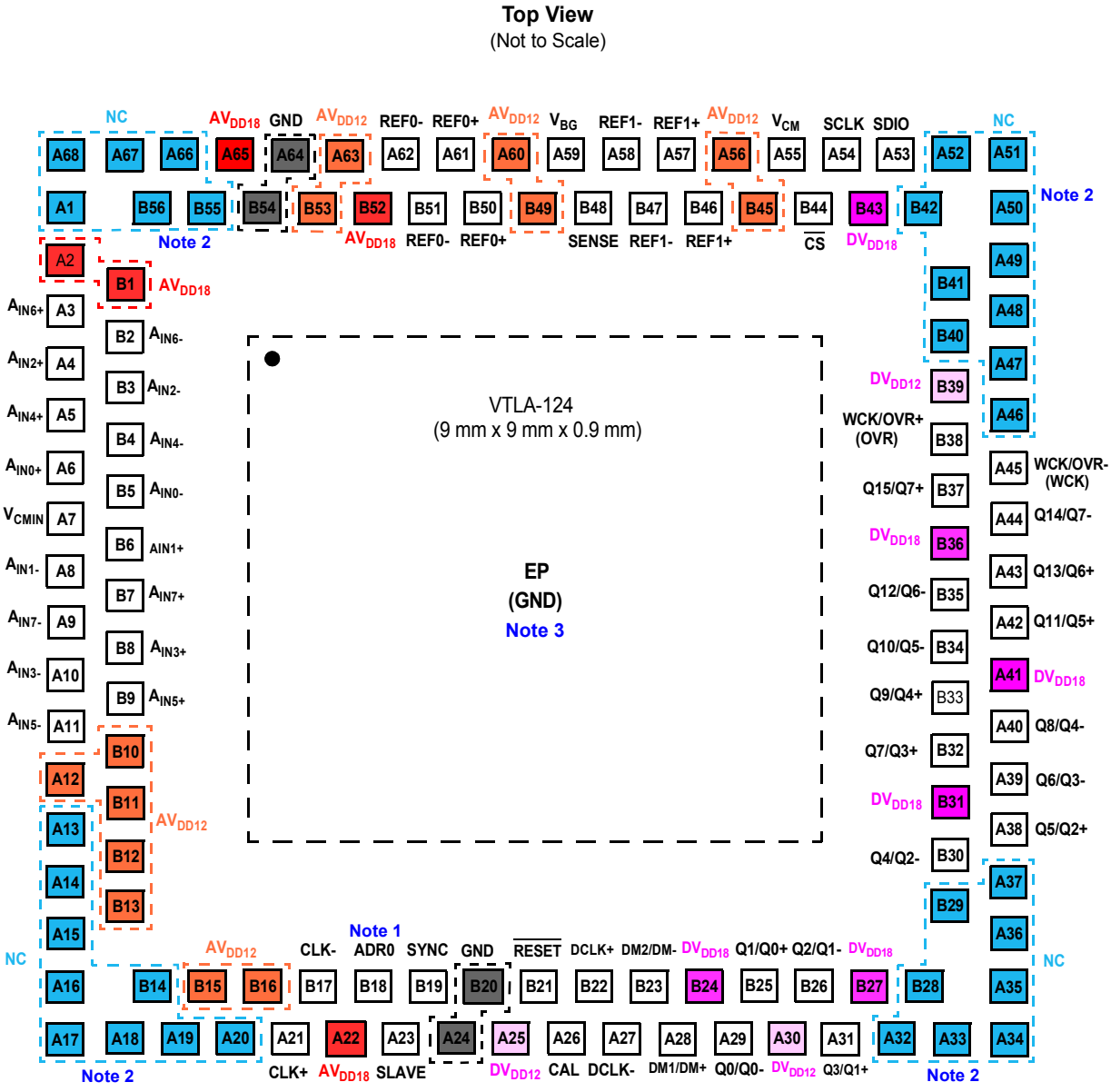


Dimension: 8 mm x 8 mm x 1.08 mm
Ball Pitch: 0.65 mm
Ball Diameter: 0.4 mm

(b) TFBGA-121 Package.

NOTES:

1.0 PACKAGE PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Note 1: Tie to GND or DV_{DD18}. ADR1 is internally bonded to GND.

2: NC – Not connected pins. These pins can float or be tied to ground.

3: Exposed pad (EP – back pad of the package) is the common ground (GND) for analog and digital supplies. Connect this pad to a clean ground reference on the PCB.

FIGURE 1-1: *VTLA-124 Package. See Table 1-1 for the pin descriptions and Table 1-3 for active and inactive ADC output pins for various ADC resolution modes.*

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124

Pin No.	Name	I/O Type	Description
Power Supply Pins			
A2, A22, A65, B1, B52	AV_{DD18}	Supply	Supply voltage input (1.8V) for analog section
A12, A56, A60, A63, B10, B11, B12, B13, B15, B16, B45, B49, B53	AV_{DD12}		Supply voltage input (1.2V) for analog section
A25, A30, B39	DV_{DD12}		Supply voltage input (1.2V) for digital section
A41, B24, B27, B31, B36, B43	DV_{DD18}		Supply voltage input (1.8V) for digital section and all digital I/O
EP	GND		Exposed pad: Common ground pin for digital and analog sections
ADC Analog Input Pins			
A3	A_{IN6+}	Analog Input	Channel 6 differential analog input (+)
B2	A_{IN6-}		Channel 6 differential analog input (-)
A4	A_{IN2+}		Channel 2 differential analog input (+)
B3	A_{IN2-}		Channel 2 differential analog input (-)
A5	A_{IN4+}		Channel 4 differential analog input (+)
B4	A_{IN4-}		Channel 4 differential analog input (-)
A6	A_{IN0+}		Channel 0 differential analog input (+)
B5	A_{IN0-}		Channel 0 differential analog input (-)
B6	A_{IN1+}		Channel 1 differential analog input (+)
A8	A_{IN1-}		Channel 1 differential analog input (-)
B7	A_{IN7+}		Channel 7 differential analog input (+)
A9	A_{IN7-}		Channel 7 differential analog input (-)
B8	A_{IN3+}		Channel 3 differential analog input (+)
A10	A_{IN3-}		Channel 3 differential analog input (-)
B9	A_{IN5+}		Channel 5 differential analog input (+)
A11	A_{IN5-}		Channel 5 differential analog input (-)
A21	CLK+		Differential clock input (+)
B17	CLK-		Differential clock input (-)
Reference Pins(1)			
A57, B46	REF1+	Analog Output	Differential reference 1 (+) voltage
A58, B47	REF1-		Differential reference 1 (-) voltage
A61, B50	REF0+		Differential reference 0 (+) voltage
A62, B51	REF0-		Differential reference 0 (-) voltage
SENSE, Bandgap and Common-Mode Voltage Pins			
B48	SENSE	Analog Input	Analog input full-scale range selection. See Table 4-2 for SENSE voltage settings.
A59	V_{BG}	Analog Output	Internal bandgap output voltage Connect a decoupling capacitor (2.2 µF)
A7	V_{CMIN}	Analog Input	Common-mode voltage input for auto-calibration Connect V_{CM} voltage(2)
A55	V_{CM}		Common-mode output voltage (900 mV) for analog input signal Connect a decoupling capacitor (0.1 µF)(3)

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
Digital I/O Pins			
B18	ADR0	Digital Input	SPI address selection pin (A0 bit). Tie to GND or DV_{DD18}.(4)
A23	SLAVE		Slave or Master selection pin in AutoSync (12). If not used, tie to GND.
B19	SYNC	Digital Input/ Output	Digital synchronization pin for AutoSync (12) If not used, leave it floating.
B21	$\overline{\text{RESET}}$	Digital Input	Reset control input: **High:** Normal operating mode **Low:** Reset mode(5)
A26	CAL	Digital Output	Calibration status flag digital output: **High:** Calibration is complete **Low:** Calibration is not complete(6)
B22	DCLK+		**LVDS**: Differential digital clock output (+) **CMOS:** Digital clock output(7)
A27	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Unused (leave floating)

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
ADC Output Pins[8]			
B23	DM2/DM-	Digital Output	**18-bit mode:** Digital data output (last two LSb bits)[9] **Other modes:** Not used
A28	DM1/DM+		
A29	Q0/Q0-		Digital data output: CMOS = Q0 DDR LVDS = Q0- (Even bit first), Q8- (MSb byte first) Serialized LVDS = Q- for the last selected channel (n) = 8
B25	Q1/Q0+		Digital data output: CMOS = Q1 DDR LVDS = Q0+ (Even bit first), Q8+ (MSb byte first) Serialized LVDS = Q+ for the last selected channel (n) = 8
B26	Q2/Q1-		Digital data output: CMOS = Q2 DDR LVDS = Q1- (Even bit first), Q9- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 7
A31	Q3/Q1+		Digital data output: CMOS = Q3 DDR LVDS = Q1+ (Even bit first), Q9+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 7
B30	Q4/Q2-		Digital data output: CMOS = Q4 DDR LVDS = Q2- (Even bit first), Q10- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 6
A38	Q5/Q2+		Digital data output: CMOS = Q5 DDR LVDS = Q2+ (Even bit first), Q10+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 6
A39	Q6/Q3-		Digital data output: CMOS = Q6 DDR LVDS = Q3- (Even bit first), Q11- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 5
B32	Q7/Q3+		Digital data output: CMOS = Q7 DDR LVDS = Q3+ (Even bit first), Q11+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 5
A40	Q8/Q4-		Digital data output: CMOS = Q8 DDR LVDS = Q4- (Even bit first), Q12- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 4
B33	Q9/Q4+		Digital data output: CMOS = Q9 DDR LVDS = Q4+ (Even bit first), Q12+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 4
B34	Q10/Q5-		Digital data output: CMOS = Q10 DDR LVDS = Q5- (Even bit first), Q13- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 3

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
A42	Q11/Q5+	Digital Output	Digital data output: CMOS = Q11 DDR LVDS = Q5+ (Even bit first), Q13+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 3
B35	Q12/Q6-		Digital data output: CMOS = Q12 DDR LVDS = Q6- (Even bit first), Q14- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 2
A43	Q13/Q6+		Digital data output: CMOS = Q13 DDR LVDS = Q6+ (Even bit first), Q14+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 2
A44	Q14/Q7-		Digital data output: CMOS = Q14 DDR LVDS = Q7- (Even bit first), Q15- (MSb byte first) Serialized LVDS = Q- for the first selected channel (n) = 1
B37	Q15/Q7+		Digital data output: CMOS = Q15 DDR LVDS = Q7+ (Even bit first), Q15+ (MSb byte first) Serialized LVDS = Q+ for the first selected channel (n) = 1
B38	WCK/OVR+ (OVR)		**WCK:** Word clock sync digital output **OVR:** Input overrange indication digital output[(11)]
A45	WCK/OVR- (WCK)		
SPI Interface Pins			
A53	SDIO	Digital Input/ Output	SPI data input/output
A54	SCLK	Digital Input	SPI serial clock input
B44	$\overline{CS}$		SPI Chip Select input
Not Connected Pins			
A1, A13 - A20, A32 - A37, A46 - A52, A66 - A68, B14, B28, B29, B40, B41, B42, B55, B56	NC		These pins can be tied to ground or left floating.
Pins that need to be grounded			
A24, A64, B20, B54	GND		These pins are not supply pins, but need to be tied to ground.

Notes:

1. These pins are for the internal reference voltage outputs. They should not be driven. External decoupling circuits are required. See **Section 4.5.3, "Decoupling Circuits for Internal Voltage Reference and Bandgap Output"** for details.
2. V_{CMIN} is used for Auto-Calibration only. V_{CMIN}+ and V_{CMIN}- should be tied together always. There should be no voltage difference between the two pins. Typically both V_{CMIN}+ and V_{CMIN}- are tied to the V_{CM} output pin together, but they can be tied to another common-mode voltage if external V_{CM} is used. This pin has High Z input in Shutdown, Standby and Reset modes.
3. When the V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), the V_{CM} pin should be decoupled with a 0.1 µF capacitor, and should be directly tied to the V_{CMIN}+ and V_{CMIN}- pins.
4. ADR1 (for A1 bit) is internally bonded to GND ('0'). If ADR0 is dynamically controlled, ADR0 must be held constant while $\overline{CS}$ is "Low".
5. The device is in Reset mode while this pin stays "Low". On the rising edge of $\overline{RESET}$, the device exits Reset mode, initializes all internal user registers to default values, and begins power-up calibration.
6. CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or a soft reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes, this pin will maintain the prior condition.
7. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital signal post-processing, PLL and/or DLL. See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
8. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The output pins shown here are for the "Even bit first", which is the default setting of OUTPUT_MODE<1:0> in Address 0x62 (Register 5-20). The even data bits (Q0, Q2, Q4, Q6, Q8, Q10, Q12, Q14) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11, Q13, Q15) appear when DCLK+ is "Low". See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control. See Figures 2-2 to 2-6 for LVDS output timing diagrams.
9. Available for the MCP37231-200 and MCP37D31-200 devices only.
   Leave these pins floating (No Connect) if not used.
10. **18-bit mode:** DM1/DM+ and DM2/DM- are the last LSb bits. DM2/DM- is the LSb. In LVDS output, DM1/DM+ and DM2/DM- are the LSb pair. DM1/DM+ appears at the falling edge and DM2/DM- is at the rising edge of the DCLK+.
    Other than 18-bit mode: DM1/DM+ and DM2/DM- are High Z in LVDS mode.
11. **CMOS output mode:** WCK/OVR- is WCK and WCK/OVR+ is OVR.
    DDR LVDS output mode: The rising edge of DCLK+ is WCK and the falling edge is OVR.
    OVR: OVR will be held "High" when analog input overrange is detected. Digital signal post-processing will cause OVR to assert early relative to the output data. See Figure 2-2 for LVDS timing of these bits.
    WCK: WCK is normally "Low". WCK is "High" while data from the first channel is sent out. In single-channel mode, WCK stays "High" except when in I/Q output mode. In serialized LVDS (octal) output mode, the WCK output is asserted "High" on the MSb bit. See **Section 4.12.5 "Word Clock (WCK)"** for further WCK description.
12. (a) SLAVE = "High": The device is selected as slave and the SYNC pin becomes input pin.
    (b) SLAVE = "Low": The device is selected as master and the SYNC pin becomes output pin. In SLAVE/SYNC operation, master and slave devices are synchronized to the same clock.

Top View
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11
A	SDIO	V_{CM}	REF1+	REF1-	V_{BG}	REF0+	REF0-	GND	GND	A_{IN4-}	A_{IN2+}
B	SCLK	$\overline{CS}$	GND	GND	SENSE	AV_{DD12}	AV_{DD12}	AV_{DD18}	AV_{DD18}	A_{IN4+}	A_{IN2-}
C	WCK/ OVR- (WCK)	WCK/ OVR+ (OVR)	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN6-}	A_{IN0+}
D	Q14/Q7-	Q15/Q7+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN6+}	A_{IN0-}
E	Q12/Q6-	Q13/Q6+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN5+}	A_{IN1+}
F	Q10/Q5-	Q11/Q5+	DV_{DD18}	DV_{DD18}	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN5-}	A_{IN1-}
G	Q8/Q4-	Q9/Q4+	DV_{DD18}	DV_{DD18}	GND	GND	AV_{DD12}	AV_{DD12}	GND	A_{IN7-}	A_{IN3+}
H	Q6/Q3-	Q7/Q3+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	A_{IN7+}	A_{IN3-}
J	Q4/Q2-	Q5/Q2+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	V_{CMIN}^+	V_{CMIN}^-
K	Q2/Q1-	Q3/Q1+	DM1/DM+	DCLK-	CAL	GND	SLAVE	ADR0	ADR1	GND	GND
L	Q0/Q0-	Q1/Q0+	DM2/DM-	DCLK+	$\overline{RESET}$	SYNC	GND	CLK+	CLK-	GND	AV_{DD18}

Analog
Digital
All others: Supply Voltage

Notes:

- Die dimension: 8 mm x 8 mm x 1.08 mm.
- Ball dimension: (a) Ball Pitch = 0.65 mm, (b) Ball Diameter = 0.4 mm.
- Flip-chip solder ball composition: Sn with Ag 1.8%.
- Solder sphere composition: SAC-405 (Sn/Au 4%/Cu 0.5%).

FIGURE 1-2: *TFBGA-121 Package. See Table 1-2 for the pin descriptions and Table 1-3 for active and inactive ADC output pins for various ADC resolution modes.*

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121

Ball No.	Name	I/O Type	Description
A1	SDIO	Digital Input/ Output	SPI data input/output
A2	V_{CM}	Analog Output	Common-mode output voltage (900 mV) for analog input signal Connect a decoupling capacitor (0.1 µF)[1]
A3	REF1+		Differential reference voltage 1 (+/-). Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating.
A4	REF1-		
A5	V_{BG}		Internal bandgap output voltage A decoupling capacitor (2.2 µF) is embedded in the TFBGA package. Leave this pin floating.
A6	REF0+		Differential reference 0 (+/-) voltage. Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating.
A7	REF0-		
A8	GND	Supply	Common ground for analog and digital sections
A9			
A10	A_{IN4-}	Analog Input	Channel 4 differential analog input (-)
A11	A_{IN2+}		Channel 2 differential analog input (+)
B1	SCLK	Digital Input	SPI serial clock input
B2	$\overline{CS}$		SPI Chip Select input
B3	GND	Supply	Common ground for analog and digital sections
B4			
B5	SENSE	Analog Input	Analog input range selection. See Table 4-2 for SENSE voltage settings.
B6	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
B7			
B8	AV_{DD18}		Supply voltage input (1.8V) for analog section
B9			
B10	A_{IN4+}	Analog Input	Channel 4 differential analog input (+)
B11	A_{IN2-}		Channel 2 differential analog input (-)
C1	WCK/OVR- (WCK)	Digital Output	**WCK:** Word clock sync digital output **OVR:** Input overrange indication digital output[2]
C2	WCK/OVR+ (OVR)		
C3	GND	Supply	Common ground for analog and digital sections
C4			
C5	AV_{DD12}		Supply voltage input (1.2V) for analog section
C6			
C7			
C8	GND		Common ground pin for analog and digital sections
C9			
C10	A_{IN6-}	Analog Input	Channel 6 differential analog input (-)
C11	A_{IN0+}		Channel 0 differential analog input (+)
D1	Q14/Q7-	Digital Output	Digital data output[3] CMOS = Q14 DDR LVDS = Q7- (Even bit first), Q15- (MSb byte first) Serialized LVDS = Q- for the first selected channel (n = 1)
D2	Q15/Q7+		Digital data output[3] CMOS = Q15 DDR LVDS = Q7+ (Even bit first), Q15+ (MSb byte first) Serialized LVDS = Q+ for the first selected channel (n = 1)

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
D3	GND	Supply	Common ground for analog and digital sections
D4			
D5	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
D6			
D7			
D8	GND		Common ground for analog and digital sections
D9			
D10	A_{IN6+}	Analog Input	Channel 6 differential analog input (+)
D11	A_{IN0-}		Channel 0 differential analog input (-)
E1	Q12/Q6-	Digital Output	Digital data output(3) CMOS = Q12 DDR LVDS = Q6- (Even bit first), Q14- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 2
E2	Q13/Q6+		Digital data output(3) CMOS = Q13 DDR LVDS = Q6+ (Even bit first), Q14+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 2
E3	GND	Supply	Common ground for analog and digital sections
E4			
E5	AV_{DD12}		Supply voltage input (1.2V) for analog section
E6			
E7			
E8	GND		Common ground for analog and digital sections
E9			
E10	A_{IN5+}	Analog Input	Channel 5 differential analog input (+)
E11	A_{IN1+}		Channel 1 differential analog input (+)
F1	Q10/Q5-	Digital Output	Digital data output(3) CMOS = Q10 DDR LVDS = Q5- (Even bit first), Q13- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 3
F2	Q11/Q5+		Digital data output(3) CMOS = Q11 DDR LVDS = Q5+ (Even bit first), Q13+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 3
F3	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV_{DD18} potential.
F4			
F5	AV_{DD12}		Supply voltage input (1.2V) for analog section
F6			
F7			
F8	GND		Common ground for analog and digital sections
F9			
F10	A_{IN5-}	Analog Input	Channel 5 differential analog input (-)
F11	A_{IN1-}		Channel 1 differential analog input (-)

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
G1	Q8/Q4-	Digital Output	Digital data output[3] CMOS = Q8 DDR LVDS = Q4- (Even bit first), Q12- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 4
G2	Q9/Q4+		Digital data output[3] CMOS = Q9 DDR LVDS = Q4+ (Even bit first), Q12+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 4
G3	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section All digital input pins are driven by the same DV_{DD18} potential
G4			
G5	GND		Common ground for analog and digital sections
G6			
G7	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
G8			
G9	GND		Common ground for analog and digital sections
G10	A_{IN7-}	Analog Input	Channel 7 differential analog input (-)
G11	A_{IN3+}		Channel 3 differential analog input (+)
H1	Q6/Q3-	Digital Output	Digital data output[3] CMOS = Q6 DDR LVDS = Q3- (Even bit first), Q11- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 5
H2	Q7/Q3+		Digital data output[3] CMOS = Q7 DDR LVDS = Q3+ (Even bit first), Q11+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 5
H3	DV_{DD12}	Supply	Supply voltage input (1.2V) for digital section
H4			
H5	GND		Common ground for analog and digital sections
H6			
H7			
H8			
H9			
H10	A_{IN7+}	Analog Input	Channel 7 differential analog input (+)
H11	A_{IN3-}		Channel 3 differential analog input (-)
J1	Q4/Q2-	Digital Output	Digital data output[3] CMOS = Q4 DDR LVDS = Q2- (Even bit first), Q10- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 6
J2	Q5/Q2+		Digital data output[3] CMOS = Q5 DDR LVDS = Q2+ (Even bit first), Q10+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 6
J3	DV_{DD12}	Supply	DC supply voltage input pin for digital section (1.2V)
J4			
J5	GND		Common ground for analog and digital sections
J6			
J7			
J8			
J9			

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
J10	V_{CMIN+}	Analog Input	Common-mode voltage input for auto-calibration[4] These two pins should be tied together and connected to V_{CM} voltage.
J11	V_{CMIN-}		
K1	Q2/Q1-	Digital Output	Digital data output[3] CMOS = Q2 DDR LVDS = Q1- (Even bit first), Q9- (MSb byte first) Serialized LVDS = Q- for channel order (n) = 7
K2	Q3/Q1+		Digital data output[3] CMOS = Q3 DDR LVDS = Q1+ (Even bit first), Q9+ (MSb byte first) Serialized LVDS = Q+ for channel order (n) = 7
K3	DM1/DM+		**18-bit mode:** Digital data output. DM1 and DM2 are the last two LSb bits[5] **Other modes:** Not used
K4	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Not used (leave floating)
K5	CAL	Digital Output	Calibration status flag digital output[6] **High:** Calibration is complete **Low:** Calibration is not complete
K6	GND	Supply	Common ground pin for analog and digital sections
K7	SLAVE	Digital Input	Slave or Master selection pin in AutoSync [10]. If not used, tie to GND.
K8	ADR0		SPI address selection pin (A0 bit). Tie to GND or $DV_{DD}18$[7]
K9	ADR1		SPI address selection pin (A1 bit). Tie to GND or $DV_{DD}18$[7]
K10	GND	Supply	Common ground for analog and digital sections
K11			
L1	Q0/Q0-	Digital Output	Digital data output[3] CMOS = Q0 DDR LVDS = Q0- (Even bit first), Q8- (MSb byte first) Serialized LVDS = Q- for the last selected channel (n=8)
L2	Q1/Q0+		Digital data output[8] CMOS = Q1 DDR LVDS = Q0+ (Even bit first), Q8+ (MSb byte first) Serialized LVDS = Q+ for the last selected channel (n=8)
L3	DM2/DM-		**18-bit mode:** Digital data output. DM1 and DM2 are the last two LSb bits[5] **Other modes:** Not used
L4	DCLK+		**LVDS:** Differential digital clock output (+) **CMOS:** Digital clock output[8]
L5	$\overline{RESET}$	Digital Input	Reset control input: **High**: Normal operating mode **Low:** Reset mode[9]
L6	SYNC	Digital Input/ Output	Digital synchronization pin for AutoSync[10] If not used, leave it floating.
L7	GND	Supply	Common ground for analog and digital sections
L8	CLK+	Analog Input	Differential clock input (+)
L9	CLK-		Differential clock input (-)
L10	GND	Supply	Common ground for analog and digital sections
L11	AV_{DD18}	Analog Input	Supply voltage input (1.8V) for analog section

Notes:

1. When the V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), the V_{CM} pin should be decoupled with a 0.1 µF capacitor, and should be directly tied to the V_{CMIN}+ and V_{CMIN}- pins.
2. **CMOS output mode:** WCK/OVR- is WCK and WCK/OVR+ is OVR.
   DDR LVDS output mode: The rising edge of DCLK+ is WCK and the falling edge is OVR.
   OVR: OVR will be held "High" when analog input overrange is detected. Digital signal post-processing will cause OVR to assert early relative to the output data. See Figure 2-2 for LVDS timing of these bits.
   WCK: WCK is normally "Low". WCK is "High" while data from the first channel is sent out. In single-channel mode, WCK stays "High" except when in I/Q output mode. In serialized LVDS (octal) output mode, the WCK output is asserted "High" on the MSb bit. See **Section 4.12.5 "Word Clock (WCK)"** for further WCK description.
3. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The output pins shown here are for the "Even bit first", which is the default setting of OUTPUT_MODE<1:0> in Address 0x62 (Register 5-20). The even data bits (Q0, Q2, Q4, Q6, Q8, Q10, Q12, Q14) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11, Q13, Q15) appear when DCLK+ is "Low". See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control. See Figures 2-2 to 2-6 for LVDS output timing diagrams.
4. V_{CMIN} is used for Auto-Calibration only. V_{CMIN}+ and V_{CMIN}- should be tied together always. There should be no voltage difference between the two pins. Typically both V_{CMIN}+ and V_{CMIN}- are tied to the V_{CM} output pin together, but they can be tied to another common-mode voltage if external V_{CM} is used. This pin has High Z input in Shutdown, Standby and Reset modes.
5. Available for the MCP37231-200 and MCP37D31-200 devices only.
   Leave these pins floating (No Connect) if not used.
   18-bit mode: DM1/DM+ and DM2/DM- are the last LSb bits. DM2/DM- is the LSb. In LVDS output, DM1/DM+ and DM2/DM- are the LSb pair. DM1/DM+ appears at the falling edge and DM2/DM- is at the rising edge of the DCLK+.
   Other than 18-bit mode: DM1/DM+ and DM2/DM- are High Z in LVDS mode.
6. CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or a soft reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes, this pin will maintain the prior condition.
7. If the SPI address is dynamically controlled, the Address pin must be held constant while $\overline{CS}$ is "Low".
8. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital signal post-processing, PLL and/or DLL. See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
9. The device is in Reset mode while this pin stays "Low". On the rising edge of $\overline{RESET}$, the device exits Reset mode, initializes all internal user registers to default values, and begins power-up calibration.
10. (a) SLAVE = "High": The device is selected as slave and the SYNC pin becomes input pin.
    (b) SLAVE = "Low": The device is selected as master and the SYNC pin becomes output pin. In SLAVE/SYNC operation, master and slave devices are synchronized to the same clock.

TABLE 1-3: DATA OUTPUT PINS FOR EACH RESOLUTION OPTION

ADC Resolution	Output Pin Name																	
	Q15/ Q7+	Q14/ Q7-	Q13/ Q6+	Q12/ Q6-	Q11/ Q5+	Q10/ Q5-	Q9/ Q4+	Q8/ Q4-	Q7/ Q3+	Q6/ Q3-	Q5/ Q2+	Q4/ Q2-	Q3/ Q1+	Q2/ Q1-	Q1/ Q0+	Q0/ Q0-	DM1/ DM+	DM2 /DM-
18-bit mode	Q15 pin is MSb (bit 17), and DM2 is LSb (bit 0)																	
16-bit mode	Q15 pin is MSb, and Q0 is LSb																Not used(2)	
14-bit mode(1)	Q15 pin is MSb, and Q2 is LSb														Not used(2)			
12-bit mode	Q15 pin is MSb, and Q4 is LSb												Not used(2)					
10-bit mode	Q15 pin is MSb, and Q6 is LSb										Not used(2)							

Note 1: The MCP37221-200 and MCP37D21-200 devices have the 14-bit mode option only, while the MCP37231-200 and MCP37D31-200 have all listed resolution options.

2: Output condition at “not-used” output pin:

- ‘0’ in CMOS mode. Leave these pins floating.
- High Z state in LVDS mode

2.0 ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings†

Analog and digital supply voltage (AV_{DD12}, DV_{DD12}) ..... -0.3V to 1.32V
Analog and digital supply voltage (AV_{DD18}, DV_{DD18}) ..... -0.3V to 1.98V
All inputs and outputs with respect to GND ..... –0.3V to AV_{DD18} + 0.3V
Differential input voltage ..... $|AV_{DD18} - GND|$
Current at input pins ..... ±2 mA
Current at output and supply pins ..... ±250 mA
Storage temperature ..... -65°C to +150°C
Ambient temperature with power applied (T_A) ..... -55°C to +125°C
Maximum junction temperature (T_J) ..... +150°C
ESD protection on all pins ..... 2 kV HBM
Solder reflow profile ..... See Microchip Application Note AN233 (DS00233)

Notice†: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 Electrical Specifications

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Requirements						
Analog Supply Voltage	AV_{DD18}	1.71	1.8	1.89	V	
	AV_{DD12}	1.14	1.2	1.26	V	
Digital Supply Voltage	DV_{DD18}	1.71	1.8	1.89	V	Note 1
	DV_{DD12}	1.14	1.2	1.26	V	
Analog Supply Current						
Analog Supply Current During Conversion	I_{DD_A18}	—	27	46	mA	at AV_{DD18} pin
	I_{DD_A12}	—	185	252	mA	at AV_{DD12} pin
Digital Supply Current						
Digital Supply Current During Conversion	I_{DD_D12}	—	97	226	mA	at DV_{DD12} pin
Digital I/O Current in CMOS Output Mode	I_{DD_D18}	—	27	—	mA	at DV_{DD18} pin DCLK = 100 MHz
Digital I/O Current in LVDS Mode	I_{DD_D18}	Measured at DV_{DD18} Pin				
		—	55	81	mA	3.5 mA mode
			39	—	mA	1.8 mA mode
			69			5.4 mA mode
Supply Current during Power-Saving Modes						
During Standby Mode	$I_{STANDBY\_AN}$	—	84	—	mA	Address 0x00<4:3> = 1,1 (2)
	$I_{STANDBY\_DIG}$	—	36	—		
During Shutdown Mode	I_{DD_SHDN}	—	23	—	mA	Address 0x00<7,0> = 1,1 (3)

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PLL Circuit						
PLL Circuit Current	I_{DD_PLL}	—	17	—	mA	PLL enabled. Included in analog supply current specification.
Total Power Dissipation(4)						
Power Dissipation During Conversion, Excluding Digital I/O	P_{DISS_ADC}	—	387	—	mW	
Total Power Dissipation During Conversion with CMOS Output Mode	P_{DISS_CMOS}	—	436	—	mW	f_S = 200 Msps, DCLK = 100 MHz
Total Power Dissipation During Conversion with LVDS Output Mode	P_{DISS_LVDS}	—	486	—	mW	3.5 mA mode
			457	—		1.8 mA mode
			511			5.4 mA mode
During Standby Mode	$P_{DISS\_STANDBY}$	—	144	—	mW	Address 0x00<4:3> = 1,1(2)
During Shutdown Mode	P_{DISS_SHDN}	—	27.6	—	mW	Address 0x00<7,0> = 1,1(3)
Power-on Reset (POR) Voltage						
Threshold Voltage	VPOR	—	800	—	mV	Applicable to AV_{DD12} only
Hysteresis	VPOR_HYST	—	40	—	mV	(POR tracks AV_{DD12})
SENSE Input(5,7)						
SENSE Input Voltage	V_{SENSE}	GND	—	AV_{DD12}	V	V_{SENSE} selects reference
SENSE Pin Input Resistance	R_{IN_SENSE}	—	500	—	Ω	To virtual ground at 0.55V. 400 mV < V_{SENSE} < 800 mV
Current Sink into SENSE Pin	I_{SENSE}	—	4.5	—	µA	SENSE = 1.2V
			636			SENSE = 0.8V
			-2			SENSE = 0V
Reference and Common-Mode Voltages						
Internal Reference Voltage (Selected by V_{SENSE})	V_{REF}	—	0.74	—	V	V_{SENSE} = GND
		—	1.49	—		V_{SENSE} = AV_{DD12}
		—	1.86 x V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV
Common-Mode Voltage Output	V_{CM}	—	0.9	—	V	Available at V_{CM} pin
Reference Voltage Output(7,8)	VREF1	—	0.4	—	V	V_{SENSE} = GND
		—	0.8	—		V_{SENSE} = AV_{DD12}
		—	0.4 - 0.8	—		400 mV < V_{SENSE} < 800 mV
	VREF0	—	0.7	—	V	V_{SENSE} = GND
		—	1.4	—		V_{SENSE} = AV_{DD12}
		—	0.7 - 1.4	—		400 mV < V_{SENSE} < 800 mV
Bandgap Voltage Output	V_{BG}	—	0.55	—	V	Available at V_{BG} pin

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Analog Inputs						
Full-Scale Differential Analog Input Range(5,7)	A_{FS}	—	1.4875	—	V_{P-P}	V_{SENSE} = GND
		—	2.975	—		V_{SENSE} = AVDD12
		—	3.71875 x V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV
Analog Input Bandwidth	f_{IN_3dB}	—	500	—	MHz	A_{IN} = -3 dBFS
Differential Input Capacitance	C_{IN}	5	6	7	pF	**Note 5**, **Note 9**
Analog Input Channel Cross-Talk	XTALK	—	100	—	dBc	**Note 10**
Analog Input Leakage Current (A_{IN}+, A_{IN}- pins)	I_{LI_AH}	—	—	+1	µA	V_{IH} = AV_{DD12}
	I_{LI_AL}	-1	—	—	µA	V_{IL} = GND
ADC Conversion Rate(11)						
Conversion Rate	f_S	40	—	200	Msps	Tested at 200 Msps
Clock Inputs (CLK+, CLK-)(12)						
Clock Input Frequency	f_{CLK}	—	—	250	MHz	**Note 5**
Differential Input Voltage	V_{CLK_IN}	300	—	800	mV_{P-P}	**Note 5**
Clock Jitter	CLK_{JITTER}	—	175	—	f_{SRMS}	**Note 5**
Clock Input Duty Cycle(5)		49	50	51	%	Duty cycle correction disabled
		30	50	70	%	Duty cycle correction enabled
Input Leakage Current at CLK input pin	I_{LI_CLKH}	—	—	+110	µA	V_{IH} = AV_{DD12}
	I_{LI_CLKL}	-20	—	—	µA	V_{IL} = GND
Converter Accuracy(6)						
ADC Resolution (with no missing code)		—	—	16	bits	MCP37231/MCP37D31
		—	—	14	bits	MCP37221/MCP37D21
Offset Error		—	±5	±61	LSb	MCP37231/MCP37D31
		—	±1.25	±15.25	LSb	MCP37221/MCP37D21
Gain Error	G_{ER}	—	±0.5	—	% of FS	
Integral Nonlinearity	INL	—	±2	—	LSb	MCP37231/MCP37D31
		—	±0.5	—	LSb	MCP37221/MCP37D21
Differential Nonlinearity	DNL	—	±0.4	—	LSb	MCP37231/MCP37D31
		—	±0.1	—	LSb	MCP37221/MCP37D21
Analog Input Common-Mode Rejection Ratio	$CMRR_{DC}$	—	70	—	dB	DC measurement

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dynamic Accuracy(6,15)						
Spurious Free Dynamic Range	SFDR	78	90	—	dBc	f_{IN} = 15 MHz
		77	85	—	dBc	f_{IN} = 70 MHz
Signal-to-Noise Ratio	SNR f_{IN} = 15 MHz	73.3	74.7	—	dBFS	MCP37231/MCP37D31
		—	74.2	—	dBFS	MCP37221/MCP37D21
	SNR f_{IN} = 70 MHz	—	74.2	—	dBFS	MCP37231/MCP37D31
		—	73.7	—	dBFS	MCP37221/MCP37D21
Effective Number of Bits (ENOB)(13)	ENOB f_{IN} = 15 MHz	—	12.1	—	bits	MCP37231/MCP37D31
		—	12	—	bits	MCP37221/MCP37D21
	ENOB f_{IN} = 70 MHz	—	12	—	bits	MCP37231/MCP37D31
		—	11.7	—	bits	MCP37221/MCP37D21
Total Harmonic Distortion (for all resolutions, first 13 harmonics)	THD	78	89	—	dBc	f_{IN} = 15 MHz
		77	82	—	dBc	f_{IN} = 70 MHz
Worst Second or Third Harmonic Distortion	HD2 or HD3	—	90	—	dBc	f_{IN} = 15 MHz
		—	83	—	dBc	f_{IN} = 70 MHz
Two-Tone Intermodulation Distortion fIN_1 = 15 MHz, fIN_2 = 17 MHz	IMD	—	90.5	—	dBc	A_{IN} = -7 dBFS, with two input frequencies
Digital Logic Input and Output (Except LVDS Output)						
Schmitt Trigger High-Level Input Voltage	V_{IH}	0.7 DV_{DD18}	—	DV_{DD18}	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	GND	—	0.3 DV_{DD18}	V	
Hysteresis of Schmitt Trigger Inputs (All digital inputs)	V_{HYST}	—	0.05 DV_{DD18}	—	V	
Low-Level Output Voltage	V_{OL}	—	—	0.3	V	I_{OL} = -3 mA, all digital I/O pins
High-Level Output Voltage	V_{OH}	DV_{DD18} – 0.5	1.8	—	V	I_{OL} = +3 mA, all digital I/O pins
Digital Data Output (CMOS Mode)						
Maximum External Load Capacitance	C_{LOAD}	—	10	—	pF	From output pin to GND
Internal I/O Capacitance	C_{INT}	—	4	—	pF	Note 5

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Digital Data Output (LVDS Mode)(5)						
LVDS High-Level Differential Output Voltage	V_{H_LVDS}	200	300	400	mV	100Ω differential termination, LVDS bias = 3.5 mA
LVDS Low-Level Differential Output Voltage	V_{L_LVDS}	-400	-300	-200	mV	100Ω differential termination, LVDS bias = 3.5 mA
LVDS Common-Mode Voltage	V_{CM_LVDS}	1	1.15	1.4	V	
Output Capacitance	C_{INT_LVDS}	—	4	—	pF	Internal capacitance from output pin to GND
Differential Load Resistance (LVDS)	R_{LVDS}	—	100	—	Ω	Across LVDS output pairs
Input Leakage Current on Digital I/O Pins						
Data Output Pins	I_{LI_DH}	—	—	+1	µA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-1	—	—	µA	V_{IL} = GND
I/O Pins except Data Output Pins	I_{LI_DH}	—	—	+6	µA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-35	—	—	µA	V_{IL} = GND(14)

Notes:

1. This 1.8V digital supply voltage is used for the digital I/O circuit, including SPI, CMOS and LVDS data output drivers.
2. Standby Mode: Most of the internal circuits are turned off, except the internal reference, clock, bias circuits and SPI interface.
3. Shutdown Mode: All circuits including reference and clock are turned off except the SPI interface.
4. Power dissipation (typical) is calculated by using the following equation:

   (a) During operation:

   $P_{DISS} = V_{DD18} \times (I_{DD\_A18} + I_{DD\_D18}) + V_{DD12} \times (I_{DD\_A12} + I_{DD\_D12})$, where I_{DD_D18} is the digital I/O current for LVDS or CMOS output. V_{DD18} = 1.8V and V_{DD12} = 1.2V are used for typical value calculation.

   (b) During Standby mode:

   $P_{DISS\_STANDBY} = (I_{STANDBY\_AN} + I_{STANDBY\_DIG}) \times 1.2V$

   (c) During Shutdown mode:

   $P_{DISS\_SHDN} = I_{DD\_SHDN} \times 1.2V$
5. This parameter is ensured by design, but not 100% tested in production.
6. This parameter is ensured by characterization, but not 100% tested in production.
7. See Table 4-2 for details.
8. Differential reference voltage output at REF1+/- and REF0+/- pins. $V_{REF1} = V_{REF1}+ - V_{REF1}-$. $V_{REF0} = V_{REF0}+ - V_{REF0}-$. These references should not be driven.
9. Input capacitance refers to the effective capacitance between one differential input pin pair.
10. Channel cross-talk is measured when A_{IN} = -1 dBFS at 12 MHz is applied on one channel while other channel(s) are terminated with 50Ω. See Figure 3-39 for details.
11. The ADC core conversion rate. In multi-channel mode, the conversion rate of an individual channel is f_S/N, where N is the number of input channels used.
12. See Figure 4-8 for the details of the clock input circuit.
13. ENOB = (SINAD - 1.76)/6.02.
14. This leakage current is due to the internal pull-up resistor.
15. Dynamic performance is characterized with CH(n)_DIG_GAIN<7:0> = 0011-1000.

TABLE 2-2: TIMING REQUIREMENTS - LVDS AND CMOS OUTPUTS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps (ADC Core), Resolution = 16-bit, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, DCLK_PHDLY_DLL<2:0> = 000, +25°C is applied for typical value.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Aperture Delay	t_A	—	1	—	ns	**Note 1**
Out-of-Range Recovery Time	t_{OVR}	—	1	—	Clocks	**Note 1**
Output Clock Duty Cycle		—	50	—	%	**Note 1**
Pipeline Latency	$T_{LATENCY}$	—	28	—	Clocks	**Note 2**, **Note 4**
System Calibration(1)						
Power-Up Calibration Time	T_{PCAL}	—	2^{27}	—	Clocks	First 2^{27} sample clocks after power-up
Background Calibration Update Rate	T_{BCAL}	—	2^{30}	—	Clocks	Per 2^{30} sample clocks after T_{PCAL}
$\overline{\text{RESET}}$ Low Time	T_{RESET}	5	—	—	ns	See Figure 2-8 for details(1)
AutoSync (1,6)						
Sync Output Time Delay	T_{SYNC_OUT}	—	1	—	Clocks	
Maximum Recommended ADC Clock Rate for AutoSync		—	200	—	MHz	**Single-Channel mode**
		—	160	—		**Multi-Channel mode**
LVDS Data Output Mode(1,5)						
Input Clock to Output Clock Propagation Delay	t_{CPD}	—	5.7	—	ns	
Output Clock to Data Propagation Delay	t_{DC}	—	0.5	—	ns	
Input Clock to Output Data Propagation Delay	t_{PD}	—	5.8	—	ns	
CMOS Data Output Mode(1)						
Input Clock to Output Clock Propagation Delay	t_{CPD}	—	3.8	—	ns	
Output Clock to Data Propagation Delay	t_{DC}	—	0.7	—	ns	
Input Clock to Output Data Propagation Delay	t_{PD}	—	4.5	—	ns	

Note 1: This parameter is ensured by design, but not 100% tested in production.

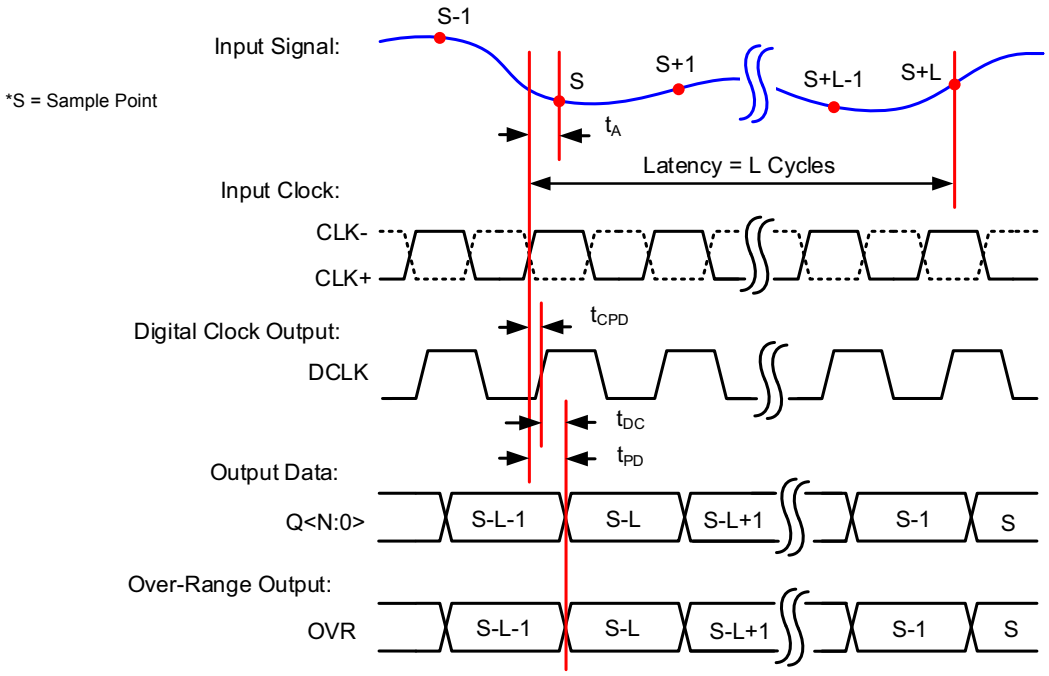
2: This parameter is ensured by characterization, but not 100% tested in production.

3: t_{RISE} = approximately less than 10% of duty cycle.

4: Output latency is measured without using fractional delay recovery (FDR), decimation filter or digital down-converter options.

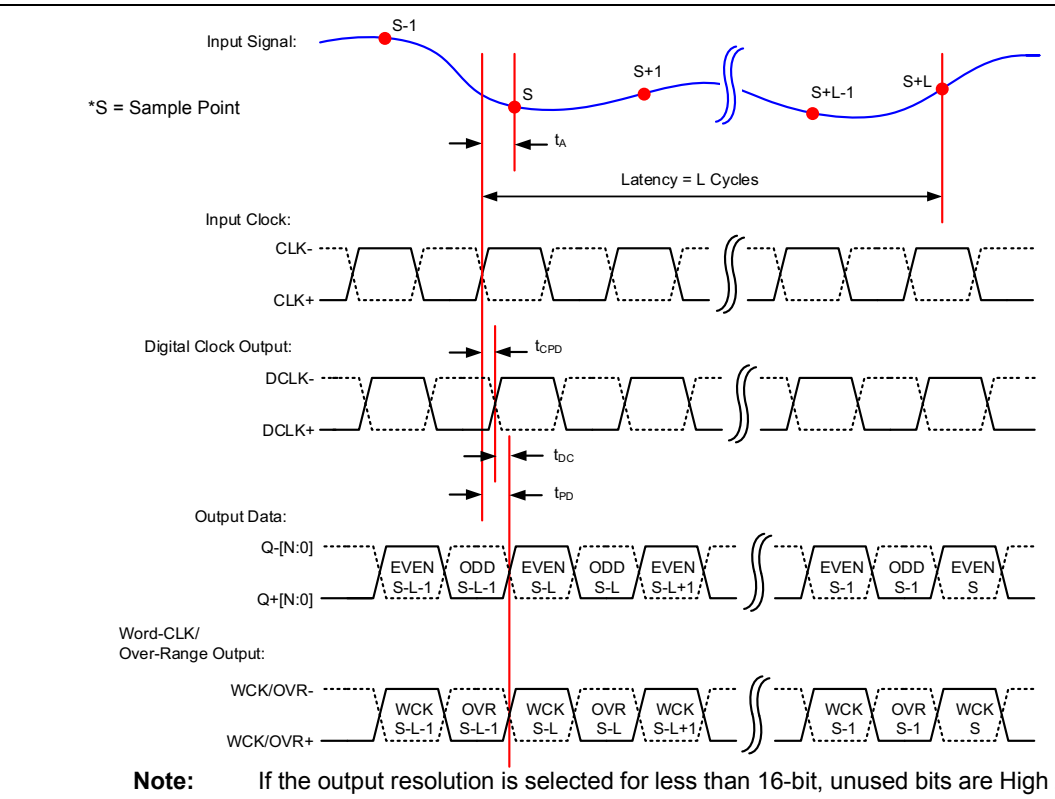
5: The time delay can be adjusted with the DCLK_PHDLY_DLL<2:0> setting.

6: Characterized with a single slave device. The maximum ADC sample rate for AutoSync mode may be reduced if multiple slave devices are used.



Note: If the output resolution is selected for less than 16-bit, unused bits are '0's.

FIGURE 2-1: *Timing Diagram - CMOS Output.*



Note: If the output resolution is selected for less than 16-bit, unused bits are High Z.

FIGURE 2-2: *Timing Diagram - LVDS Output with Even Bit First Option.*

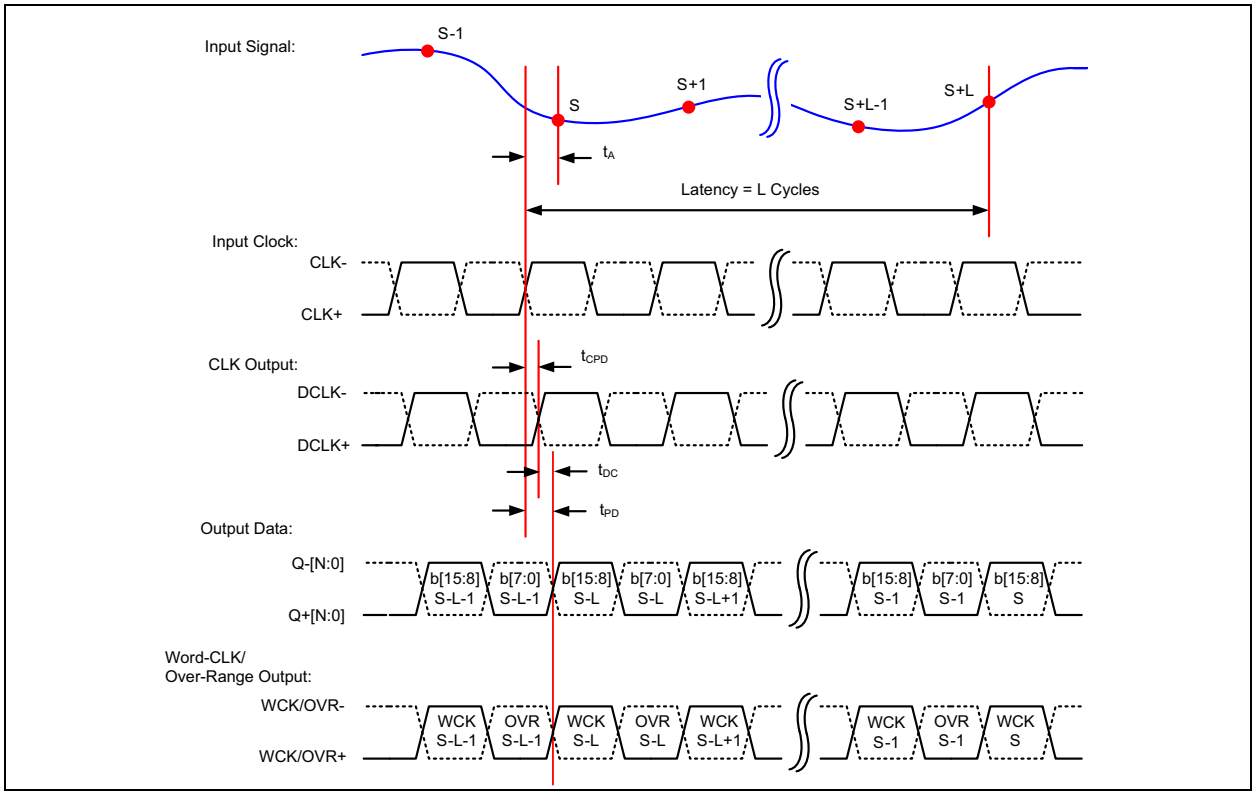


FIGURE 2-3: *Timing Diagram - LVDS Output with MSb Byte First Option. This output option is available for 16-bit mode only.*