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MCP37220-200
MCP37D20-200

200 Msps, 14-Bit Low-Power Single-Channel ADC

Features

- Sample Rates: 200 Msps
- Signal-to-Noise Ratio (SNR) with f_{IN} = 15 MHz and -1 dBFS:
  - 67.8 dBFS (typical) at 200 Msps
- Spurious-Free Dynamic Range (SFDR) with f_{IN} = 15 MHz and -1 dBFS:
  - 96 dBc (typical) at 200 Msps
- Power Dissipation with LVDS Digital I/O:
  - 346 mW at 200 Msps
- Power Dissipation with CMOS Digital I/O:
  - 304 mW at 200 Msps, output clock = 100 MHz
- Power Dissipation Excluding Digital I/O:
  - 256 mW at 200 Msps
- Power-Saving Modes:
  - 89 mW during Standby
  - 24 mW during Shutdown
- Supply Voltage:
  - Digital Section: 1.2V, 1.8V
  - Analog Section: 1.2V, 1.8V
- Selectable Full-Scale Input Range: up to 1.8 V_{P-P}
- Analog Input Bandwidth: 650 MHz
- Output Interface:
  - Parallel CMOS, DDR LVDS
- Output Data Format:
  - Two's complement or offset binary
- Optional Output Data Randomizer
- Digital Signal Post-Processing (DSPP) Options:
  - Decimation filters for improved SNR
  - Offset and Gain adjustment
  - Digital Down-Conversion (DDC) with I/Q or f_S/8 output (MCP37D20-200)
- Built-In ADC Linearity Calibration Algorithms:
  - Harmonic Distortion Correction (HDC)
  - DAC Noise Cancellation (DNC)
  - Dynamic Element Matching (DEM)
  - Flash Error Calibration
- Serial Peripheral Interface (SPI)
- Package Options:
  - VTLA-124 (9 mm x 9 mm x 0.9 mm)
  - TFBGA-121 (8 mm x 8 mm)
- No external reference decoupling capacitor required for TFBGA Package
- Industrial Temperature Range: -40°C to +85°C

Typical Applications

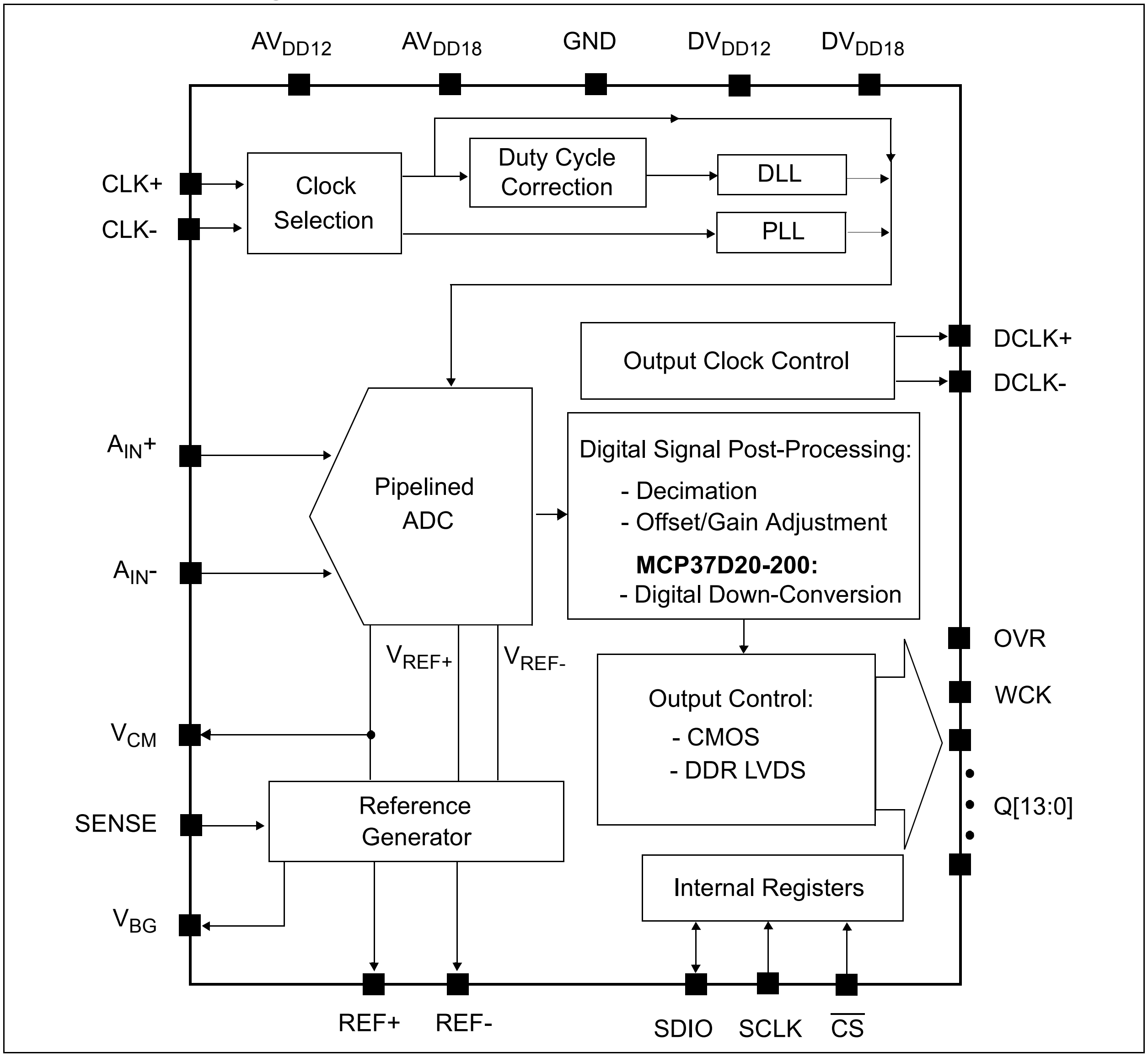
- Communication Instruments
- Microwave Digital Radio
- Cellular Base Stations
- Radar
- Scanners and Low-Power Portable Instruments
- Industrial and Consumer Data Acquisition System

Device Offering[1]

Part Number	Sample Rate	Resolution	Digital Decimation (FIR Filters)	Digital Down-Conversion	Noise-Shaping Requantizer
MCP37220-200	200 Msps	14	Yes	No	No
MCP37D20-200	200 Msps	14	Yes	Yes	No
MCP37210-200	200 Msps	12	Yes	No	Yes
MCP37D10-200	200 Msps	12	Yes	Yes	Yes

1: Devices in the same package type are pin-compatible.

Functional Block Diagram



Description

The MCP37220-200 is a single-channel 200 Msps 14-bit pipelined ADC, with built-in high-order digital decimation filters, gain and offset adjustment.

The MCP37D20-200 is also a single-channel 200 Msps 14-bit pipelined ADC, with built-in digital down-conversion in addition to the features offered by the MCP37220-200.

Both devices feature harmonic distortion correction and DAC noise cancellation that enables high-performance specifications with SNR of 67.8 dBFS (typical) and SFDR of 96 dBc (typical).

The output decimation filter option improves SNR performance up to 83.9 dBFS with the 512x decimation setting.

The digital down-conversion option in the MCP37D20-200 can be utilized with the decimation and quadrature output (I and Q data) options and offers great flexibility in digital communication system design, including cellular base-stations and narrow-band communication systems.

These A/D converters exhibit industry-leading low-power performance with only 348 mW operation while using the LVDS output interface at 200 Msps. This superior low-power operation, coupled with high dynamic performance, makes these devices ideal for portable communication devices, sonar, radar and high-speed data acquisition systems.

These devices also include various features designed to maximize flexibility in the user's applications and minimize system cost, such as a programmable PLL clock, output data rate control and phase alignment, and programmable digital pattern generation. The device's operational modes and feature sets are configured by setting up the user-programmable internal registers.

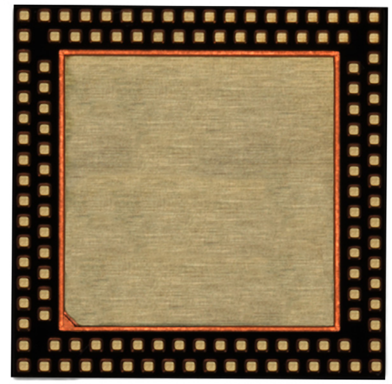
The device samples the analog input on the rising edge of the clock. The digital output code is available after 23 clock cycles of data latency. Latency will increase if any of the digital signal post-processing (DSPP) options are enabled.

The differential full-scale analog input range is programmable up to 1.8 V_{P-P}. The ADC output data can be coded in two's complement or offset binary representation, with or without the data randomizer option. The output data is available with a full-rate CMOS or Double-Data-Rate (DDR) LVDS interface.

The device is available in Pb-free VTLA-124 and TFBGA-121 packages. The device operates over the commercial temperature range of -40°C to +85°C.

Package Types

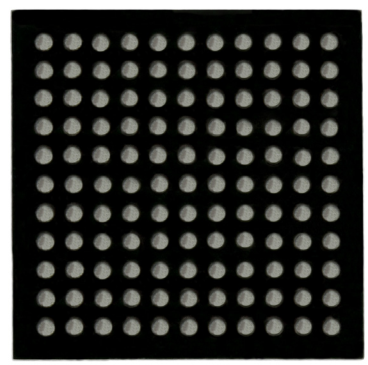
Bottom View



Dimension: 9 mm x 9 mm x 0.9 mm

(a) VTLA-124 Package.

Bottom View

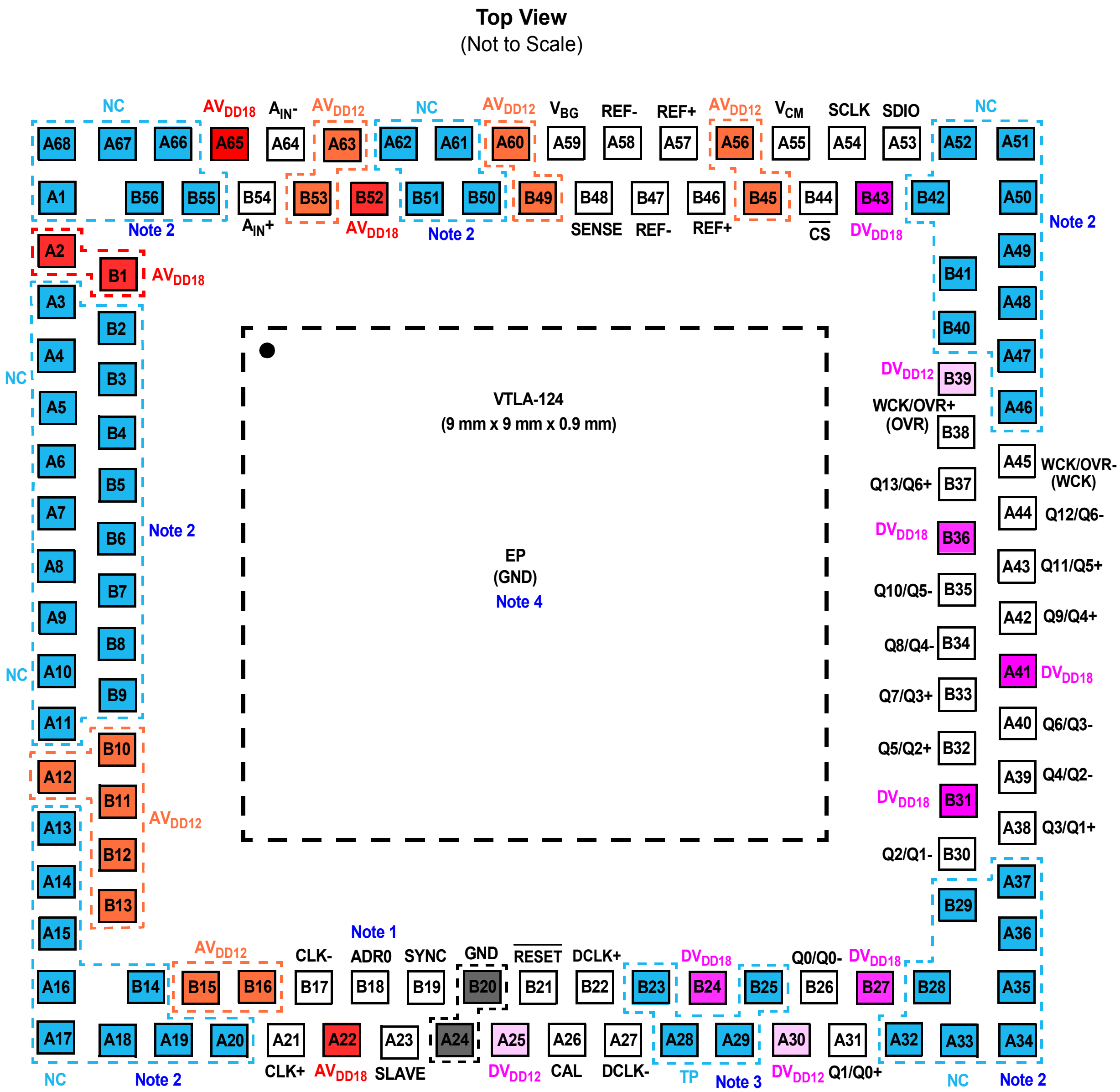


Dimension: 8 mm x 8 mm x 1.08 mm
Ball Pitch: 0.65 mm
Ball Diameter: 0.4 mm

(b) TFBGA-121 Package.

NOTES:

1.0 PACKAGE PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Note 1: Tie to GND or DV_{DD18}. ADR1 is internally bonded to GND.

2: NC – Not connected pin. This pin can float or be tied to ground.

3: TP – Test pin. Leave this pin floating and do not tie to ground or supply.

4: Exposed pad (EP – back pad of the package) is the common ground (GND) for analog and digital supplies. Connect this pad to a clean ground reference on the PCB.

FIGURE 1-1: *VTLA-124 Package.*

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124

Pin No.	Name	I/O Type	Description
Power Supply Pins			
A2, A22, A65, B1, B52	AV_{DD18}	Supply	Supply voltage input (1.8V) for analog section
A12, A56, A60, A63, B10, B11, B12, B13, B15, B16, B45, B49, B53	AV_{DD12}		Supply voltage input (1.2V) for analog section
A25, A30, B39	DV_{DD12}		Supply voltage input (1.2V) for digital section
A41, B24, B27, B31, B36, B43	DV_{DD18}		Supply voltage input (1.8V) for digital section and all digital I/O
EP	GND		Exposed pad: Common ground pin for digital and analog sections
ADC Analog Input Pins			
B54	A_{IN}+	Analog Input	Differential analog input (+)
A64	A_{IN}-		Differential analog input (-)
A21	CLK+		Differential clock input (+)
B17	CLK-		Differential clock input (-)
Reference Pins [(1)]			
A57, B46	REF+	Analog Output	Differential reference voltage (+)
A58, B47	REF-		Differential reference voltage (-)
SENSE, Bandgap and Common-Mode Voltage Pins			
B48	SENSE	Analog Input	Analog input full-scale range selection. See Table 4-2 for SENSE voltage settings.
A59	V_{BG}	Analog Output	Internal bandgap output voltage. Connect a decoupling capacitor (2.2 µF)
A55	V_{CM}		Common-mode output voltage for analog input signal. Connect a decoupling capacitor (0.1 µF)[(2)]
Digital I/O Pins			
B18	ADR0	Digital Input	SPI address selection pin (A0 bit). Tie to GND or DV_{DD18}[(3)]
A23	SLAVE		Not used. Tie to GND[(9)]
B19	SYNC	Digital Input/Output	Not used. Leave this pin floating[(9)]
B21	$\overline{\text{RESET}}$	Digital Input	Reset control input: **High:** Normal operating mode **Low:** Reset mode[(4)]
A26	CAL	Digital Output	Calibration status flag digital output: **High:** Calibration is complete **Low:** Calibration is not complete[(5)]
B22	DCLK+		**LVDS**: Differential digital clock output (+) **CMOS:** Digital clock output[(6)]
A27	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Unused (leave floating)

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
ADC Output Pins [(7)](#)			
B26	Q0/Q0-	Digital Output	Digital data output: CMOS = Q0 DDR LVDS = Q0-
A31	Q1/Q0+		Digital data output: CMOS = Q1 DDR LVDS = Q0+
B30	Q2/Q1-		Digital data output: CMOS = Q2 DDR LVDS = Q1-
A38	Q3/Q1+		Digital data output: CMOS = Q3 DDR LVDS = Q1+
A39	Q4/Q2-		Digital data output: CMOS = Q4 DDR LVDS = Q2-
B32	Q5/Q2+		Digital data output: CMOS = Q5 DDR LVDS = Q2+
A40	Q6/Q3-		Digital data output: CMOS = Q6 DDR LVDS = Q3-
B33	Q7/Q3+		Digital data output: CMOS = Q7 DDR LVDS = Q3+
B34	Q8/Q4-		Digital data output: CMOS = Q8 DDR LVDS = Q4-
A42	Q9/Q4+		Digital data output: CMOS = Q9 DDR LVDS = Q4+
B35	Q10/Q5-		Digital data output: CMOS = Q10 DDR LVDS = Q5-
A43	Q11/Q5+		Digital data output: CMOS = Q11 DDR LVDS = Q5+
A44	Q12/Q6-		Digital data output: CMOS = Q12 DDR LVDS = Q6-
B37	Q13/Q6+		Digital data output: CMOS = Q13 DDR LVDS = Q6+
B38	WCK/ OVR+ (OVR)		**OVR:** Input overrange indication digital output[(8)] **WCK:** - **MCP37220:** No output - **MCP37D20:** Word clock synchronizes with digital output in I/Q data mode
A45	WCK/OVR- (WCK)		
SPI Interface Pins			
A53	SDIO	Digital Input/ Output	SPI data input/output
A54	SCLK	Digital Input	SPI serial clock input
B44	$\overline{CS}$		SPI Chip Select input

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
Not Connected Pins			
A1, A3 - A7, A8 - A11, A13 - A20, A32 - A37, A46 - A52, A61 - A62, A66 - A68, B2 - B9, B14, B28, B29, B40, B41, B42, B50 - B51, B55, B56	NC		These pins can be tied to ground or left floating.
Pins that need to be grounded			
A24, A64, B20, B54	GND		These pins are not supply pins, but need to be tied to ground.
Output Test Pins			
A28 - A29, B23, B25	TP	Digital Output	Output test pins. Do not use. Always leave these pins floating. Do not tie to ground or supply.

Notes:

1. These pins are for the internal reference voltage output. They should not be driven. External decoupling circuit is required. See **Section 4.3.3 "Decoupling Circuits for Internal Voltage Reference and Bandgap Output"** for details.
2. When V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), V_{CM} pin should be decoupled with a 0.1 µF capacitor.
3. ADR1 (for A1 bit) is internally bonded to GND ('0'). If ADR0 is dynamically controlled, ADR0 must be held constant while $\overline{CS}$ is "Low".
4. The device is in Reset mode while this pin stays "Low". On the rising edge of $\overline{RESET}$, the device exits the Reset mode, initializes all internal user registers to default values and begins power-up calibration.
5. CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or a Soft Reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes, this pin will maintain the prior condition.
6. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital signal post-processing (DSPP) and PLL (or DLL). See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
7. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The output pins shown here are for the "Even bit first" setting, which is the default setting of OUTPUT_MODE<1:0> in Address 0x62 (Register 5-20). The even data bits (Q0, Q2, Q4, Q6, Q8, Q10, Q12) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11, Q13) appear when DCLK+ is "Low". See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control. See Figure 2-2 for LVDS output timing diagrams.
8. **OVR:** OVR will be held "High"' when analog input overrange is detected. Digital signal post-processing (DSPP) will cause OVR to assert early relative to the output data. See Figure 2-2 for LVDS timing of these bits.
   WCK: Available for the I/Q output mode only in the MCP37D20. WCK is normally "Low" in I/Q output mode, and "High" when it outputs in-phase (I) data.
   (a) MCP37220 and MCP37D20 operating outside I/Q output mode: WCK/OVR+ is OVR and WCK/OVR- is logic '0' (not used). In DDR LVDS output mode, the rising edge of DCLK+ is OVR.
   (b) I/Q output mode in the MCP37D20: In CMOS output mode, WCK/OVR+ is OVR and WCK/OVR- is WCK. WCK is synchronized to in-phase (I) data. In DDR LVDS output mode, WCK/OVR+ and WCK/OVR- are multiplexed. The rising edge of DCLK+ is OVR and the falling edge is WCK.
9. This pin function is not released yet.

Top View
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11
A	SDIO	V_{CM}	REF+	REF-	V_{BG}	TP1	TP1	A_{IN-}	A_{IN+}	GND	GND
B	SCLK	$\overline{CS}$	GND	GND	SENSE	AV_{DD12}	AV_{DD12}	AV_{DD18}	AV_{DD18}	GND	GND
C	WCK/ OVR- (WCK)	WCK/ OVR+ (OVR)	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
D	Q12/Q6-	Q13/Q6+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
E	Q10/Q5-	Q11/Q5+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
F	Q8/Q4-	Q9/Q4+	DV_{DD18}	DV_{DD18}	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	GND	GND
G	Q6/Q3-	Q7/Q3+	DV_{DD18}	DV_{DD18}	GND	GND	AV_{DD12}	AV_{DD12}	GND	GND	GND
H	Q4/Q2-	Q5/Q2+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	GND	GND
J	Q2/Q1-	Q3/Q1+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	GND	GND
K	Q0/Q0-	Q1/Q0+	TP2	DCLK-	CAL	GND	SLAVE	ADR0	ADR1	GND	GND
L	TP2	TP2	TP2	DCLK+	$\overline{RESET}$	SYNC	GND	CLK+	CLK-	GND	AV_{DD18}

Analog (green)
Digital (yellow)
All others: Supply Voltage

Notes:
- Die dimension: 8 mm x 8 mm x 1.08 mm.
- Ball dimension: (a) Ball Pitch = 0.65 mm, (b) Ball Diameter = 0.4 mm.
- Solder sphere composition (SnAgCu).

FIGURE 1-2: *TFBGA-121 Package. Decoupling capacitors for reference pins and V_{BG} are embedded in the package.*

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121

Ball No.	Name	I/O Type	Description
A1	SDIO	Digital Input/Output	SPI data input/output
A2	V_{CM}	Analog Output	Common-mode output voltage for analog input signal Connect a decoupling capacitor (0.1 µF)(1)
A3	REF+		Differential reference voltage (+/-). Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating.
A4	REF-		
A5	V_{BG}		Internal bandgap output voltage A decoupling capacitor (2.2 µF) is embedded in the TFBGA package. Leave this pin floating.
A6	TP1	Analog Output	Analog test pins. Leave these pins floating.
A7			
A8	A_{IN-}	Analog Input	Differential analog input (-)
A9	A_{IN+}		Differential analog input (+)
A10	GND	Supply	Common ground for analog and digital sections
A11			
B1	SCLK	Digital Input	SPI serial clock input
B2	$\overline{CS}$		SPI chip select input
B3	GND	Supply	Common ground for analog and digital sections
B4			
B5	SENSE	Analog Input	Analog input range selection. See Table 4-2 for SENSE voltage settings.
B6	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
B7			
B8	AV_{DD18}		Supply voltage input (1.8V) for analog section
B9			
B10	GND	Supply	Common ground for analog and digital sections
B11			
C1	WCK/OVR- (WCK)	Digital Output	**OVR:** Input overrange indication digital output(2) **WCK:** - **MCP37220:** No output - **MCP37D20:** Word clock synchronizes with digital output in I/Q data mode
C2	WCK/OVR+ (OVR)		
C3	GND	Supply	Common ground for analog and digital sections
C4			
C5	AV_{DD12}		Supply voltage input (1.2V) for analog section
C6			
C7			
C8	GND		Common ground pin for analog and digital sections
C9			
C10			
C11			

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
D1	Q12/Q6-	Digital Output	Digital data output[(3)] CMOS = Q12 DDR LVDS = Q6-
D2	Q13/Q6+		Digital data output[(3)] CMOS = Q13 DDR LVDS = Q6+
D3	GND	Supply	Common ground for analog and digital sections
D4			
D5	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
D6			
D7			
D8	GND	Supply	Common ground for analog and digital sections
D9			
D10			
D11			
E1	Q10/Q5-	Digital Output	Digital data output[(3)] CMOS = Q10 DDR LVDS = Q5-
E2	Q11/Q5+		Digital data output[(3)] CMOS = Q11 DDR LVDS = Q5+
E3	GND	Supply	Common ground for analog and digital sections
E4			
E5	AV_{DD12}		Supply voltage input (1.2V) for analog section
E6			
E7			
E8	GND		Common ground for analog and digital sections
E9			
E10			
E11			
F1	Q8/Q4-	Digital Output	Digital data output[(3)] CMOS = Q8 DDR LVDS = Q4-
F2	Q9/Q4+		Digital data output[(3)] CMOS = Q9 DDR LVDS = Q4+
F3	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV_{DD18} potential.
F4			
F5	AV_{DD12}		Supply voltage input (1.2V) for analog section
F6			
F7			
F8	GND		Common ground for analog and digital sections
F9			
F10			
F11			

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
G1	Q6/Q3-	Digital Output	Digital data output(3) CMOS = Q6 DDR LVDS = Q3-
G2	Q7/Q3+		Digital data output(3) CMOS = Q7 DDR LVDS = Q3+
G3	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV_{DD18} potential
G4			
G5	GND		Common ground for analog and digital sections
G6			
G7	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
G8			
G9	GND		Common ground for analog and digital sections
G10			
G11			
H1	Q4/Q2-	Digital Output	Digital data output(3) CMOS = Q4 DDR LVDS = Q2-
H2	Q5/Q2+		Digital data output(3) CMOS = Q5 DDR LVDS = Q2+
H3	DV_{DD12}	Supply	Supply voltage input (1.2V) for digital section
H4			
H5	GND		Common ground for analog and digital sections
H6			
H7			
H8			
H9			
H10			
H11			
J1	Q2/Q1-	Digital Output	Digital data output(3) CMOS = Q2 DDR LVDS = Q1-
J2	Q3/Q1+		Digital data output(3) CMOS = Q3 DDR LVDS = Q1+
J3	DV_{DD12}	Supply	DC supply voltage input pin for digital section (1.2V)
J4			
J5	GND		Common ground for analog and digital sections
J6			
J7			
J8			
J9			
J10			
J11			

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
K1	Q0/Q0-	Digital Output	Digital data output(3) CMOS = Q0 DDR LVDS = Q0-
K2	Q1/Q0+		Digital data output(3) CMOS = Q1 DDR LVDS = Q0+
K3	TP2		Output test pin. Do not use. Do not tie to ground or supply. Always leave this pin floating.
K4	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Unused (leave floating)
K5	CAL		Calibration status flag digital output(4) **High:** Calibration is complete **Low:** Calibration is not complete
K6	GND	Supply	Common ground pin for analog and digital sections
K7	SLAVE	Digital Input	Not used. Tie this pin to GND(8)
K8	ADR0		SPI address selection pin (A0 bit). Tie to GND or DV_{DD18}(5)
K9	ADR1		SPI address selection pin (A1 bit). Tie to GND or DV_{DD18}(5)
K10	GND	Supply	Common ground for analog and digital sections
K11			
L1	TP2	Digital Output	Output test pins. Do not use. Do not tie to ground or supply. Always leave these pins floating.
L2			
L3			
L4	DCLK+		**LVDS:** Differential digital clock output (+) **CMOS:** Digital clock output(6)
L5	$\overline{RESET}$	Digital Input	Reset control input: **High**: Normal operating mode **Low:** Reset mode(7)
L6	SYNC	Digital Input/ Output	Not used. Leave this pin floating(8)
L7	GND	Supply	Common ground for analog and digital sections
L8	CLK+	Analog Input	Differential clock input (+)
L9	CLK-		Differential clock input (-)
L10	GND	Supply	Common ground for analog and digital sections
L11	AV_{DD18}	Analog Input	Supply voltage input (1.8V) for analog section

Notes:

1. When V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), the V_{CM} pin should be decoupled with a 0.1 µF capacitor.
2. **OVR:** OVR will be held "High"' when analog input overrange is detected. Digital signal post-processing (DSPP) will cause OVR to assert early relative to the output data. See Figure 2-2 for LVDS timing of these bits.
   WCK: Available for the I/Q output mode only in the MCP37D20. In the I/Q output mode, WCK is normally "Low", and "High" when it outputs in-phase (I) data.
   - **(a) MCP37220 and MCP37D20 operating outside I/Q output mode**: WCK/OVR+ is OVR and WCK/OVR- is logic '0' (not used). In DDR LVDS output mode, the rising edge of DCLK+ is OVR.
   - **(b) I/Q output mode in the MCP37D20:** In CMOS output mode, WCK/OVR+ is OVR and WCK/OVR- is WCK. WCK is synchronized to in-phase (I) data. In DDR LVDS output mode, WCK/OVR+ and WCK/OVR- are multiplexed. The rising edge of DCLK+ is OVR and the falling edge is WCK.
3. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The output pins shown here are for the "Even bit first" setting, which is the default setting of OUTPUT_MODE<1:0> in Address 0x62 (Register 5-20). The even data bits (Q0, Q2, Q4, Q6, Q8, Q10, Q12) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11, Q13) appear when DCLK+ is "Low". See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control.
   See Figure 2-2 for LVDS output timing diagram.
4. CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or a Soft Reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes this pin will maintain the prior condition.
5. If the SPI address is dynamically controlled, the Address pin must be held constant while $\overline{CS}$ is "Low".
6. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital signal post-processing (DSPP) and PLL (or DLL). See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
7. The device is in Reset mode while this pin stays "Low". On the rising edge of $\overline{RESET}$, the device exits the Reset mode, initializes all internal user registers to default values, and begins power-up calibration.
8. This pin function is not released yet.

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings †

Analog and Digital Supply Voltage (AV_{DD12}, DV_{DD12}) .... -0.3V to 1.32V
Analog and Digital Supply Voltage (AV_{DD18}, DV_{DD18}) .... -0.3V to 1.98V
All Inputs and Outputs with respect to GND .... -0.3V to AV_{DD18} + 0.3V
Differential Input Voltage .... |AV_{DD18} - GND|
Current at Input Pins .... ±2 mA
Current at Output and Supply Pins .... ±250 mA
Storage Temperature .... -65°C to +150°C
Ambient Temperature with Power Applied (T_A) .... -55°C to +125°C
Maximum Junction Temperature (T_J) .... +150°C
ESD Protection on all Pins .... 2 kV HBM
Solder Reflow Profile .... See Microchip Application Note AN233 (DS00233)

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 Electrical Specifications

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Requirements						
Analog Supply Voltage	AV_{DD18}	1.71	1.8	1.89	V	
	AV_{DD12}	1.14	1.2	1.26	V	
Digital Supply Voltage	DV_{DD18}	1.71	1.8	1.89	V	Note 1
	DV_{DD12}	1.14	1.2	1.26	V	
Analog Supply Current						
Analog Supply Current during Conversion	I_{DD_A18}	—	0.03	0.1	mA	at AV_{DD18} Pin
	I_{DD_A12}	—	141	159	mA	at AV_{DD12} Pin
Digital Supply Current						
Digital Supply Current during Conversion	I_{DD_D12}	—	72	109	mA	at DV_{DD12} Pin
Digital I/O Current in CMOS Output Mode	I_{DD_D18}	—	27	—	mA	at DV_{DD18} Pin DCLK = 100 MHz
Digital I/O Current in LVDS Mode	I_{DD_D18}	**Measured at DV_{DD18} Pin**				
		—	50	75	mA	3.5 mA mode
			35	—	mA	1.8 mA mode
			62			5.4 mA mode
Supply Current during Power-Saving Modes						
During Standby Mode	$I_{STANDBY\_AN}$	—	45	—	mA	Address 0x00<4:3> = 1,1[(2)]
	$I_{STANDBY\_DIG}$	—	29	—		
During Shutdown Mode	I_{DD_SHDN}	—	20	—	mA	Address 0x00<7,0> = 1,1[(3)]

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PLL Circuit						
PLL Circuit Current	I_{DD_PLL}	—	17	—	mA	PLL enabled. Included in analog supply current specification.
Total Power Dissipation[4]						
Power Dissipation during Conversion, excluding Digital I/O	P_{DISS_ADC}	—	256	—	mW	
Total Power Dissipation during Conversion with CMOS Output Mode	P_{DISS_CMOS}	—	304	—	mW	f_S = 200 Msps, DCLK = 100 MHz
Total Power Dissipation during Conversion with LVDS Output Mode	P_{DISS_LVDS}	—	346	—	mW	3.5 mA mode
			319			1.8 mA mode
			367			5.4 mA mode
During Standby Mode	$P_{DISS\_STANDBY}$	—	89	—	mW	Address 0x00<4:3> = 1,1[2]
During Shutdown Mode	P_{DISS_SHDN}	—	24	—	mW	Address 0x00<7,0> = 1,1[3]
Power-On Reset (POR) Voltage						
Threshold Voltage	V_{POR}	—	800	—	mV	Applicable to AV_{DD12} only (POR tracks AV_{DD12})
Hysteresis	V_{POR_HYST}	—	40	—	mV	
SENSE Input[5,7,13]						
SENSE Input Voltage	V_{SENSE}	GND	—	AV_{DD12}	V	V_{SENSE} selects reference
SENSE Pin Input Resistance	R_{IN_SENSE}	—	694	—	Ω	V_{SENSE} = 0.8V
		—	154.8	—	kΩ	V_{SENSE} = 1.2V
Current Sink into SENSE Pin	I_{SENSE}	—	360	—	µA	V_{SENSE} = 0.8V
		—	4.2	—	µA	V_{SENSE} = 1.2V
Reference and Common-Mode Voltages						
Internal Reference Voltage[7,8]	V_{REF}	—	0.4	—	V	V_{SENSE} = GND
		—	0.8	—		V_{SENSE} = AV_{DD12}
		—	V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV
Common-Mode Voltage Output	V_{CM}	—	0.55	—	V	Available at V_{CM} pin
Bandgap Voltage Output	V_{BG}	—	0.55	—	V	Available at V_{BG} pin

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Analog Inputs						
Full-Scale Differential Analog Input Range(5,7)	A_{FS}	—	0.9	—	V_{P-P}	V_{SENSE} = GND
		—	1.8	—		V_{SENSE} = AV_{DD12}
		—	2.25 x V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV
Analog Input Bandwidth	f_{IN_3dB}	—	650	—	MHz	A_{IN} = -3 dBFS
Differential Input Capacitance	C_{IN}	—	1.6	—	pF	Note 5, Note 9
Analog Input Leakage Current (A_{IN}+, A_{IN}- pins)	I_{LI_AH}	—	—	+50	µA	V_{IH} = AV_{DD12}
	I_{LI_AL}	-50	—	—	µA	V_{IL} = GND
ADC Conversion Rate						
Conversion Rate	f_S		—	200	Msps	Tested at 200 Msps
Clock Inputs (CLK+, CLK-)(10)						
Clock Input Frequency	f_{CLK}	—	—	250	MHz	Note 5
Differential Input Voltage	V_{CLK_IN}	300	—	800	mV_{P-P}	Note 5
Clock Jitter	CLK_{JITTER}	—	175	—	fS_{RMS}	Note 5
Clock Input Duty Cycle(5)		49	50	51	%	Duty cycle correction disabled
		30	50	70	%	Duty cycle correction enabled
Input Leakage Current at CLK input pin	I_{LI_CLKH}	—	—	+110	µA	V_{IH} = AV_{DD12}
	I_{LI_CLKL}	-20	—	—	µA	V_{IL} = GND
Converter Accuracy(6)						
ADC Resolution (with no missing code)		—	—	14	bits	
Offset Error		—	±15	±45	LSb	
Gain Error	G_{ER}	—	±0.5	—	% of FS	
Integral Nonlinearity	INL	—	±1.5	—	LSb	
Differential Nonlinearity	DNL	—	±0.4	—	LSb	
Analog Input Common-Mode Rejection Ratio	$CMRR_{DC}$	—	70	—	dB	DC measurement

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Dynamic Accuracy(6,14)						
Spurious Free Dynamic Range	SFDR	82	96	—	dBc	f_{IN} = 15 MHz
		—	80	—	dBc	f_{IN} = 70 MHz
Signal-to-Noise Ratio (for all resolutions)	SNR	66.1	67.8	—	dBFS	f_{IN} = 15 MHz
		—	67.2	—		f_{IN} = 70 MHz
Effective Number of Bits (ENOB)(11)	ENOB	—	10.9	—	bits	f_{IN} = 15 MHz
		—	10.9	—		f_{IN} = 70 MHz
Total Harmonic Distortion (first 13 harmonics)	THD	83	89	—	dBc	f_{IN} = 15 MHz
			81	—	dBc	f_{IN} = 70 MHz
Worst Second or Third Harmonic Distortion	HD2 or HD3	—	95.8	—	dBc	f_{IN} = 15 MHz
		—	82	—	dBc	f_{IN} = 70 MHz
Two-Tone Intermodulation Distortion f_{IN1} = 15 MHz, f_{IN2} = 17 MHz	IMD	—	92.7	—	dBc	A_{IN} = -7 dBFS, with two input frequencies
Digital Logic Input and Output (Except LVDS Output)						
Schmitt Trigger High-Level Input Voltage	V_{IH}	0.7 DV_{DD18}	—	DV_{DD18}	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	GND	—	0.3 DV_{DD18}	V	
Hysteresis of Schmitt Trigger Inputs (All digital inputs)	V_{HYST}	—	0.05 DV_{DD18}	—	V	
Low-Level Output Voltage	V_{OL}	—	—	0.3	V	I_{OL} = -3 mA, all digital I/O pins
High-Level Output Voltage	V_{OH}	DV_{DD18} – 0.5	1.8	—	V	I_{OL} = + 3mA, all digital I/O pins
Digital Data Output (CMOS Mode)						
Maximum External Load Capacitance	C_{Load}	—	10	—	pF	From output pin to GND
Internal I/O Capacitance	C_{INT}	—	4	—	pF	**Note 5**
Digital Data Output (LVDS Mode)(5)						
LVDS High-Level Differential Output Voltage	V_{H_LVDS}	200	300	400	mV	100Ω differential termination, LVDS bias = 3.5 mA
LVDS Low-Level Differential Output Voltage	V_{L_LVDS}	-400	-300	-200	mV	100Ω differential termination, LVDS bias = 3.5 mA

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = Sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
LVDS Common-Mode Voltage	V_{CM_LVDS}	1	1.15	1.4	V	
Output Capacitance	C_{INT_LVDS}	—	4	—	pF	Internal capacitance from output pin to GND
Differential Load Resistance (LVDS)	R_{LVDS}	—	100	—	Ω	Across LVDS output pairs
Input Leakage Current on Digital I/O Pins						
Data Output Pins	I_{LI_DH}	—	—	+1	μA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-1	—	—	μA	V_{IL} = GND
I/O Pins except Data Output Pins	I_{LI_DH}	—	—	+6	μA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-35	—	—	μA	V_{IL} = GND(12)

Notes:

1. This 1.8V digital supply voltage is used for the digital I/O circuit, including SPI, CMOS and LVDS data output drivers.
2. Standby mode: Most of the internal circuits are turned-off except internal reference, clock, bias circuits and SPI interface.
3. Shutdown mode: All circuits, including reference and clock, are turned-off except the SPI interface.
4. Power dissipation is calculated by using the following equation.

   (a) During operation:

   $P_{DISS} = V_{DD18} \times (I_{DD\_A18} + I_{DD\_D18}) + V_{DD12} \times (I_{DD\_A12} + I_{DD\_D12})$, where I_{DD_D18} is the digital I/O current for LVDS or CMOS output. V_{DD18} = 1.8V and V_{DD12} = 1.2V are used for typical value calculation.

   (b) During Standby mode:

   $P_{DISS\_STANDBY} = (I_{STANDBY\_AN} + I_{STANDBY\_DIG}) \times 1.2V$

   (c) During Shutdown mode:

   $P_{DISS\_SHDN} = I_{DD\_SHDN} \times 1.2\ V$
5. This parameter is ensured by design, but not 100% tested in production.
6. This parameter is ensured by characterization, but not 100% tested in production.
7. See Table 4-1 for details.
8. Differential reference voltage output at REF+/REF- pins: $V_{REF} = V_{REF}+ - V_{REF}-$.
9. Input capacitance refers to the effective capacitance between differential input pin pair.
10. See Figure 4-8 for details of clock input circuit.
11. ENOB = (SINAD - 1.76)/6.02.
12. This leakage current is due to internal pull-up resistor.
13. R_{IN_SENSE} is calculated from SENSE pin to virtual ground at 0.55V for 400 mV < V_{SENSE} <800 mV. $R_{SENSE} = (V_{SENSE} - 0.55V)/I_{SENSE}$.
14. Dynamic performance is characterized with DIG_GAIN<7:0> = `0011-1000`.

TABLE 2-2: TIMING REQUIREMENTS – LVDS AND CMOS OUTPUTS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, DCLK_PHDLY_DLL<2:0> = 000, +25°C is applied for typical value.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Aperture Delay	t_A	—	1	—	ns	Note 1
Out-of-Range Recovery Time	t_{OVR}	—	1	—	Clocks	Note 1
Output Clock Duty Cycle		—	50	—	%	Note 1
Pipeline Latency	$T_{LATENCY}$	—	23	—	Clocks	Note 2, Note 4
System Calibration[1]						
Power-Up Calibration Time	T_{PCAL}	—	3×2^{26}	—	Clocks	First 3×2^{26} sample clocks after power-up
Background Calibration Update Rate	T_{BCAL}	—	2^{30}	—	Clocks	Per 2^{30} sample clocks after T_{PCAL}
$\overline{\text{RESET}}$ Low Time	T_{RESET}	5	—	—	ns	See Figure 2-6 for details[1]
LVDS Data Output Mode[1,5]						
Input Clock to Output Clock Propagation Delay	t_{CPD}	—	5.7	—	ns	
Output Clock to Data Propagation Delay	t_{DC}	—	0.5	—	ns	
Input Clock to Output Data Propagation Delay	t_{PD}	—	5.8	—	ns	
CMOS Data Output Mode[1]						
Input Clock to Output Clock Propagation Delay	t_{CPD}	—	3.8	—	ns	
Output Clock to Data Propagation Delay	t_{DC}	—	0.7	—	ns	
Input Clock to Output Data Propagation Delay	t_{PD}	—	4.5	—	ns	

Note 1: This parameter is ensured by design, but not 100% tested in production.
2: This parameter is ensured by characterization, but not 100% tested in production.
3: t_{RISE} = approximately less than 10% of duty cycle.
4: Output latency is measured without using decimation filter and digital down-converter options.
5: The time delay can be adjusted with the DCLK_PHDLY_DLL<2:0> setting.

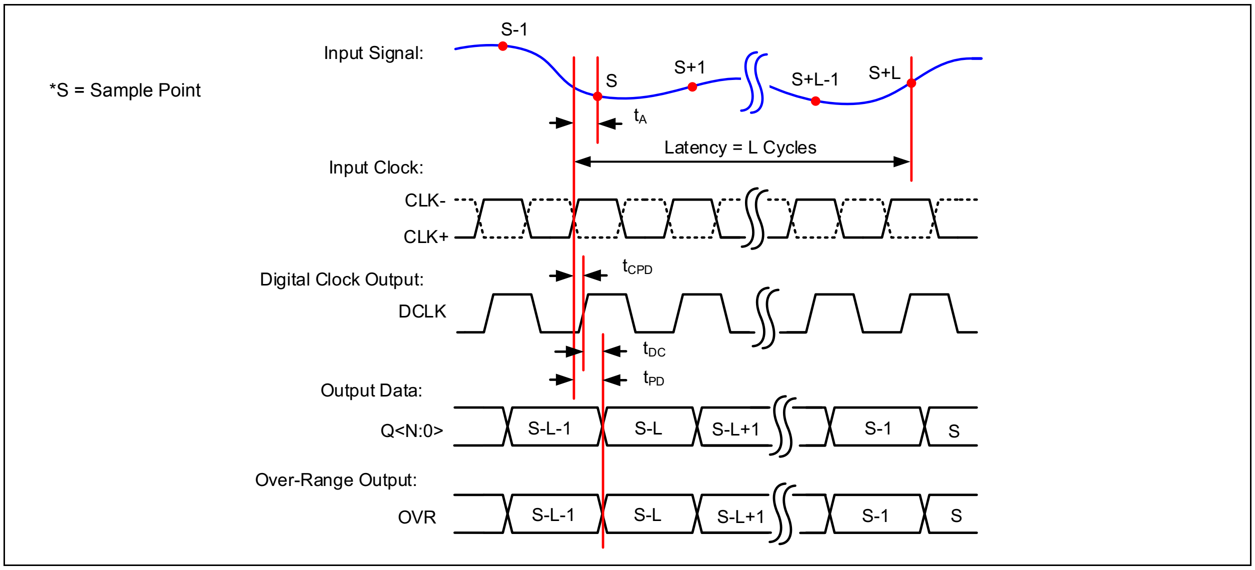


FIGURE 2-1: *Timing Diagram – CMOS Output.*

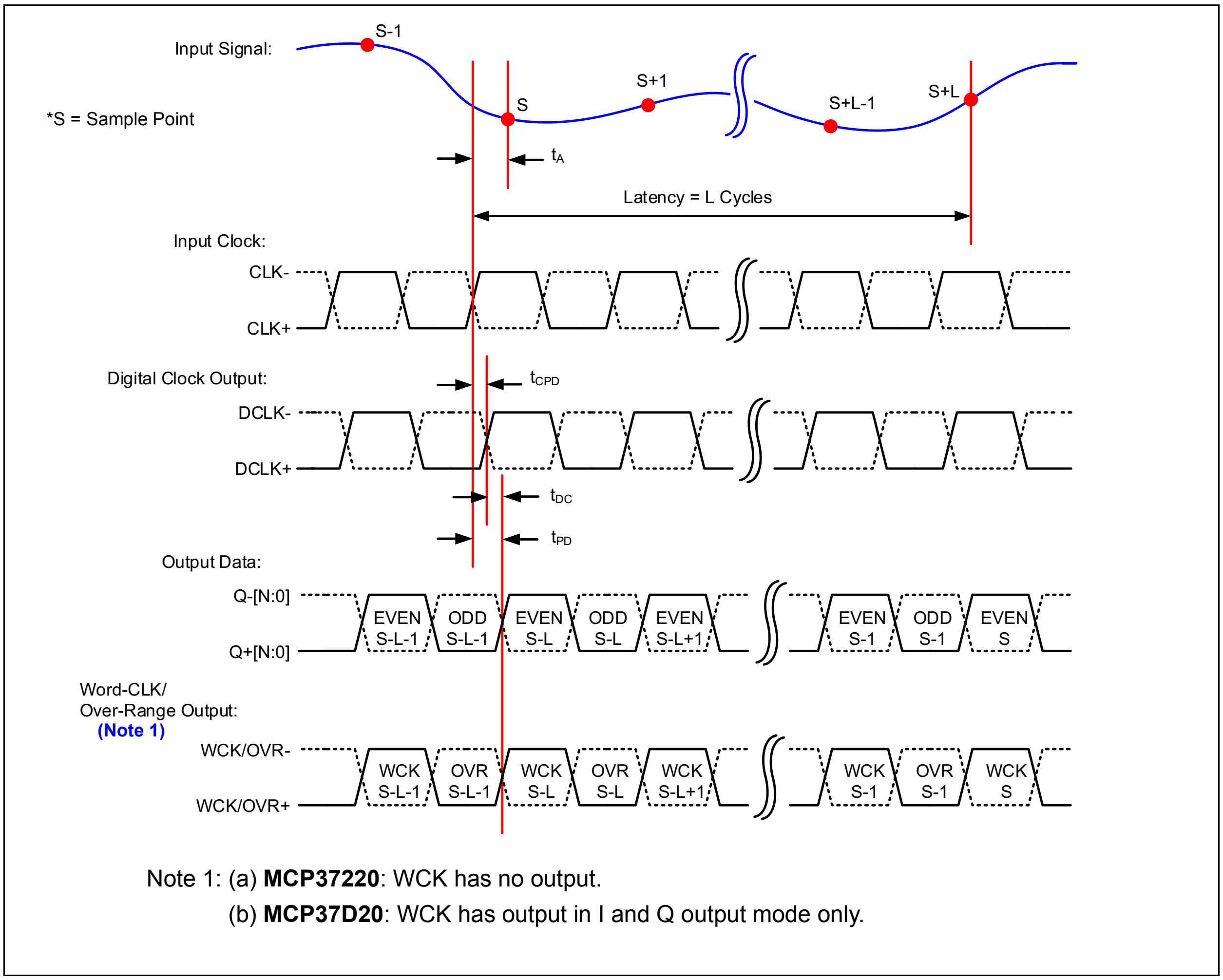


FIGURE 2-2: *Timing Diagram – LVDS Output with Even Bit First.*

TABLE 2-3: SPI SERIAL INTERFACE TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value. All timings are measured at 50%.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Serial Clock Frequency, f_{SCK} = 50 MHz						
$\overline{CS}$ Setup Time	t_{CSS}	10	—	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	20	—	—	ns	
$\overline{CS}$ Disable Time	t_{CSD}	20	—	—	ns	
Data Setup Time	t_{SU}	2	—	—	ns	
Data Hold Time	t_{HD}	4	—	—	ns	
Serial Clock High Time	t_{HI}	8	—	—	ns	
Serial Clock Low Time	t_{LO}	8	—	—	ns	**Note 1**
Serial Clock Delay Time	t_{CLD}	20	—	—	ns	
Serial Clock Enable Time	t_{CLE}	20	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	20	ns	
Output Disable Time	t_{DIS}	—	—	10	ns	**Note 1**

Note 1: This parameter is ensured by design, but not 100% tested in production.

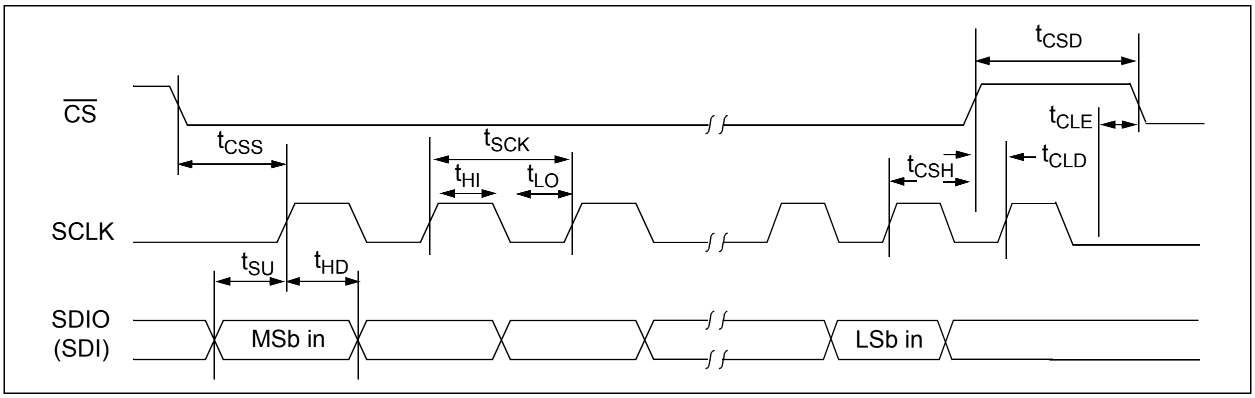


FIGURE 2-3: *SPI Serial Input Timing Diagram.*

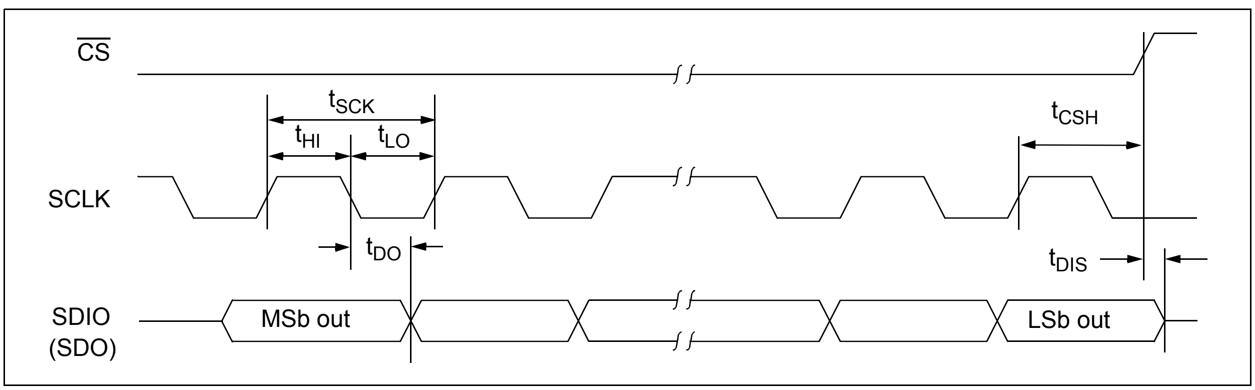


FIGURE 2-4: *SPI Serial Output Timing Diagram.*

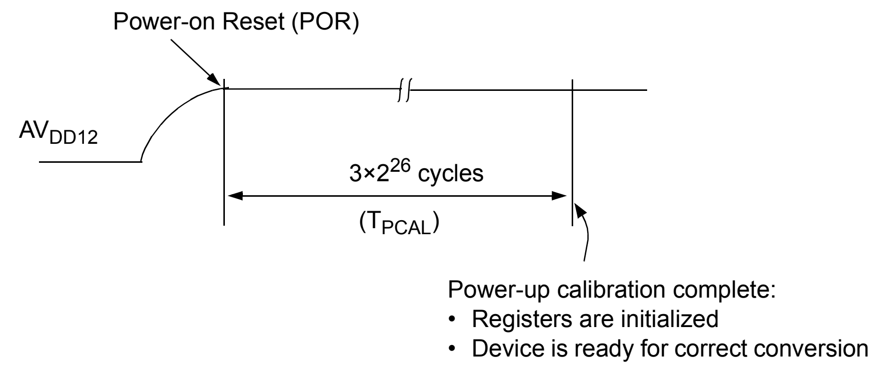


FIGURE 2-5: *POR-Related Events: Register Initialization and Power-Up Calibration.*

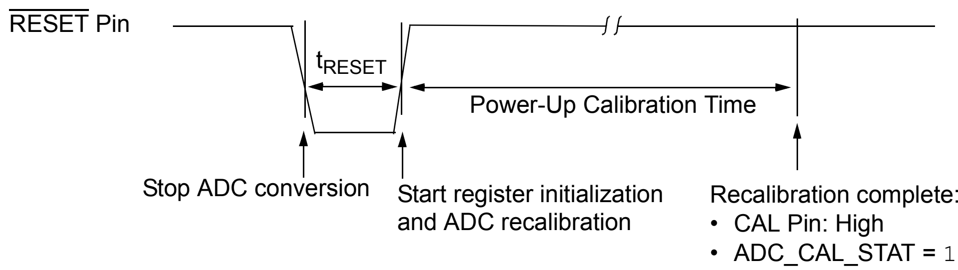


FIGURE 2-6: *$\overline{\text{RESET}}$ Pin Timing Diagram.*

TABLE 2-4: TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters		Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges(1)							
Operating Temperature Range		T_A	-40	—	+85	°C	
Thermal Package Resistances(2)							
121L Ball-TFBGA (8 mm x 8 mm)	Junction-to-Ambient Thermal Resistance	θ_{JA}	—	40.2	—	°C/W	
	Junction-to-Case Thermal Resistance	θ_{JC}	—	8.4	—	°C/W	
124L VTLA (9 mm x 9 mm)	Junction-to-Ambient Thermal Resistance	θ_{JA}	—	21	—	°C/W	
	Junction-to-Case (top) Thermal Resistance	θ_{JC}	—	8.7	—	°C/W	

Note 1: Maximum allowed power dissipation (P_{DMAX}) = (T_{JMAX} – T_A)/θ_{JA}.
2: This parameter value is achieved by package simulations.

NOTES:

3.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, $AV_{DD18} = DV_{DD18}$ = 1.8V, $AV_{DD12} = DV_{DD12}$ = 1.2V, GND = 0V, SENSE = AV_{DD12}, Differential Analog Input (A_{IN}) = sine wave with amplitude of -1 dBFS, f_{IN} = 70 MHz, Clock Input = 200 MHz, f_S = 200 Msps, PLL and decimation filters are disabled, DIG_GAIN<7:0> = `0011-1000`.

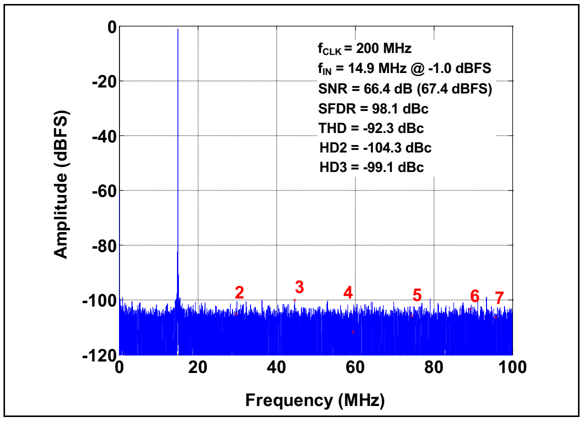


FIGURE 3-1: *FFT for 14.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -1 dBFS.*

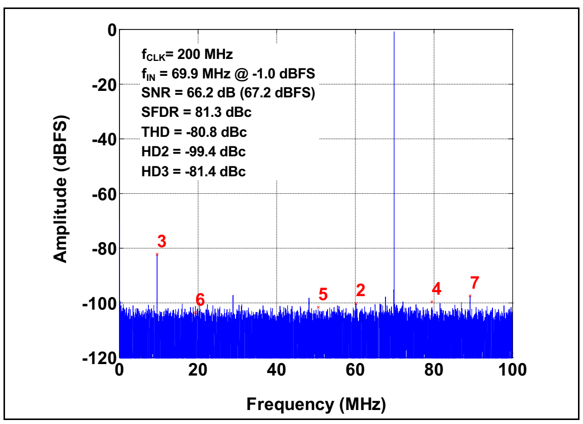


FIGURE 3-2: *FFT for 69.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -1 dBFS.*

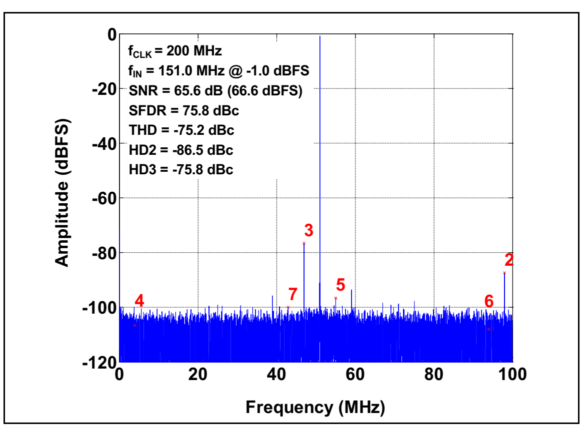


FIGURE 3-3: *FFT for 151 MHz Input Signal: f_S = 200 Msps, A_{IN} = -1 dBFS.*

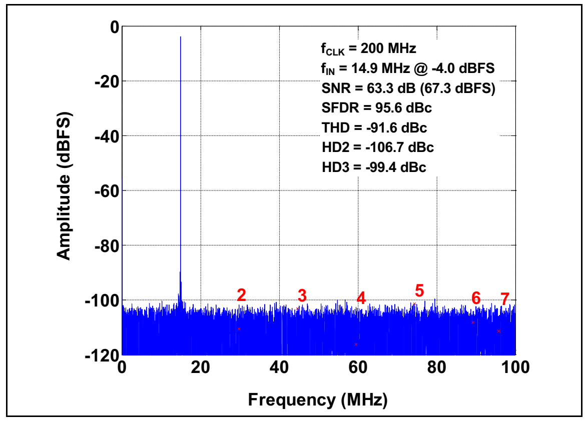


FIGURE 3-4: *FFT for 14.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -4 dBFS.*

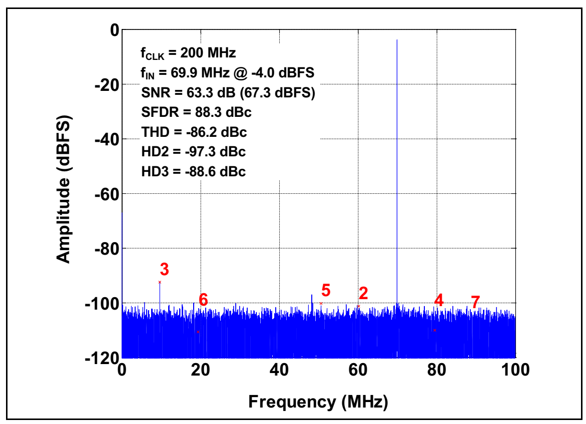


FIGURE 3-5: *FFT for 69.9 MHz Input Signal: f_S = 200 Msps, A_{IN} = -4 dBFS.*

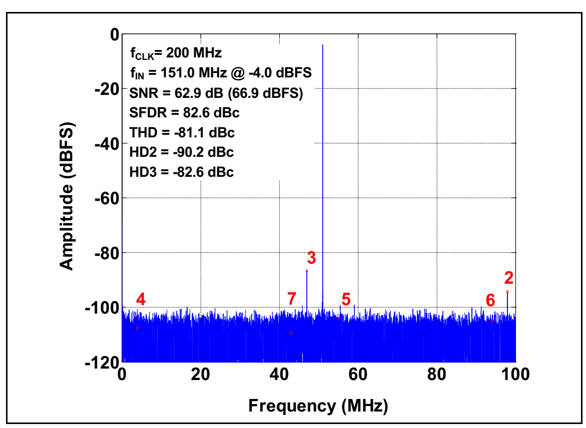


FIGURE 3-6: *FFT for 151 MHz Input Signal: f_S = 200 Msps, A_{IN} = -4 dBFS.*