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MCP3901

Two-Channel Analog Front End

Features

- Two Synchronous Sampling 16/24-bit Resolution Delta-Sigma A/D Converters with Proprietary Multi-Bit Architecture
- 91 dB SINAD, -104 dBc Total Harmonic Distortion (THD) (up to 35th harmonic), 109 dB Spurious-free Dynamic Range (SFDR) for Each Channel
- Programmable Data Rate up to 64 ksps
- Ultra Low-Power Shutdown mode with <2 µA
- -133 dB Crosstalk Between the Two Channels
- Low Drift Internal Voltage Reference: 12 ppm/°C
- Differential Voltage Reference Input Pins
- High Gain PGA on Each Channel (up to 32 V/V)
- Phase Delay Compensation Between the Two Channels with 1 µs time Resolution
- Separate Modulator Outputs for Each Channel
- High-Speed, Addressable 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Independent Analog and Digital Power Supplies: 4.5V-5.5V AV_{DD}, 2.7V-5.5V DV_{DD}
- Low-Power Consumption: (14 mW typical at 5V)
- Available in Small 20-lead SSOP and QFN Packages
- Industrial Temperature Ranges:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

Applications

- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring

Description

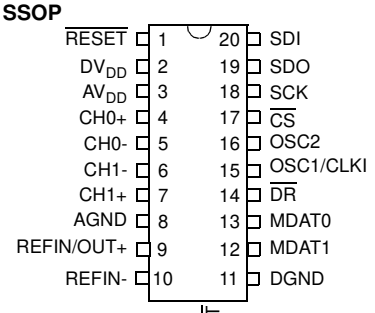
The MCP3901 is a dual channel Analog Front End (AFE) containing two synchronous sampling Delta-Sigma Analog-to-Digital Converters (ADC), two PGAs, phase delay compensation block internal voltage reference, modulator output block, and high-speed 20 MHz SPI compatible serial interface. The converters contain a proprietary dithering algorithm for reduced Idle tones and improved THD.

The internal register map contains 24-bit wide ADC data words, a modulator output byte, as well as six writable control registers to program gain, oversampling ratio, phase, resolution, dithering, shutdown, Reset and several communication features. The communication is largely simplified with various Continuous Read modes that can be accessed by the Direct Memory Access (DMA) of an MCU and with a separate data ready pin that can be connected directly to an Interrupt Request (IRQ) input of an MCU.

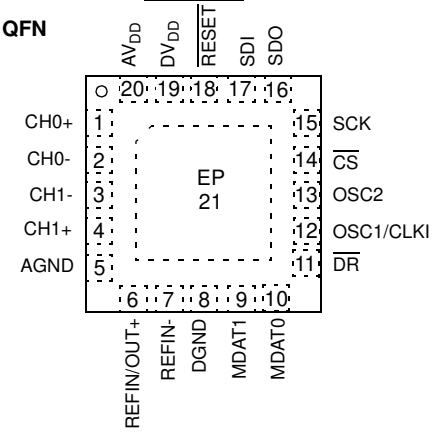
The MCP3901 is capable of interfacing to a large variety of voltage and current sensors, including shunts, current transformers, Rogowski coils and Hall-effect sensors.

Package Type

20-Lead SSOP

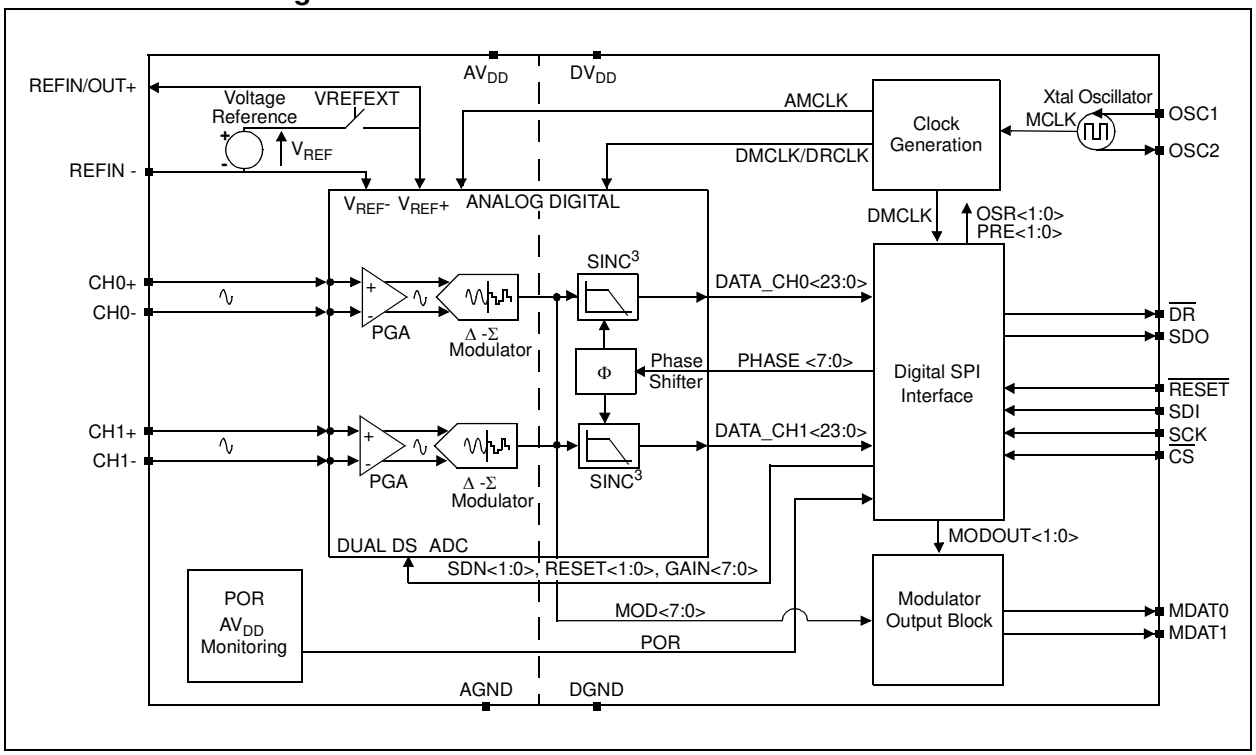


20-Lead QFN



* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} 7.0V
Digital inputs and outputs w.r.t. A_{GND}..... -0.6V to V_{DD} +0.6V
Analog input w.r.t. A_{GND} ....-6V to +6V
V_{REF} input w.r.t. A_{GND} ..... -0.6V to V_{DD} +0.6V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) .....7.0 kV, 400V
ESD on all other pins (HBM,MM) .....7.0 kV, 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 5.5V; -40°C < T_A < +85°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS = 333 mV_{RMS} @ 50/60 Hz

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	2.37	+2%	V	VREFEXT = 0
Temperature Coefficient	TC_{REF}	—	12	—	ppm/°C	VREFEXT = 0
Output Impedance	$ZOUT_{REF}$	—	7	—	kΩ	AV_{DD} = 5V, VREFEXT = 0
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Differential Input Voltage Range (V_{REF+} – V_{REF-})	V_{REF}	2.2	—	2.6	V	V_{REF} = (V_{REF+} – V_{REF-}), VREFEXT = 1
Absolute Voltage on REFIN+ Pin	V_{REF+}	1.9	—	2.9	V	VREFEXT = 1
Absolute Voltage on REFIN- Pin	V_{REF-}	-0.3	—	0.3	V	
ADC Performance						
Resolution (No Missing Codes)		24	—	—	bits	OSR = 256 (See Table 5-3)
Sampling Frequency	f_S	See Table 4-2			kHz	f_S = DMCLK = MCLK/ (4 x PRESCALE)

Note 1: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance is specified at -0.5 dB below the maximum signal range, V_{IN} = -0.5 dBFS @ 50/60 Hz = 353 mV_{RMS}, V_{REF} = 2.4V.

2: See terminology section for definition.

3: This parameter is established by characterization and not 100% tested.

4: For these operating currents, the following bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

5: For these operating currents, the following Configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

6: Applies to all gains. Offset error is dependant on PGA gain setting (see Figure 2-19 for typical values).

7: Outside of this range, the ADC accuracy is not specified. An extended input range of ±6V can be applied continuously to the part with no risk for damage.

8: For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz, AMCLK = MCLK/PRESCALE. When using a crystal, the CLKEXT bit should be equal to '0'.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 5.5V; -40°C < T_A < +85°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS = 333 mV_{RMS} @ 50/60 Hz

Parameters	Symbol	Min	Typical	Max	Units	Conditions
Output Data Rate	f_D	See Table 4-2			ksps	f_D = DRCLK = DMCLK/ OSR = MCLK/ (4 x PRESCALE x OSR)
Analog Input Absolute Voltage on CH0+, CH0-, CH1+, CH1- Pins	CHn+	-1	—	+1	V	All analog input channels, measured to AGND **(Note 7)**
Analog Input Leakage Current	A_{IN}	—	1	—	nA	**(Note 4)**
		—	2	—	nA	-40°C < T_A < 125°C
Differential Input Voltage Range	(CHn+ – CHn-)	—	—	500/GAIN	mV	**(Note 1)**
Offset Error **(Note 2)**	V_{OS}	-3	—	+3	mV	**(Note 6)**
Offset Error Drift		—	3	—	µV/°C	From -40°C to +125°C
Gain Error **(Note 2)**	GE	—	-0.4	—	%	G = 1
		-2.5	—	+2.5	%	All Gains
Gain Error Drift		—	1	—	ppm/°C	From -40°C to +125°C
Integral Nonlinearity **(Note 2)**	INL	—	15	—	ppm	GAIN = 1, DITHER = On
Input Impedance	Z_{IN}	350	—	—	kΩ	Proportional to 1/AMCLK
Signal-to-Noise and Distortion Ratio **(Notes 2, 3)**	SINAD	89	91	—	dB	OSR = 256, DITHER = On
		78	79	—	dB	
Total Harmonic Distortion **(Notes 2, 3)**	THD	—	-104	-102	dB	OSR = 256, DITHER = On
		—	-85	-84	dB	
Signal-to-Noise Ratio **(Notes 2, 3)**	SNR	89	91	—	dB	OSR = 256, DITHER = On
		80	81	—	dB	
Spurious Free Dynamic Range **(Note 2)**	SFDR	—	109	—	dB	OSR = 256, DITHER = On
		—	87	—	dB	
Crosstalk (50/60 Hz) **(Note 2)**	CTALK	—	-133	—	dB	OSR = 256, DITHER = On

Note 1: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance is specified at -0.5 dB below the maximum signal range, V_{IN} = -0.5 dBFS @ 50/60 Hz = 353 mV_{RMS}, V_{REF} = 2.4V.

2: See terminology section for definition.

3: This parameter is established by characterization and not 100% tested.

4: For these operating currents, the following bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

5: For these operating currents, the following Configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

6: Applies to all gains. Offset error is dependant on PGA gain setting (see Figure 2-19 for typical values).

7: Outside of this range, the ADC accuracy is not specified. An extended input range of ±6V can be applied continuously to the part with no risk for damage.

8: For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz, AMCLK = MCLK/PRESCALE. When using a crystal, the CLKEXT bit should be equal to '0'.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 5.5V; -40°C < T_A < +85°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS = 333 mV_{RMS} @ 50/60 Hz

Parameters	Symbol	Min	Typical	Max	Units	Conditions
AC Power Supply Rejection	AC PSRR	—	-77	—	dB	AV_{DD} and DV_{DD} = 5V + 1 V_{PP} @ 50/60 Hz
DC Power Supply Rejection	DC PSRR	—	-77	—	dB	AV_{DD} and DV_{DD} = 4.5 to 5.5V
DC Common-Mode Rejection Ratio (**Note 2**)	CMRR	—	-72	—	dB	V_{CM} varies from -1V to +1V
Oscillator Input						
Master Clock Frequency Range	MCLK	1	—	16.384	MHz	(**Note 8**)
Power Specifications						
Operating Voltage, Analog	AV_{DD}	4.5	—	5.5	V	
Operating Voltage, Digital	DV_{DD}	2.7	3.6	5.5	V	
Power On Reset Threshold	POR	—	4.2	—	V	(**Note 3**)
		—	4.6	—		-40°C < T_A < 125°C, (**Note 3**)
Operating Current, Analog (**Note 4**)	AI_{DD}	—	2.1	2.8	mA	BOOST<1:0> = 00
		—	2.1	3.3	mA	-40°C < T_A < 125°C, BOOST<1:0> = 00
		—	3.8	5.6	mA	BOOST<1:0> = 11
		—	3.8	7	mA	-40°C < T_A < 125°C, BOOST<1:0> = 11
Operating Current, Digital	DI_{DD}	—	0.45	1.0	mA	DV_{DD} = 5V, MCLK = 4 MHz
		—	0.25	0.45	mA	DV_{DD} = 2.7V, MCLK = 4 MHz
		—	1.2	1.6	mA	DV_{DD} = 5V, MCLK = 8.192 MHz
Shutdown Current, Analog	$I_{DDS,A}$	—	—	1	µA	AV_{DD} pin only (**Note 5**)
Shutdown Current, Digital	$I_{DDS,D}$	—	—	1	µA	DV_{DD} pin only (**Note 5**)

Note 1: This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic performance is specified at -0.5 dB below the maximum signal range, V_{IN} = -0.5 dBFS @ 50/60 Hz = 353 mV_{RMS}, V_{REF} = 2.4V.

2: See terminology section for definition.

3: This parameter is established by characterization and not 100% tested.

4: For these operating currents, the following bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

5: For these operating currents, the following Configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

6: Applies to all gains. Offset error is dependant on PGA gain setting (see Figure 2-19 for typical values).

7: Outside of this range, the ADC accuracy is not specified. An extended input range of ±6V can be applied continuously to the part with no risk for damage.

8: For proper operation and to keep ADC accuracy, AMCLK should always be in the range of 1 to 5 MHz with BOOST bits off. With BOOST bits on, AMCLK should be in the range of 1 to 8.192 MHz, AMCLK = MCLK/PRESCALE. When using a crystal, the CLKEXT bit should be equal to '0'.

SERIAL INTERFACE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply: AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 5.5V, -40°C < T_A < +85°C, C_{LOAD} = 30 pF

Parameters	Sym	Min	Typ	Max	Units	Conditions
Serial Clock Frequency	f_{SCK}	— —	— —	20 10	MHz MHz	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} < 5.5
$\overline{CS}$ Setup Time	t_{CSS}	25 50	— —	— —	ns ns	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} ≤ 5.5
$\overline{CS}$ Hold Time	t_{CSH}	50 100	— —	— —	ns ns	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} < 5.5
$\overline{CS}$ Disable Time	t_{CSD}	50	—	—	ns	
Data Setup Time	t_{SU}	5 10	— —	— —	ns ns	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} < 5.5
Data Hold Time	t_{HD}	10 20	— —	— —	ns ns	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} < 5.5
Serial Clock High Time	t_{HI}	20 50	— —	— —	ns ns	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} < 5.5
Serial Clock Low Time	t_{LO}	20 50	— —	— —	ns ns	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} < 5.5
Serial Clock Delay Time	t_{CLD}	50	—	—	ns	
Serial Clock Enable Time	t_{CLE}	50	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	50	ns	2.7 ≤ DV_{DD} < 5.5
Modulator Output Valid from AMCLK High	t_{DOMDAT}	—	—	1/2 * AMCLK	s	
Output Hold Time	t_{HO}	0	—	—	ns	**(Note 1)**
Output Disable Time	t_{DIS}	— —	— —	25 50	ns ns	4.5 ≤ DV_{DD} ≤ 5.5 2.7 ≤ DV_{DD} < 5.5 **(Note 1)**
Reset Pulse Width ($\overline{RESET}$)	t_{MCLR}	100	—	—	ns	2.7 ≤ DV_{DD} < 5.5
Data Transfer Time to $\overline{DR}$ (data ready)	t_{DODR}	—	—	50	ns	2.7 ≤ DV_{DD} < 5.5
Data Ready Pulse Low Time	t_{DRP}	—	1/DMCLK	—	µs	2.7 ≤ DV_{DD} < 5.5
Schmitt Trigger High-Level Input Voltage	V_{IH1}	.7 DV_{DD}	—	DV_{DD} + 1	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL1}	-0.3	—	0.2 DV_{DD}	V	
Hysteresis of Schmitt Trigger Inputs (all digital inputs)	V_{HYS}	300	—	—	mV	
Low-Level Output Voltage, SDO Pin	V_{OL}	—	—	0.4	V	SDO pin only, I_{OL} = +2.0 mA, V_{DD} = 5.0V
Low-level output voltage, $\overline{DR}$ and MDAT Pins	V_{OL}	—	—	0.4	V	$\overline{DR}$ and MDAT pins only, I_{OL} = +800 mA, V_{DD} = 5.0V
High-level output voltage, SDO pin	V_{OH}	DV_{DD} – 0.5	—	—	V	SDO pin only, I_{OH} = -2.0 mA, V_{DD} = 5.0V
High-level output voltage, $\overline{DR}$ and MDAT pins	V_{OH}	DV_{DD} – 0.5	—	—	V	$\overline{DR}$ and MDAT pins only, I_{OH} = -800 µA, V_{DD} = 5.0V
Input leakage current	I_{LI}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{IN} = DGND or DV_{DD}
Output leakage current	I_{LO}	—	—	±1	µA	$\overline{CS}$ = DV_{DD}, V_{OUT} = DGND or DV_{DD}
Internal capacitance (all inputs and outputs)	C_{INT}	—	—	7	pF	T_A = 25°C, SCK = 1.0 MHz, DV_{DD} = 5.0V **(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 4.5 to 5.5V, DV_{DD} = 2.7 to 5.5V

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	(Note 1)
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 20L SSOP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 20L QFN	θ_{JA}	—	43	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

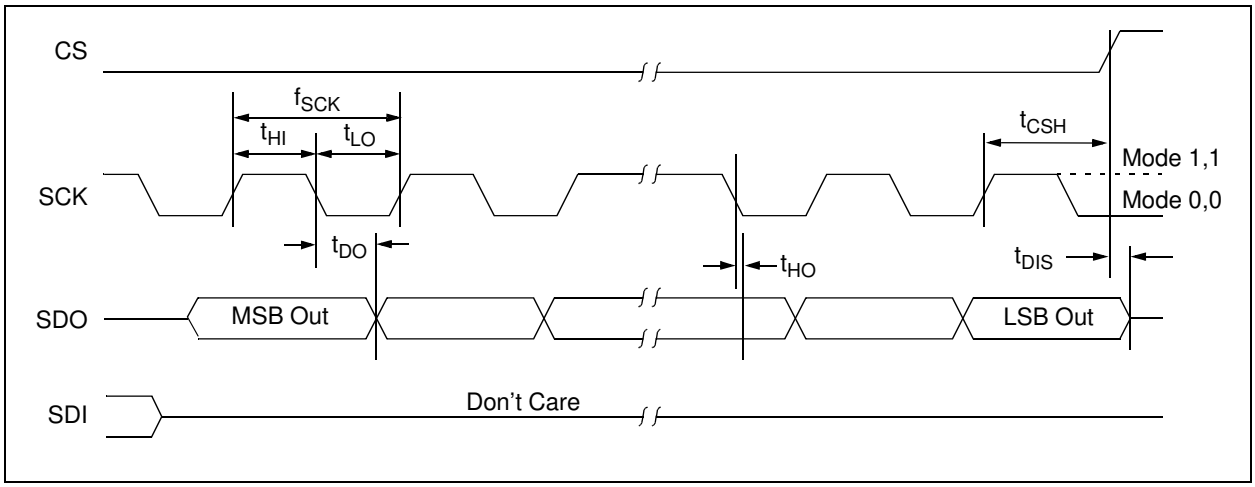


FIGURE 1-1: *Serial Output Timing Diagram.*

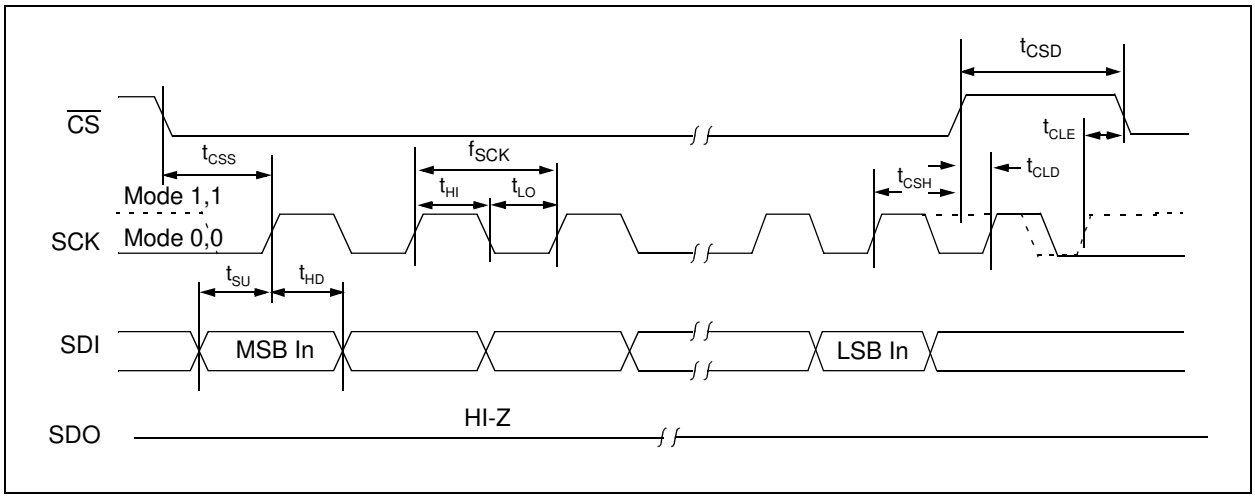


FIGURE 1-2: *Serial Input Timing Diagram.*

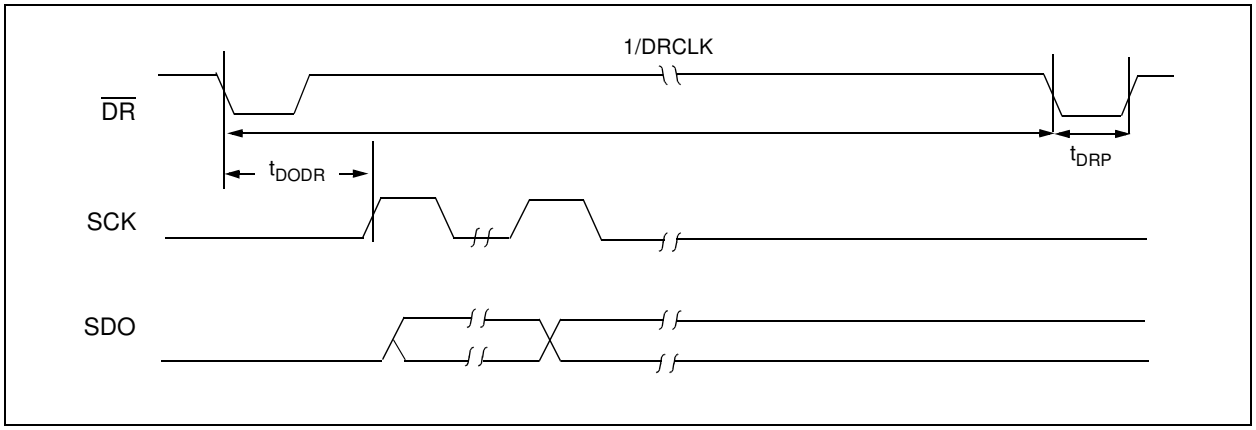


FIGURE 1-3: *Data Ready Pulse Timing Diagram.*

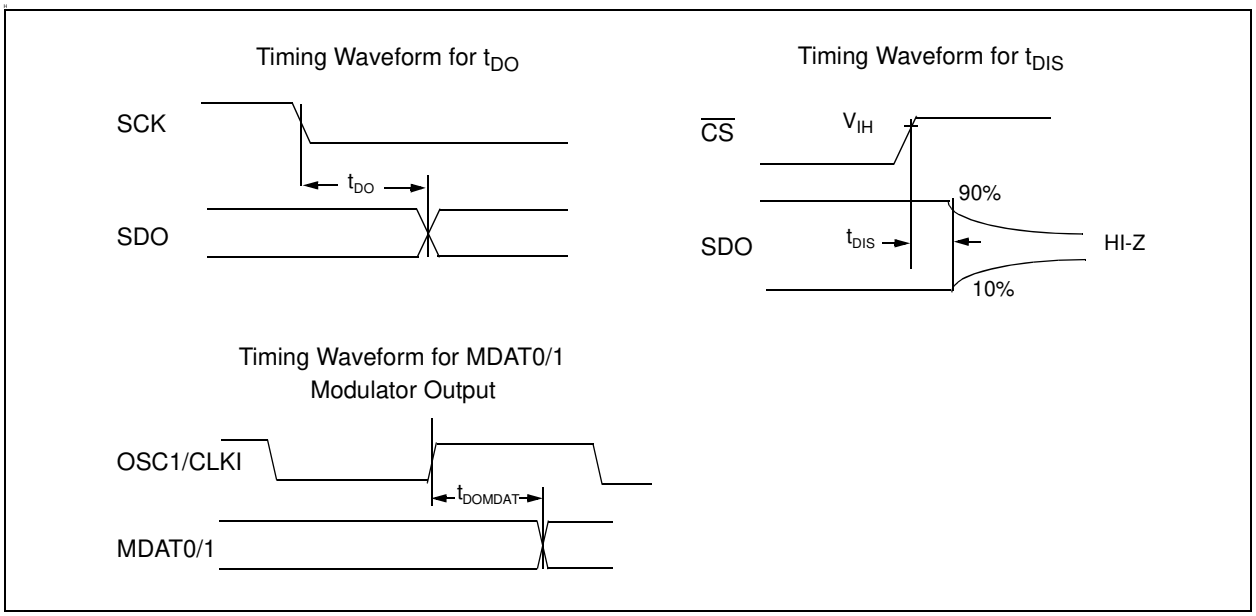


FIGURE 1-4: *Specific Timing Diagrams.*

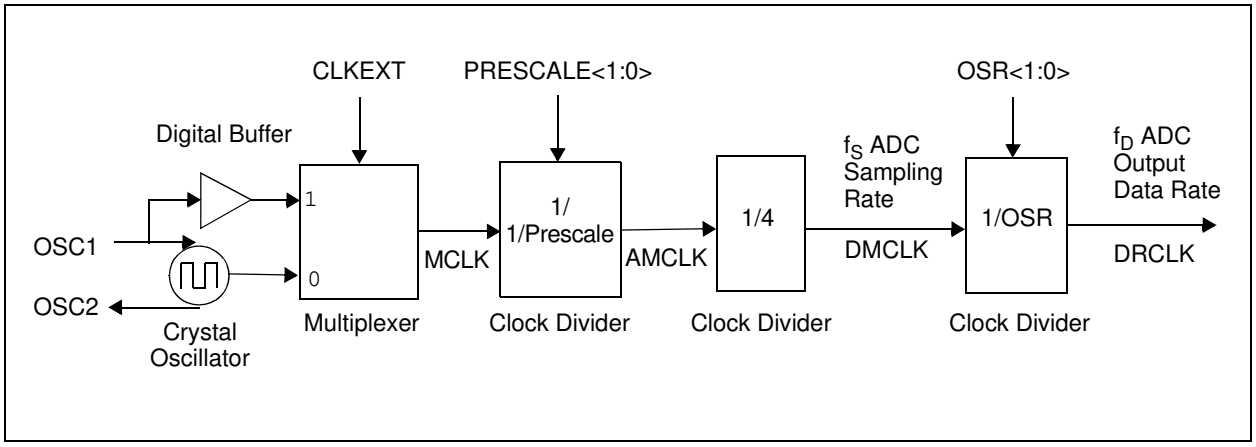


FIGURE 1-5: *MCP3901 Clock Detail.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 5.0V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

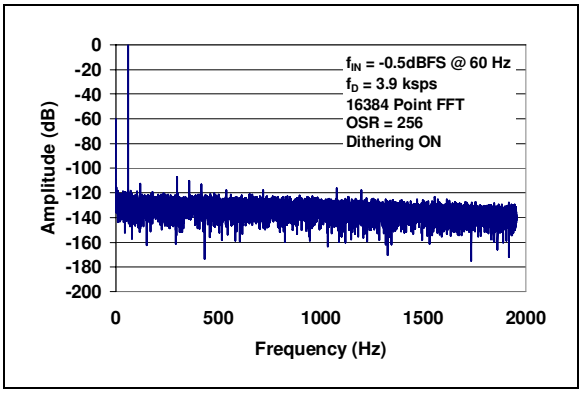


FIGURE 2-1: *Spectral Response.*

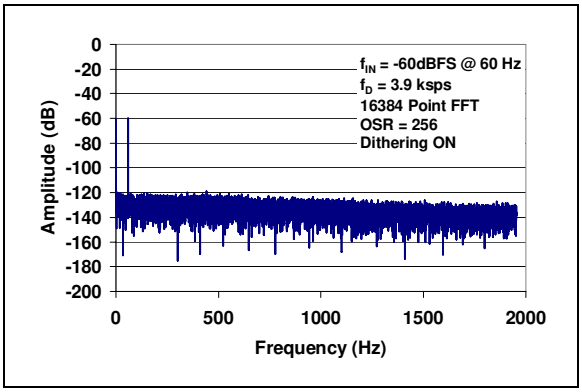


FIGURE 2-2: *Spectral Response.*

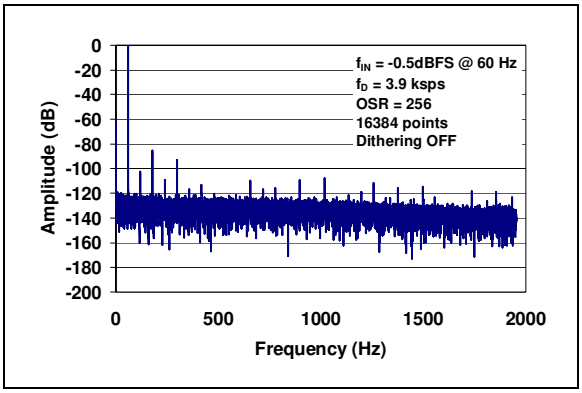


FIGURE 2-3: *Spectral Response.*

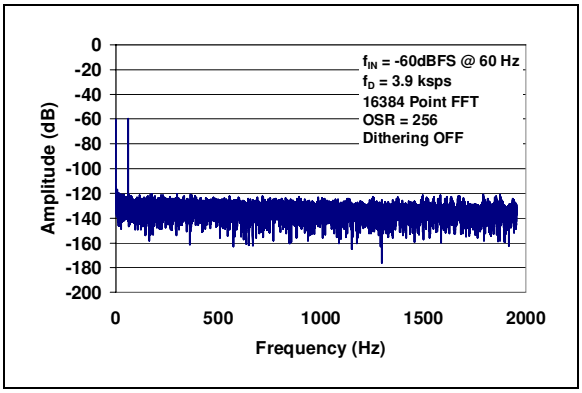


FIGURE 2-4: *Spectral Response.*

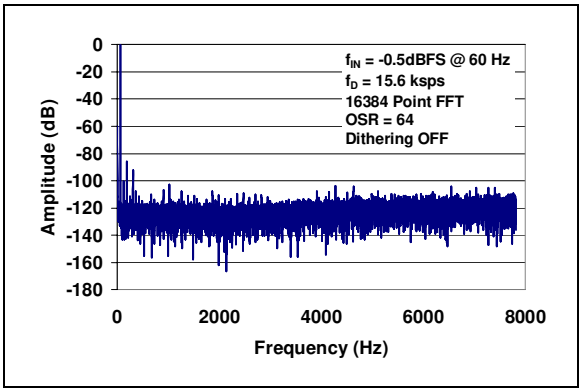


FIGURE 2-5: *Spectral Response.*

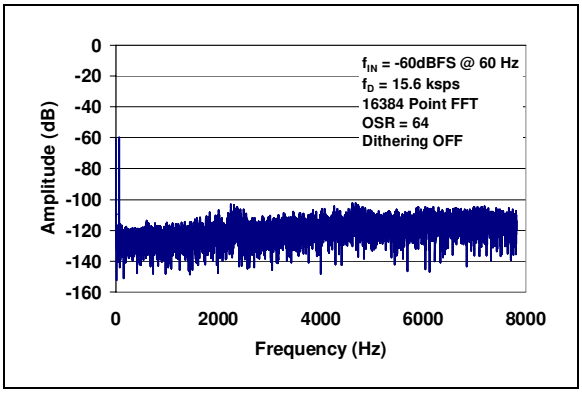


FIGURE 2-6: *Spectral Response.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 5.0V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

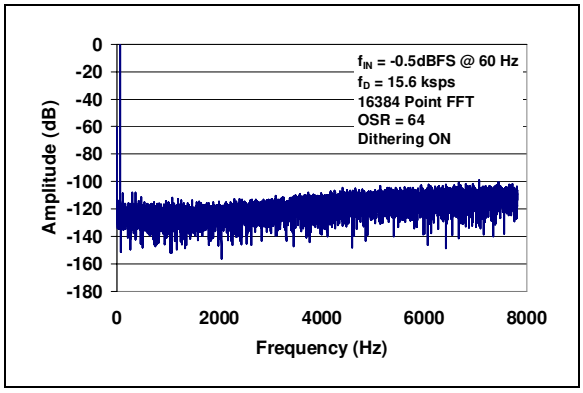


FIGURE 2-7: *Spectral Response.*

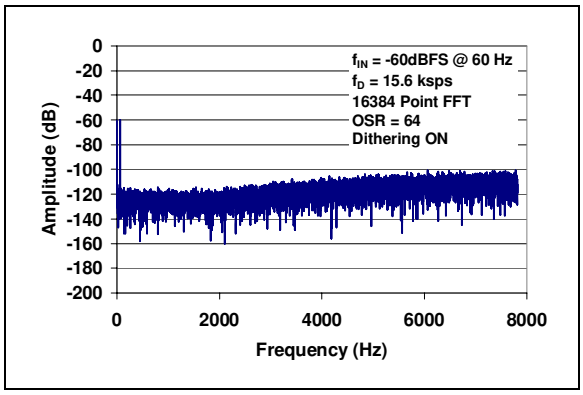


FIGURE 2-8: *Spectral Response.*

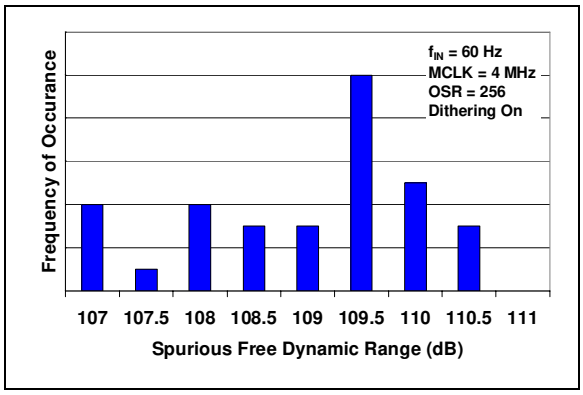


FIGURE 2-9: *Spurious Free Dynamic Range Histogram.*

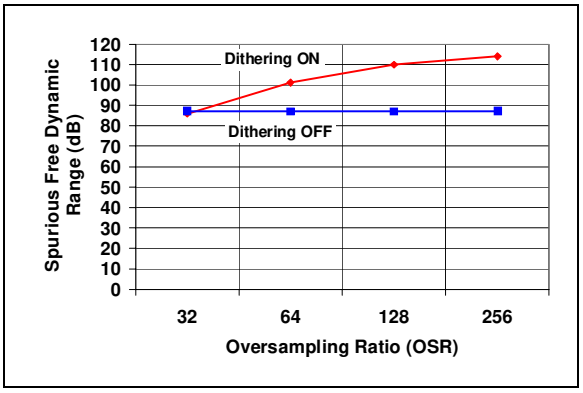


FIGURE 2-10: *Spurious Free Dynamic Range vs. Oversampling Ratio.*

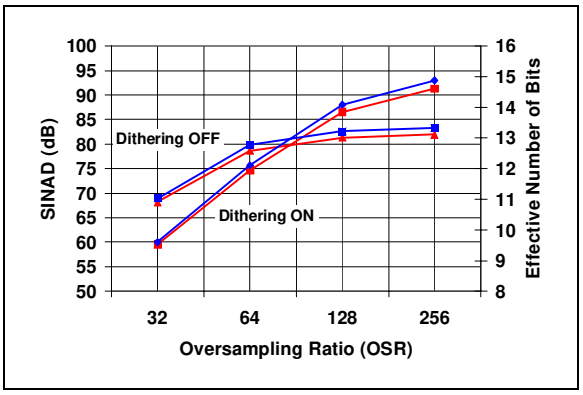


FIGURE 2-11: *Signal-to-Noise and Distortion and Effective Number of Bits vs. Oversampling Ratio.*

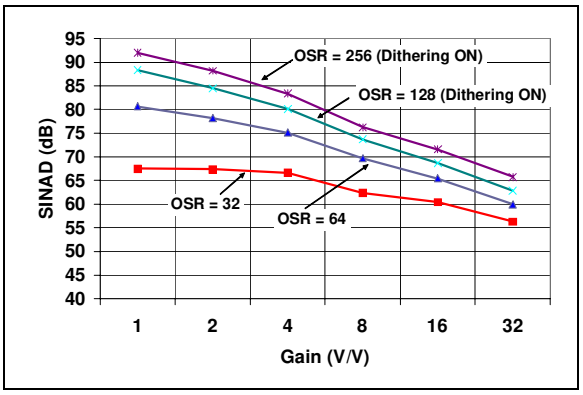


FIGURE 2-12: *Signal-to-Noise and Distortion vs. Gain.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 5.0V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

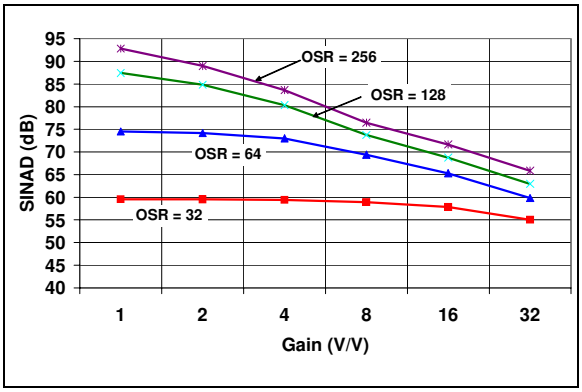


FIGURE 2-13: *Signal-to-Noise and Distortion vs. Gain (Dithering On).*

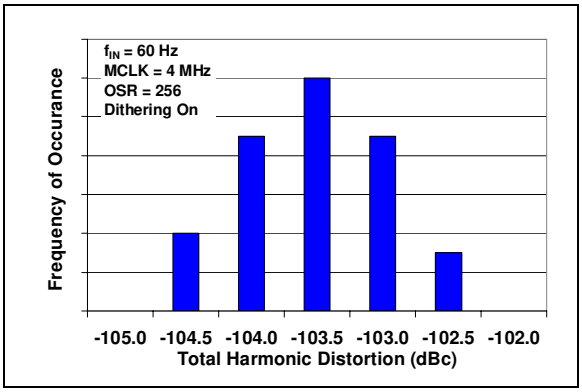


FIGURE 2-16: *Total Harmonic Distortion Histogram (Dithering On).*

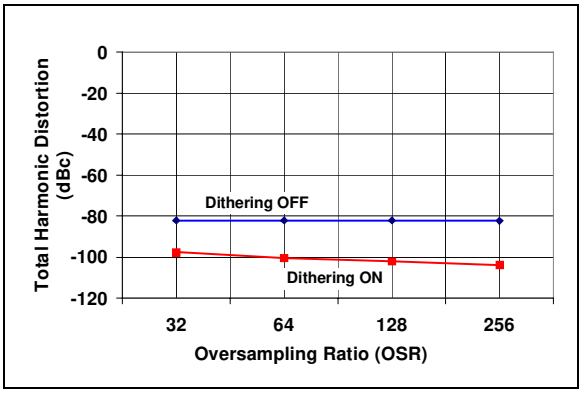


FIGURE 2-14: *Total Harmonic Distortion vs. Oversampling Ratio.*

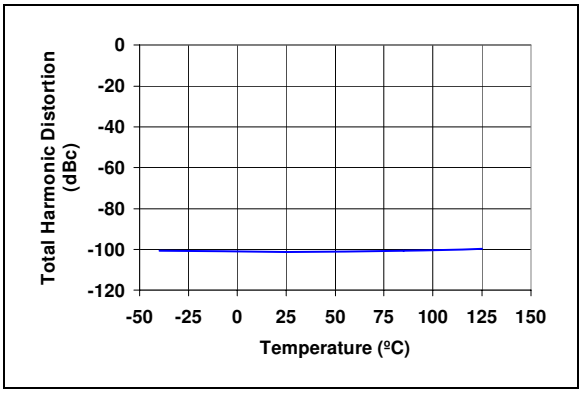


FIGURE 2-17: *Total Harmonic Distortion vs. Temperature.*

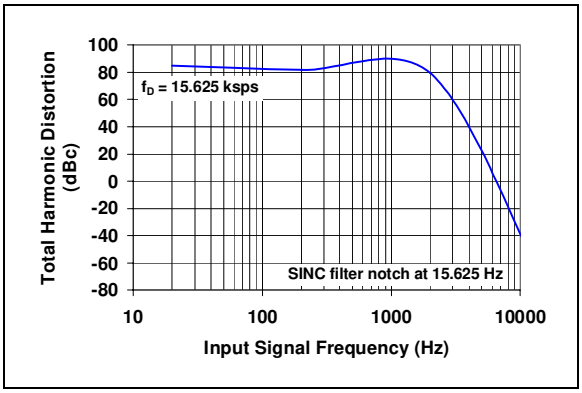


FIGURE 2-15: *Total Harmonic Distortion vs. Input Signal Frequency.*

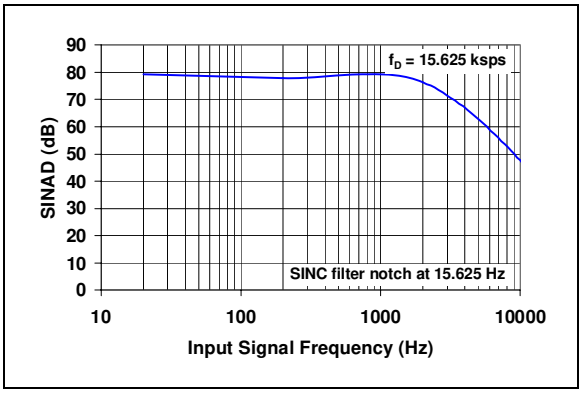


FIGURE 2-18: *Signal-to-Noise and Distortion vs. Input Frequency.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 5.0V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

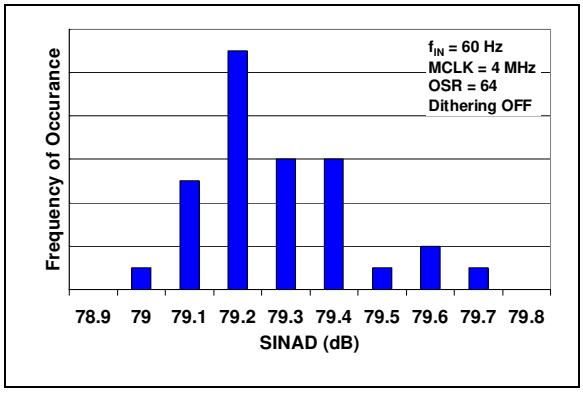


FIGURE 2-19: *Signal-to-Noise and Distortion Histogram.*

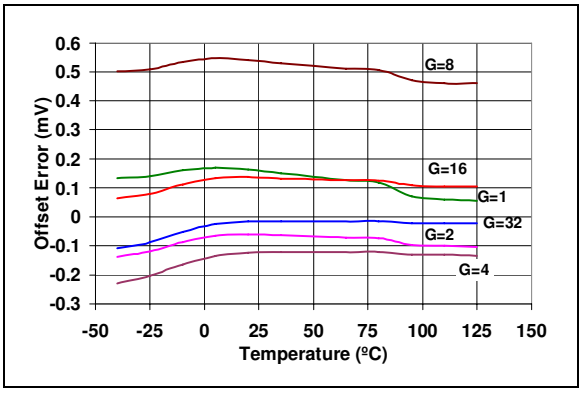


FIGURE 2-22: *Channel 0 Offset vs. Temperature.*

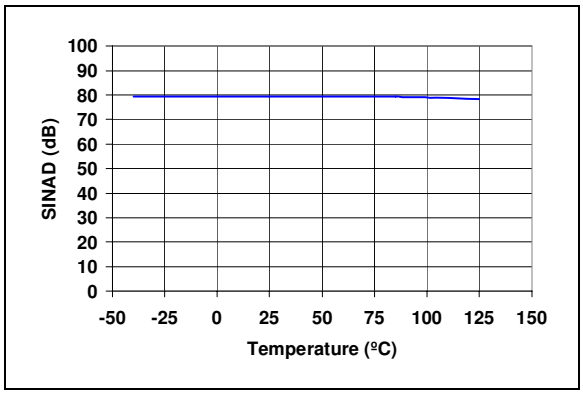


FIGURE 2-20: *Signal-to-Noise and Distortion vs. Temperature.*

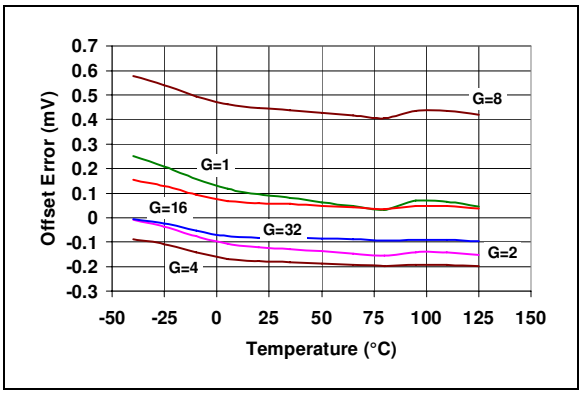


FIGURE 2-23: *Channel 1 Offset vs. Temperature.*

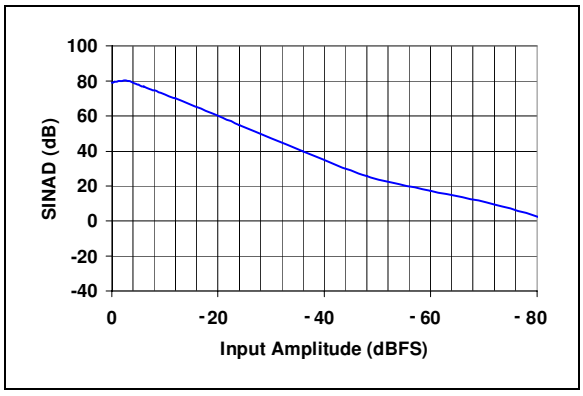


FIGURE 2-21: *Signal-to-Noise and Distortion vs. Input Signal Amplitude.*

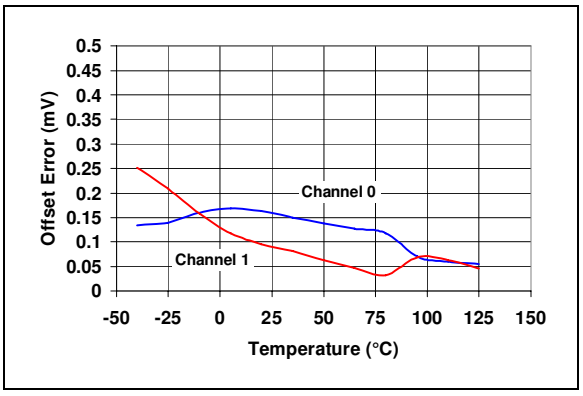


FIGURE 2-24: *Channel-to-Channel Offset Match vs. Temperature.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 5.0V; T_A = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

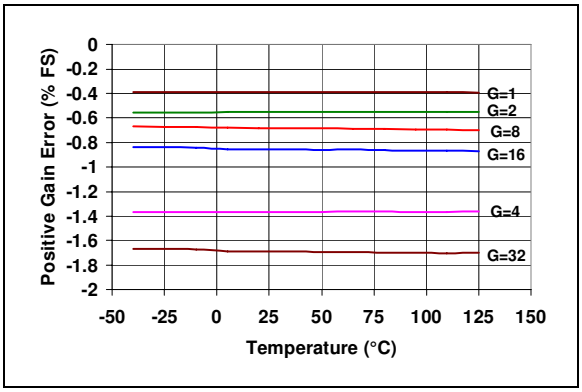


FIGURE 2-25: *Positive Gain Error vs. Temperature.*

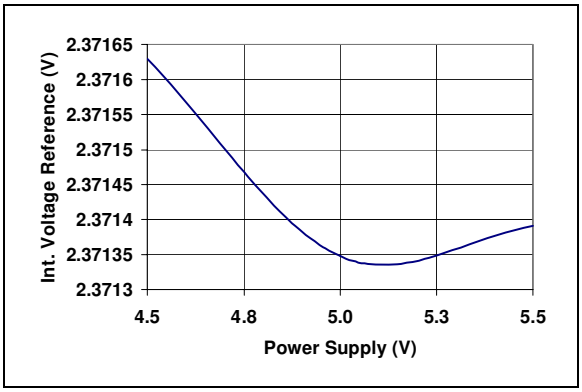


FIGURE 2-28: *Internal Voltage Reference vs. Supply Voltage.*

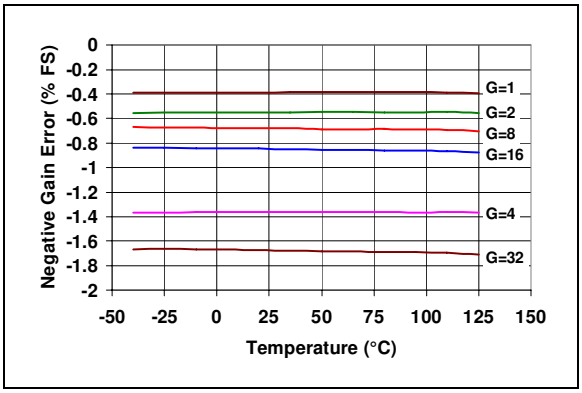


FIGURE 2-26: *Negative Gain Error vs. Temperature*

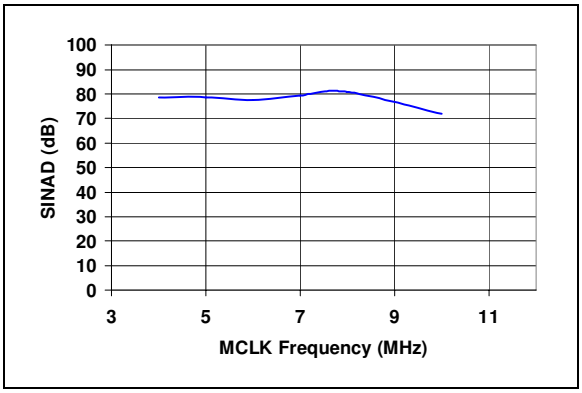


FIGURE 2-29: *Signal-to-Noise and Distortion vs. Master Clock (MCLK), BOOST ON.*

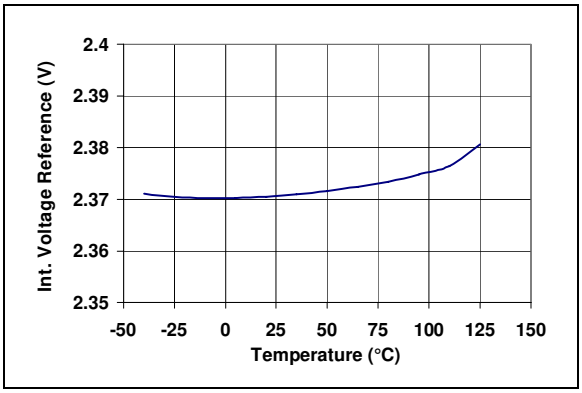


FIGURE 2-27: *Internal Voltage Reference vs. Temperature.*

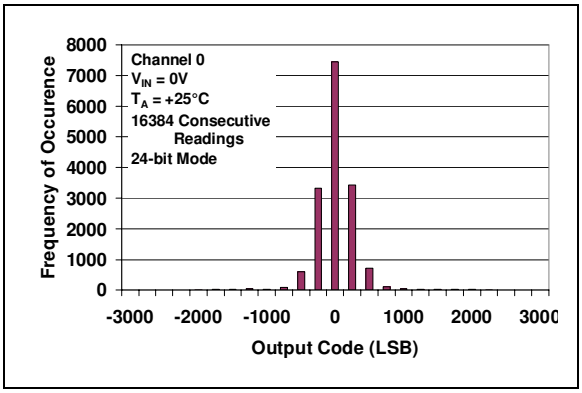


FIGURE 2-30: *Noise Histogram.*

Note: Unless otherwise indicated, AV_{DD} = 5.0V, DV_{DD} = 5.0 V; T_A = 25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 64; GAIN = 1; Dithering OFF; V_{IN} = -0.5 dBFS @ 60 Hz.

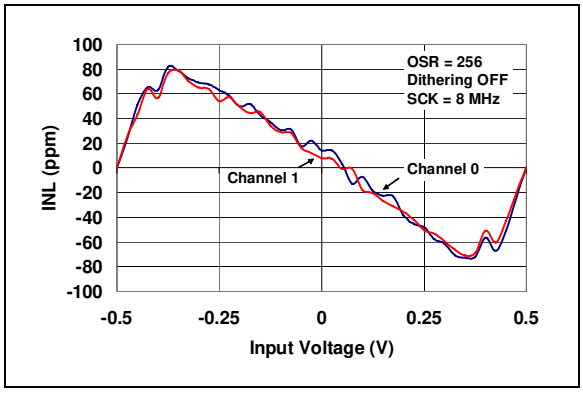


FIGURE 2-31: *Integral Nonlinearity (Dithering Off).*

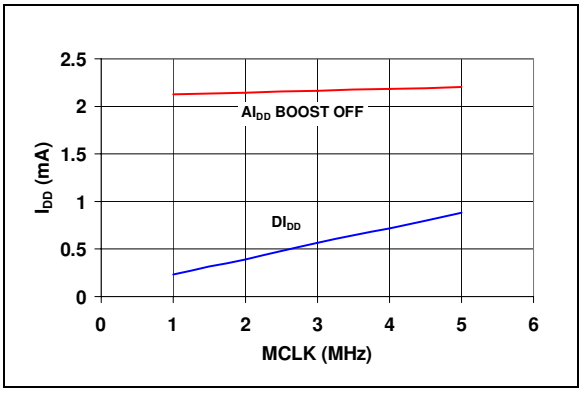


FIGURE 2-33: *Operating Current vs. Master Clock (MCLK).*

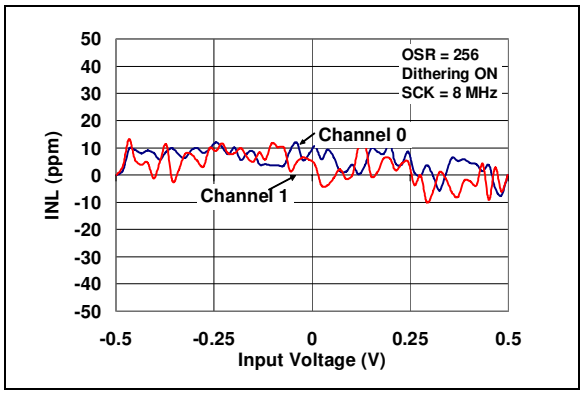


FIGURE 2-32: *Integral Nonlinearity (Dithering On).*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Symbol	Pin No.		Function
	SSOP	QFN	
$\overline{\text{RESET}}$	1	18	Master Reset Logic Input Pin
DV_{DD}	2	19	Digital Power Supply Pin
AV_{DD}	3	20	Analog Power Supply Pin
CH0+	4	1	Non-Inverting Analog Input Pin for Channel 0
CH0-	5	2	Inverting Analog Input Pin for Channel 0
CH1-	6	3	Inverting Analog Input Pin for Channel 1
CH1+	7	4	Non-Inverting Analog Input Pin for Channel 1
A_{GND}	8	5	Analog Ground Pin, Return Path for Internal Analog Circuitry
REFIN+/OUT	9	6	Non-Inverting Voltage Reference Input and Internal Reference Output Pin
REFIN-	10	7	Inverting Voltage Reference Input Pin
D_{GND}	11	8	Digital Ground Pin, Return Path for Internal Digital Circuitry
MDAT1	12	9	Modulator Data Output Pin for Channel 1
MDAT0	13	10	Modulator Data Output Pin for Channel 0
$\overline{\text{DR}}$	14	11	Data Ready Signal Output Pin
OSC1/CLKI	15	12	Oscillator Crystal Connection Pin or External Clock Input Pin
OSC2	16	13	Oscillator Crystal Connection Pin
$\overline{\text{CS}}$	17	14	Serial Interface Chip Select Pin
SCK	18	15	Serial Interface Clock Pin
SDO	19	16	Serial Interface Data Output Pin
SDI	20	17	Serial Interface Data Input Pin
EP	—	21	Exposed Thermal Pad. Must be connected to AGND.

3.1 $\overline{\text{RESET}}$

This pin is active low and places the entire chip in a Reset state when active.

When $\overline{\text{RESET}}$ = 0, all registers are reset to their default value, no communication can take place and no clock is distributed inside the part. This state is equivalent to a POR state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{\text{RESET}}$ = 0 is equivalent to when $\overline{\text{RESET}}$ = 1. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic and is reduced drastically when there is no clock running.

All the analog biases are enabled during a Reset so that the part is fully operational just after a $\overline{\text{RESET}}$ rising edge.

This input is Schmitt triggered.

3.2 Digital V_{DD} (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP3901. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 5.5V for specified operation.

3.3 Analog V_{DD} (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP3901.

This pin requires appropriate bypass capacitors and should be maintained to 5V ±10% for specified operation.

3.4 ADC Differential Analog inputs (CHn+/CHn-)

CH0- and CH0+, and CH1- and CH1+, are the two fully differential analog voltage inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±500 mV/GAIN with V_{REF} = 2.4V.

The maximum absolute voltage, with respect to AGND, for each CHn+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.5 Analog Ground (AGND)

AGND is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). To ensure accuracy and noise cancellation, this pin must be connected to the same ground as DGND, preferably with a star connection. If an analog ground plane is available, it is recommended that this pin be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system.

3.6 Non-Inverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for both ADCs or the internal voltage reference output.

When VREFEXT = 1, and an external voltage reference source can be used, the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its V_{REF}+ pin. When using an external single-ended reference, it should be connected to this pin.

When VREFEXT = 0, the internal voltage reference is enabled and connected to this pin through a switch. This voltage reference has minimal drive capability, and thus, needs proper buffering and bypass capacitances (10 µF tantalum in parallel with 0.1 µF ceramic) if used as a voltage source.

For optimal performance, bypass capacitances should be connected between this pin and AGND at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.7 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for both ADCs. When using an external differential voltage reference, it should be connected to its V_{REF-} pin. When using an external, single-ended voltage reference, or when VREFEXT = 0 (default) and using the internal voltage reference, this pin should be directly connected to AGND.

3.8 Digital Ground Connection (DGND)

DGND is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). To ensure accuracy and noise cancellation, DGND must be connected to the same ground as AGND, preferably with a star connection. If a digital ground plane is available, it is recommended that this pin be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system.

3.9 Modulator Data Output Pin for Channel 1 and Channel 0 (MDAT1/MDAT0)

MDAT0 and MDAT1 are the output pins for the modulator serial bitstreams of ADC Channels 0 and 1, respectively. These pins are high-impedance by default. When the MODOUT<1:0> are enabled, the modulator bitstream of the corresponding channel is present on the pin and updated at the AMCLK frequency. (See **Section 5.4 "Modulator Output Block"** for a complete description of the modulator outputs.) These pins can be directly connected to a MCU or DSP when a specific digital filtering is needed.

3.10 $\overline{DR}$ (Data Ready Pin)

The data ready pin indicates if a new conversion result is ready to be read. The default state of this pin is high when DR_HIZN = 1 and is high-impedance when DR_HIZN = 0 (default). After each conversion is finished, a low pulse will take place on the data ready pin to indicate the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The data ready pin is independent of the SPI interface and acts like an interrupt output. The data ready pin state is not latched and the pulse width (and period) are both determined by the MCLK frequency, over-sampling rate and internal clock prescale settings. The $\overline{DR}$ pulse width is equal to one DMCLK period and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

Note:	This pin should not be left floating when the DR_HIZN bit is low; a 100 kΩ pull-up resistor connected to D_{VDD} is recommended.

3.11 Oscillator and Master Clock Input Pins (OSC1/CLKI, OSC2)

OSC1/CLKI and OSC2 provide the master clock for the device. When CLKEXT = 0 (default), a resonant crystal or clock source with a similar sinusoidal waveform must be placed across these pins to ensure proper operation. The typical clock frequency specified is 4 MHz. However, the clock frequency can be 1 MHz to 5 MHz without disturbing ADC accuracy. With the current boost circuit enabled, the master clock can be used up to 8.192 MHz without disturbing ADC accuracy. Appropriate load capacitance should be connected to these pins for proper operation.

Note:	When CLKEXT = 1, the crystal oscillator is disabled, as well as the OSC2 input. The OSC1 becomes the master clock input, CLKI, the direct path for an external clock source; for example, a clock source generated by an MCU.

3.12 $\overline{CS}$ (Chip Select)

This pin is the SPI chip select that enables the serial communication. When this pin is high, no communication can take place. A chip select falling edge initiates the serial communication and a chip select rising edge terminates the communication. No communication can take place, even when $\overline{CS}$ is low and when $\overline{RESET}$ is low.

This input is Schmitt triggered.

3.13 SCK (Serial Data Clock)

This is the serial clock pin for SPI communication.

Data is clocked into the device on the rising edge of SCK. Data is clocked out of the device on the falling edge of SCK.

The MCP3901 interface is compatible with both SPI 0,0 and 1,1 modes. SPI modes can only be changed during a Reset.

The maximum clock speed specified is 20 MHz when DV_{DD} > 4.5V and 10 MHz otherwise.

This input is Schmitt triggered.

3.14 SDO (Serial Data Output)

This is the SPI data output pin. Data is clocked out of the device on the falling edge of SCK.

This pin stays high-impedance during the first command byte. It also stays high-impedance during the whole communication for write commands, and when the $\overline{CS}$ pin is high or when the $\overline{RESET}$ pin is low. This pin is active only when a read command is processed. Each read is processed by a packet of 8 bits.

3.15 SDI (Serial Data Input)

This is the SPI data input pin. Data is clocked into the device on the rising edge of SCK.

When $\overline{CS}$ is low, this pin is used to communicate with a series of 8-bit commands.

The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge, followed by an 8-bit command word entered through the SDI pin. Each command is either a read or a write command. Toggling SDI during a read command has no effect.

This input is Schmitt triggered.

NOTES:

4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

MCLK – Master Clock

AMCLK – Analog Master Clock

DMCLK – Digital Master Clock

DRCLK – Data Rate Clock

Oversampling Ratio (OSR)

Offset Error

Gain Error

Integral Nonlinearity Error

Signal-to-Noise Ratio (SNR)

Signal-to-Noise Ratio And Distortion (SINAD)

Total Harmonic Distortion (THD)

Spurious-Free Dynamic Range (SFDR)

MCP3901 Delta-Sigma Architecture

Idle Tones

Dithering

Crosstalk

PSRR

CMRR

ADC Reset Mode

Hardware Reset Mode ($\overline{RESET}$ = 0)

ADC Shutdown Mode

Full Shutdown Mode

4.1 MCLK – Master Clock

This is the fastest clock present in the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0 or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1 (see Figure 1-5).

4.2 AMCLK – Analog Master Clock

This is the clock frequency that is present on the analog portion of the device, after prescaling has occurred via the CONFIG1 PRESCALE<1:0> register bits. The analog portion includes the PGAs and the two Sigma-Delta modulators.

EQUATION 4-1:

$$AMCLK = \frac{MCLK}{PRESCALE}$$

TABLE 4-1: MCP3901 OVERSAMPLING RATIO SETTINGS

Config PRE<1:0>		Analog Master Clock Prescale
0	0	AMCLK = MCLK/1 (default)
0	1	AMCLK = MCLK/2
1	0	AMCLK = MCLK/4
1	1	AMCLK = MCLK/8

4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device, after prescaling and division by 4. This is also the sampling frequency, which is the rate when the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output (see Figure 1-5).

EQUATION 4-2:

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

4.4 DRCLK – Data Rate Clock

This is the output data rate (i.e., the rate at which the ADCs output new data). Each new data is signaled by a Data Ready pulse on the $\overline{DR}$ pin.

This data rate is depending on the OSR and the prescaler with the following formula:

EQUATION 4-3:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate, and since the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

The following table describes the various combinations of OSR and PRESCALE, and their associated AMCLK, DMCLK and DRCLK rates.

TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR AND PRESCALE

PRE <1:0>		OSR <1:0>		OSR	AMCLK	DMCLK	DRCLK	DRCLK (ksps)	SINAD (dB)	ENOB (bits)
1	1	1	1	256	MCLK/8	MCLK/32	MCLK/8192	0.4882	91.4	14.89
1	1	1	0	128	MCLK/8	MCLK/32	MCLK/4096	0.976	86.6	14.10
1	1	0	1	64	MCLK/8	MCLK/32	MCLK/2048	1.95	**78.7**	**12.78**
1	1	0	0	32	MCLK/8	MCLK/32	MCLK/1024	3.9	68.2	11.04
1	0	1	1	256	MCLK/4	MCLK/16	MCLK/4096	0.976	91.4	14.89
1	0	1	0	128	MCLK/4	MCLK/16	MCLK/2048	1.95	86.6	14.10
1	0	0	1	64	MCLK/4	MCLK/16	MCLK/1024	3.9	**78.7**	**12.78**
1	0	0	0	32	MCLK/4	MCLK/16	MCLK/512	7.8125	68.2	11.04
0	1	1	1	256	MCLK/2	MCLK/8	MCLK/2048	1.95	91.4	14.89
0	1	1	0	128	MCLK/2	MCLK/8	MCLK/1024	3.9	86.6	14.10
0	1	0	1	64	MCLK/2	MCLK/8	MCLK/512	7.8125	**78.7**	**12.78**
0	1	0	0	32	MCLK/2	MCLK/8	MCLK/256	15.625	68.2	11.04
0	0	1	1	256	MCLK	MCLK/4	MCLK/1024	3.9	91.4	14.89
0	0	1	0	128	MCLK	MCLK/4	MCLK/512	7.8125	86.6	14.10
0	**0**	**0**	**1**	**64**	**MCLK**	MCLK/4	MCLK/256	**15.625**	**78.7**	**12.78**
0	0	0	0	32	MCLK	MCLK/4	MCLK/128	31.25	68.2	11.04

Note: For OSR = 32 and 64, DITHER = 0. For OSR = 128 and 256, DITHER = 1.

4.5 Oversampling Ratio (OSR)

The ratio of the sampling frequency to the output data rate is OSR = DMCLK/DRCLK. The default OSR is 64 or with MCLK = 4 MHz and PRESCALE = 1, AMCLK = 4 MHz, f_S = 1 MHz, f_D = 15.625 ksps. The following bits in the CONFIG1 register are used to change the Oversampling Ratio (OSR).

TABLE 4-3: MCP3901 OVERSAMPLING RATIO SETTINGS

CONFIG OSR<1:0>		OVERSAMPLING RATIO OSR
0	0	32
0	1	64 (default)
1	0	128
1	1	256

4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together (V_{IN} = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip to chip. This offset error can easily be calibrated out by a MCU with a subtraction. The offset is specified in mV.

The offset on the MCP3901 has a low temperature coefficient; see **Section 2.0 "Typical Performance Curves"**.

4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in percent (%) compared to the ideal transfer function defined by Equation 5-3. The specification incorporates both PGA and ADC gain error contributions, but not the V_{REF} contribution (it is measured with an external V_{REF}). This error varies with PGA and OSR settings.

The gain error on the MCP3901 has a low temperature coefficient; see the typical performance curves for more information, Figure 2-24 and Figure 2-25.

4.8 Integral Nonlinearity Error

Integral nonlinearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed, or with the end points equal to zero.

It is the maximum remaining error after calibration of offset and gain errors for a DC input signal.

4.9 Signal-to-Noise Ratio (SNR)

For the MCP3901 ADC, the Signal-to-Noise ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal), when the input is a sinewave at a predetermined frequency. It is measured in dB. Usually, only the maximum Signal-to-Noise ratio is specified. The SNR calculation mainly depends on the OSR and DITHER settings of the device.

EQUATION 4-4: SIGNAL-TO-NOISE RATIO

$$SNR(dB) = 10log\left(\frac{SignalPower}{NoisePower}\right)$$

4.10 Signal-to-Noise Ratio And Distortion (SINAD)

The most important figure of merit, for the analog performance of the ADCs present on the MCP3901, is the Signal-to-Noise and Distortion (SINAD) specification.

Signal-to-Noise and distortion ratio are similar to the Signal-to-Noise ratio, with the exception that you must include the harmonics power in the noise power calculation. The SINAD specification mainly depends on the OSR and DITHER settings.

EQUATION 4-5: SINAD EQUATION

$$SINAD(dB) = 10log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD:

EQUATION 4-6: SINAD, THD AND SNR RELATIONSHIP

$$SINAD(dB) = 10log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$

4.11 Total Harmonic Distortion (THD)

The total harmonic distortion is the ratio of the output harmonic's power to the fundamental signal power for a sinewave input and is defined by Equation 4-7:

EQUATION 4-7:

$$THD(dB) = 10log\left(\frac{HarmonicsPower}{FundamentalPower}\right)$$

The THD calculation includes the first 35 harmonics for the MCP3901 specifications. The THD is usually only measured with respect to the 10 first harmonics. THD is sometimes expressed in %. For converting the THD in %, here is the formula:

EQUATION 4-8:

$$THD(\%) = 100 \times 10^{\frac{THD(dB)}{20}}$$

This specification depends mainly on the DITHER setting.

4.12 Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio between the output power of the fundamental and the highest spur in the frequency spectrum. The spur frequency is not necessarily a harmonic of the fundamental, even though it is usually the case. This figure represents the dynamic range of the ADC when a full-scale signal is used at the input. This specification depends mainly on the DITHER setting.

EQUATION 4-9:

$$SFDR(dB) = 10log\left(\frac{FundamentalPower}{HighestSpurPower}\right)$$

4.13 MCP3901 Delta-Sigma Architecture

The MCP3901 incorporates two Delta-Sigma ADCs with a multi-bit architecture. A Delta-Sigma ADC is an oversampling converter that incorporates a built-in modulator, which is digitizing the quantity of charge integrated by the modulator loop (see Figure 5-1). The quantizer is the block that is performing the Analog-to-Digital conversion. The quantizer is typically 1 bit, or a simple comparator which helps to maintain the linearity performance of the ADC (the DAC structure, is in this case, inherently linear).

Multi-bit quantizers help to lower the quantization error (the error fed back in the loop can be very large with 1-bit quantizers) without changing the order of the modulator or the OSR, which leads to better SNR figures. Typically, however, the linearity of such architectures is more difficult to achieve, since the DAC is no more simple to realize, and its linearity limits the THD of such ADCs.

The MCP3901's 5-level quantizer is a Flash ADC, composed of 4 comparators arranged with equally spaced thresholds and a thermometer coding. The MCP3901 also includes proprietary 5-level DAC architecture that is inherently linear for improved THD figures.

4.14 Idle Tones

A Delta-Sigma Converter is an integrating converter. It also has a finite quantization step (LSB) which can be detected by its quantizer. A DC input voltage that is below the quantization step should only provide an all zeros result, since the input is not large enough to be detected. As an integrating device, any Delta-Sigma will show, in this case, Idle tones. This means that the output will have spurs in the frequency content that are depending on the ratio between quantization step voltage and the input voltage. These spurs are the result of the integrated sub-quantization step inputs that will eventually cross the quantization steps after a long enough integration. This will induce an AC frequency at the output of the ADC and can be shown in the ADC output spectrum.

These Idle tones are residues that are inherent to the quantization process and the fact that the converter is integrating at all times without being reset. They are residues of the finite resolution of the conversion process. They are very difficult to attenuate and they are heavily signal dependent. They can degrade both the SFDR and THD of the converter, even for DC inputs. They can be localized in the baseband of the converter, and thus, difficult to filter from the actual input signal.

For power metering applications, Idle tones can be very disturbing because energy can be detected even at the 50 or 60 Hz frequency, depending on the DC offset of the ADCs, while no power is really present at the inputs. The only practical way to suppress or attenuate the Idle tones phenomenon is to apply dithering to the ADC. The Idle tone amplitudes are a function of the order of the modulator, the OSR and the number of levels in the quantizer of the modulator. A higher order, a higher OSR or a higher number of levels for the quantizer will attenuate the Idle tones amplitude.

4.15 Dithering

In order to suppress or attenuate the Idle tones present in any Delta-Sigma ADCs, dithering can be applied to the ADC. Dithering is the process of adding an error to the ADC feedback loop in order to "decorrelate" the outputs and "break" the Idle tones behavior. Usually, a random or pseudo-random generator adds an analog or digital error to the feedback loop of the Delta-Sigma ADC in order to ensure that no tonal behavior can happen at its outputs. This error is filtered by the feedback loop, and typically, has a zero average value so that the converter static transfer function is not disturbed by the dithering process. However, the dithering process slightly increases the noise floor (it adds noise to the part) while reducing its tonal behavior, and thus, improving SFDR and THD (see Figure 2-10 and Figure 2-14). The dithering process scrambles the Idle tones into baseband white noise and ensures that dynamic specs (SNR, SINAD, THD, SFDR) are less signal dependent. The MCP3901 incorporates a proprietary dithering algorithm on both ADCs in order to remove Idle tones and improve THD, which is crucial for power metering applications.

4.16 Crosstalk

The crosstalk is defined as the perturbation caused by one ADC channel on the other ADC channel. It is a measurement of the isolation between the two ADCs present in the chip.

This measurement is a two-step procedure:

1. Measure one ADC input with no perturbation on the other ADC (ADC inputs shorted).
2. Measure the same ADC input with a perturbation sine wave signal on the other ADC at a certain predefined frequency.

The crosstalk is then the ratio between the output power of the ADC when the perturbation is present and when it is not divided by the power of the perturbation signal.

A lower crosstalk value implies more independence and isolation between the two channels.

The measurement of this signal is performed under the following conditions:

- GAIN = 1,
- PRESCALE = 1,
- OSR = 256,
- MCLK = 4 MHz

Step 1

- CH0+ = CH0- = AGND
- CH1+ = CH1- = AGND

Step 2

- CH0+ = CH0- = AGND
- CH1+ – CH1- = 1 V_{P-P} @ 50/60 Hz (full-scale sine wave)

The crosstalk is then calculated with the following formula:

EQUATION 4-10:

$$CTalk(dB) = 10log\left(\frac{\Delta CH0Power}{\Delta CH1Power}\right)$$

4.17 PSRR

This is the ratio between a change in the power supply voltage and the ADC output codes. It measures the influence of the power supply voltage on the ADC outputs.

The PSRR specification can be DC (the power supply is taking multiple DC values) or AC (the power supply is a sinewave at a certain frequency with a certain common-mode). In AC, the amplitude of the sinewave is representing the change in the power supply.

It is defined as:

EQUATION 4-11:

$$PSRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta AV_{DD}}\right)$$

Where V_{OUT} is the equivalent input voltage that the output code translates to with the ADC transfer function. In the MCP3901 specification, AV_{DD} varies from 4.5V to 5.5V, and for AC PSRR, a 50/60 Hz sinewave is chosen, centered around 5V with a maximum 500 mV amplitude. The PSRR specification is measured with $AV_{DD} = DV_{DD}$.

4.18 CMRR

This is the ratio between a change in the common-mode input voltage and the ADC output codes. It measures the influence of the common-mode input voltage on the ADC outputs.

The CMRR specification can be DC (the common-mode input voltage is taking multiple DC values) or AC (the common-mode input voltage is a sinewave at a certain frequency with a certain common-mode). In AC, the amplitude of the sinewave is representing the change in the power supply.

It is defined as:

EQUATION 4-12:

$$CMRR(dB) = 20log\left(\frac{\Delta V_{OUT}}{\Delta V_{CM}}\right)$$

Where V_{CM} = (CHn+ + CHn-)/2 is the common-mode input voltage and V_{OUT} is the equivalent input voltage, the output code is translated to the ADC transfer function. In the MCP3901 specification, VCM varies from -1V to +1V, and for the AC specification, a 50/60 Hz sinewave is chosen, centered around 0V, with a 500 mV amplitude.

4.19 ADC Reset Mode

ADC Reset mode (also called Soft Reset mode) can only be entered through setting the RESET<1:0> bits high in the Configuration register. This mode is defined as the condition where the converters are active, but their output is forced to '0'.

The registers are not affected in this Reset mode and retain their values.

The ADCs can immediately output meaningful codes after leaving Reset mode (and after the sinc filter settling time of 3/DRCLK). This mode is both entered and exited through the setting of bits in the Configuration register.

Each converter can be placed in Soft Reset mode independently. The Configuration registers are not modified by the Soft Reset mode.

A data ready pulse will not be generated by any ADC while in Reset mode.

Reset mode also effects the modulator output block (i.e., the MDAT pin, corresponding to the channel in Reset). If enabled, it provides a bitstream corresponding to a zero output (a series of '0011' bits continuously repeated).

When an ADC exits ADC Reset mode, any phase delay present, before Reset was entered, will still be present. If one ADC was not in Reset, the ADC leaving Reset mode will automatically resynchronize the phase delay. The resynchronization is relative to the other ADC channel per the Phase Delay register block and gives $\overline{DR}$ pulses accordingly.

If an ADC is placed in Reset mode while the other is converting, it is not shutting down the internal clock. When going back out of Reset, it will be resynchronized automatically with the clock that did not stop during Reset.

If both ADCs are in Soft Reset or Shutdown modes, the clock is no longer distributed to the digital core for low-power operation. Once any of the ADC is back to normal operation, the clock is automatically distributed again.

4.20 Hard Reset Mode ($\overline{RESET}$ = 0)

This mode is only available during a Power-on-Reset (POR) or when the $\overline{RESET}$ pin is pulled low. The $\overline{RESET}$ pin low state places the device in a Hard Reset mode.

In this mode, all internal registers are reset to their default state.

The DC biases for the analog blocks are still active (i.e., the MCP3901 is ready to convert). However, this pin clears all conversion data in the ADCs. In this mode, the MDAT outputs are in high-impedance. The comparator outputs of both ADCs are forced to their Reset state ('0011'). The SINC filters are all reset, as well as their double output buffers. See serial timing for minimum pulse low time in **Section 1.0 "Electrical Characteristics"**.

During a Hard Reset, no communication with the part is possible. The digital interface is maintained in a Reset state.

4.21 ADC Shutdown Mode

ADC Shutdown mode is defined as a state where the converters and their biases are off, consuming only leakage current. After this is removed, start-up delay time (SINC filter settling time) will occur before outputting meaningful codes. The start-up delay is needed to power-up all DC biases in the channel that was in shutdown. This delay is the same as t_{POR} and any $\overline{DR}$ pulse coming within this delay should be discarded.

Each converter can be placed in Shutdown mode, independently. The CONFIG registers are not modified by the Shutdown mode. This mode is only available through programming the SHUTDOWN<1:0> bits in the CONFIG2 register.

The output data is flushed to all zeros while in ADC shutdown. No data ready pulses are generated by any ADC while in ADC Shutdown mode.

ADC Shutdown mode also effects the modulator output block (i.e., if MDAT of the channel in Shutdown mode is enabled). This pin will provide a bitstream corresponding to a zero output (series of '0011' bits continuously repeated).

When an ADC exits ADC Shutdown mode, any phase delay present before shutdown was entered will still be present. If one ADC was not in shutdown, the ADC leaving Shutdown mode will automatically resynchronize the phase delay relative to the other ADC channel, per the Phase Delay register block, and give $\overline{DR}$ pulses accordingly.

If an ADC is placed in Shutdown mode while the other is converting, it is not shutting down the internal clock. When going back out of shutdown, it will be resynchronized automatically with the clock that did not stop during Reset.

If both ADCs are in ADC Reset or ADC Shutdown modes, there is no more distribution of the clock to the digital core for low-power operation. Once any of the ADC is back to normal operation, the clock is automatically distributed again.

4.22 Full Shutdown Mode

The lowest power consumption can be achieved when SHUTDOWN<1:0> = 11 and VREFEXT = CLKEXT = 1. This mode is called "Full Shutdown mode" and no analog circuitry is enabled. In this mode, the POR AV_{DD} monitoring circuit is also disabled. When the clock is Idle (CLKI = 0 or 1 continuously), no clock is propagated throughout the chip. Both ADCs are in shutdown, the internal voltage reference is disabled and the internal oscillator is disabled.

The only circuit that remains active is the SPI interface, but this circuit does not induce any static power consumption. If SCK is Idle, the only current consumption comes from the leakage currents induced by the transistors and is less than 1 µA on each power supply.

This mode can be used to power down the chip completely and avoid power consumption when there is no data to convert at the analog inputs. Any SCK or MCLK edge coming while on this mode, will induce dynamic power consumption.

Once any of the SHUTDOWN, CLKEXT and VREFEXT bits returns to '0', the POR AV_{DD} monitoring block is back to operation and AV_{DD} monitoring can take place.

5.0 DEVICE OVERVIEW

5.1 Analog Inputs (CHn+/-)

The MCP3901 analog inputs can be connected directly to current and voltage transducers (such as shunts, current transformers, or Rogowski coils). Each input pin is protected by specialized ESD structures that are certified to pass 7 kV HBM and 400V MM contact charge. These structures allow bipolar ±6V continuous voltage, with respect to AGND, to be present at their inputs without the risk of permanent damage.

Both channels have fully differential voltage inputs for better noise performance. The absolute voltage at each pin, relative to AGND, should be maintained in the ±1V range during operation in order to ensure the specified ADC accuracy. The common-mode signals should be adapted to respect both the previous conditions and the differential input voltage range. For best performance, the common-mode signals should be maintained to AGND.

5.2 Programmable Gain Amplifiers (PGA)

The two Programmable Gain Amplifiers (PGAs) reside at the front end of each Delta-Sigma ADC. They have two functions: translate the common-mode of the input from AGND to an internal level between AGND and AV_{DD}, and amplify the input differential signal. The translation of the common-mode does not change the differential signal, but recenters the common-mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the Delta-Sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn<2:0> bits in the GAIN register. The following table represents the gain settings for the PGA:

TABLE 5-1: PGA CONFIGURATION SETTING

Gain PGA_CHn<2:0>			Gain (V/V)	Gain (dB)	V_{IN} Range (V)
0	0	0	1	0	±0.5
0	0	1	2	6	±0.25
0	1	0	4	12	±0.125
0	1	1	8	18	±0.0625
1	0	0	16	24	±0.03125
1	0	1	32	30	±0.015625

5.3 Delta-Sigma Modulator

5.3.1 ARCHITECTURE

Both ADCs are identical in the MCP3901 and they include a second-order modulator with a multi-bit DAC architecture (see Figure 5-1). The quantizer is a Flash ADC composed of 4 comparators with equally spaced thresholds and a thermometer output coding. The proprietary 5-level architecture ensures minimum quantization noise at the outputs of the modulators without disturbing linearity or inducing additional distortion. The sampling frequency is DMCLK (typically 1 MHz with MCLK = 4 MHz) so the modulator outputs are refreshed at a DMCLK rate. The modulator outputs are available in the MOD register or serially transferred on each MDAT pin.

Both modulators also include a dithering algorithm that can be enabled through the DITHER<1:0> bits in the Configuration register. This dithering process improves THD and SFDR (for high OSR settings) while slightly increasing the noise floor of the ADCs. For power metering applications and applications that are distortion-sensitive, it is recommended to keep DITHER enabled for both ADCs. In the case of power metering applications, THD and SFDR are critical specifications to optimize SNR (noise floor). This is not really problematic due to a large averaging factor at the output of the ADCs; therefore, even for low OSR settings, the dithering algorithm will show a positive impact on the performance of the application.

Figure 5-1 represents a simplified block diagram of the Delta-Sigma ADC present on MCP3901.

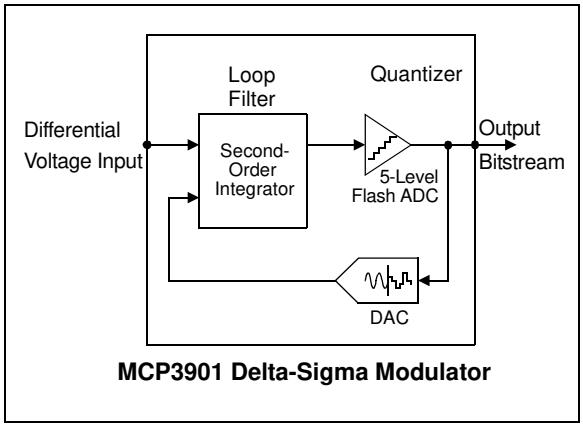


FIGURE 5-1: *Simplified Delta-Sigma ADC Block Diagram.*