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# MCP3911

## 3.3V Two-Channel Analog Front End

### Features

- Two Synchronous Sampling 16/24-bit Resolution Delta-Sigma A/D Converters
- 94.5 dB SINAD, -106.5 dBc Total Harmonic Distortion (THD) (up to 35th harmonic), 111 dB SFDR for Each Channel
- 2.7V – 3.6V $AV_{DD}$, $DV_{DD}$
- Programmable Data Rate up to 125 ksps
  - 4 MHz Maximum Sampling Frequency
- Oversampling Ratio up to 4096
- Ultra Low Power Shutdown Mode with <2 µA
- -122 dB Crosstalk between the Two Channels
- Low Drift 1.2V Internal Voltage Reference: 7 ppm/°C
- Differential Voltage Reference Input Pins
- High Gain Programmable Gain Amplifier (PGA) on Each Channel (up to 32V/V)
- Phase Delay Compensation with 1 µs Time Resolution
- Separate Modulator Output Pins for Each Channel
- Separate Data Ready Pin for Easy Synchronization
- Individual 24-bit Digital Offset and Gain Error Correction for Each Channel
- High-Speed 20 MHz SPI Interface with Mode 0,0 and 1,1 Compatibility
- Continuous Read/Write Modes for Minimum Communication
- Low Power Consumption (8.9 mW at 3.3V, 5.6 mW at 3.3V in low-power mode, typical)
- Available in Small 20-lead QFN and SSOP Packages, Pin-to-pin Compatible with MCP3901
- Extended Temperature Range: -40°C to +125°C

### Applications

- Energy Metering and Power Measurement
- Automotive
- Portable Instrumentation
- Medical and Power Monitoring
- Audio/Voice Recognition

### Description

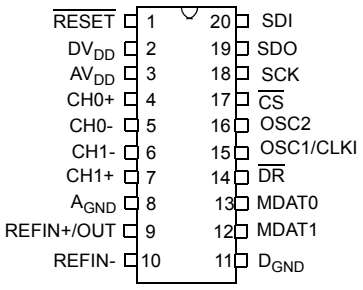
The MCP3911 is a 2.7V to 3.6V dual channel Analog Front End (AFE) containing two synchronous sampling Delta-Sigma Analog-to-Digital Converters (ADC), two PGAs, phase delay compensation block, low-drift internal voltage reference, modulator output block, digital offset and gain errors calibration registers and high-speed 20 MHz SPI compatible serial interface.

The MCP3911 ADCs are fully configurable with features such as: 16/24-bit resolution, OSR from 32 to 4096, gain from 1x to 32x, independent shutdown and reset, dithering and auto-zeroing. The communication is largely simplified with the one-byte-long commands including various continuous read/write modes that can be accessed by the Direct Memory Access (DMA) of an MCU with a separate data ready pin that can be directly connected to an Interrupt Request (IRQ) input of an MCU.

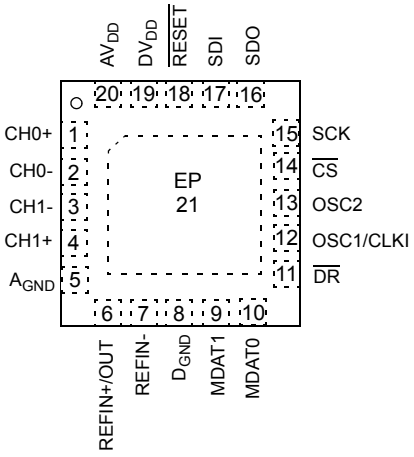
The MCP3911 is capable of interfacing a large variety of voltage and current sensors including shunts, current transformers, Rogowski coils and Hall effect sensors.

### Package Type

**20-Lead SSOP**

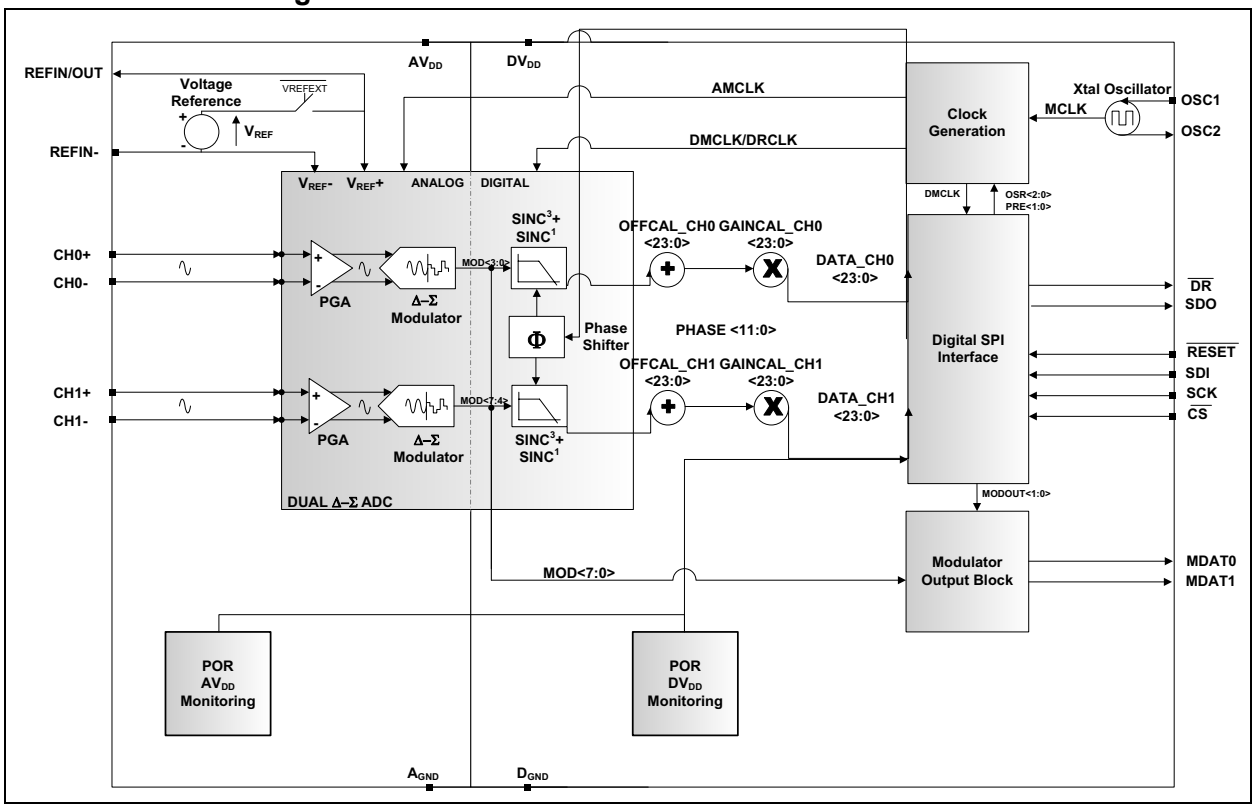



**20-Lead 4x4 QFN***




* Includes Exposed Thermal Pad (EP); see Table 3-1.

## Functional Block Diagram



# 1.0 ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS †

$V_{DD}$ ..... -0.3V to 4.0V
Digital inputs and outputs w.r.t. $A_{GND}$ ..... --0.3V to 4.0V
Analog input w.r.t. $A_{GND}$ ..... ....-2V to +2V
$V_{REF}$ input w.r.t. $A_{GND}$ ..... -0.6V to $V_{DD}$ +0.6V
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -65°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) ..... 4.0 kV, 300V
ESD on all other pins (HBM,MM) ..... 4.0 kV, 300V

**† Notice**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 1.1 Electrical Specifications

**TABLE 1-1: ANALOG SPECIFICATIONS TARGET TABLE**

| **Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = $DV_{DD}$ = 2.7V to 3.6V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, AZ_FREQ = 0, DITHER<1:0> = 11, BOOST<1:0> = 10; $V_{CM}$ = 0V; $T_A$ = -40°C to +125°C; $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$ at 50/60 Hz on both channels. | | | | | | |
|---|---|---|---|---|---|---|
| **Characteristic** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **ADC Performance** | | | | | | |
| Resolution (No Missing Codes) | | 24 | — | — | bits | OSR = 256 or greater |
| Sampling Frequency | $f_S$(DMCLK) | — | 1 | 4 | MHz | For maximum condition, BOOST<1:0> = 11 |
| Output Data Rate | $f_D$(DRCLK) | — | 4 | 125 | ksps | For maximum condition, BOOST<1:0> = 11, OSR = 32 |
| Analog Input Absolute Voltage on CH0+, CH0-, CH1+, CH1- pins | CH0+/- | -1 | | +1 | V | All analog input channels, measured to $A_{GND}$ |
| Analog Input Leakage Current | $I_{IN}$ | — | ±1 | — | nA | RESET<1:0> = 11, MCLK running continuously |
| Differential Input Voltage Range | ($CH_{n+}$ - $CH_{n-}$) | -600/GAIN | — | +600/ GAIN | mV | $V_{REF}$ = 1.2V, proportional to $V_{REF}$ |
| Offset Error | $V_{OS}$ | -1 | 0.2 | +1 | mV | **Note 4** |
| Offset Error Drift | | — | 0.5 | — | µV/°C | |
| Gain Error | GE | -4 | — | +4 | % | **Note 4** |
| Gain Error Drift | | — | 1 | — | ppm/°C | |

**Note 1:** This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at -0.5 dB below the maximum signal range, $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$, $V_{REF}$ = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies And Formulas** for definition. This parameter is established by characterization and not 100% tested. See performance graphs for other than default settings provided here.

**2:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

**3:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

**4:** Applies to all gains. Offset and gain errors depend on PGA gain setting, see **Section 2.0, Typical Performance Curves** for typical performance.

**5:** Outside of this range, the ADC accuracy is not specified. An extended input range of ±2 V can be applied continuously to the part with no damage.

**6:** For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

**TABLE 1-1: ANALOG SPECIFICATIONS TARGET TABLE (CONTINUED)**

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = $DV_{DD}$ = 2.7V to 3.6V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, AZ_FREQ = 0, DITHER<1:0> = 11, BOOST<1:0> = 10; $V_{CM}$ = 0V; $T_A$ = -40°C to +125°C; $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$ at 50/60 Hz on both channels.

| Characteristic | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Integral Non-Linearity | INL | | 5 | | ppm | |
| Differential Input Impedance | $Z_{IN}$ | 232 | — | — | kΩ | G = 1, proportional to 1/AMCLK |
| | | 142 | — | — | kΩ | G = 2, proportional to 1/AMCLK |
| | | 72 | — | — | kΩ | G = 4, proportional to 1/AMCLK |
| | | 38 | — | — | kΩ | G = 8, proportional to 1/AMCLK |
| | | 36 | — | — | kΩ | G = 16, proportional to 1/AMCLK |
| | | 33 | — | — | kΩ | G = 32, proportional to 1/AMCLK |
| Signal-to-Noise and Distortion Ratio **(Note 1)** | SINAD | 92 | 94.5 | — | dB | |
| Total Harmonic Distortion **(Note 1)** | THD | — | -106.5 | -103 | dBc | Includes the first 35 harmonics |
| Signal-to-Noise Ratio **(Note 1)** | SNR | 92 | 95 | — | dB | |
| Spurious Free Dynamic Range **(Note 1)** | SFDR | — | 111 | — | dBFS | |
| Crosstalk (50, 60 Hz) | CTALK | — | -122 | — | dB | |
| AC Power Supply Rejection | AC PSRR | — | -73 | — | dB | $AV_{DD}$ = $DV_{DD}$ = 3.3V+0.6$V_{PP}$, 50/60 Hz, 100/120 Hz |
| DC Power Supply Rejection | DC PSRR | — | -73 | — | dB | $AV_{DD}$ = $DV_{DD}$ = 2.7V to 3.6V |
| DC Common Mode Rejection | DC CMRR | — | -105 | — | dB | $V_{CM}$ from -1V to +1V |

**Note 1:** This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at -0.5 dB below the maximum signal range, $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$, $V_{REF}$ = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies And Formulas** for definition. This parameter is established by characterization and not 100% tested. See performance graphs for other than default settings provided here.

**2:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

**3:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

**4:** Applies to all gains. Offset and gain errors depend on PGA gain setting, see **Section 2.0, Typical Performance Curves** for typical performance.

**5:** Outside of this range, the ADC accuracy is not specified. An extended input range of ±2 V can be applied continuously to the part with no damage.

**6:** For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

**TABLE 1-1: ANALOG SPECIFICATIONS TARGET TABLE (CONTINUED)**

**Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = $DV_{DD}$ = 2.7V to 3.6V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, AZ_FREQ = 0, DITHER<1:0> = 11, BOOST<1:0> = 10; $V_{CM}$ = 0V; $T_A$ = -40°C to +125°C; $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$ at 50/60 Hz on both channels.

| Characteristic | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Internal Voltage Reference** | | | | | | |
| Tolerance | $V_{REF}$ | 1.176 | 1.2 | 1.224 | V | VREFEXT = 0, $T_A$ = +25°C only |
| Temperature Coefficient | $TCV_{REF}$ | — | 7 | — | ppm/°C | $T_A$ = -40°C to +125°C, VREFEXT = 0 |
| Output Impedance | $ZOUTV_{REF}$ | — | 2 | — | kΩ | VREFEXT = 0 |
| Internal Voltage Reference Operating Current | $AI_{DD}V_{REF}$ | — | 25 | — | µA | VREFEXT = 0, SHUTDOWN<1:0> = 11 |
| **Voltage Reference Input** | | | | | | |
| Input Capacitance | | — | — | 10 | pF | |
| Differential Input Voltage Range ($V_{REF}$+ – $V_{REF}$-) | $V_{REF}$ | 1.1 | — | 1.3 | V | VREFEXT = 1 |
| Absolute Voltage on REFIN+ pin | $V_{REF+}$ | $V_{REF}$- + 1.1 | — | $V_{REF}$- + 1.3 | V | VREFEXT = 1 |
| Absolute Voltage on REFIN- pin | $V_{REF-}$ | -0.1 | — | +0.1 | V | REFIN- should be connected to $A_{GND}$ when VREFEXT = 0 |
| **Master Clock Input** | | | | | | |
| Master Clock Input Frequency Range | $f_{MCLK}$ | | — | 20 | MHz | CLKEXT = 1, **Note 6** |
| Crystal Oscillator Operating Frequency Range | $f_{XTAL}$ | 1 | — | 20 | MHz | CLKEXT = 0, **Note 6** |
| Analog Master Clock | AMCLK | — | — | 16 | MHz | **Note 6** |
| **Power Supply** | | | | | | |
| Operating Voltage, Analog | $AV_{DD}$ | 2.7 | — | 3.6 | V | |
| Operating Voltage, Digital | $DV_{DD}$ | 2.7 | — | 3.6 | V | |
| Operating Current, Analog (**Note 2**) | $I_{DD,A}$ | — | 1.5 | 2.3 | mA | BOOST<1:0> = 00 |
| | | — | 1.8 | 2.8 | mA | BOOST<1:0> = 01 |
| | | — | 2.5 | 3.5 | mA | BOOST<1:0> = 10 |
| | | — | 4.4 | 6.25 | mA | BOOST<1:0> = 11 |

**Note 1:** This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at -0.5 dB below the maximum signal range, $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$, $V_{REF}$ = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies And Formulas** for definition. This parameter is established by characterization and not 100% tested. See performance graphs for other than default settings provided here.

**2:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

**3:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

**4:** Applies to all gains. Offset and gain errors depend on PGA gain setting, see **Section 2.0, Typical Performance Curves** for typical performance.

**5:** Outside of this range, the ADC accuracy is not specified. An extended input range of ±2 V can be applied continuously to the part with no damage.

**6:** For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

**TABLE 1-1: ANALOG SPECIFICATIONS TARGET TABLE (CONTINUED)**

| **Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = $DV_{DD}$ = 2.7V to 3.6V, MCLK = 4 MHz; PRE<1:0> = 00; OSR = 256; GAIN = 1; VREFEXT = 0, CLKEXT = 1, AZ_FREQ = 0, DITHER<1:0> = 11, BOOST<1:0> = 10; $V_{CM}$ = 0V; $T_A$ = -40°C to +125°C; $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$ at 50/60 Hz on both channels. | | | | | | |
|---|---|---|---|---|---|---|
| **Characteristic** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| Operating Current, Digital | $I_{DD,D}$ | — | 0.2 | 0.3 | mA | MCLK = 4 MHz, proportional to MCLK |
| | | — | 0.7 | — | mA | MCLK = 16 MHz, proportional to MCLK |
| Shutdown Current, Analog | $I_{DDS,A}$ | — | — | 1 | µA | $AV_{DD}$ pin only **(Note 3)** |
| Shutdown Current, Digital | $I_{DDS,D}$ | — | — | 1 | µA | $DV_{DD}$ pin only (**Note 3**) |

**Note 1:** This specification implies that the ADC output is valid over this entire differential range and that there is no distortion or instability across this input range. Dynamic Performance specified at -0.5 dB below the maximum signal range, $V_{IN}$ = 1.2$V_{PP}$ = 424 $mV_{RMS}$, $V_{REF}$ = 1.2V at 50/60 Hz. See **Section 4.0, Terminologies And Formulas** for definition. This parameter is established by characterization and not 100% tested. See performance graphs for other than default settings provided here.

**2:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 00, RESET<1:0> = 00, VREFEXT = 0, CLKEXT = 0.

**3:** For these operating currents, the following configuration bit settings apply: SHUTDOWN<1:0> = 11, VREFEXT = 1, CLKEXT = 1.

**4:** Applies to all gains. Offset and gain errors depend on PGA gain setting, see **Section 2.0, Typical Performance Curves** for typical performance.

**5:** Outside of this range, the ADC accuracy is not specified. An extended input range of ±2 V can be applied continuously to the part with no damage.

**6:** For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-2 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-2.

## 1.2 Serial Interface Characteristics

**TABLE 1-2: SERIAL DC CHARACTERISTICS TABLE**

| **Electrical Specifications:** Unless otherwise indicated, all parameters apply at $DV_{DD}$ = 2.7 to 3.6V, $T_A$ = -40°C to +125°C, $C_{LOAD}$ = 30 pF, applies to all digital I/O. | | | | | | |
|---|---|---|---|---|---|---|
| **Characteristics** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Test Conditions** |
| High-level Input Voltage | $V_{IH}$ | 0.7 $DV_{DD}$ | — | | V | Schmitt Triggered |
| Low-level Input Voltage | $V_{IL}$ | — | — | 0.3 $DV_{DD}$ | V | Schmitt Triggered |
| Input Leakage Current | $I_{LI}$ | — | — | ±1 | µA | $\overline{CS}$ = $DV_{DD}$, $V_{IN}$ = $D_{GND}$ to $DV_{DD}$ |
| Output leakage Current | $I_{LO}$ | — | — | ±1 | µA | $\overline{CS}$ = $DV_{DD}$, $V_{OUT}$ = $D_{GND}$ or $DV_{DD}$ |
| Hysteresis of Schmitt Trigger Inputs | $V_{HYS}$ | — | 200 | — | mV | **Note 2**, $DV_{DD}$ = 3.3V only |
| Low-level Output Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = +2.1 mA, $DV_{DD}$ = 3.3V |
| High-level Output Voltage | $V_{OH}$ | $DV_{DD}$ -0.5 | — | — | V | $I_{OH}$ = -2.1 mA, $DV_{DD}$ = 3.3V |
| Internal Capacitance (all inputs and outputs) | $C_{INT}$ | — | — | 7 | pF | $T_A$ = +25°C, SCK = 1.0 MHz, $DV_{DD}$ = 3.3V (**Note 1**) |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** This parameter is established by characterization and not production tested.

**TABLE 1-3: SERIAL AC CHARACTERISTICS TABLE**

| **Electrical Specifications:** Unless otherwise indicated, all parameters apply at $DV_{DD}$ = 2.7 to 3.6V, $T_A$ = -40°C to +125°C, GAIN = 1, $C_{LOAD}$ = 30 pF. | | | | | | |
|---|---|---|---|---|---|---|
| **Characteristics** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Test Conditions** |
| Serial Clock frequency | $f_{SCK}$ | — | — | 20 | MHz | |
| $\overline{CS}$ setup time | $t_{CSS}$ | 25 | — | — | ns | |
| $\overline{CS}$ hold time | $t_{CSH}$ | 50 | — | — | ns | |
| $\overline{CS}$ disable time | $t_{CSD}$ | 50 | — | — | ns | |
| Data setup time | $t_{SU}$ | 5 | — | — | ns | |
| Data hold time | $t_{HD}$ | 10 | — | — | ns | |
| Serial Clock high time | $t_{HI}$ | 20 | — | — | ns | |
| Serial Clock low time | $t_{LO}$ | 20 | — | — | ns | |
| Serial Clock delay time | $t_{CLD}$ | 50 | — | — | ns | |
| Serial Clock enable time | $t_{CLE}$ | 50 | — | — | ns | |
| Output valid from SCK low | $t_{DO}$ | — | — | 25 | ns | |
| Modulator output valid from AMCLK high | $t_{DOMDAT}$ | — | — | 1/(2 x AMCLK) | s | |
| Output hold time | $t_{HO}$ | 0 | — | — | ns | **(Note 1)** |
| Output disable time | $t_{DIS}$ | — | — | 25 | ns | **(Note 1)** |
| Reset Pulse Width ($\overline{RESET}$) | $t_{MCLR}$ | 100 | — | — | ns | |
| Data Transfer Time to $\overline{DR}$ (Data Ready) | $t_{DODR}$ | | — | 25 | ns | **(Note 2)** |
| Modulator Mode Entry to Modulator Data Present | $t_{MODSU}$ | | — | 100 | ns | |
| Data Ready Pulse Low Time | $t_{DRP}$ | | 1/DMCLK | — | µs | |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**2:** This parameter is established by characterization and not production tested.

**TABLE 1-4: TEMPERATURE SPECIFICATIONS TABLE**

| **Electrical Specifications:** Unless otherwise indicated, all parameters apply at $AV_{DD}$ = 2.7 to 3.6V, $DV_{DD}$ = 2.7 to 3.6V. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Operating Temperature Range | $T_A$ | -40 | — | +125 | °C | **Note 1** |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistances** | | | | | | |
| Thermal Resistance, 20L QFN | $\theta_{JA}$ | — | 43 | — | °C/W | |
| Thermal Resistance, 20L SSOP | $\theta_{JA}$ | — | 87.3 | — | °C/W | |

**Note 1:** The internal junction temperature ($T_J$) must not exceed the absolute maximum specification of +150°C.

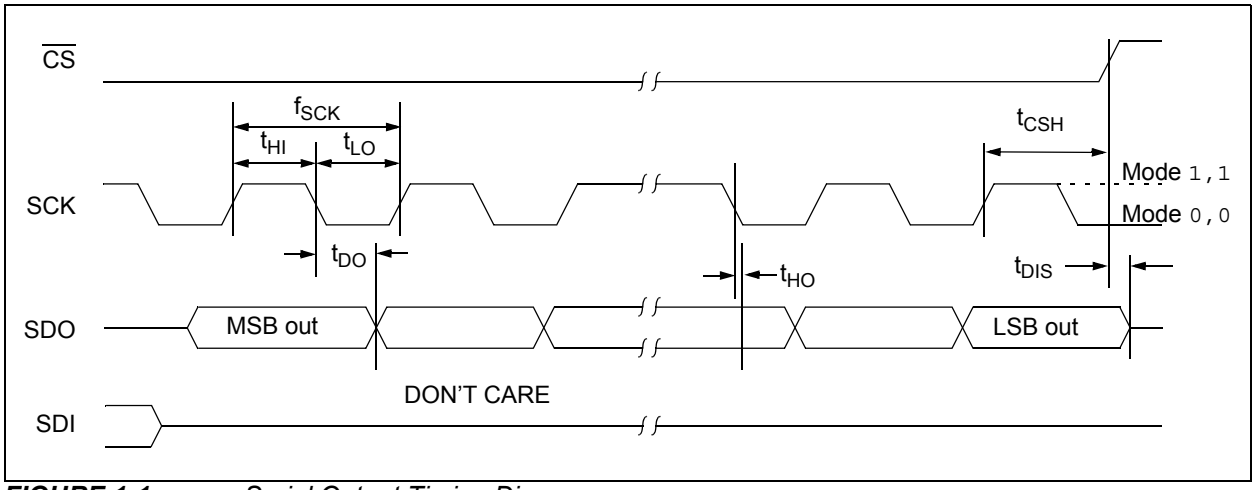



***FIGURE 1-1:*** *Serial Output Timing Diagram.*

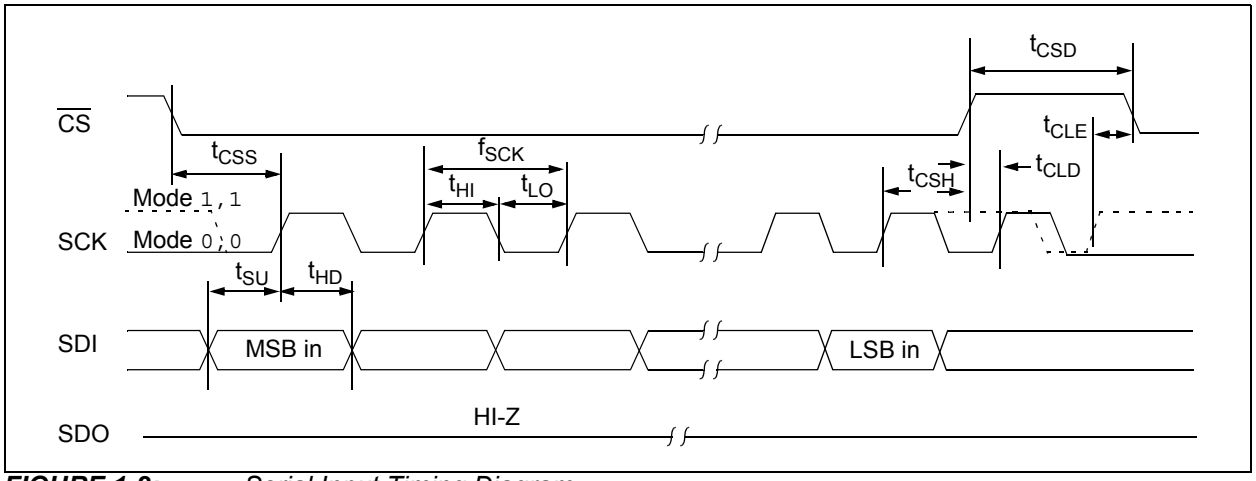



***FIGURE 1-2:*** *Serial Input Timing Diagram.*

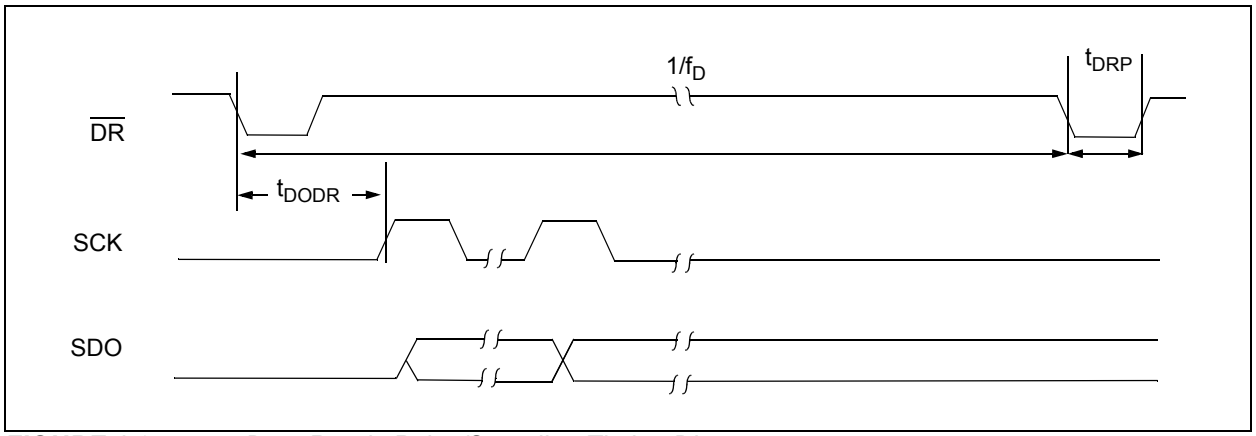



***FIGURE 1-3:*** *Data Ready Pulse/Sampling Timing Diagram.*

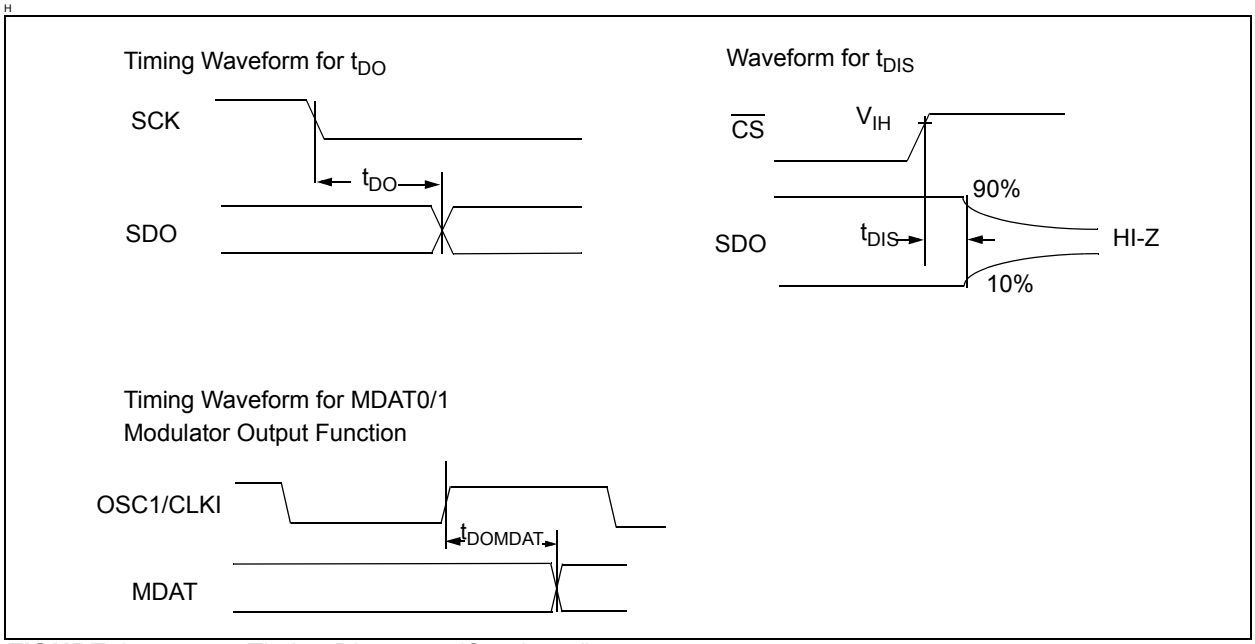



***FIGURE 1-4:*** *Timing Diagrams (Continued).*

**NOTES:**

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $AV_{DD}$ = 3.3V, $DV_{DD}$ = 3.3V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; $V_{IN}$ = -0.5 dBFS at 60 Hz, VREFEXT = 0; CLKEXT = 1, AZ_FREQ = 0; BOOST = 1X.

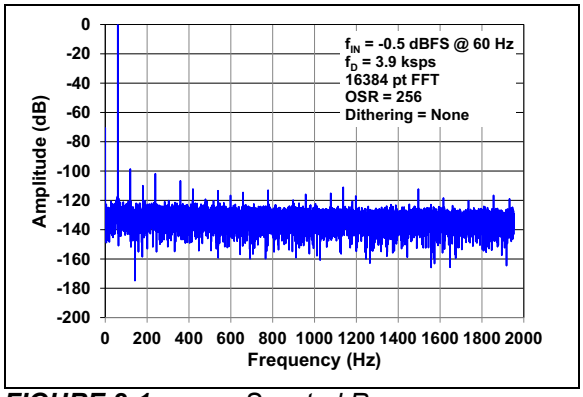



***FIGURE 2-1:*** *Spectral Response.*

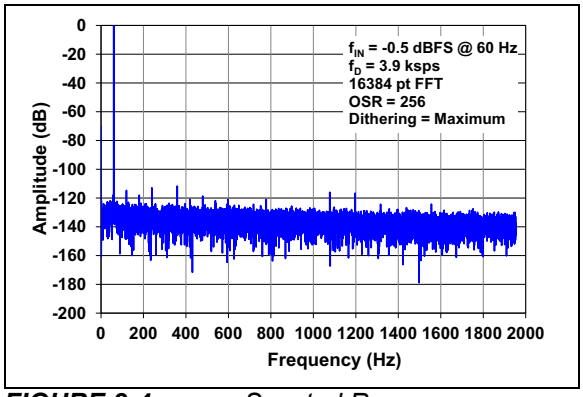



***FIGURE 2-4:*** *Spectral Response.*

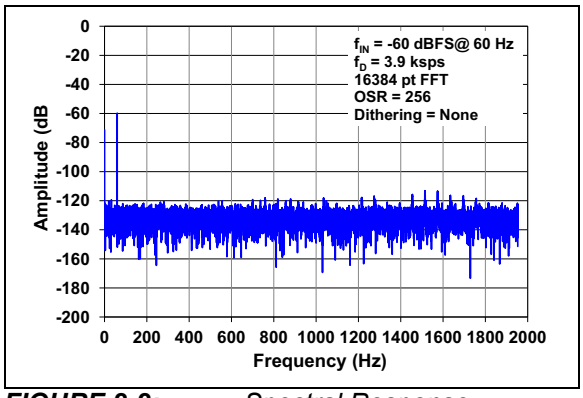



***FIGURE 2-2:*** *Spectral Response.*

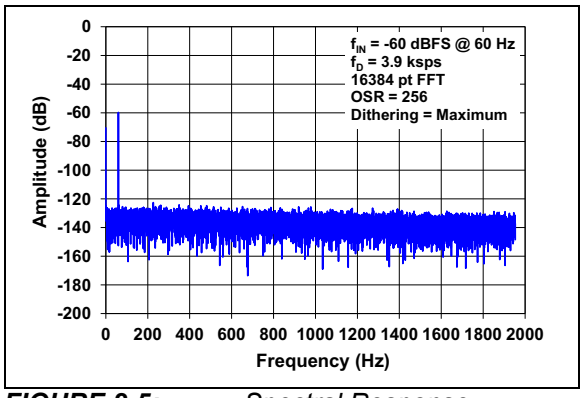



***FIGURE 2-5:*** *Spectral Response.*

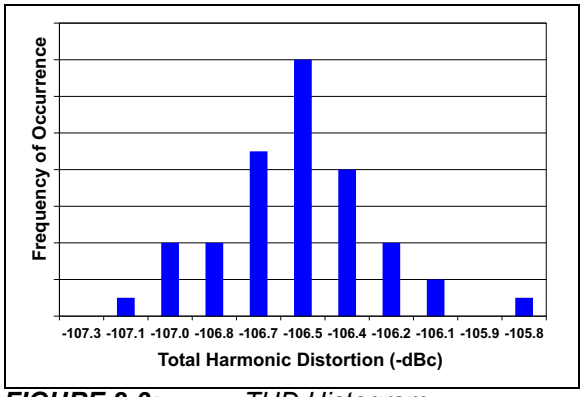



***FIGURE 2-3:*** *THD Histogram.*

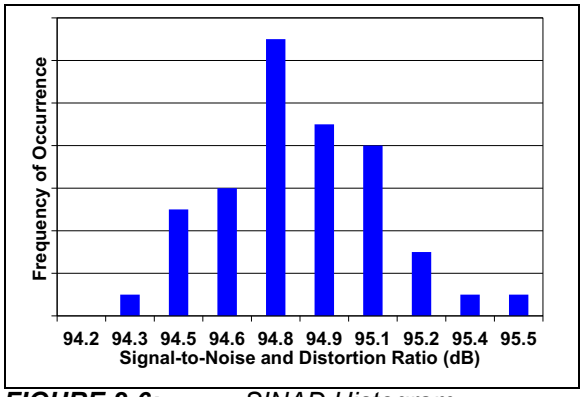



***FIGURE 2-6:*** *SINAD Histogram.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 3.3V, $DV_{DD}$ = 3.3V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; $V_{IN}$ = -0.5 dBFS at 60 Hz, VREFEXT = 0; CLKEXT = 1, AZ_FREQ = 0; BOOST = 1X.

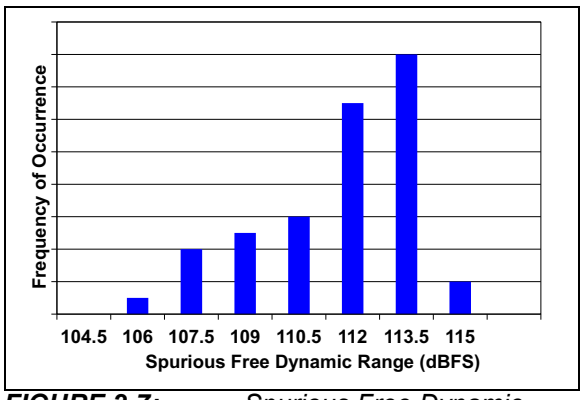



***FIGURE 2-7:*** *Spurious Free Dynamic Range Histogram.*

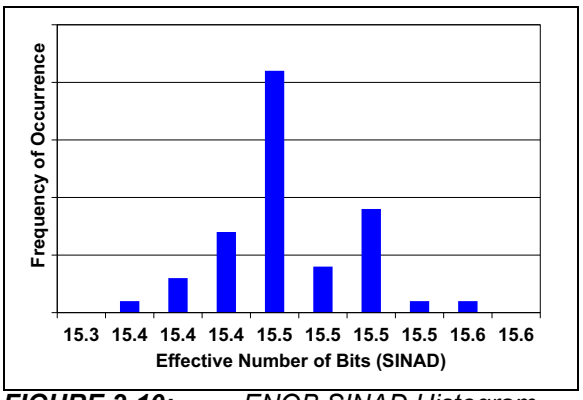



***FIGURE 2-10:*** *ENOB SINAD Histogram.*

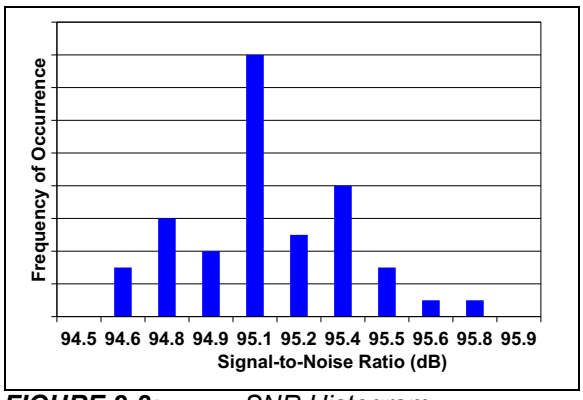



***FIGURE 2-8:*** *SNR Histogram.*

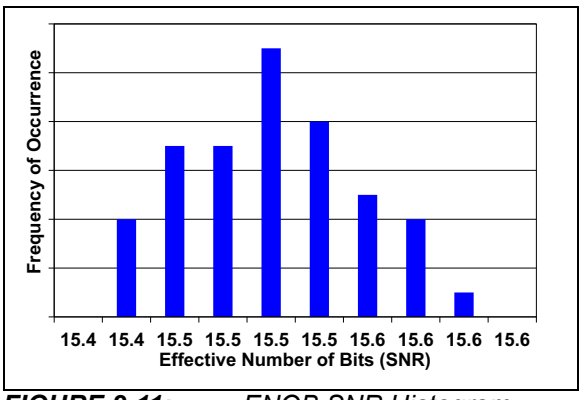



***FIGURE 2-11:*** *ENOB SNR Histogram.*

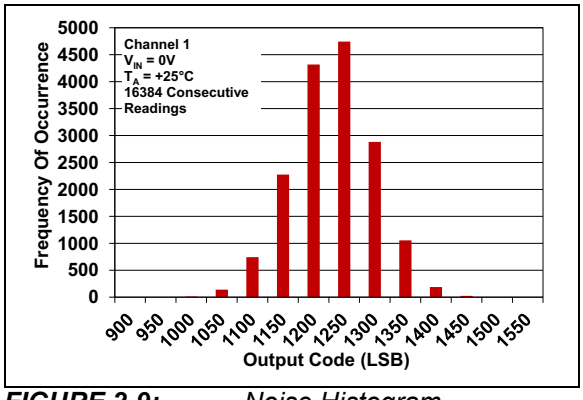



***FIGURE 2-9:*** *Noise Histogram.*

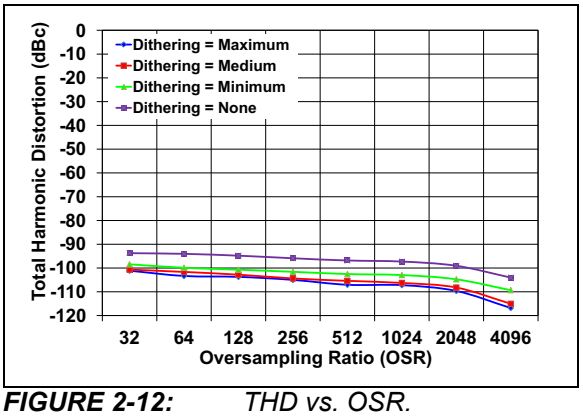



***FIGURE 2-12:*** *THD vs. OSR.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 3.3V, $DV_{DD}$ = 3.3V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; $V_{IN}$ = -0.5 dBFS at 60 Hz, VREFEXT = 0; CLKEXT = 1, AZ_FREQ = 0; BOOST = 1X.

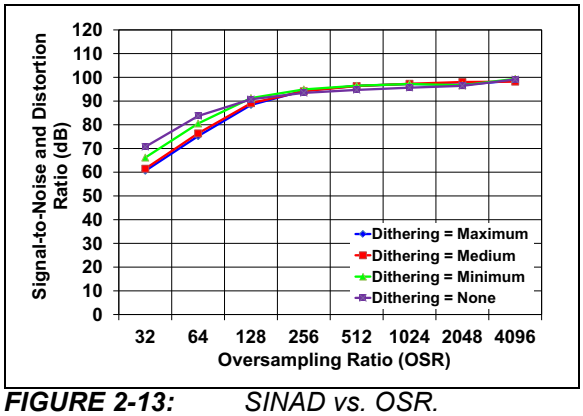



***FIGURE 2-13:*** *SINAD vs. OSR.*

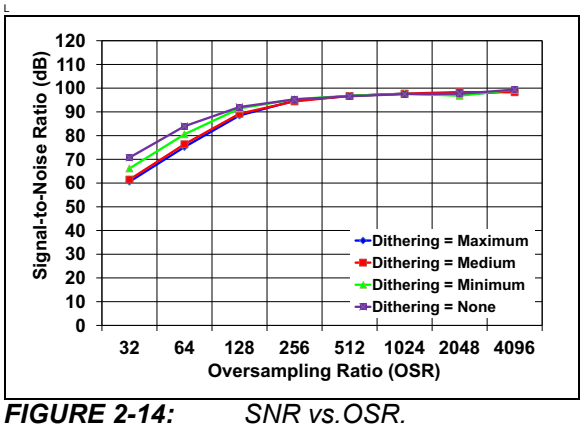



***FIGURE 2-14:*** *SNR vs.OSR.*

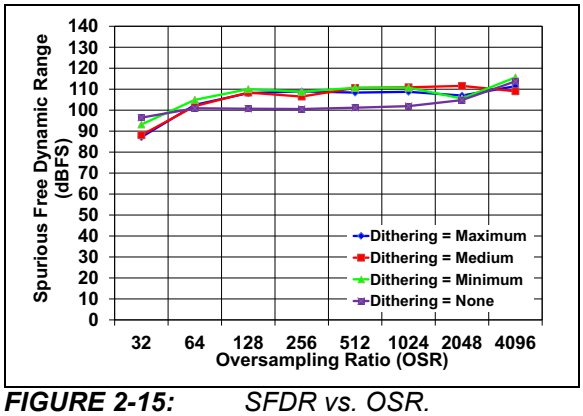



***FIGURE 2-15:*** *SFDR vs. OSR.*

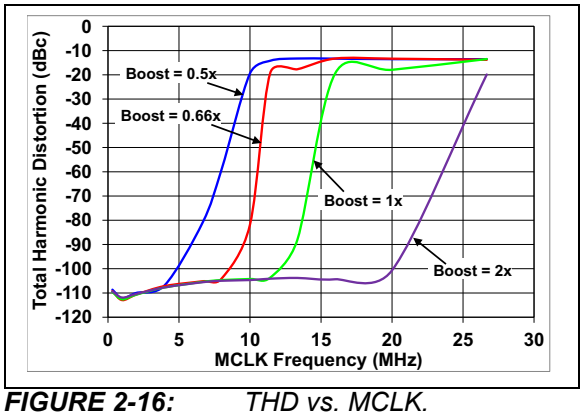



***FIGURE 2-16:*** *THD vs. MCLK.*

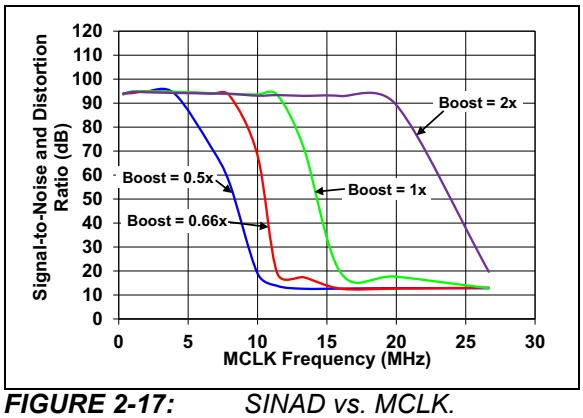



***FIGURE 2-17:*** *SINAD vs. MCLK.*

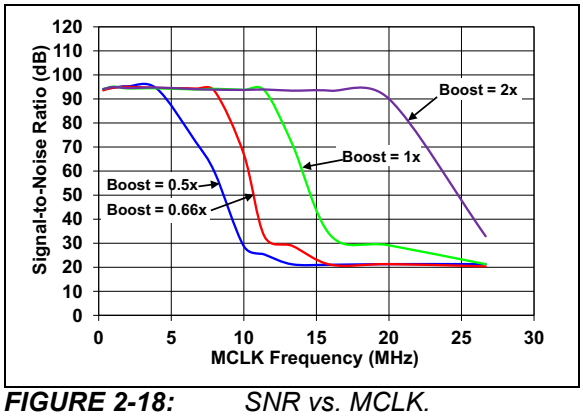



***FIGURE 2-18:*** *SNR vs. MCLK.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 3.3V, $DV_{DD}$ = 3.3V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; $V_{IN}$ = -0.5 dBFS at 60 Hz, VREFEXT = 0; CLKEXT = 1, AZ_FREQ = 0; BOOST = 1X.

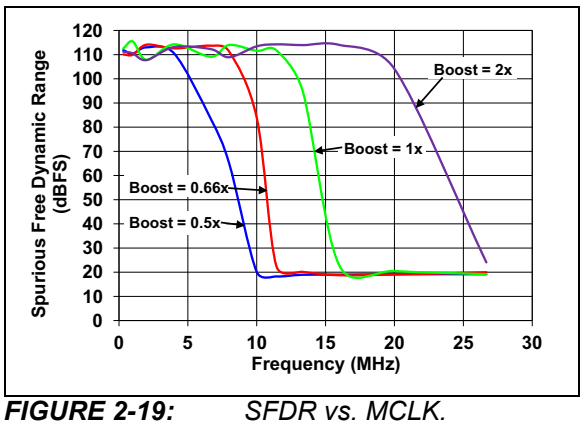



***FIGURE 2-19:*** *SFDR vs. MCLK.*

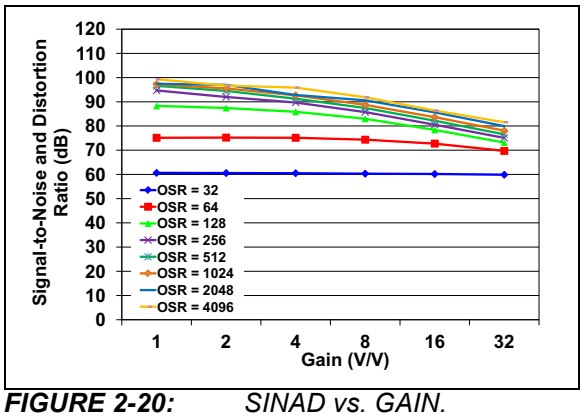



***FIGURE 2-20:*** *SINAD vs. GAIN.*

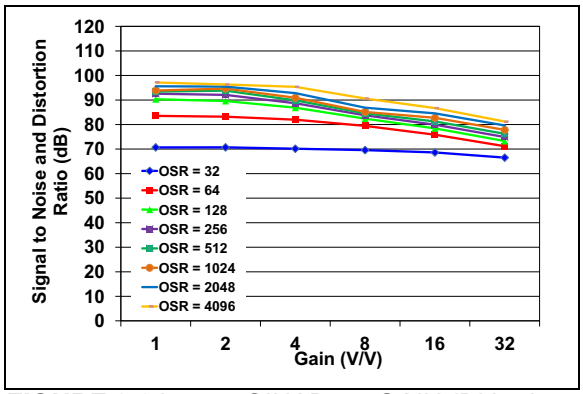



***FIGURE 2-21:*** *SINAD vs. GAIN (Dithering Off).*

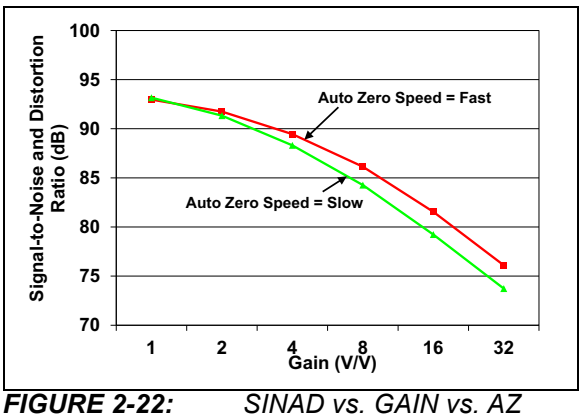



***FIGURE 2-22:*** *SINAD vs. GAIN vs. AZ Speed Chart.*

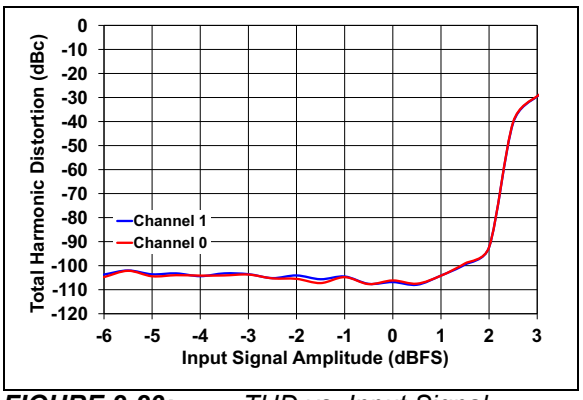



***FIGURE 2-23:*** *THD vs. Input Signal Amplitude.*

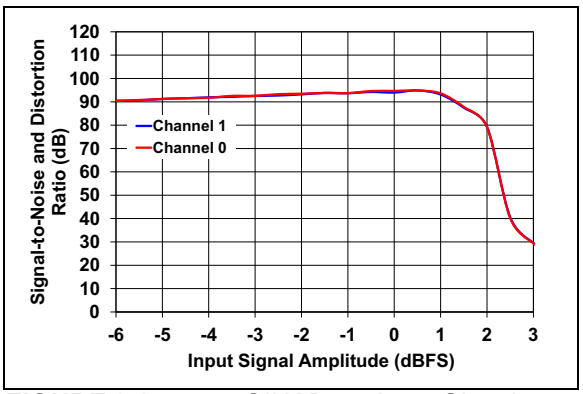



***FIGURE 2-24:*** *SINAD vs. Input Signal Amplitude.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 3.3V, $DV_{DD}$ = 3.3V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; $V_{IN}$ = -0.5 dBFS at 60 Hz, VREFEXT = 0; CLKEXT = 1, AZ_FREQ = 0; BOOST = 1X.

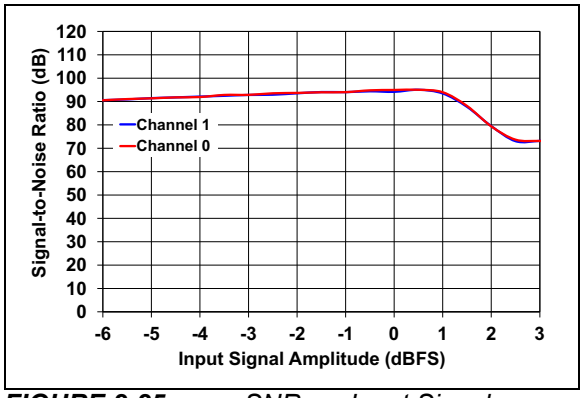



***FIGURE 2-25:*** *SNR vs. Input Signal Amplitude.*

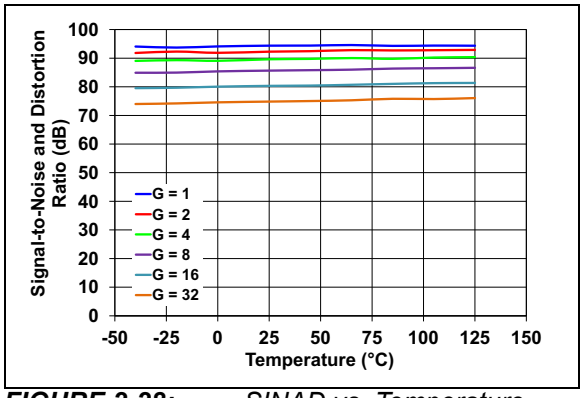



***FIGURE 2-28:*** *SINAD vs. Temperature.*

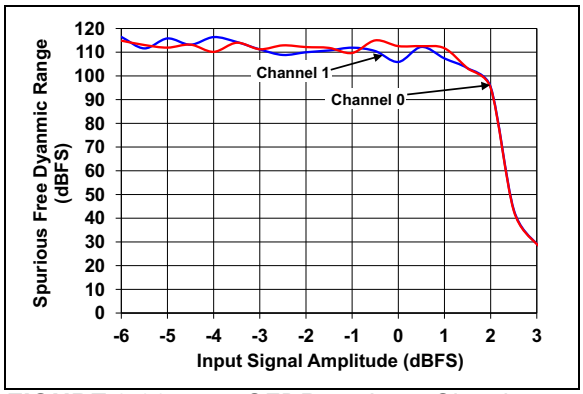



***FIGURE 2-26:*** *SFDR vs. Input Signal Amplitude.*

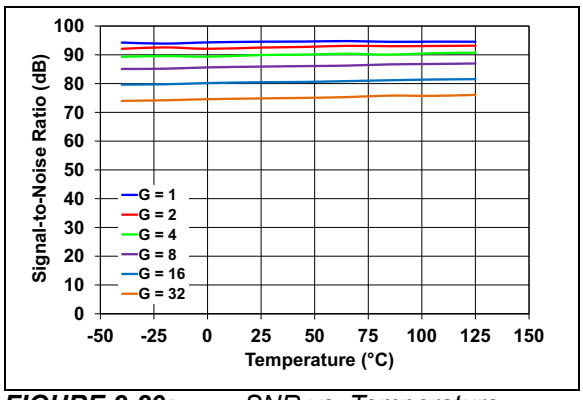



***FIGURE 2-29:*** *SNR vs. Temperature.*

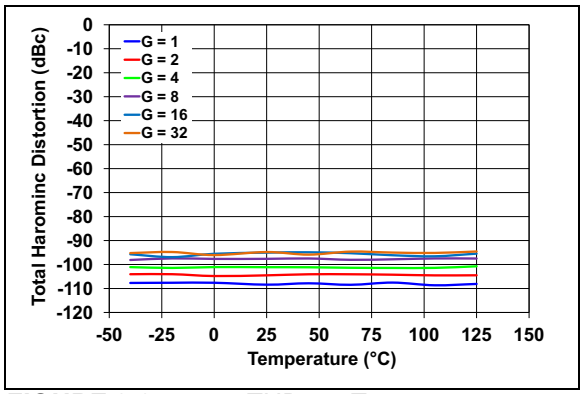



***FIGURE 2-27:*** *THD vs. Temperature.*

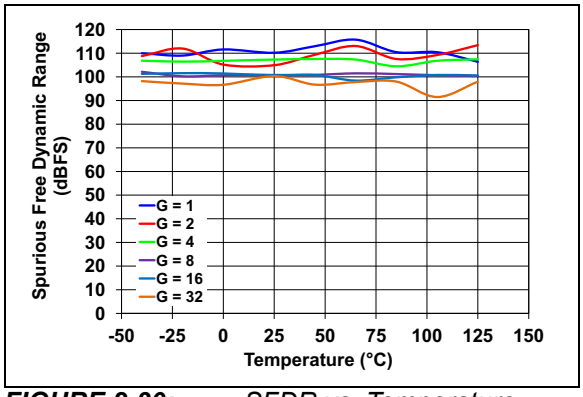



***FIGURE 2-30:*** *SFDR vs. Temperature.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 3.3V, $DV_{DD}$ = 3.3V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; $V_{IN}$ = -0.5 dBFS at 60 Hz, VREFEXT = 0; CLKEXT = 1, AZ_FREQ = 0; BOOST = 1X.

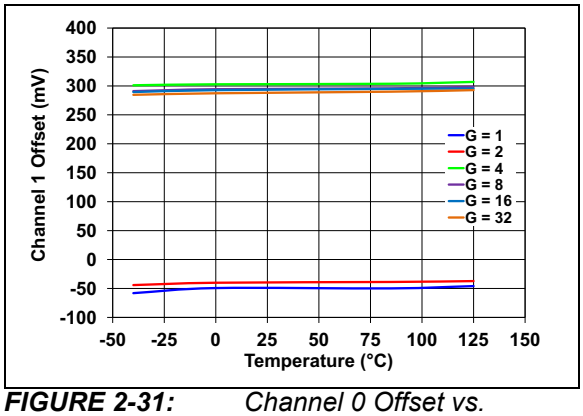



***FIGURE 2-31:*** *Channel 0 Offset vs. Temperature.*

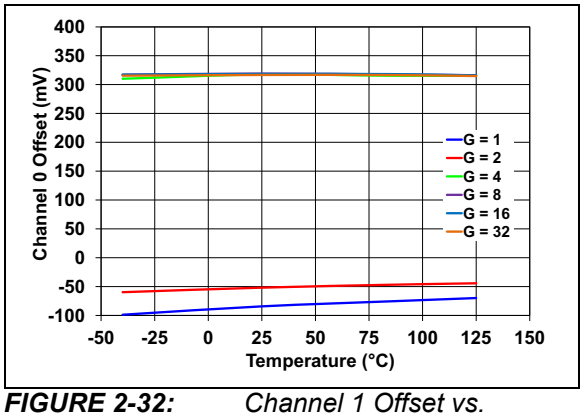



***FIGURE 2-32:*** *Channel 1 Offset vs. Temperature.*

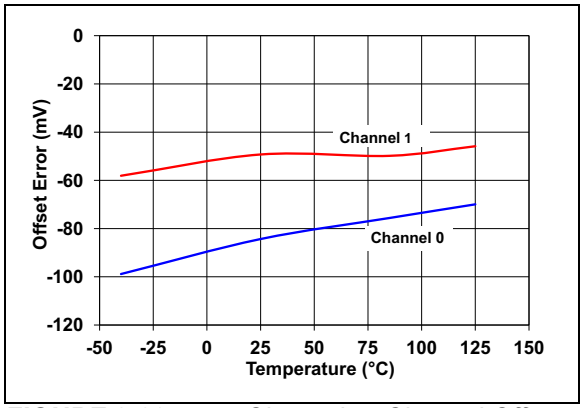



***FIGURE 2-33:*** *Channel-to-Channel Offset Match vs. Temperature.*

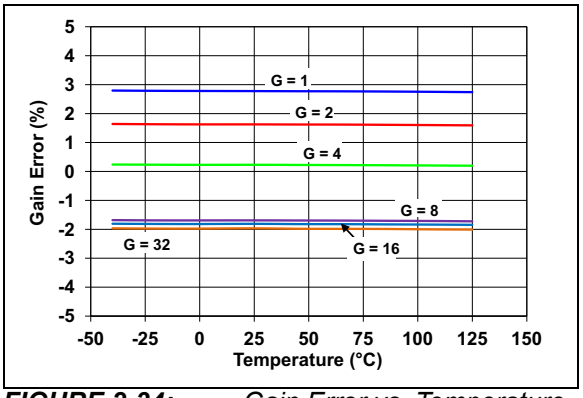



***FIGURE 2-34:*** *Gain Error vs. Temperature.*

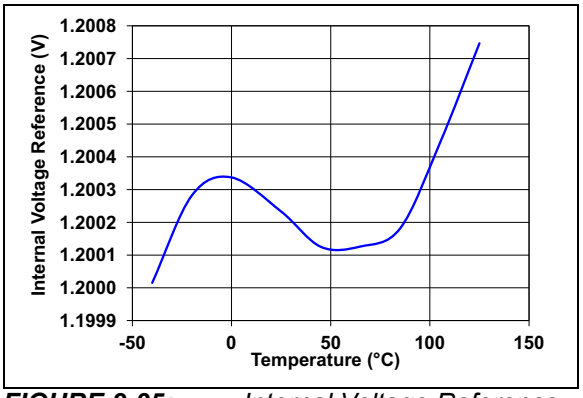



***FIGURE 2-35:*** *Internal Voltage Reference vs. Temperature.*

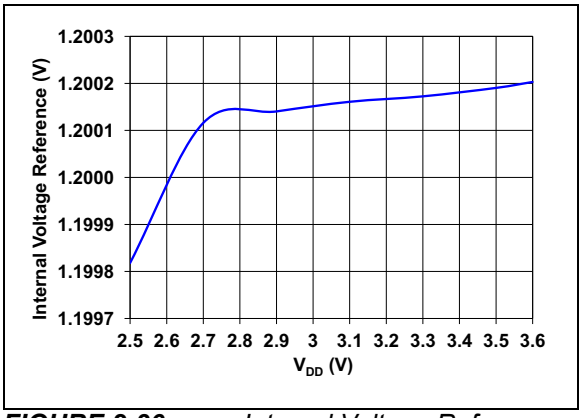



***FIGURE 2-36:*** *Internal Voltage Reference vs. Supply Voltage.*

**Note:** Unless otherwise indicated, $AV_{DD}$ = 3.3V, $DV_{DD}$ = 3.3V; $T_A$ = +25°C, MCLK = 4 MHz; PRESCALE = 1; OSR = 256; GAIN = 1; Dithering = Maximum; $V_{IN}$ = -0.5 dBFS at 60 Hz, VREFEXT = 0; CLKEXT = 1, AZ_FREQ = 0; BOOST = 1X.

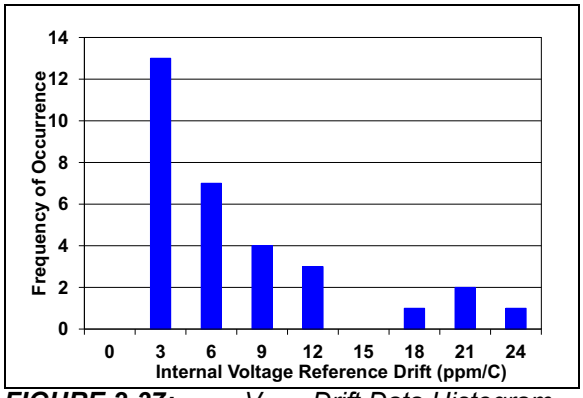



***FIGURE 2-37:*** *$V_{REF}$ Drift Data Histogram Chart.*

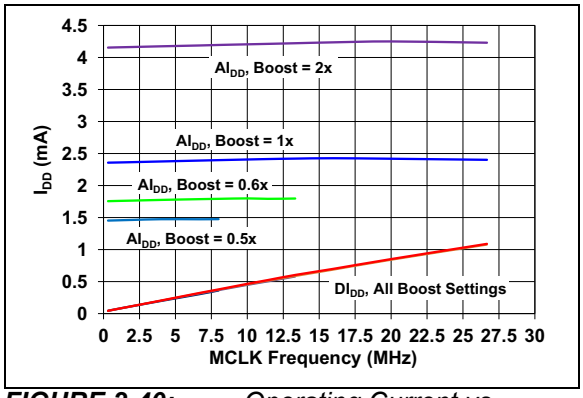



***FIGURE 2-40:*** *Operating Current vs. MCLK, $V_{DD}$ = 3.3V.*

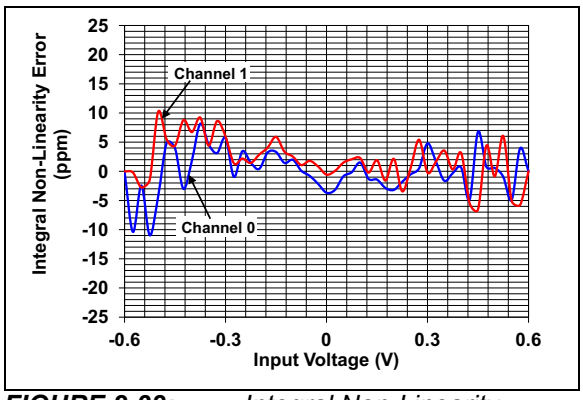



***FIGURE 2-38:*** *Integral Non-Linearity (Dithering Maximum).*

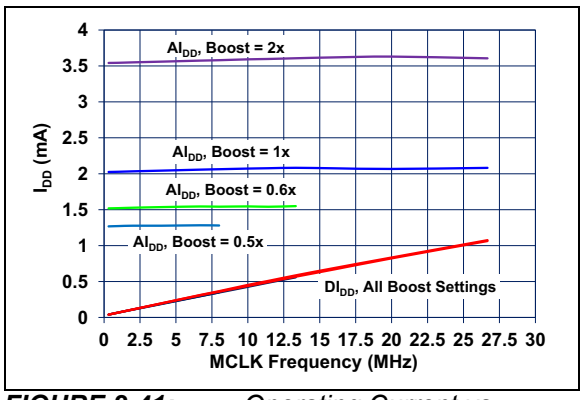



***FIGURE 2-41:*** *Operating Current vs. MCLK, $V_{DD}$ = 2.7V.*

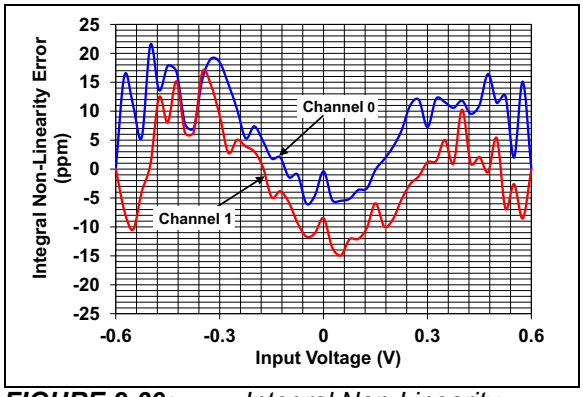



***FIGURE 2-39:*** *Integral Non-Linearity (Dithering Off).*

**NOTES:**

## 3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Pin No. SSOP | Pin No. QFN | Symbol | Function |
|---|---|---|---|
| 1 | 18 | $\overline{\text{RESET}}$ | Master Reset Logic Input Pin |
| 2 | 19 | $DV_{DD}$ | Digital Power Supply Pin |
| 3 | 20 | $AV_{DD}$ | Analog Power Supply Pin |
| 4 | 1 | CH0+ | Non-Inverting Analog Input Pin for Channel 0 |
| 5 | 2 | CH0- | Inverting Analog Input Pin for Channel 0 |
| 6 | 3 | CH1- | Inverting Analog Input Pin for Channel 1 |
| 7 | 4 | CH1+ | Non-Inverting Analog Input Pin for Channel 1 |
| 8 | 5 | $A_{GND}$ | Analog Ground Pin, Return Path for internal analog circuitry |
| 9 | 6 | REFIN+/OUT | Non-Inverting Voltage Reference Input and Internal Reference Output Pin |
| 10 | 7 | REFIN- | Inverting Voltage Reference Input Pin |
| 11 | 8 | $D_{GND}$ | Digital Ground Pin, Return Path for internal digital circuitry |
| 12 | 9 | MDAT1 | Modulator Data Output Pin for Channel 1 |
| 13 | 10 | MDAT0 | Modulator Data Output Pin for Channel 0 |
| 14 | 11 | $\overline{\text{DR}}$ | Data Ready Signal Output Pin |
| 15 | 12 | OSC1/CLKI | Oscillator Crystal Connection Pin or External Clock Input Pin |
| 16 | 13 | OSC2 | Oscillator Crystal Connection Pin |
| 17 | 14 | $\overline{\text{CS}}$ | Serial Interface Chip Select Pin |
| 18 | 15 | SCK | Serial Interface Clock Input Pin |
| 19 | 16 | SDO | Serial Interface Data Input Pin |
| 20 | 17 | SDI | Serial Interface Data Input Pin |
| — | 21 | EP | Exposed Thermal Pad. Must be connected to $A_{GND}$ or left floating. |

### 3.1 Master Reset ($\overline{\text{RESET}}$)

This pin is active-low and places the entire chip in a Reset state when active.

When $\overline{\text{RESET}} = D_{GND}$, all registers are reset to their default value, no communication can take place and no clock is distributed inside the part except in the input structure, if MCLK is applied (if idle, no clock is distributed). This state is equivalent to a POR state.

Since the default state of the ADCs is on, the analog power consumption when $\overline{\text{RESET}} = D_{GND}$ is equivalent to $\overline{\text{RESET}} = V_{DD}$. Only the digital power consumption is largely reduced because this current consumption is essentially dynamic and is reduced drastically when there is no clock running.

All the analog biases are enabled during a Reset so that the part is fully operational just after a $\overline{\text{RESET}}$ rising edge, if the MCLK is applied during the rising edge. If not applied, there is a small time after $\overline{\text{RESET}}$ when the conversion may not be accurate, corresponding to the startup of the charge pump of the input structure.

This input is Schmitt-triggered.

### 3.2 Digital $V_{DD}$ ($DV_{DD}$)

$DV_{DD}$ is the power supply pin for the digital circuitry within the MCP3911. For specified operation, this pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V.

### 3.3 Analog $V_{DD}$ ($AV_{DD}$)

$AV_{DD}$ is the power supply pin for the analog circuitry within the MCP3911. For specified operation, this pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V.

### 3.4 ADC Differential Analog inputs (CHn+/CHn-)

The two fully differential analog voltage inputs for the Delta-Sigma ADCs are:

- CH0 and CH0+
- CH1 and CH1+

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV/GAIN with $V_{REF}$ = 1.2V.

The maximum differential voltage is proportional to the $V_{REF}$ voltage. The maximum absolute voltage, with respect to $A_{GND}$, for each CHn+/- input pin is ±1V with no distortion, and ±2V with no breaking after continuous voltage. This maximum absolute voltage is not proportional to the $V_{REF}$ voltage.

### 3.5 Analog Ground ($A_{GND}$)

$A_{GND}$ is the ground connection to internal analog circuitry (see the **Functional Block Diagram**). To ensure accuracy and noise cancellation, this pin must be connected to the same ground as $D_{GND}$, preferably with a star connection. If an analog ground plane is available, it is recommended that this pin is tied to this Printed Circuit Board (PCB) plane. This plane should also reference all other analog circuitry in the system.

### 3.6 Non-Inverting Reference Input, Internal Reference Output (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for both ADCs or the internal voltage reference output.

When VREFEXT = 1, an external voltage reference source can be used and the internal voltage reference is disabled. When using an external differential voltage reference, it should be connected to its $V_{REF+}$ pin. When using an external single-ended reference, it should be connected to this pin.

When VREFEXT = 0, the internal voltage reference is enabled and connected to this pin through a switch. If used as a voltage source, this voltage reference has a minimal drive capability and thus needs proper buffering and bypass capacitances. A 0.1 µF ceramic capacitor is sufficient in most cases.

If the voltage reference is only used as an internal $V_{REF}$, adding bypass capacitance on REFIN+/OUT is not necessary for keeping ADC accuracy. If left floating, a minimal 0.1 µF ceramic capacitance can be connected to avoid EMI/EMC susceptibility issues due to the antenna created by the REFIN+/OUT pin.

### 3.7 Inverting Reference Input (REFIN-)

This pin is the inverting side of the differential voltage reference input for both ADCs. When using an external differential voltage reference, it should be connected to its $V_{REF-}$ pin. When using an external single-ended voltage reference or when VREFEXT = 0 (Default) and using the internal voltage reference, this pin should be directly connected to $A_{GND}$.

### 3.8 Digital Ground Connection ($D_{GND}$)

$D_{GND}$ is the ground connection to the internal digital circuitry (see **Functional Block Diagram**). To ensure optimal accuracy and noise cancellation, $D_{GND}$ must be connected to the same ground as $A_{GND}$, preferably with a star connection. If a digital ground plane is available, it is recommended that this pin is tied to this PCB plane. This plane should also reference all other digital circuitry in the system.

### 3.9 Modulator Data Output Pin for Channel 1 and Channel 0 (MDAT1/MDAT0)

MDAT0 and MDAT1 are the output pins for the modulator serial bitstreams of ADC Channels 0 and 1, respectively. These pins are high impedance when their corresponding MODOUT bit is logic low. When the MODOUT<1:0> is enabled, the modulator bit stream of the corresponding channel is present on the pin and updated at the AMCLK frequency (see **Section 5.4 "Modulator Output Block"** for a complete description of the modulator outputs). These pins can be directly connected to an MCU or a DSP when a specific digital filtering is needed.

### 3.10 Data Ready Output ($\overline{DR}$)

The data ready pin indicates that a new conversion result is ready to be read. The default state of this pin is high when $\overline{DR}$_HIZ = 1 and is high-impedance when $\overline{DR}$_HIZ = 0 (Default). After each conversion is finished, a logic-low pulse takes place on the data ready pin to indicate that the conversion result is ready as an interrupt. This pulse is synchronous with the master clock and has a defined and constant width.

The data ready pin is independent of the SPI interface and acts like an interrupt output. The data ready pin state is not latched and the pulse width (and period) are both determined by the MCLK frequency, over-sampling rate and internal clock pre-scale settings. The $\overline{DR}$ pulse width is equal to one DMCLK period, and the frequency of the pulses is equal to DRCLK (see Figure 1-3).

| **Note:** | This pin should not be left floating when $\overline{DR}$_HIZ bit is low; a 100 kΩ pull-up resistor connected to $DV_{DD}$ is recommended. |
|---|---|

### 3.11 Oscillator and Master Clock Input Pins (OSC1/CLKI, OSC2)

OSC1/CLKI and OSC2 provide the master clock (MCLK) for the device. When CLKEXT = 0, a resonant crystal or clock source with a similar sinusoidal waveform must be placed across these pins to ensure proper operation. The typical clock frequency specified is 4 MHz. For proper operation and optimizing ADC accuracy, AMCLK should be limited to the maximum frequency defined in Table 5-3 as a function of the BOOST and PGA settings chosen. MCLK can take larger values as long as the prescaler settings (PRE<1:0>) limit AMCLK = MCLK/PRESCALE in the defined range in Table 5-3. For proper operation, appropriate load capacitance should be connected to these pins.

### 3.12 Chip Select ($\overline{CS}$)

This pin is the SPI chip select that enables the serial communication. When this pin is high, no communication can take place. A chip select falling edge initiates the serial communication and a chip select rising edge terminates the communication. No communication can take place when $\overline{CS}$ is low or when $\overline{RESET}$ is low.

This input is Schmitt-triggered.

### 3.13 Serial Data Clock (SCK)

This is the serial clock pin for SPI communication.

Data is clocked into the device on the RISING edge, and out of the device on the FALLING edge of SCK.

The MCP3911 interface is compatible with both SPI 0,0 and 1,1 modes. SPI modes can be changed during a $\overline{CS}$ high time.

The maximum clock speed specified is 20 MHz.

This input is Schmitt-triggered.

### 3.14 Serial Data Output (SDO)

This is the SPI data output pin. Data is clocked out of the device on the FALLING edge of SCK.

This pin stays high-impedance during the first command byte. It also stays high-impedance during the whole communication for write commands and when $\overline{CS}$ pin is high, or when $\overline{RESET}$ pin is low. This pin is active only when a read command is processed. Each read is processed by packet of 8 bits.

### 3.15 Serial Data Input (SDI)

This is the SPI data input pin. Data is clocked into the device on the RISING edge of SCK.

When $\overline{CS}$ is low, this pin is used to communicate with a series of 8-bit commands.

The interface is half-duplex (inputs and outputs do not happen at the same time).

Each communication starts with a chip select falling edge followed by an 8-bit command word entered through the SDI pin. Each command is either a Read or a Write command. Toggling SDI during a Read command has no effect.

This input is Schmitt-triggered.

**NOTES:**

## 4.0 TERMINOLOGIES AND FORMULAS

This section defines the terms and formulas used throughout this data sheet. The following terms are defined:

- **MCLK – Master Clock**
- **AMCLK – Analog Master Clock**
- **DMCLK - Digital Master Clock**
- **DRCLK - Data Rate Clock**
- **OSR – Oversampling Ratio**
- **Offset Error**
- **Gain Error**
- **Integral Non-Linearity Error**
- **Signal-to-Noise Ratio (SNR)**
- **Signal-to-Noise Ratio and Distortion (SINAD)**
- **Total Harmonic Distortion (THD)**
- **Spurious-Free Dynamic Range (SFDR)**
- **MCP3911 Delta-Sigma Architecture**
- **Idle Tones**
- **Dithering**
- **Crosstalk**
- **PSRR**
- **CMRR**
- **ADC Reset Mode**
- **Hard Reset Mode (RESET = DGND)**
- **ADC Shutdown Mode**
- **Full Shutdown Mode**

### 4.1 MCLK – Master Clock

This is the fastest clock present in the device. This is the frequency of the crystal placed at the OSC1/OSC2 inputs when CLKEXT = 0 or the frequency of the clock input at the OSC1/CLKI when CLKEXT = 1. See Figure 4-1.

### 4.2 AMCLK – Analog Master Clock

This is the clock frequency that is present on the analog portion of the device, after prescaling has occurred via the CONFIG PRE<1:0> register bits. The analog portion includes the PGAs and the two Delta-Sigma modulators.

$$AMCLK = \frac{MCLK}{PRESCALE}$$

**TABLE 4-1: MCP3911 OVERSAMPLING RATIO SETTINGS**

| Config PRE<1:0> | | Analog Master Clock Prescale |
|---|---|---|
| 0 | 0 | AMCLK = MCLK/ 1 (default) |
| 0 | 1 | AMCLK = MCLK/ 2 |
| 1 | 0 | AMCLK = MCLK/ 4 |
| 1 | 1 | AMCLK = MCLK/ 8 |

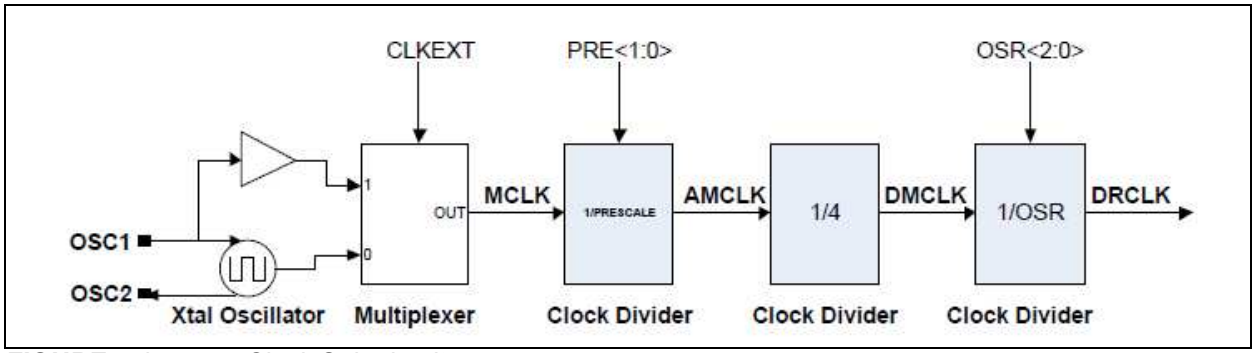



***FIGURE 4-1:*** *Clock Sub-circuitry.*

### 4.3 DMCLK - Digital Master Clock

This is the clock frequency that is present on the digital portion of the device after prescaling and division by 4. This is also the sampling frequency, that is the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to one sample and one modulator output. See Figure 4-1.

**EQUATION 4-1:**

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times PRESCALE}$$

### 4.4 DRCLK - Data Rate Clock

This is the output data rate, i.e., the rate at which the ADCs output new data. Each new data is signaled by a data ready pulse on the $\overline{DR}$ pin.

This data rate is depending on the OSR and the prescaler with the following formula:

**EQUATION 4-2:**

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times PRESCALE}$$

Since this is the output data rate and the decimation filter is a SINC (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

The following table describes the various combinations of OSR and PRESCALE and their associated AMCLK, DMCLK and DRCLK rates.

**TABLE 4-2: DEVICE DATA RATES IN FUNCTION OF MCLK, OSR, AND PRESCALE, MCLK = 4 MHz**

| PRE <1:0> | | OSR <2:0> | | | OSR | AMCLK | DMCLK | DRCLK | DRCLK (ksps) | SINAD (dB) Note 1 | ENOB from SINAD (bits) Note 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 4096 | MCLK/8 | MCLK/32 | MCLK/131072 | 0.035 | 98 | 16 |
| 1 | 1 | 1 | 1 | 1 | 2048 | MCLK/8 | MCLK/32 | MCLK/65536 | 0.061 | 98 | 16 |
| 1 | 1 | 1 | 1 | 1 | 1024 | MCLK/8 | MCLK/32 | MCLK/32768 | 0.122 | 97 | 15.8 |
| 1 | 1 | 1 | 1 | 1 | 512 | MCLK/8 | MCLK/32 | MCLK/16384 | 0.244 | 96 | 15.6 |
| 1 | 1 | 0 | 1 | 1 | 256 | MCLK/8 | MCLK/32 | MCLK/8192 | 0.488 | 95 | 15.5 |
| 1 | 1 | 0 | 1 | 0 | 128 | MCLK/8 | MCLK/32 | MCLK/4096 | 0.976 | 90 | 14.7 |
| 1 | 1 | 0 | 0 | 1 | 64 | MCLK/8 | MCLK/32 | MCLK/2048 | 1.95 | 83 | 13.5 |
| 1 | 1 | 0 | 0 | 0 | 32 | MCLK/8 | MCLK/32 | MCLK/1024 | 3.9 | 70 | 11.3 |
| 1 | 0 | 1 | 1 | 1 | 4096 | MCLK/4 | MCLK/16 | MCLK/65536 | 0.061 | 98 | 16 |
| 1 | 0 | 1 | 1 | 1 | 2048 | MCLK/4 | MCLK/16 | MCLK/32768 | 0.122 | 98 | 16 |
| 1 | 0 | 1 | 1 | 1 | 1024 | MCLK/4 | MCLK/16 | MCLK/16384 | 0.244 | 97 | 15.8 |
| 1 | 0 | 1 | 1 | 1 | 512 | MCLK/4 | MCLK/16 | MCLK/8192 | 0.488 | 96 | 15.6 |
| 1 | 0 | 0 | 1 | 1 | 256 | MCLK/4 | MCLK/16 | MCLK/4096 | 0.976 | 95 | 15.5 |
| 1 | 0 | 0 | 1 | 0 | 128 | MCLK/4 | MCLK/16 | MCLK/2048 | 1.95 | 90 | 14.7 |
| 1 | 0 | 0 | 0 | 1 | 64 | MCLK/4 | MCLK/16 | MCLK/1024 | 3.9 | 83 | 13.5 |
| 1 | 0 | 0 | 0 | 0 | 32 | MCLK/4 | MCLK/16 | MCLK/512 | 7.8125 | 70 | 11.3 |
| 0 | 1 | 1 | 1 | 1 | 4096 | MCLK/2 | MCLK/8 | MCLK/32768 | 0.122 | 98 | 16 |
| 0 | 1 | 1 | 1 | 1 | 2048 | MCLK/2 | MCLK/8 | MCLK/16384 | 0.244 | 98 | 16 |
| 0 | 1 | 1 | 1 | 1 | 1024 | MCLK/2 | MCLK/8 | MCLK/8192 | 0.488 | 97 | 15.8 |
| 0 | 1 | 1 | 1 | 1 | 512 | MCLK/2 | MCLK/8 | MCLK/4096 | 0.976 | 96 | 15.6 |
| 0 | 1 | 0 | 1 | 1 | 256 | MCLK/2 | MCLK/8 | MCLK/2048 | 1.95 | 95 | 15.5 |
| 0 | 1 | 0 | 1 | 0 | 128 | MCLK/2 | MCLK/8 | MCLK/1024 | 3.9 | 90 | 14.7 |
| 0 | 1 | 0 | 0 | 1 | 64 | MCLK/2 | MCLK/8 | MCLK/512 | 7.8125 | 83 | 13.5 |
| 0 | 1 | 0 | 0 | 0 | 32 | MCLK/2 | MCLK/8 | MCLK/256 | 15.625 | 70 | 11.3 |
| 0 | 0 | 1 | 1 | 1 | 4096 | MCLK | MCLK/4 | MCLK/16384 | 0.244 | 98 | 16 |
| 0 | 0 | 1 | 1 | 0 | 2048 | MCLK | MCLK/4 | MCLK/8192 | 0.488 | 98 | 16 |
| 0 | 0 | 1 | 0 | 1 | 1024 | MCLK | MCLK/4 | MCLK/4096 | 0.976 | 97 | 15.8 |
| 0 | 0 | 1 | 0 | 0 | 512 | MCLK | MCLK/4 | MCLK/2048 | 1.95 | 96 | 15.6 |
| 0 | 0 | 0 | 1 | 1 | 256 | MCLK | MCLK/4 | MCLK/1024 | 3.9 | 95 | 15.5 |
| 0 | 0 | 0 | 1 | 0 | 128 | MCLK | MCLK/4 | MCLK/512 | 7.8125 | 90 | 14.7 |
| 0 | 0 | 0 | 0 | 1 | 64 | MCLK | MCLK/4 | MCLK/256 | 15.625 | 83 | 13.5 |
| 0 | 0 | 0 | 0 | 0 | 32 | MCLK | MCLK/4 | MCLK/128 | 31.25 | 70 | 11.3 |

**Note 1:** For OSR = 32 and 64, DITHER = None. For OSR = 128 and higher, DITHER = Maximum. The SINAD values are given from GAIN = 1.

## 4.5 OSR – Oversampling Ratio

This is the ratio of the sampling frequency to the output data rate. OSR = DMCLK/DRCLK. The default OSR is 256 or with MCLK = 4 MHz, PRESCALE = 1, AMCLK = 4 MHz, $f_S$ = 1 MHz, $f_D$ = 3.90625 ksps. The following bits in the CONFIG register are used to change the oversampling ratio (OSR).

**TABLE 4-3: MCP3911 OVERSAMPLING RATIO SETTINGS**

| Config | | | Oversampling Ratio OSR |
|---|---|---|---|
| OSR<2:0> | | | |
| 0 | 0 | 0 | 32 |
| 0 | 0 | 1 | 64 |
| 0 | 1 | 0 | 128 |
| 0 | 1 | 1 | 256 (DEFAULT) |
| 1 | 0 | 0 | 512 |
| 1 | 0 | 1 | 1024 |
| 1 | 1 | 0 | 2048 |
| 1 | 1 | 1 | 4096 |

## 4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together ($V_{IN}$ = 0V). The specification incorporates both PGA and ADC offset contributions. This error varies with PGA and OSR settings. The offset is different on each channel and varies from chip to chip. The offset is specified in µV. The offset error can be digitally compensated independently on each channel through the OFFCAL registers with a 24-bit calibration word.

The offset on the MCP3911 has a low temperature coefficient (see **Section 2.0, Typical Performance Curves** for more information, see Figure 2-33).

## 4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in percentage (%) compared to the ideal transfer function defined by Equation 5-3. The specification incorporates both PGA and ADC gain error contributions but not the $V_{REF}$ contribution (it is measured with an external $V_{REF}$).

This error varies with PGA and OSR settings. The gain error can be digitally compensated independently on each channel through the GAINCAL registers with a 24-bit calibration word.

The gain error on the MCP3911 has a low temperature coefficient. For more information, see Figure 2-34.

## 4.8 Integral Non-Linearity Error

Integral non-linearity error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed or with the end points equal to zero.

It is the maximum remaining error after the calibration of offset and gain errors for a DC input signal.

## 4.9 Signal-to-Noise Ratio (SNR)

For the MCP3911 ADCs, the signal-to-noise ratio is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal), when the input is a sinewave at a predetermined frequency. It is measured in dB. Usually, only the maximum signal-to-noise ratio is specified. The SNR figure depends mainly on the OSR and DITHER settings of the device.

**EQUATION 4-3: SIGNAL-TO-NOISE RATIO**

$$SNR(dB) = 10log\left(\frac{SignalPower}{NoisePower}\right)$$

## 4.10 Signal-to-Noise Ratio and Distortion (SINAD)

The most important figure of merit for the analog performance of the ADCs present on the MCP3911 is the Signal-to-Noise and Distortion (SINAD) specification.

Signal-to-noise and distortion ratio is similar to signal-to-noise ratio, with the exception that you must include the harmonics power in the noise power calculation. The SINAD specification depends mainly on the OSR and DITHER settings.

**EQUATION 4-4: SINAD EQUATION**

$$SINAD(dB) = 10log\left(\frac{SignalPower}{Noise + HarmonicsPower}\right)$$

The calculated combination of SNR and THD per the following formula also yields SINAD:

**EQUATION 4-5: SINAD, THD, AND SNR RELATIONSHIP**

$$SINAD(dB) = 10log\left[10^{\left(\frac{SNR}{10}\right)} + 10^{\left(\frac{-THD}{10}\right)}\right]$$

## 4.11 Total Harmonic Distortion (THD)

The total harmonic distortion is the ratio of the output harmonics power to the fundamental signal power for a sinewave input and is defined by Equation 4-6.